1 Main Waveforms

Synchronization Circuit 1: Out U3-TLC555D (C1), Gate of Q4 (C2), Synch_Master signal (C3)

Synchronization Circuit 2: Out U3-TLC555D (C1), Synch_Master signal (C3), Synch Slave (C4)
Current Sharing 1 (I_{out}<0.5A \text{ Vin}=9V): V_{dsQ1}, V_{dsQ2}

Current Sharing 2 (I_{out}<0.15A \text{ Vin}=6.5V): V_{dsQ1} (C1), V_{dsQ2} (C2)
Current Sharing 3 (Iout=10A Vin=6.5V): VdsQ1 (C1), VdsQ2 (C2)

Current Sharing 4 (Vin=9V Iout=5A): CsenseQ1 (C1), Vsense Q2 (C2)
2 Efficiency and Load Regulation

The following table shows the measured values:

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3 Control Loop Frequency Response

The figures below show the open loop response for 6.5V, 9V, 12V input voltage

Vin=6.5V, Vin=9V, Vin=12V @ 15A Output

Vin=6.5V, Vin=9V, Vin=12V @ Discontinuous Mode (no load)
4 Load Transients

Vout (C1), Iout (C2, 10A/V current probe)
5 Output and Input Ripple Voltage

Input Voltage Ripple (C3), Output Voltage Ripple (C2) at full load 15A @ Vin=6.5V

Input Voltage Ripple (C3), Output Voltage Ripple (C2) at full load 15A @ Vin=9V
Output Power Continuous 10A Vin=6.5V

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