**TI Designs – Precision: Verified Design**

**Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design**

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**Circuit Description**

This low-drift, bidirectional, single-supply, low-side current sensing reference design can accurately detect load currents from -2.5 A to +2.5 A. The linear range of the output is from 250 mV to 2.75 V. Positive current is represented by output voltages from 1.5 V to 2.75 V whereas negative current is represented by output voltages from 250 mV to 1.5V. The difference amplifier is the INA213B current shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

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**Design Resources**

- Design Archive
  - TINA-TI™
  - REF2030
  - INA213

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5.0 V
- Load current: ±2.5 A
- Output: 250 mV – 2.75 V
- Maximum Shunt Voltage: ±25 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Calculated, and Measured Performance

<table>
<thead>
<tr>
<th></th>
<th>Goal</th>
<th>Calculated</th>
<th>Simulated</th>
<th>Un-calibrated</th>
<th>Calibrated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Scale Range Error (25°C)</td>
<td>±0.1%</td>
<td>±0.117%</td>
<td>±0.032%</td>
<td>±0.036%</td>
<td>±0.004%</td>
</tr>
<tr>
<td>Full Scale Range Error (-40°C to 125°C)</td>
<td>±0.15%</td>
<td>±0.2%</td>
<td>N/A</td>
<td>±0.052%</td>
<td>±0.061%</td>
</tr>
</tbody>
</table>

Figure 1: Measured Transfer Function
2 Theory of Operation

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of the bus voltage, \( V_{bus} \). When sensing bidirectional currents, use a differential amplifier with a reference pin. This allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (\( V+ \)) and the reference voltage (\( \text{REF}, \) or \( V_{BIAS} \)) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 2 depicts the general circuit topology for a low-drift, low-side, bidirectional current sensing solution.

This topology is particularly useful when interfacing with an analog-to-digital converter, as shown on the cover page. Not only will \( V_{\text{REF}} \) and \( V_{\text{BIAS}} \) track over temperature, their matching is much better than alternate topologies. A common alternate topology is discussed in Section 7.1.

![Low-drift Reference Circuit](image)

**Figure 2:** Low-drift, low-side, bidirectional circuit topology

2.1 Transfer Function

The transfer function for the circuit given in Figure 2 is shown in Equation (1).

\[
V_{\text{OUT}} = G \times (\pm V_{\text{shunt}}) + V_{\text{BIAS}} = G \times (\pm I_{\text{LOAD}} \times R_{\text{shunt}}) + V_{\text{BIAS}}
\] (1)
3 Component Selection

3.1 Shunt Resistor ($R_{shunt}$)

As shown in Figure 2, the value of $V_{shunt}$ is the ground potential for the system load. If the value of $V_{shunt}$ is too large, it may cause issues when interfacing with systems whose ground potential is truly 0 V. If the value of $V_{shunt}$ is too negative, it may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore it is important to limit the voltage across the shunt resistor. Equation (2) can be used to calculate the maximum value of $R_{shunt}$.

$$R_{sh(max)} = \frac{V_{sh(max)}}{I_{load(max)}}$$ (2)

Given that the maximum shunt voltage is ±25 mV and load current range is ±2.5 A, the maximum shunt resistance is calculated as shown in Equation (3).

$$R_{sh(max)} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{25\text{mV}}{2.5\text{A}} = 10\text{m}\Omega$$ (3)

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor was selected because it has the following specifications:

- $R_{nom}: 10\text{ m}\Omega$
- Tolerance: 0.1% (max)
- Drift: 15 ppm/°C (max)
- 4-terminal (Kelvin-connected)

3.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

- Single-supply (3V)
- Reference voltage input
- Low initial input offset voltage ($V_{os}$)
- Low-drift
- Fixed gain
- Low-side sensing (input common-mode range below ground)
For this design, a current shunt monitor (INA213B) was selected. The INA21x family topology is shown in Figure 3.

![INA21x Current Shunt Monitor Topology](image)

**Figure 3: INA21x Current Shunt Monitor Topology**

The INA213B has the following specifications:

- Supply Voltage Range: +2.7 V to +26 V
- Common-mode Input: -100 mV < V\text{cm} < +26 V
- Output swing (V+ = 3 V): 50 mV < V\text{out} < 2.8 V
- Reference voltage input
- V\text{os} = ±5 µV (typ)
- V\text{os-drift} = 0.1 µV/°C (typ)
- Fixed Gain = 50 V/V

Therefore, the INA213B is an excellent choice for this application. Other differential amplifiers were considered but ultimately eliminated for a variety of reasons. In general, instrumentation amplifiers that are powered with a single supply have limited output swing when the input common-mode voltage is near ground. In addition, they require external resistors to set their gain. This is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce the accuracy of the solution at small load currents. In addition, difference amplifiers typically have a gain of 1 V/V. When adjustable, however, they use external resistors which are not conducive to low-drift applications.
3.3 Reference

The reference for this application should have the following features:

- Dual output
  - 3.0V
  - 1.5V
- Low-drift

For this design, the REF2030 was selected. The REF20xx family topology is shown in Figure 4.

![Figure 4: REF20xx Topology](image)

The REF2030 has the following specifications:

- Input Voltage: 3.02V to 5.5 V
- \( V_{\text{BIAS}} \) output: 1.5 V
- \( V_{\text{REF}} \) output: 3.0 V
- Output Drift: 3 ppm/°C (typ), 8 ppm/°C (max)
- Output voltage accuracy = ±0.05% (max)
4 Simulation & Error Calculation

4.1 Simulation

Figure 5 depicts the TINA-TI® simulation schematic.

Figure 5: TINA-TI® Schematic

Figure 6 depicts the output for load currents ($I_{in}$) from -2.5 A to +2.5A. Notice the output is 1.5 V when the input current is 0 A. For positive current (0 A to 2.5 A) the output range is from 1.5 V to 2.75 V. Similarly, for negative currents (0 A to -2.5 A) the output range is from 1.5 V to 250 mV. This is consistent with the original design of the circuit.

Figure 6: Functionality Simulation
A 1000-point Monte-Carlo analysis of the circuit in Figure 5 was performed after setting the tolerance of $R_{\text{shunt}}$ to 0.1%. Figure 7 depicts a histogram of the output voltage at maximum load current.

![Figure 7: Output Voltage Histogram for Maximum Load (2.5 A)](image)

Please note that this does not include errors associated with temperature drift. In addition, only typical performance of the INA213B and REF2030 are modeled.

The distribution statistics for maximum and minimum load current are summarized in Table 2.

| Vout @ 2.5 A | 247.499021µV | 2.750031V |
| Vout @ -2.5 A | 250.06895mV | 250.065852mV |

Using the average (or mean) and the standard deviation from the simulation, a six-sigma ($\pm 3\sigma$) calculation of the full-scale error for maximum load (2.5 A) is calculated using Equation (4). This represents the error with 99.7% confidence.

$$E_{\%FSR} = 100 \times \frac{(\mu \pm 3\sigma) - V_{\text{out-ideal}}}{FSR} = \pm 0.031\%$$ (4)

Similarly, the error for minimum load current can be calculated using the same equation.

4.2 Simulated Results Summary

Table 3 is a summary of the simulated error results.

| Full Scale Error @ -2.5 A, 25°C | ±0.1% | ±0.032% |
| Full Scale Error @ +2.5 A, 25°C | ±0.1% | ±0.031% |
4.3 Error Calculation

Two types of errors will be discussed: initial accuracy and drift. Accuracy errors include:

- Shunt resistor tolerance: $\alpha_{\text{shunt, tol}} = 0.1\%$ (max)
- INA initial input offset voltage: $V_{\text{os,INA}} = 5\ \mu\text{V}$ (typ)
- INA PSRR: $V_{\text{os,INA}_{\text{PSRR}}} = 0.1\ \mu\text{V/V}$ (typ)
- INA CMRR: $V_{\text{os,INA}_{\text{CMRR}}} = 120\ \text{dB}$ (typ)
- INA gain error: $\alpha_{\text{INA}_{\text{GE}}} = 0.02\%$ (typ)
- Reference output accuracy: $\alpha_{\text{REF, output}} = 0.05\%$ (max)

It should be noted that these error sources can be greatly reduced at $25^\circ\text{C}$ by performing a two point system calibration. Drift errors, on the other hand, can only be reduced by performing the calibration over temperature. The drift errors include:

- Shunt resistor drift: $\delta_{\text{shunt, drift}} = 15\ \text{ppm/}^\circ\text{C}$ (max)
- INA offset voltage drift: $\delta_{\text{INA, drift, } V_{\text{os}}} = 0.1\ \mu\text{V/}^\circ\text{C}$ (typ)
- INA gain error drift: $\delta_{\text{INA, drift, GE}} = 3\ \text{ppm/}^\circ\text{C}$ (typ)
- Reference output drift: $\delta_{\text{REF, drift, output}} = 3\ \text{ppm/}^\circ\text{C}$ (typ)

Equation (5) can be used to convert specifications given in parts per million (ppm) to a percentage (%), and vice versa.

$$\% = \frac{\text{ppm}}{10,000} \quad (5)$$

Equation (6) can be used to convert specifications given in decibels (dB) to a linear representation.

$$\frac{V}{V} = \frac{1}{10^{\frac{\text{dB}}{20}}} \quad (6)$$

For some error calculations a full-scale range (FSR) is required. The FSR for this design is determined by the voltage across the shunt resistor, which is $\pm25\ \text{mV}$ (or 50 mV).

For drift errors, the largest change in temperature ($\Delta T$) is $100^\circ\text{C}$, which is the difference between the maximum specified temperature ($125^\circ\text{C}$) and room temperature ($25^\circ\text{C}$). This temperature change is used when calculating drift errors for the shunt resistor and INA213B. Since the REF2030 uses the box method to determine drift, the temperature range used for calculations is the entire operating range, or $165^\circ\text{C}$.

Finally, errors due to CMRR and PSRR specifications require an adjustment depending on the difference between the system’s requirements and how the devices were characterized. For example, the INA213B was characterized using a common-mode voltage of 12 V. The common-mode voltage in this design is $\sim0\text{V}$. This discrepancy causes an input-referred offset voltage.

All calculations for this system can be found in Appendix B.
4.3.1 Initial Accuracy

Table 4 summarizes the initial accuracy calculations from Appendix B.

<table>
<thead>
<tr>
<th>Error Source</th>
<th>$R_{\text{shunt}}$ (ppm)</th>
<th>INA213B (ppm)</th>
<th>REF2030 (ppm)</th>
<th>Total (ppm, RSS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td></td>
<td>100 FSR</td>
<td>500 FSR</td>
<td>510 FSR</td>
</tr>
<tr>
<td>CMRR</td>
<td></td>
<td>240 FSR</td>
<td>240 FSR</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td></td>
<td>4 FSR</td>
<td>4 FSR</td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td>1000</td>
<td>200</td>
<td></td>
<td>1020</td>
</tr>
<tr>
<td>Total (ppm, RSS)</td>
<td>1000</td>
<td>328 FSR</td>
<td>500 FSR</td>
<td>1165 FSR (0.117%)</td>
</tr>
</tbody>
</table>

4.3.2 Temperature Drift

Table 5 summarizes the total temperature drift calculations from Appendix B.

<table>
<thead>
<tr>
<th>Error Source</th>
<th>$R_{\text{shunt}}$ (ppm)</th>
<th>INA213B (ppm)</th>
<th>REF2030 (ppm)</th>
<th>Total (ppm, RSS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Drift</td>
<td>200 FSR</td>
<td>495</td>
<td></td>
<td>534 FSR</td>
</tr>
<tr>
<td>Gain Error Drift</td>
<td>1500</td>
<td>361 FSR</td>
<td>495</td>
<td>1621 FSR (0.24%)</td>
</tr>
<tr>
<td>Total (ppm, RSS)</td>
<td>1500</td>
<td>361 FSR</td>
<td>495</td>
<td></td>
</tr>
</tbody>
</table>

4.3.3 Total System Error

Equation (7) calculate the total system error over temperature.

$$E_{\text{system}} = \sqrt{1165\text{ppm}^2 + 162\text{ppm}^2} = 199\text{ppm} = 0.2\%$$ (7)
5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB layout is depicted in Figure 8. Please follow common PCB layout practices such as placing power supply bypass capacitors close to the devices’ supply pins. In addition, be sure to Kelvin-connect the shunt resistor. In this case, the shunt resistor has 4 terminals and is already Kelvin-connected. Finally, be sure to minimize any impedance between the shunt and ground plane. This was accomplished by pouring the ground plane without thermal relief spokes and placing the GND connection as close to $R_{\text{shunt}}$ as possible.

![Figure 8: PCB Layout](image-url)
6 Verification & Measured Performance

6.1 Transfer Function

Data was collected by sweeping the load current from -2.5A to +2.5A and measuring the output of the INA213B. In addition, the load current, reference voltage, and bias voltage were measured. Finally, data was taken at the following temperatures: -40°C, -25°C, 0°C, 25°C, 50°C, 85°C, and 125°C.

Figure 9 depicts the measured transfer function of the design at 25°C.

![Graph: Vout vs. Load Current (25°C)](image-url)
6.2 Un-calibrated Error

Equation (8) was used to calculate the error for each measurement sweep. Un-calibrated error includes both initial accuracy errors (e.g., offset voltage, CMRR, etc.) and errors associated with temperature drift.

Note that the load current was measured and used in the calculations as the ideal load current. This removes any errors associated with the generation of the load current.

\[ E_{\%FSR} = 100 \times \frac{V_{out-meas} - V_{out-ideal}}{FSR} \] (8)

Where

\[ V_{out-ideal} = V_{bias-ideal} + (I_{load-meas} \times R_{shunt-ideal} \times G_{ideal}) = 1.5V + \left( I_{load-meas} \times 10\,\Omega \times 50\,\frac{V}{V} \right) \] (9)

\[ FSR = V_{out-max-ideal} - V_{out-min-ideal} = 2.75V - 250mV = 2.5V \] (10)

Figure 10 depicts the measured error versus load current for all temperatures.

The largest error (-522 ppm) occurs at maximum load current and an ambient temperature of 125°C. The typical calculated error for this design is ±1996 ppm.
Figure 11 shows the measured error of this system with respect to the calculated error limits.

![Figure 11: Total Unadjusted Error with Min/Max Error Limits](image)

6.3 Calibration

Performing a 2-point calibration at 25°C removes the errors associated with offset voltage, gain error, etc. The two data points selected for this calibration occur at ~25% and ~75% of the full load current range, or -1.88623 A and +1.88613 A, respectively. Table 6 depicts the data required for the calibration.

<table>
<thead>
<tr>
<th></th>
<th>I_{load(25%)} = -1.88623A</th>
<th>I_{load(75%)} = +1.88613A</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{out} (V)</td>
<td>Measured (M)</td>
<td>Ideal (I)</td>
</tr>
<tr>
<td>V_{out} (V)</td>
<td>0.556213</td>
<td>0.556885</td>
</tr>
</tbody>
</table>

The gain correction factor (α) and offset correction factor (β) are calculated as shown in Equations (11) and (12), respectively. It is important to note that these values are not gain or offset error terms.

\[
\alpha = \frac{V_{out-ideal@75\%} - V_{out-ideal@25\%}}{V_{out-meas@75\%} - V_{out-meas@25\%}} = \frac{2.443065 - 0.556885}{2.44315 - 0.556213} = 0.99959882 \tag{11}
\]

\[
\beta = (\alpha \times V_{out-meas@25\%}) - V_{out-ideal@25\%} = (0.99959882 \times 0.556213) - 0.556885 = -896.14153134 \mu \tag{12}
\]
Equation (13) can be applied to the un-calibrated output voltage to obtain the calibrated output voltage.

\[ V_{\text{out-cal}} = (V_{\text{out-uncal}} - \beta) \times \alpha \]  

(13)

Figure 12 compares the un-calibrated and calibrated performance at 25°C.

The error decreased from -355 ppm to -40.5 ppm. Applying the correction factors from the 25°C data to error curves with a similar, positive slope will decrease the error. However, applying the correction factors to an error curve with a negative slope can actually increase the error.
Figure 13 shows that the error at 125°C increased from -522 ppm to -606 ppm after applying the 25°C correction factors.

![Error vs. Load Current (125°C)](image)

Figure 13: Effect of 25°C Calibration Factors at 125°C

Figure 14 shows the calibrated error for all temperatures. The largest error (-606 ppm) occurs at maximum load current and an ambient temperature of 125°C. This error is larger than the un-calibrated solution. Therefore, if the un-calibrated error is unacceptable, a multi-temperature calibration is required.

![Calibrated Error vs. Load Current](image)

Figure 14: Effects of 25°C Calibration Factors on All Temps
Table 7 summarizes the measured results.

<table>
<thead>
<tr>
<th>Measured</th>
<th>Goal</th>
<th>Un-calibrated</th>
<th>Calibrated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Scale Range Error (25°C)</td>
<td>±0.1%</td>
<td>±0.0355%</td>
<td>±0.004%</td>
</tr>
<tr>
<td>Full Scale Range Error (-40°C to 125°C)</td>
<td>±0.15%</td>
<td>±0.0522%</td>
<td>±0.0606%</td>
</tr>
</tbody>
</table>

7 Modifications

The shunt resistor may be increased/decreased depending on the load current range. In order to maintain the output voltage range, however, the current shunt monitor gain should be increased or decreased accordingly. Please note that current shunt monitors typically have fixed gains. If the load current increases, be sure to keep in mind the power that needs to be dissipated by the shunt resistor.

Besides the shunt resistor and current shunt monitor, the REF2030 may be replaced with a discrete solution. The following section will show the complete analysis for such a modification.

7.1 Discrete Topology

A common method for generating the supply voltage ($V_{REF}$) and reference voltage ($V_{BIAS}$) is shown in Figure 15. This method uses 4 discrete components: reference, voltage divider ($R_1$ and $R_2$), and a buffer amplifier. The output of the reference device is divided down according to Equation (14).

$$V_{BIAS} = V_{REF} \times \frac{R_2}{R_1 + R_2}$$

Figure 15: Discrete Topology
The drift performance of $V_{\text{REF}}$ ($\delta_{V_{\text{REF}}}$) is determined by the reference drift. Table 8 compares low-drift reference devices with the REF2030.

**Table 8. Low-drift Reference Comparison**

<table>
<thead>
<tr>
<th>Device</th>
<th>Output (V)</th>
<th>Drift (ppm/°C, typ)</th>
<th>Drift Tracking (ppm/°C, typ)</th>
<th>Accuracy (max)</th>
<th>Cost (1ku)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF2030</td>
<td>3.0</td>
<td>3</td>
<td>2</td>
<td>0.05%</td>
<td>$1.40</td>
</tr>
<tr>
<td>REF5030</td>
<td>3.0</td>
<td>2.5</td>
<td>N/A</td>
<td>0.05%</td>
<td>$2.95</td>
</tr>
<tr>
<td>REF5030A</td>
<td>3.0</td>
<td>3</td>
<td>N/A</td>
<td>0.1%</td>
<td>$1.35</td>
</tr>
<tr>
<td>REF3230</td>
<td>3.0</td>
<td>4</td>
<td>N/A</td>
<td>0.2%</td>
<td>$1.70</td>
</tr>
</tbody>
</table>

The REF5030A was selected because of cost and accuracy.

The drift performance of the $V_{\text{BIAS}}$ output will depend on the drifts of the reference ($\delta_{\text{REF}}$), resistor divider network ($\delta_{\text{RDIV}}$), and buffer amplifier ($\delta_{\text{BUF}}$). Equation (15) depicts the total drift for the $V_{\text{BIAS}}$ output ($\delta_{\text{Vbias}}$).

$$\delta_{\text{Vbias}} = \sqrt{\delta_{\text{REF}}^2 + \delta_{\text{RDIV}}^2 + \delta_{\text{BUF}}^2}$$  \hspace{1cm} (15)

As shown by Equation (16), the drift tracking between $V_{\text{ref}}$ and $V_{\text{bias}}$ is determined by $\delta_{\text{RDIV}}$ and $\delta_{\text{BUF}}$ since $\delta_{\text{REF}}$ is common to both outputs.

$$\delta_{\text{tracking}} = \sqrt{\delta_{\text{RDIV}}^2 + \delta_{\text{BUF}}^2}$$  \hspace{1cm} (16)

The drift and accuracy of the resistor divider network is determined by the drift and tolerance of one of the resistors. For a comparable low-drift solution, each resistor should have no more than 5 ppm/°C drift and a tolerance of 0.1% or less. As of the publication of this document, the following resistor was selected as the most appropriate choice:

- PCF0603-13-4K99BT1
  - Resistance: 4.99kΩ
  - Tolerance: 0.1%
  - Drift: 5 ppm/°C
  - Total Cost (1ku): $0.48 ($0.24 each)

The drift of the buffer amplifier’s error contributions are not as significant as the reference or resistor divider because the full-scale range (FSR) is 1.5V. Targeting 0.1% error due to input offset voltage and 1 ppm/°C drift error, the amplifier should have less than 1.5 mV offset voltage and 1.5 μV/°C drift.

Table 9 lists op amps that should be considered for the discrete solution.

**Table 9. Op Amps for Discrete Topology**

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{\text{os}}$ (mV, max)</th>
<th>$V_{\text{os}}$ Drift (μV/°C, max)</th>
<th>Bandwidth (MHz)</th>
<th>$I_q$ (mA, max)</th>
<th>Cost (1ku)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA377</td>
<td>1.0</td>
<td>2</td>
<td>5.5</td>
<td>1.05</td>
<td>$0.40</td>
</tr>
<tr>
<td>OPA336NA</td>
<td>0.5</td>
<td>1.5 (typ)</td>
<td>0.1</td>
<td>0.032</td>
<td>$0.65</td>
</tr>
<tr>
<td>LMV831</td>
<td>1.0</td>
<td>1.5</td>
<td>3.3</td>
<td>0.27</td>
<td>$0.40</td>
</tr>
</tbody>
</table>

The LMV831 is the amplifier of choice due to performance, power, and cost. Note that if the LMV831 is supplied by $V_{\text{REF}}$, there will be no additional error due to CMRR.
Table 10 compares the discrete topology (LMV831, REF5030A, and PCF0603-13-4K99RBT1) with the REF2030 over temperature. The error calculations for the discrete solution can be found in Appendix C.

<table>
<thead>
<tr>
<th>Device(s)</th>
<th>Output</th>
<th>Accuracy (ppm)</th>
<th>Drift (ppm)</th>
<th>Total (ppm, RSS)</th>
<th>Tracking (ppm/°C, max)</th>
<th>Matching (ppm, 25°C)</th>
<th>Cost (1ku)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF2030</td>
<td>3.0V, 1.5V</td>
<td>500</td>
<td>495</td>
<td>704</td>
<td>7</td>
<td>100</td>
<td>$1.40</td>
</tr>
<tr>
<td>LMV831, REF5030A</td>
<td>V_ref (3.0V)</td>
<td>1000</td>
<td>495</td>
<td>1116</td>
<td>5</td>
<td>1014 (FSR, RSS)</td>
<td>$2.23</td>
</tr>
<tr>
<td></td>
<td>V_bias (1.5V)</td>
<td>1424</td>
<td>704</td>
<td>1941</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

While the performance of V_ref in the discrete topology is close to the REF2030, the V_bias output has considerably more error. Note that the total error for V_bias includes the error from V_ref. While the tracking of the two outputs is slightly better for the discrete topology, the matching of the outputs is dominated by the resistor divider accuracy and offset voltage of the buffer amplifier.

For approximately triple the cost the accuracy of the discrete topology could be increased by selecting 0.01% resistors. This would reduce the V_bias accuracy error to 1019 ppm, the V_bias total error to 1667 ppm, and the matching error to 194 ppm.

Despite the additional cost and error, the discrete solution has great value when V_bias ≠ V_ref/2. The resistor divider can be adjusted accordingly. However, this will introduce an error due to the CMRR of the device. The analysis will be similar to that of the PSRR error calculation.

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments’ difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University’s Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

Timothy Claycomb joined the Precision Linear Applications team in February 2014. Before joining the team, he was an intern in the summer of 2013. Timothy received his BSEE from Michigan State University.

9 Acknowledgements & References

The authors would like to thank Collin Wells and Art Kay for their technical contributions to this design.
Appendix A.

A.1 Electrical Schematic

![Electrical Schematic Diagram]

Figure A-1: Electrical Schematic

A.2 Bill of Materials

<table>
<thead>
<tr>
<th>Item #</th>
<th>Quantity</th>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Supplier Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>C1</td>
<td>10μF</td>
<td>CAP, TA, 10μF, 25V, +/-10%, 0.5 μm, SMD</td>
<td>AVX</td>
<td>TPSC10R625R0500</td>
<td>478-1762-1-ND</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C2</td>
<td>1μF</td>
<td>CAP, CERM, 1μF, 16V, +/-10%, X7R, 0603</td>
<td>TDK</td>
<td>C1606X7R1C105K080AC</td>
<td>445-1604-1-ND</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>C3, C4, C6</td>
<td>0.1μF</td>
<td>CAP, CERM, 0.1μF, 25V, +/-10%, X7R, 0603</td>
<td>AVX</td>
<td>06033C104K047A</td>
<td>478-3741-1-ND</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>C5, C7</td>
<td>220μF</td>
<td>CAP, CERM, 220μF, 25V, +/-10%, C0G, X7R, 0603</td>
<td>AVX</td>
<td>06035A101J102A</td>
<td>478-1175-1-ND</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>Rshunt</td>
<td>100ohm</td>
<td>RES, 0.010, 1%, 1W, CS2512</td>
<td>Vishay Resistor</td>
<td>Y14870R01000B6W</td>
<td>Y1487-01-ND</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>Vout</td>
<td>White</td>
<td>Test Point, Compact, White, TH</td>
<td>Keystone</td>
<td>5007</td>
<td>5007K-N</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>VCC</td>
<td>Red</td>
<td>Test Point, TH, Compact, Red</td>
<td>Keystone</td>
<td>5005</td>
<td>5005K-N</td>
</tr>
<tr>
<td>8</td>
<td>4</td>
<td>GND</td>
<td>Black</td>
<td>Test Point, TH, Compact, Black</td>
<td>Keystone</td>
<td>5006</td>
<td>5006K-N</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>Vbias</td>
<td>Yellow</td>
<td>Test Point, Compact, Yellow, TH</td>
<td>Keystone</td>
<td>5009</td>
<td>5009K-N</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>Vref</td>
<td>Orange</td>
<td>Test Point, Compact, Orange, TH</td>
<td>Keystone</td>
<td>5008</td>
<td>5008K-N</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>in</td>
<td>Yellow</td>
<td>Test Point, Compact, Yellow, TH</td>
<td>Keystone</td>
<td>5000</td>
<td>5000K-N</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>U1</td>
<td>IC CFAMP CURR SENSE 14KHZ 9070-6</td>
<td>Texas Instruments</td>
<td>INA213BDCK</td>
<td>INA213BDCKR-N</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>U2</td>
<td>Dual output, low-drift reference</td>
<td>Texas Instruments</td>
<td>REF2030ADDC</td>
<td>REF2030ADDC</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>4</td>
<td>N/A</td>
<td>STANDOFF HEX 4-40TH ALUM 1/2</td>
<td>Keystone</td>
<td>2205</td>
<td>2205K-N</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>4</td>
<td>N/A</td>
<td>MACHINE SCREW PAN PHILLIPS 4-40</td>
<td>B&amp;F Fastener Supply</td>
<td>PMSSS 440 0005 PH</td>
<td>H703-N</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>1</td>
<td>N/A</td>
<td>PCB FOR TI REF DESIGN TIPD156</td>
<td>American PCB Company</td>
<td>TIPD156</td>
<td>TIPD156</td>
<td></td>
</tr>
</tbody>
</table>

Figure A-2: Bill of Materials
Appendix B.

B.1 MATHCAD Calculations

System Specifications

\[ R_{\text{shunt}} = 10 \cdot 10^{-3} \Omega \]

\[ I_{\text{load\_max}} = 2.5 \text{A} \quad I_{\text{load\_min}} = -2.5 \text{A} \]

\[ V_{\text{shunt\_max}} = R_{\text{shunt}} I_{\text{load\_max}} = 25 \times 10^{-3} \text{V} \]

\[ V_{\text{shunt\_min}} = R_{\text{shunt}} I_{\text{load\_min}} = -25 \times 10^{-3} \text{V} \]

\[ \text{FSR} := V_{\text{shunt\_max}} - V_{\text{shunt\_min}} = 50 \times 10^{-3} \text{V} \]

\[ T_{\text{ambient}} := 25 \text{C} \]

\[ T_{\text{max}} := 125 \text{C} \]

\[ \Delta T := T_{\text{max}} - T_{\text{ambient}} = 100 \times 10^0 \text{C} \]

Conversions

\[ \text{dB}(x) := 10 \frac{\text{V}}{\text{V}} \times 20 \]

\[ \text{ppm} := \frac{1}{1000000} \]

Shunt Resistor Errors

Accuracy

\[ E_{\text{shunt\_tol}} = \alpha_{\text{shunt\_tol}} = 1 \times 10^3 \text{ppm} \]

Drift

\[ E_{\text{shunt\_drift}} = \Delta T \cdot \delta_{\text{shunt\_drift}} = 1.5 \times 10^3 \text{ppm} \]

Shunt Specifications

\[ \alpha_{\text{shunt\_tol}} = 0.1\% \]

\[ \delta_{\text{shunt\_drift}} = 15 \frac{\text{ppm}}{\text{C}} \]
INA213 Errors

INA Accuracy Specifications

\[ V_{os_{-}INA} := 5 \mu V \quad V_{s_{-}INA_{-}spec} := 5V \quad V_{s_{-}INA_{-}sys} := 3V \]

\[ V_{os_{-}INA}^{PSRR} := 0.1 \frac{\mu V}{V} \quad \alpha_{INA_{-}GE} := 0.02\% \]

\[ V_{cm_{-}INA_{-}spec} := 12V \quad V_{cm_{-}sys} := 0V \quad V_{os_{-}INA_{-}CMRR} := \text{dB(120)} = 1 \times 10^{0} \frac{\mu V}{V} \]

Accuracy

\[ E_{INA_{-}Vos} := \frac{V_{os_{-}INA}}{FSR} = 100 \times 10^{0} \text{ ppm} \]

\[ E_{INA_{-}PSRR} := \left( \frac{V_{s_{-}INA_{-}spec} - V_{s_{-}INA_{-}sys}}{V_{os_{-}INA_{-}PSRR}} \right) \frac{V_{os_{-}INA}}{FSR} = 4 \times 10^{0} \text{ ppm} \]

\[ E_{INA_{-}GE} := \alpha_{INA_{-}GE} = 200 \times 10^{0} \text{ ppm} \]

\[ E_{INA_{-}CMRR} := \left( \frac{V_{cm_{-}INA_{-}spec} - V_{cm_{-}sys}}{V_{os_{-}INA_{-}CMRR}} \right) \frac{V_{os_{-}INA}}{FSR} = 240 \times 10^{0} \text{ ppm} \]

Drift

\[ E_{INA_{-}drift_{-}GE} := \Delta T \cdot \delta_{INA_{-}drift_{-}GE} = 300 \times 10^{0} \text{ ppm} \]

\[ E_{INA_{-}drift_{-}Vos} := \left( \frac{V_{os_{-}INA_{-}drift}}{FSR} \right) \Delta T = 200 \times 10^{0} \text{ ppm} \]

INA Drift Specification:

\[ \delta_{INA_{-}drift_{-}GE} = 3 \frac{\text{ppm}}{C} \]

\[ V_{os_{-}INA_{-drift}} := 0.1 \frac{\mu V}{C} \]
REF2030 Errors

**Accuracy**

\[ E_{\text{REF\_output}} = \alpha_{\text{REF\_output}} = 500 \times 10^0 \text{ ppm} \]

**Drift**

\[ E_{\text{REF\_drift}} = (165C) \cdot \delta_{\text{REF\_drift\_output}} = 495 \times 10^0 \text{ ppm} \]

**REF Accuracy Specifications**

\[ \alpha_{\text{REF\_output}} = 0.05\% \]

**REF Drift Specifications**

\[ \delta_{\text{REF\_drift\_output}} = \frac{3 \text{ ppm}}{C} \]

**System Error**

**Accuracy**

\[
E_{\text{accuracy\_RSS}} = \sqrt{E_{\text{REF\_output}}^2 + E_{\text{INA\_CMRR}}^2 + \ldots + E_{\text{INA\_GE}}^2 + E_{\text{INA\_PSRR}}^2 + \ldots + E_{\text{INA\_Vos}}^2 + E_{\text{shunt\_tol}}^2} = 1.165 \times 10^3 \text{ ppm}
\]

\[ E_{\text{accuracy\_total}} = E_{\text{REF\_output}} + E_{\text{INA\_CMRR}} + E_{\text{INA\_GE}} + \ldots + E_{\text{INA\_PSRR}} + E_{\text{INA\_Vos}} + E_{\text{shunt\_tol}} = 2.044 \times 10^3 \text{ ppm} \]

**Drift**

\[
E_{\text{drift\_RSS}} = \sqrt{E_{\text{REF\_drift}}^2 + E_{\text{INA\_drift\_Vos}}^2 + \ldots + E_{\text{INA\_drift\_GE}}^2 + E_{\text{shunt\_drift}}^2} = 1.62 \times 10^3 \text{ ppm}
\]

\[ E_{\text{drift\_total}} = E_{\text{REF\_drift}} + E_{\text{INA\_drift\_Vos}} + E_{\text{INA\_drift\_GE}} + E_{\text{shunt\_drift}} = 2.495 \times 10^3 \text{ ppm} \]

**Total**

\[
E_{\text{total\_RSS}} = \sqrt{E_{\text{accuracy\_RSS}}^2 + E_{\text{drift\_RSS}}^2} = 1.996 \times 10^3 \text{ ppm}
\]

\[ E_{\text{total}} = E_{\text{accuracy\_total}} + E_{\text{drift\_total}} = 4.539 \times 10^3 \text{ ppm} \]
Appendix C.

C.1 MATHCAD Calculations for Discrete Solution

System Specifications

FSR := 1.5V

T_{ambient} = 25°C  T_{max} = 125°C

\Delta T := T_{max} - T_{ambient} = 100 \times 10^0°C

V_{s_buf} := 3.0V

V_{s_spec} := 3.3V

Conversions

\text{dB}(x) := \frac{1}{10} \log_{10} \left( \frac{V}{x} \right) \quad \text{ppm} := \frac{1}{1000000} \left( \frac{V}{x} \right)

Resistor Divider Errors

Accuracy

E_{res_tol} := \alpha_{res_tol} = 1 \times 10^3 \cdot \text{ppm}

\Delta \text{res_drift} := \Delta T \cdot \delta_{res_drift} = 500 \times 10^0 \cdot \text{ppm}

Resistor Specifications

\alpha_{res_tol} := 0.1\%

\delta_{res_drift} := 5 \text{ ppm}/\text{C}

Buffer Amplifier Errors

Accuracy

E_{buf_{Vos}} = \frac{V_{os_typ}}{FSR} = 166.667 \times 10^0 \cdot \text{ppm}

V_{os_typ} := 0.25\text{mV}

V_{os_PSRR} := \text{dB}(93) = 22.387 \times 10^0 \frac{\mu\text{V}}{\text{V}}

V_{os_drif} := 0.5 \frac{\mu\text{V}}{\text{C}}

\text{ppm}

E_{buf_{PSRR}} = \left( \frac{V_{s_spec} - V_{s_buf}}{FSR} \right) \cdot V_{os_PSRR} = 4.477 \times 10^0 \cdot \text{ppm}

Drift

E_{buf_{drift_{Vos}}} = \frac{V_{os_drif}}{FSR} \cdot \Delta T = 33.333 \times 10^0 \cdot \text{ppm}
Reference Errors

Accuracy

$$E_{\text{REF\_output}} = \alpha_{\text{REF\_output}} \times 1 \times 10^3 \text{ ppm}$$

Drift

$$E_{\text{REF\_drift}} = 165 \times \delta_{\text{REF\_drift\_output}} \times 495 \times 10^0 \text{ ppm}$$

Reference Specifications

- $$\alpha_{\text{REF\_output}} = 0.1\%$$
- $$\delta_{\text{REF\_drift\_output}} = \frac{3 \text{ ppm}}{C}$$

Alternate System Error

Vref Accuracy

$$E_{\text{accuracy\_vref}} = E_{\text{REF\_output}} = 1 \times 10^3 \text{ ppm}$$

Vref Drift

$$E_{\text{drift\_vref}} = E_{\text{REF\_drift}} = 495 \times 10^0 \text{ ppm}$$

Vref Total

$$E_{\text{total\_vref\_RSS}} = \sqrt{E_{\text{accuracy\_vref}}^2 + E_{\text{drift\_vref}}^2} = 1.116 \times 10^3 \text{ ppm}$$

$$E_{\text{total\_vref}} = E_{\text{accuracy\_vref}} + E_{\text{drift\_vref}} = 1.495 \times 10^3 \text{ ppm}$$
Vbias Accuracy

\[ E_{\text{accuracy\_bias\_RSS}} = \sqrt{E_{\text{res\_tol}}^2 + E_{\text{buf\_Vos}}^2 + E_{\text{buf\_PSRR}}^2 + E_{\text{REF\_output}}^2} = 1.424 \times 10^3 \text{ ppm} \]

\[ E_{\text{accuracy\_bias\_total}} = E_{\text{res\_tol}} + E_{\text{buf\_Vos}} + E_{\text{buf\_PSRR}} + E_{\text{REF\_output}} = 2.171 \times 10^3 \text{ ppm} \]

Vbias Drift

\[ E_{\text{drift\_bias\_RSS}} = \sqrt{E_{\text{res\_drift}}^2 + E_{\text{buf\_drift\_Vos}}^2 + E_{\text{REF\_drift}}^2} = 704.369 \times 10^0 \text{ ppm} \]

\[ E_{\text{drift\_bias\_total}} = E_{\text{res\_drift}} + E_{\text{buf\_drift\_Vos}} + E_{\text{REF\_drift}} = 1.028 \times 10^3 \text{ ppm} \]

Vbias Total

\[ E_{\text{total\_bias\_RSS}} = \sqrt{E_{\text{total\_vref\_RSS}}^2 + E_{\text{accuracy\_bias\_RSS}}^2 + E_{\text{drift\_bias\_RSS}}^2} \]

\[ E_{\text{total\_bias}} = E_{\text{accuracy\_bias\_total}} + E_{\text{drift\_bias\_total}} = 3.199 \times 10^3 \text{ ppm} \]

Matching

\[ \alpha_{\text{matching}} = \sqrt{\alpha_{\text{res\_tol}}^2 + \left(\frac{V_{\text{os\_max}}}{\text{FSR}}\right)^2} = 1.014 \times 10^{-3} \]

\[ \alpha_{\text{matching}} = 1.014 \times 10^3 \text{ ppm} \]

Tracking

\[ \delta_{\text{tracking\_total}} = \delta_{\text{res\_drift}} + \frac{V_{\text{os\_drift}}}{\text{FSR}} = 5.333 \times 10^1 \text{ ppm} \]
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