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16-Bit Analog Mixed Input and Output Module for Programmable Logic Controllers (PLCs)

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Design Resources

TIDA-00170	I/P and O/P Module Design
TIDA-00123	I/O Controller Design Files
ADS8688	Product Folder
DAC8760	Product Folder
ISO7421	Product Folder
SN74HC595	Product Folder
LM5069	Product Folder
LM5017	Product Folder
ISO7141	Product Folder
TPS7A1650	Product Folder
TPS7A3001	Product Folder
TPS7A4700	Product Folder

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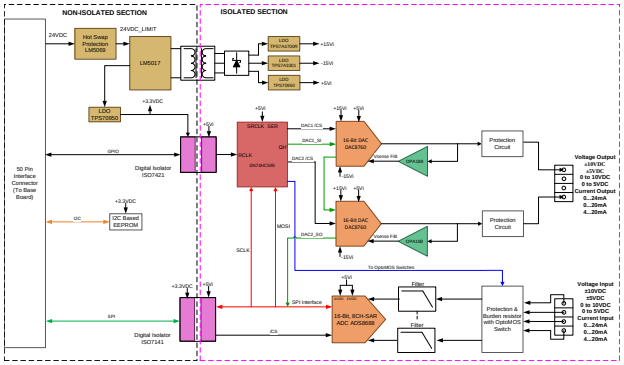
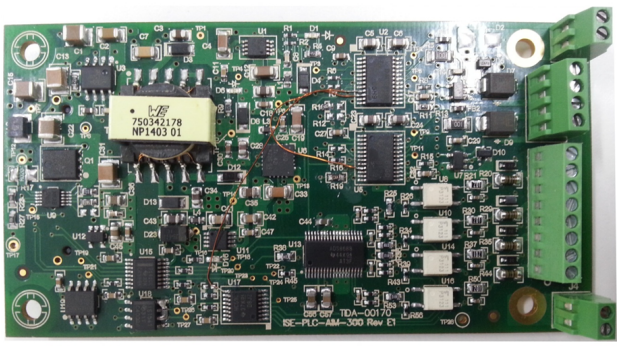
Design Features

- Four Channel User Programmable Analog Inputs:
  - Voltage I/P: (Typical ZIN 1 MΩ) up to ±10 V
  - Current I/P: (Typical ZIN 300 Ω) up to 24 mA
  - Sampling Rate up to 300 kSPS (Single Channel)
  - Accuracy up to ±0.1% FSR at 25°C
- Two Selectable Analog Output Channels:
  - Current O/P: Up to 24 mA
  - Voltage O/P: Up to ±10 V
  - Accuracy up to ±0.2% FSR at 25°C
- Onboard Isolated Fly-Buck™ Power Supply with Inrush Current Protection
- Slim Form Factor 96 × 50.8 × 10 mm (L × W × H)
- Pluggable to I/O Controller Platform (TIDA-00123) for Easy Evaluation
- LabView™-Based GUI for Signal-Chain Analysis and Functional Testing
- Designed to Comply with IEC61000-4 Standards for ESD, EFT, and Surge

Featured Applications

- PLC: Current and Voltage Input Module
- Remote PLCs and DCS
- Data Acquisition Systems
- Test and Measurement





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1 System Overview

The TIDA-00170 is a reference design for industrial control analog mixed I/O module. The reference design is suitable for process control end equipment like programmable logic controllers (PLCs), distributed control systems (DCS), and data acquisition systems (DAS). The modules digitize standard industrial voltage-current inputs, bipolar or unipolar voltage ranges up to ±10 V, and control using analog signal voltage and current. Analog outputs are commonly used to control actuators, valves, and motors in industrial environment the modules employ standard analog output ranges such as ±5 V, ±10 V, 0 to 5 V, 0 to 10 V, 4 to 20 mA, 0 to 20 mA, or 0 to 24 mA.

In this reference design, the analog input channels can measure all standard industrial voltages up to ±10 V and current inputs up to 24 mA. Four channels are provided on the module, and each channel can be software configured as current or voltage input. The SAR-based architecture of the ADS8688 ADC provides better sampling rate than delta-sigma architecture, and on-chip PGA allows flexible input ranges.

The module features two simultaneous outputs with 16-bit resolution; the voltage output can be used to provide an input to a microprocessor-based data acquisition or control system while the current output can be used for analog transmission, operator interface, or an analog backup system.

For functional isolation of the digital signals between the host microcontroller and the measurement side, especially to achieve high common mode performance two digital isolators, the ISO7141 and the ISO7421 are used. The isolation of the power supply is achieved using an LM5017-based Fly-Buck converter. The module has an onboard EEPROM to store calibration data and module configuration data. This reference design also highlights the TI products like the inrush current-limit controller; isolated Fly-Buck controller, low noise LDO, and shift register expander that can be used in the PLC signal chain.

The module has been designed to be pluggable to the I/O controller platform (TIDA-00123) for quick testing and evaluation. Input and output channels include protection circuitry that has been tested and verified to comply with IEC61000-4 standards for electrostatic discharge (ESD), electrical fast transient (EFT), and surge requirements with an I/O controller platform.

The schematics, BOM, PCB layout (Altium tool), Gerber, Tiva™ C Series MCU software, and the executable for an easy-to-use graphical user interface (GUI) are also provided (see Section 9).

2 Design Specification

Table 1 provides specifications of the Analog Input Output Module.

Table 1. Specifications of Analog Input Output Module

PARAMETER	SPECIFICATIONS AND FEATURES	
ANALOG INPUT		
Number of channels	Four channels (Voltage/Current programmable)	
I/O range	Voltage: • ±10 V • ±5 V • ±2.5 V • 0 to 10 V • 0 to 5 V	Current: • 0 to 20 mA • 4 to 20 mA • 0 to 24 mA
Input impedance (ZIN)	Voltage >1 MΩ	Current <300 Ω
Overall accuracy (un-calibrated)	Voltage input: ±0.1% FSR at 25°C	Current Input: ±0.1% FSR at 25°C
Sampling speed	300 kSPS (with digital isolation)	
ANALOG OUTPUT		
Number of channels	Two channels (Voltage and current programmable)	
Output range	Voltage: • ±10 V • ±5 V • 0 to 10 V • 0 to 5 V	Current: • 0 to 20 mA • 4 to 20 mA • 0 to 24 mA
Overall accuracy (un-calibrated)	Voltage input: ±0.2% FSR at 25°C	Current input: ±0.2% FSR at 25°C
Settling time	500 nS	
Power supply isolation	250-V DC (continuous) 1500-V AC for one minutes (withstand)	
ESD immunity	IEC 61000-4-2: • 4-kV contact discharges • 8-kV air discharges	
EFT immunity	IEC 61000-4-4: ±2 kV at 5 kHz on signal ports	
Surge transient immunity	IEC 61000-4-5: ±1 kV line-earth (CM) on signal ports	
Operating temp. range	0°C to 60°C	
Storage temperature	–40°C to 85°C	
Form factor (L × W)	90 × 50.8 mm (small industrial form factor)	

3 Block Diagram

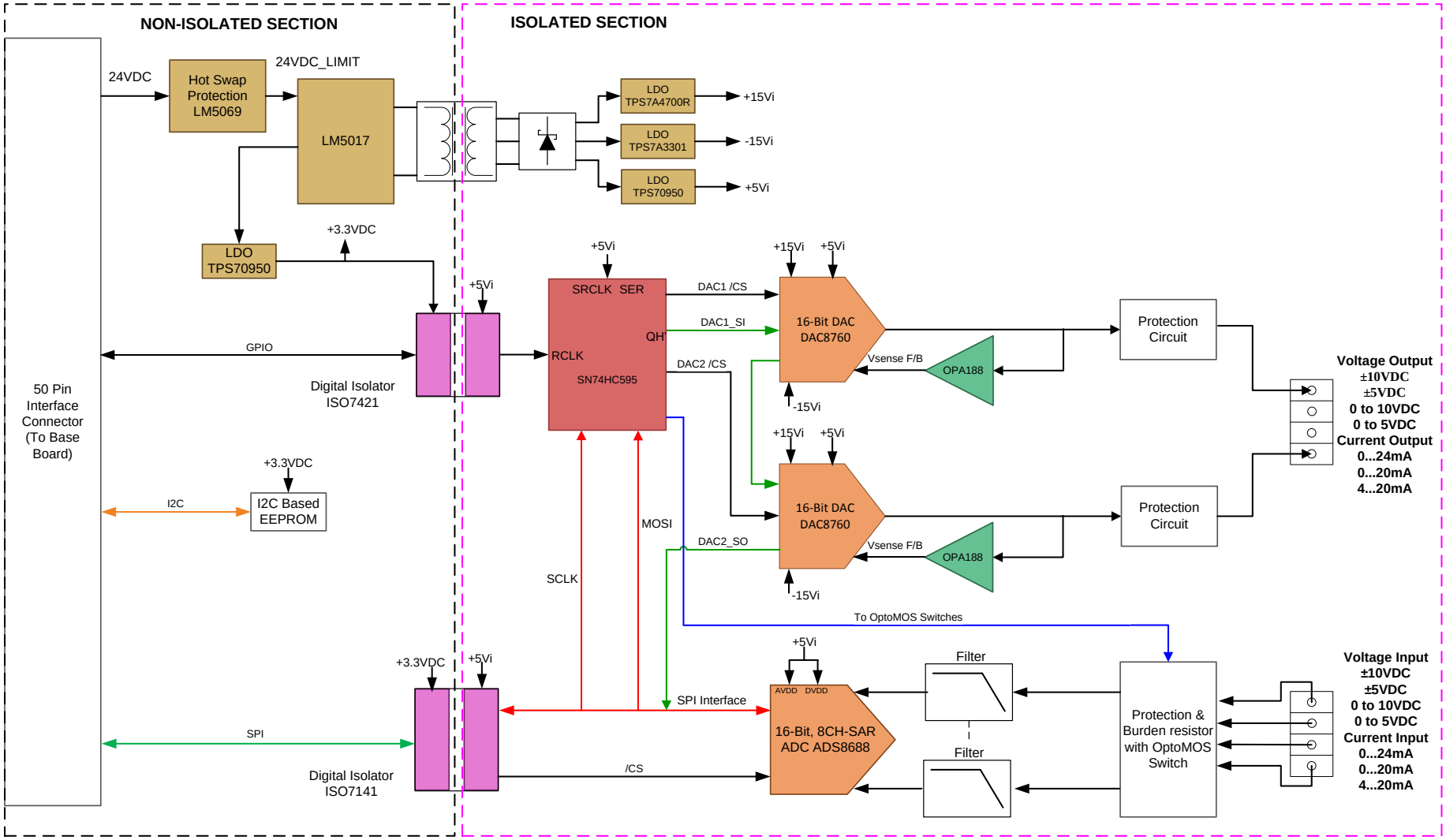


Figure 1. System Block Diagram

4 Highlighted Products

The module has four analog input channels and two analog output channels. Each analog input channel can be configured as a current or voltage input with software configuration. The design utilizes the ADS8688, a 16-bit, single-supply SAR ADC, with on-chip PGA and reference. The on-chip PGA provides high input impedance (typically 1 MΩ) and the filter rejects noise interference. The on-chip 4.096-V ultra-low drift voltage reference is used as the reference for the ADC core.

For the analog output, the design uses 16-bits resolution DAC8760 digital-to-analog converter (DAC). The device can be programmed as a current output with a range of 4 to 20 mA, 0 to 20 mA, or 0 to 24 mA, or as a voltage output with a range of 0 to 5 V, 0 to 10 V, ±5 V, or ±10 V with a 10% overrange (0 to 5.5 V, 0 to 11 V, ±5.5 V, or ±11 V). For wiring flexibility, the module outputs of both voltage and current are placed on a single terminal, this arrangement reduces the number of connectors and hence benefits cost reduction.

Both the DAC and ADC can be configured through SPI interface. To save number of isolators, shift register SN74HC595 and two DACs are configured in daisy chain mode. The ADC has a separate slave select line, which is directly controlled by the host microcontroller. The digital isolation is achieved using ISO7141 and ISO7421. The host microcontroller communicates over SPI bus with SN74HC595 – Shift register used as IO expander. The shift register controls the TLP3123 - Low RON Opto-switch which is used to switch between voltage to current input modes and LATCH pins of both the DACs. The input channel configuration is done in microcontroller firmware.

A low cost LM5017, a constant on-time synchronous buck regulator in Fly-Buck configuration with an external transformer, is used to generate isolated power supply. The LM5017 has a wide input supply range, making it ideal for accepting a 24-V industrial supply. The device can accept up to 100 V, making it reliable against input transients. The Fly-Buck power supply isolates and steps down the input voltage down to 6 V, 18 V, and –18 V connecting the low dropout (LDO) regulators to generate regulated voltage rails of 5 V, 15 V, and –15 V to power the ADS8688, DAC8760 DVDD, and other circuitry. The LM5017 features a number of other safety and reliability functions, such as undervoltage lockout (UVLO), thermal shutdown, and peak current limit protection. The module is hot-swappable, so it can be inserted or removed from socket in the backplane without disturbing system power. The hot-swappable feature is accomplished using LM5069.

I/O analog signals are protected against high voltage fast transient events often expected in an industrial environment. The protection circuitry makes use of TVS and ESD diodes. The RC low-pass mode filters are used on each analog input before it reaches to ADS8688, which then the low-pass filters eliminate any high frequency noise pickups and minimize aliasing.

5 Circuit Design and Component Selection

5.1 Power Supply and Isolation Design

The module is rated for a nominal power supply input of 24-V DC. For maximum flexibility, module can accept supply voltages in the range of 16-V to 36-V DC.

The LM5069, a positive voltage in-rush current protection controller, provides intelligent control of the power supply connections during insertion and removal of a module from live system or power source. The LM5069 provides in-rush current limiting during turn-on and monitoring of the load current for faults during normal operation. Additional functions include undervoltage lockout (UVLO) and overvoltage lockout (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current of the module is limited to 2.75 A. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the safe operating area (SOA).

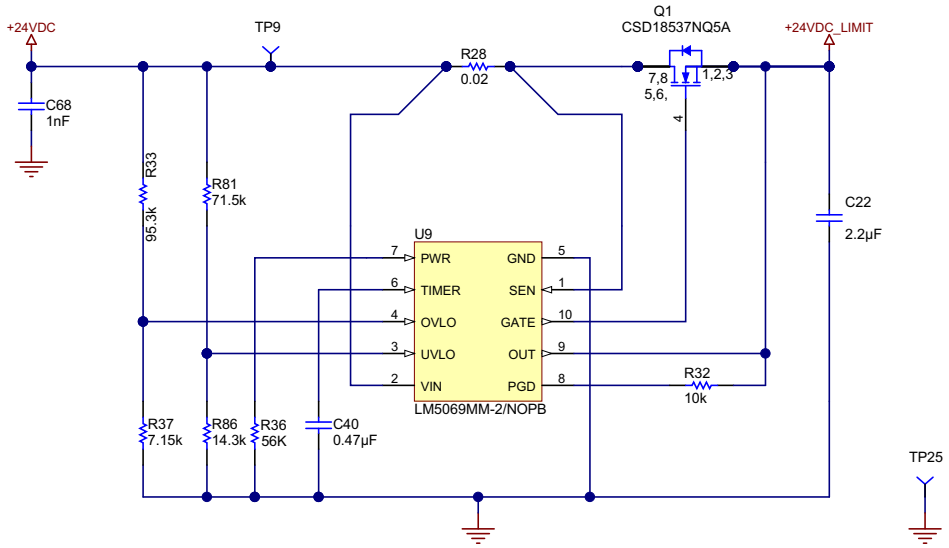


Figure 2. Inrush Current Limit

The desired current limit threshold:

$$I_{LIM} = \frac{55\ mV}{R28} = \frac{55\ mV}{20\ m\Omega} = 2.75\ A \quad (1)$$

For proper operation of device, sense resistor R17 must be smaller than 100 mΩ.

NOTE: Current sense resistor (R17) must be placed close to LM5069. Connections from R17 to the LM5069 should be made using the Kelvin technique. See Figure 3.

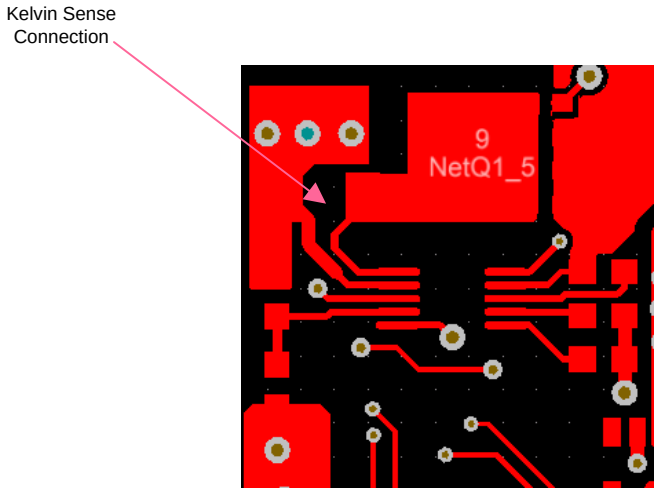


Figure 3. Kelvin Sense Connection for Sense Resistor

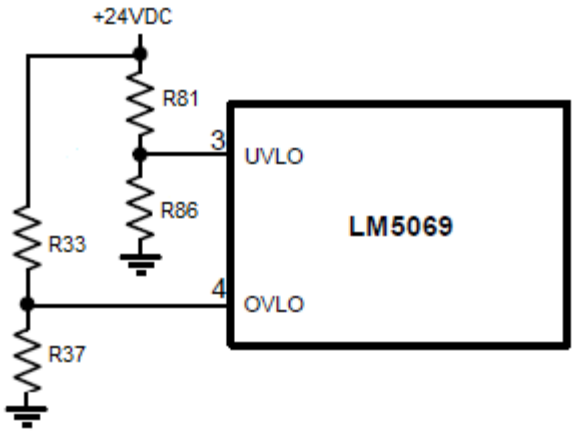


Figure 4. UVLO and OVLO Using External Resistors

To define all four thresholds accurately, use four resistors for UVLO and OVLO. The upper and lower UVLO thresholds:

VUV(HYS)

$$R65 = \frac{V_{UVH} - V_{UHL}}{21\mu A} = \frac{1.5\,V}{21\mu A} = 71.42k = 71.5k\,(\text{standard value}) \quad (2)$$

$$R66 = \frac{2.5\,V \times R81}{VUVL - 2.5\,V} = \frac{2.5 \times 71.5k}{15\,V - 2.5\,V} = 14.3\,k \quad (3)$$

Therefore, VUVH = 16.50 V and VUVL = 15 V with a hysteresis of 1.5 V that keeps the device from responding to power-on glitches during start up.

Choose the upper and lower OVLO thresholds:

$$R23 = \frac{VOVH - VOVL}{21\mu A} = \frac{2\,V}{21\mu A} = 95.3k \quad (4)$$

$$R27 = \frac{2.5\,V \times R2}{VOVH - 2.5\,V} = \frac{2.5\,V \times 95.3k}{36\,V - 2.5\,V} = 7.11k = 7.15k\,(\text{standard value}) \quad (5)$$

Therefore, VOVH = 35.82 V and VOVL = 33.82 V with a hysteresis of 2 V.

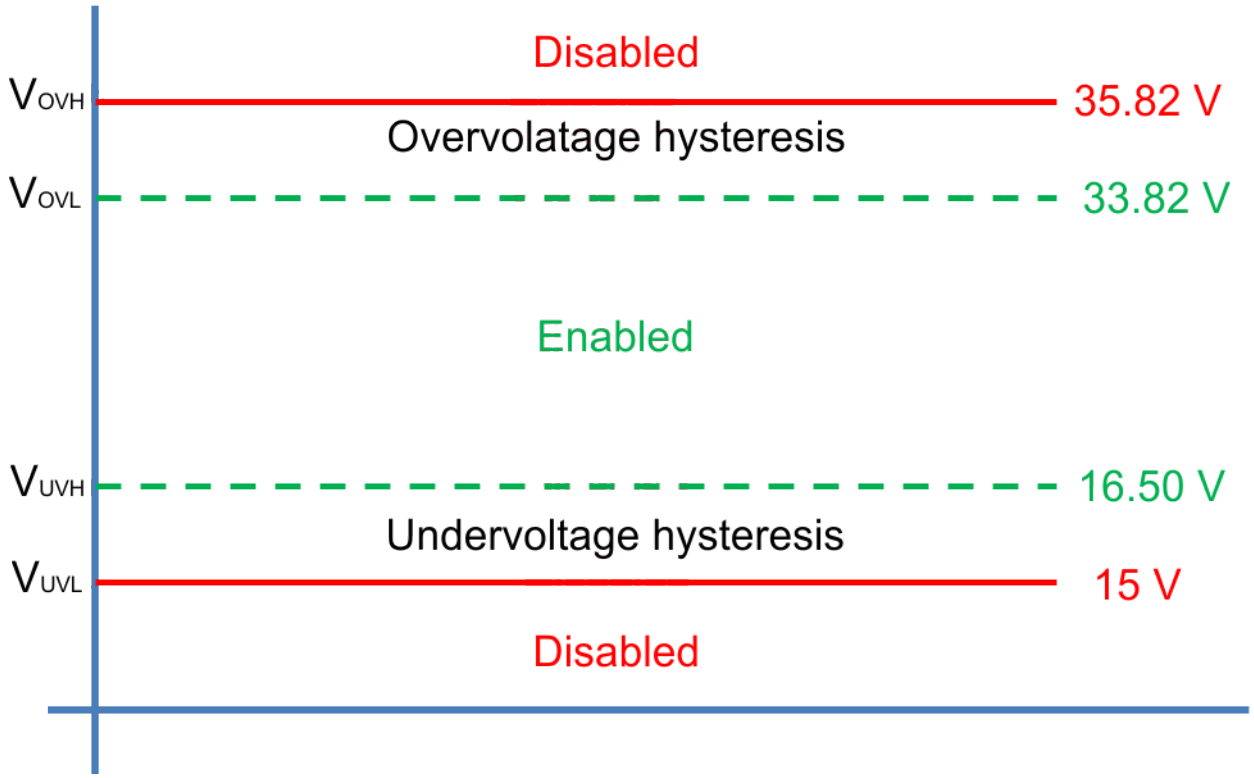


Figure 5. UVLO and OVLO Hysteresis

Refer to the LM5069 datasheet and LM5069EVAL evaluation board for device operation, design procedure, and recommended PCB layout guidelines.

In industrial systems, signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. Also isolation avoids ground loops. The LM5017 is a synchronous buck regulator with integrated MOSFET. The LM5017 is configured in Fly-Buck topology to generate non-isolated 3.3 V and isolated 5 V, 15 V, and –15 V from 24-V DC. An isolated Fly-Buck converter uses a coupled inductor windings to generate isolated outputs. In Fly-Buck topology, there is no need for an opto-coupler or auxiliary winding as the secondary output closely tracks the primary output voltage, resulting in a cost effective and smaller-sized solution.

Table 2. Fly-Buck Design Specifications

SR. NO.	DESIGN SPECIFICATIONS	KEY PARAMETERS
1	Input voltage range (VIN)	16 to 36 V
2	Primary output voltage (VOUT1)	10 V (3.3 V after LDO)
3	Secondary output voltage (VOUT2)	5 V
4	Primary load current (IOUT1)	30 mA
5	Secondary load current (IOUT2)	120 mA
6	Switching frequency (fsw)	1 MHz

The non-isolated output voltage (VCC_NON_ISO) is set by two external resistors (R3, R70). The regulated output voltage is calculated as follows:

$$V_{CC}\_NON\_ISO = 1.225 \times \left(1 + \frac{R70}{R3}\right) = 1.225 \times \left(1 + \frac{196\ K}{28\ K}\right) = 10\ V \quad (6)$$

The operating frequency can be calculated as follows:

$$F_{SW} = \frac{V_{OUT}}{10^{-10} \times R_{ON}} \quad (7)$$

$$R_{ON} = \frac{10\ V}{10^{-10} \times 1\ MHz} = 100\ K\Omega \quad (8)$$

Minimum recommended on-time is 100 ns at max input voltage.

$$T_{ON\_MAX} = \frac{10^{-10} \times R_{ON}}{V_{IN\_MIN}} = 0.67\ \mu S \quad (9)$$

Similarly,

$$T_{ON\_MIN} = \frac{10^{-10} \times R_{ON}}{V_{IN\_MAX}} = 0.29\ \mu S \quad (10)$$

VCC_NON_ISO is given to TPS70933DBVT LDO that generates +3.3V_NON_ISO and capable of delivering 30 mA of output current. The +3.3V_NON_ISO is used to power-up an EEPROM and two digital isolators.

Selection of rectifier diode D2:
The reverse bias voltage across D2 when the high side buck switch is on:

$$V_{D2} = \frac{Nsec}{Npri} \times V_{IN\_MAX} = \frac{1}{1.55} \times 35 = 23\ V \quad (11)$$

Considering safety margin the PIV of secondary diode should be greater than 35 V, Therefore, the 60-V Schottky diode PMEG6010CEH,115 is selected.

Rectified output (+VCC_ISO) on the secondary side will be

$$+VCC\_ISO = \left(\frac{Nsec}{Npri} \times V_{CC}\_NON\_ISO\right) - VFD2 = 6.45 - 0.4\ V = 6.05\ V \quad (12)$$

D4 is connected to generate –18V_ISO, which is used to detect sensor open condition. The load current of –18V_ISO rail is negligible as compared to +5V_ISO.

Refer to the LM5017 datasheet for device operation and application note AN-2292 for Fly-Buck converter design procedure and recommended PCB layout guidelines.

Do not power the ADCs and DAC directly from switching regulator's output as it contains ripple noise due to the switching frequency and high frequency noise from rapid transitions in the voltage or currents. Applying power directly to ADC would deteriorate the performance. Therefore, power ADCs from low noise LDOs with high PSRR. The LDO selected for the design is TPS7A16xx. The LDO has a wide input voltage range up to 60 V and has a 30-dB PSRR at 100 kHz. Therefore, the ripple noise from switching regulator can adequately attenuated by TPS7A16xx. Typically, the PSRR of the LDOs is high at lower frequencies, tends to decrease at higher frequencies, and becomes zero above a few MHz. The TPS7A16xx has a better PSRR at higher frequencies and eliminates the need of a bulky LC filter.

Table 3. Design Specifications and Key Parameters

SR. NO.	DESIGN SPECIFICATIONS	KEY PARAMETERS
1	Input voltage range (VIN)	6.2-V DC
2	Output voltage (VOUT)	5 V (Fixed)
3	Output current (IOUT)	80 mA
4	VDO	200 to 300 mV at 80 mA
5	Thermal shutdown	170°C
6	TJ_MAX	125°C
7	θJA Junction-to-ambient thermal resistance	66.2°C/W

Input and Output Capacitors

The TPS7A16 family linear regulators achieve stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF. The 22-µF, X5R ceramic capacitor is connected to maximize AC performance and to achieve better stability over temperature. Although an input bulk capacitor is not required for stability, it is good analog design practice to connect a 1- to 22-µF capacitor from VIN to GND. This design connects the 22-µF capacitor at the input. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR.

Thermal Protection

Thermal protection in TPS7A1650 disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is again enabled.

Power Dissipation

Pulse Power Dissipation P_P	= $(V_{IN} – V_{OUT}) \times I_{OUT}$
	= (6.2 – 5) × 120 mA
	= 144 mW
T_J	= TA(max) + (θ_{JA} × PD)
	= 70 + (212.1 × 144 mW)
	= 100.54°C

TJ < TJIC, hence no need of heat sink for TPS7A1650.

Refer to the TPS7A1650 datasheet for device operation and recommended PCB layout guidelines.

5.2 ADC

The design utilizes the ADS8688, a 16-bit, 500-kSPS, 8-channel, single-supply, SAR ADC. The ADS8688 can operate at throughput rate of 500 kSPS with no missing code and INL ±0.75LSB. The ADS8688 can accept bipolar and unipolar analog input signals with a single 5-V supply. The single 5-V supply is required for ADC operation which reduces design complexity and cost. The ADS8688 has five software-selectable input ranges: ±10.24 V, ±5.12 V, ±2.56 V, 0 to 5.12 V, and 0 to 10.24 V. Each analog input channel can be independently programmed to one of the five input ranges. The device offers a 1-MΩ, constant resistive input impedance irrespective of the selected input range. The ADS8688 has on-chip low-drift reference of 4.096 V, which enables accurate conversion. The on-chip PGA uses the gain and ensures maximum of the ADC's input dynamic range. Depending on the range of the input signal, the PGA gain is adjusted by setting the Range_CHn in the program register.

The device also offers an integrated front-end signal processing including a multiplexer, second-order anti-aliasing filter, ADC driver amplifier, and an extended industrial temperature range, making the ADS8688 ideal for any standard industrial analog input measurements. The basic block diagram is shown in Figure 6.

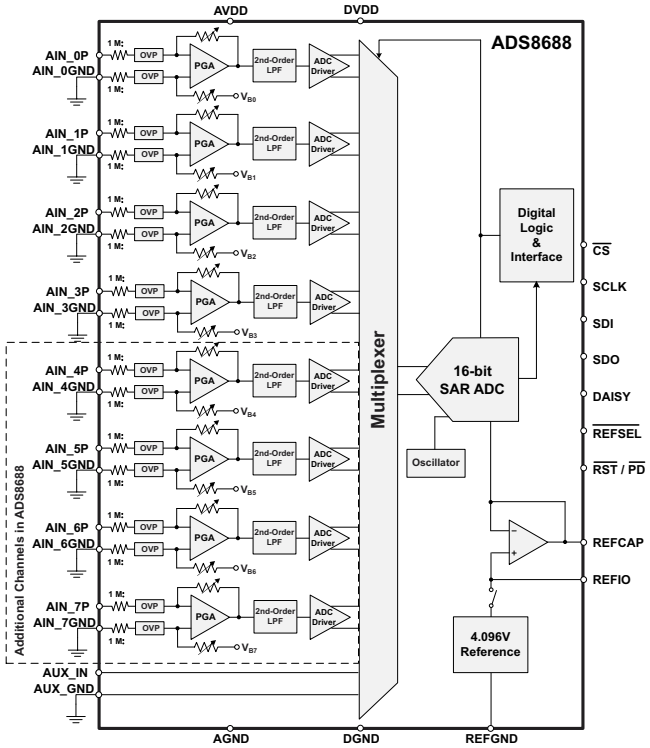


Figure 6. Internal Block Diagram of ADS8688

Table 4 details the analog input range configuration with the on-chip 4.096-V reference:

Table 4. Input Range Selection Bits Configuration

ANALOG INPUT RANGE	Range_CHn [2:0]		
	BIT 2	BIT 1	BIT 0
±10.24 V	0	0	0
±5.12 V	0	0	1
±2.56 V	0	1	0
0 to 10.24 V	1	0	1
0 to 5.12 V	1	1	0

5.2.1 ADC Reference

The ADS8688 can operate with a on-chip 4.096-V reference or optional external reference. The type of reference used is set by an external /REFSEL pin of ADS8688. The on-chip reference has been used for this reference design. Also, the ADS8688 provides an external reference with an R80 and R85 resistor combination:

- If R80 is populated and R85 is not populated, the ADS8688 operates on internal reference of 4.096V.
- If R85 is populated and R80 is not populated, connect external reference between TP14 and TP18 (SGND).

The output of the internal reference buffer comes out at the REFCAP pin, which is decoupled with the REFGND pin using a 22-µF and 1-µF capacitor for better performance. Place these decoupling capacitors close to REFCAP pin of the ADS8688 to shunt the noise to the ground and reduce the effect noise on the ADC. Use a variety of capacitor values in parallel to give a good response to a broad range of noise.

5.2.2 Analog Input and Filter

The module contains a terminal block providing connection for four analog input channels, which are specifically designed to interface with analog current and voltage input signals. For industrial control modules, analog input voltage and current ranges include ±10 V, ±5 V, ±2.5 V, 0 to 5 V, 0 to 10 V, 4 to 20 mA, and 0 to 20 mA. All four channels provided on the module are software configurable as a current or voltage input for above mentioned industrial voltage ranges.

The host microcontroller loads shift register SN74HC595 with appropriate bits SN74HC595to turn on or off the 200-Ω burden resistance. When the input is set to receive a 0- to 20-mA current, the switches are configured to provide a 200-Ω load resistor on the input, providing 0 to 4 V to the ADC with a full-scale voltage of 5 V.

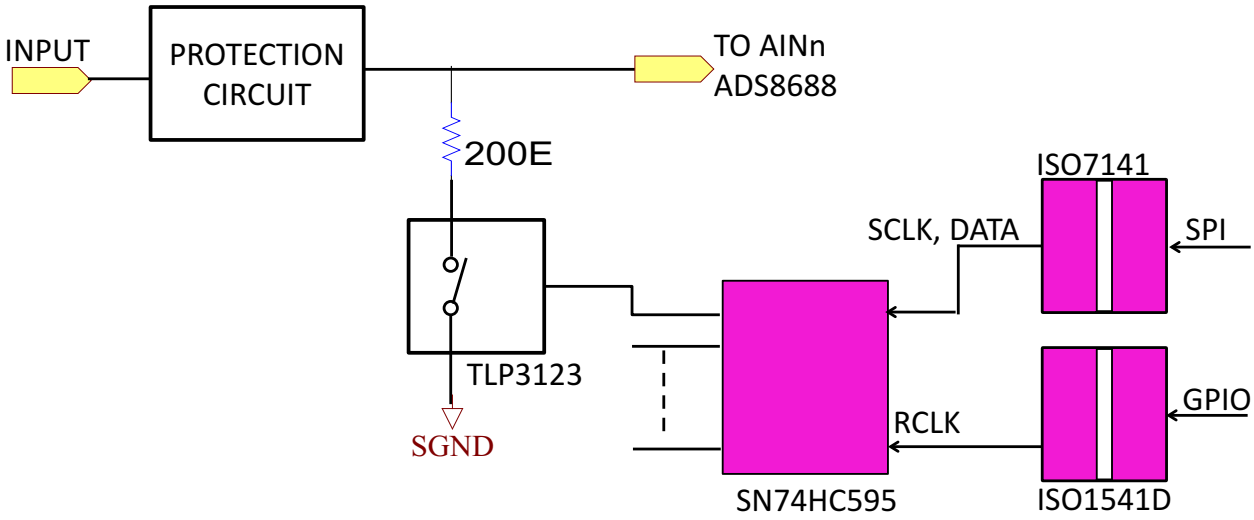


Figure 7. Analog Input Section

The ADS8688 on-chip input circuitry consists of eight single-ended analog inputs multiplexed into a single ADC core. The ADC reads the selected input signal and converts it to a digital value. The multiplexer switches each input channel to the ADC. Multiplexing provides an economical means for a single ADC core to convert multiple analog signals. However, on-chip multiplexing also affects the speed at which an input signal can change and still be detected by the converter.

Table 5. SPI Propagation Delay

ADC clock to DOUT output delay	25 ns (Max)
Isolator propagation delay	23 ns (Max; round delay)
Microcontroller setup time required	17.15 ns (Min)
Total delay	88.15 ns

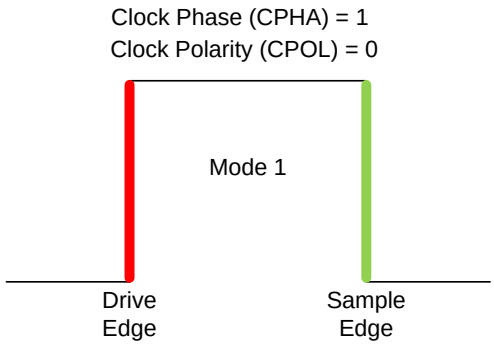


Figure 8. SPI Clock

Therefore, the max SPI clock speed up to which SPI works with isolator is 10 MHz.

Sampling Time and RC Filter Design

FUNCTION	VALUE
Maximum SPI clock frequency	= 10 MHz
One SPI clock cycle period (CP)	= 100 ns
Time required to read correct 16 bits for one channel (Throughput)	= (NSCLK × XCP) + tDV_CSDO where • NSCLK = number of SPI clocks required for read operation • tDV_CSDO = Delay time: CS falling to data enable for ADS8688 • CP = One SPI clock cycle period
	= (33 × 100 ns) + 10 ns
	= 3.3 µ + 10 ns
	= 3.31 µs
Sampling frequency	$= \frac{1}{3.31\ \mu Sec}$
	= 302 kSPS
RC low pass filter cut-off frequency ≤ Sampling Frequency / 5	$= \frac{300\ ksps}{5}$
	= 60 kHz
RC low pass filter cut-off frequency fC	$= \frac{1}{2 \times \pi \times RC}$
R4 = 100 Ω, C12	= 27 nF (standard value)
The R4 and C12 forms RC filter 1 and R21 and C23 forms second RC filter. The dynamic impedance of each filter order affects its neighboring filter. To reduce the loading effect we can make the impedance of each following stage Rx10 and C/10 the previous stage, so R21 = 10 × R4 and C23 = C12/10.	
Consider R21 = 1 k, C23	= 2.7 nF (standard value)
The two RC filters forms 2nd order RC filter. It has roll-off 40dB/Decade after 60kHz and for higher frequencies.	
Settling for the RC low pass filter	= 5 × RFLTCFLT (time constant)
	= 5 × (1000 Ω × 2.7 nF)
	= 13 µs
The external RFLT CFLT Low Pass filter network must settle within the next sample acquisition time.	
Sampling time	$= \frac{1}{60\ kHz}$
	= 17 µs
Settling for the RC low pass filter < Sampling time	
CHANNEL SCANNING TIME	
With moving average of four samples	= 4 × 17 µs = 68 µs
There are total four channel in ADS8688, so time required to scan all four channels	= 4 × 68 µs = 272 µs

The voltage input has an impedance of 1 MΩ and when changing to a current input the smaller 200-Ω burden resistor is switched on using Opto-MOS with low on-state resistance.

5.2.3 Protection from ESD, EFT, and Surge for Analog Input

The goal of EMC protection circuitry is to shunt any sort of external transient to earth ground with low impedance and protect the analog I/O module from damage. The module includes onboard EMC protection circuit and has been tested and verified to fully comply with the specifications listed in Table 6.

Table 6. IEC 61000 Specifications

TEST AND STANDARD	TEST LEVEL
IEC 61000-4-2 Electrostatic Discharge (ESD)	±4-kV contact discharges ±8-kV air discharges
IEC 61000-4-4 Burst-Electrical Fast Transients (EFT)	±2 kV at 5 kHz on signal ports
IEC 61000-4-5 Surge	±1-kV CM on signal ports

The transient voltage suppressor (TVS) diodes are used to clamp the surge voltage to safer limits with high-voltage capacitors Y-caps in parallel. In addition, two Y-caps have been placed at key locations to shunt transient energy quickly to earth ground. The Y-caps provide quick and low impedance to fast transients and TVS diodes provide immunity against high voltage spikes.

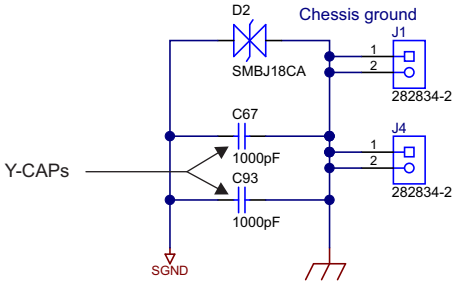


Figure 9. Y-Caps Placement

The voltage surge has the highest energy. Let's consider the case of 1 kV (CM) at a 8/20-µs surge on input lines.

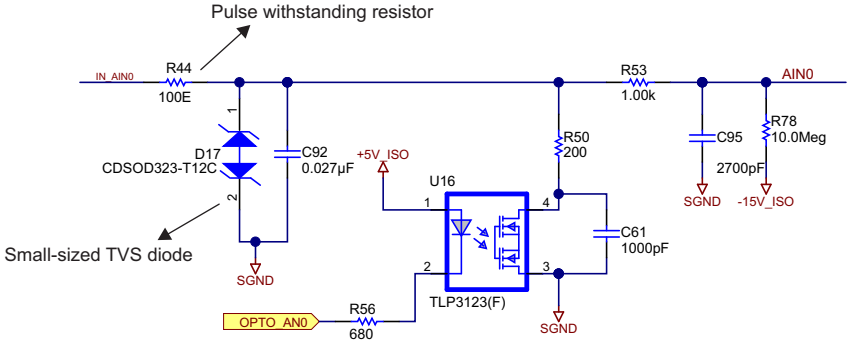


Figure 10. Analog Input Protection Circuit

Impedance in path,

ZTOTAL	= $Z_{SURGE\_GENERATOR}$ + $Z_{CON\_NETWORK}$ + $R_{SERIES\_RESISTOR}$
	= 2 Ω + 40 Ω + 100 Ω
	= 142 Ω

The internal over-voltage protection circuit of ADS8688 can withstand up to ±20 V on the analog input pins. Therefore clamping voltage must be less than 20 V. The CDSOD323-T12SC Rating: VBR = 13.3 V, V_{CMAX} = 27.3 V at 8/20 µs at I_{PP} = 14A, PPP = 350 W, and maximum leakage current = 1 µA

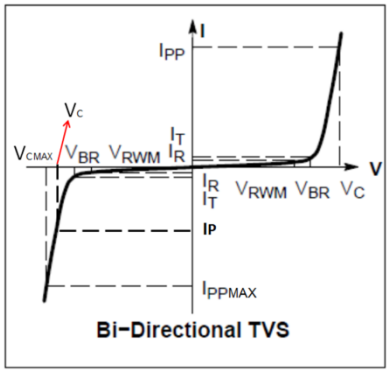


Figure 11. Characteristics of the TVS Diode

Linear or straight line equation:

$$V_C = \frac{I_P}{I_{PP}}(V_C - V_{BR}) + V_{BR} \quad (13)$$

$$I_P = \frac{(1000\,V - V_C)}{ZTOTAL} = \frac{(1000\,V - V_C)}{142\,\Omega} \quad (14)$$

Put IP into the Equation of VC and solve the equation from CDSOD323-T12SC datasheet values.

V_C = 20 V

Pulse power dissipation:

$$P_P = V_C \times I_P = 20 \times 6.9\,A = 138\,W \quad (15)$$

5.3 DAC

DAC8760 is designed for industrial and process control applications. DAC8760 can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA; or as a voltage output with a range of 0 to 5 V, 0 to 10 V, ±5 V, or ±10 V, with a 10% overrange (0 to 5.5 V, 0 to 11 V, ±5.5 V, or ±11 V). Both current and voltage outputs can be simultaneously enabled while being controlled by a single data register. DAC8760 internal block diagram is shown in Figure 12.

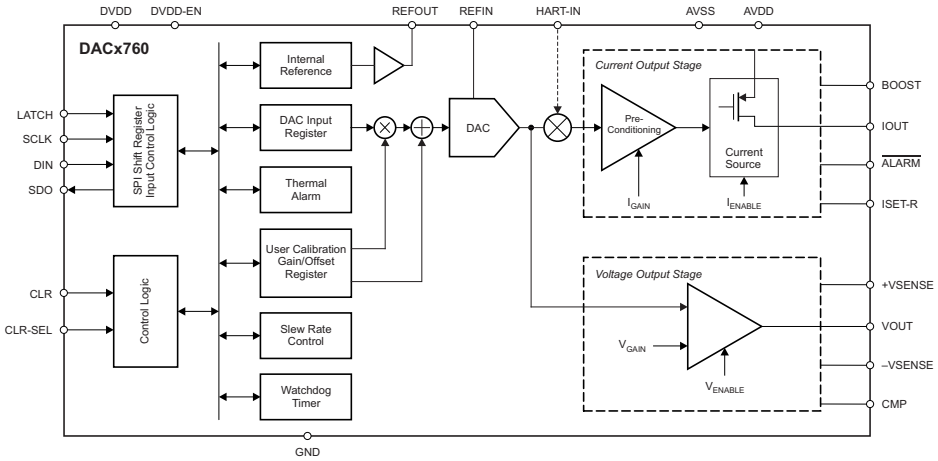


Figure 12. Internal Block Diagram of DAC8760

5.3.1 Voltage Output

When DAC8760 is configured for voltage output, the maximum allowed load is 1 kΩ at 10 mA. For voltage output, the module uses 15 V and –15 V at power supply rails thus providing 5 V of headroom. The equation for DAC8760 to generate 16-bit code required voltage output is:

For unipolar output mode:

$$Vout = Vref \times Gain \times \frac{Code}{2^N} \quad (16)$$

For bipolar output mode:

$$Vout = Vref \times Gain \times \frac{Code}{2^N} - Gain \times \frac{Vref}{2} \quad (17)$$

where

- Code is the decimal equivalent of the code loaded to the DAC
- N is the bits of resolution, 16 for DAC8760
- Vref is the reference voltage; for internal reference, Vref = 5.0 V
- Gain is automatically selected for a desired voltage output range

5.3.2 Current Output

DAC8760 current output stage consists of a pre-conditioner and a current source. This stage provides current output according to the DAC code. The output range can be programmed as 0 to 20 mA, 0 to 24 mA, or 4 to 20 mA. Optionally, an external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals AVDD minus 2.5 V. In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 33.5 V. After power-on, the IOUT pin is in Hi-Z state with no output. In this design, an external 15-kΩ 0.1% resistor is connected between ISET-R pin and GND. The equation for DAC 16-bit code to current output is:

For a 0 to 20-mA output range:

$$Iout = 20\,mA \times \frac{Code}{2^N} \tag{18}$$

For a 0 to 24-mA output range:

$$Iout = 20\,mA \times \frac{Code}{2^N} \tag{19}$$

where

- Code in the decimal equivalent of the code loaded to the DAC
- N is the bits of resolution, 16 for DAC8760

5.3.3 Voltage Sense

The Vsense and –Vsense enable sensing of load. Ideally, Vsense and –Vsense connect to Vout at the terminals. As the Vout and Iout are tied together when used as current output, this connection produces a gain error due to leakage current of the Vsense pin. This leakage current introduces gain error of -0.36%. This error can be minimized by using a high input impedance, low input bias current op-amp. In the reference design, the Vsense is connected to Vout through a high impedance buffer using OPA188, which has a typical input bias current of 160 pA. This reduces the gain error to <0.008%.

5.3.4 HART Option

The DAC8760 is also provisioned to provide HART output. In this reference design, HART pins are made available to the user by test points. For details on HART utilization, refer the DAC8760 datasheet.

5.3.5 SPI and Daisy-Chained DACs

DAC8760 is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that can operate at clock rates of up to 31 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. To save number of isolators, shift register SN74HC595 and two DACs are configured in daisy chain mode as shown in Figure 13.

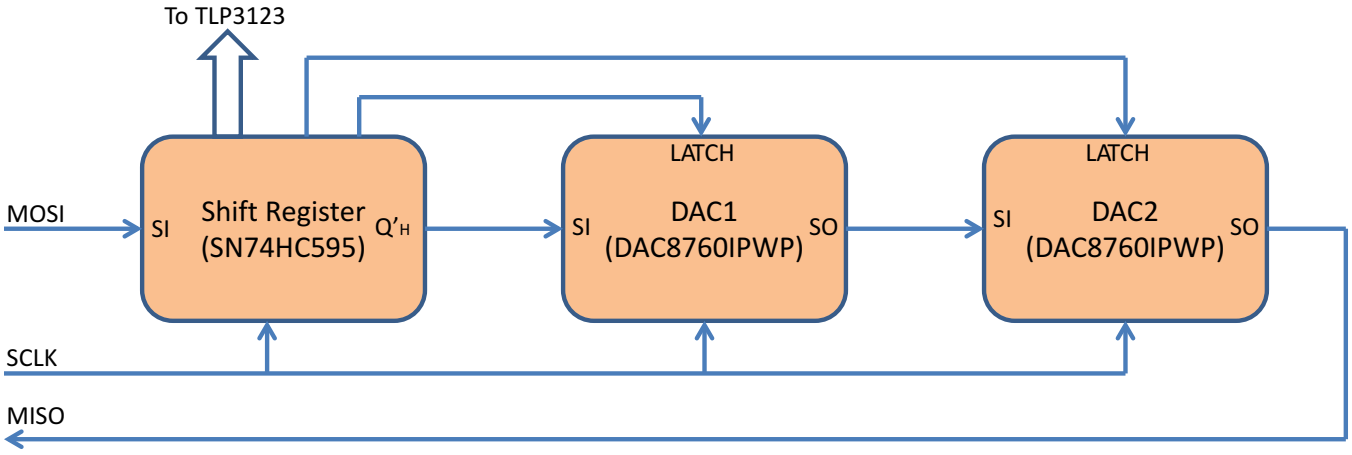


Figure 13. Daisy-Chain Configuration

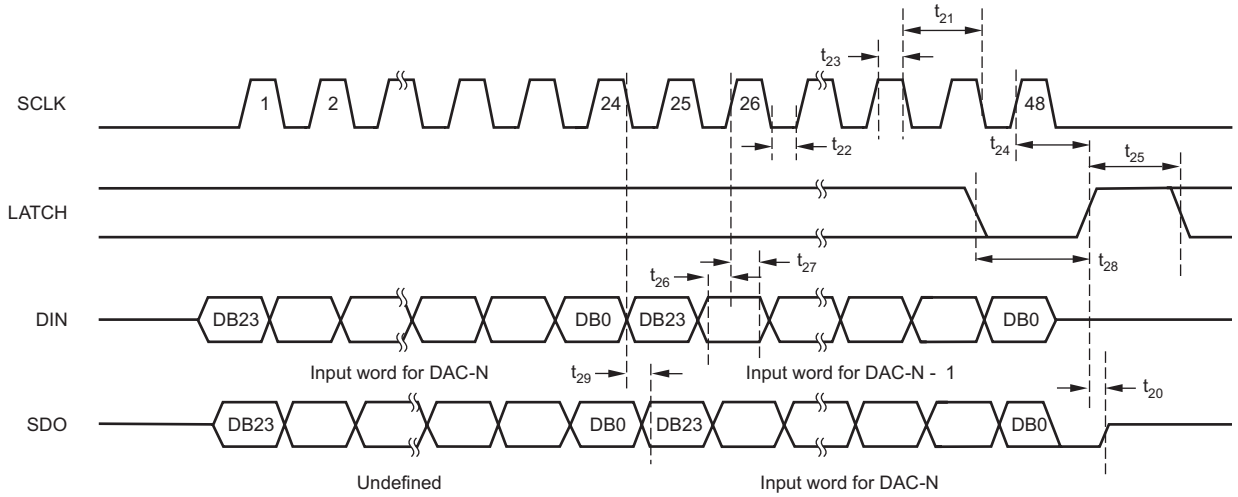


Figure 14. Daisy-Chain Mode DAC8760 Timing

The Q'H and SDO pins are used to daisy chain the three devices together. The rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of the WRITE cycle. When the serial transfer to all the devices is complete, LATCH is made HIGH by asserting RCLK of the shift register. This action transfers the data from SPI shift registers to the device internal registers of the respective DAC. In daisy chain, the number of clocks in each frame depends on the number of devices. Each frame has 56 clocks.

Total write time estimation for a two DAC design:

$$T = (24 \times F_S) + T_{su} + T_{sr\_o} + T_{1\_2} + T_{pd}$$

where

- F_S = SPI clock rate in Hz
- T_{su} = Setup time
- T_{sr_o} = Shift register SCLK to Q'H delay
- T_{LE} = Software overhead from host to change the LATCH line status (as an I/O port pin)
- T_s = Analog output settling time (Refer to datasheet of DAC8760) (20)

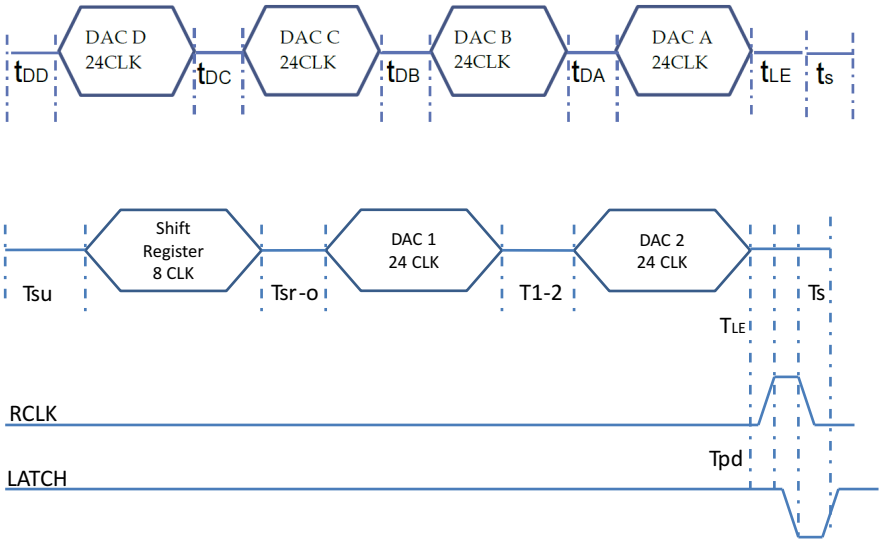


Figure 15. Daisy-Chain Mode Timing

5.3.6 Filter and Protection for ESD, EFT, and Surge

The output stage is designed to withstand an 8-kV ESD, 1-kV EFT and 1-kV Surge. Every channel is protected by a TVS SMBJ18CA. This circuit clamps overvoltage inputs approximately 25 V. The ESD protection diodes also protects against overvoltage inputs. Layout guidelines have to be followed to ensure compliance to EMC standards. The protection devices are selected to dissipate the required energy.

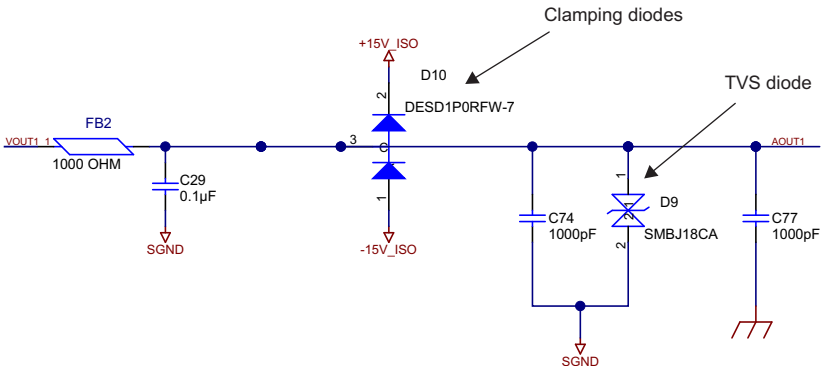


Figure 16. Analog Output Protection

5.3.7 Digital Isolation

In industrial systems, signals are transmitted from long distance and variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. The High Speed Digital Isolator ISO7141CC and ISO7421 connect the SPI Host to the ADS8688 SPI. With these digital isolators, the host processor on the base board maintains 2.5 kV_{RMS} of galvanic isolation for one minute from any high voltage condition appearing at the Analog I/O Module from the field side.

The ISO7141CC isolates SCLK, MISO, MOSI, and /CS signals of SPI interface. The ISO7421 isolates control signals of the ADC and DAC. Both of the products have achieved UL, CSA, and VDE safety approvals.

5.4 Interface

The analog I/O module has the following connectors:

1. J1, J4: 2-pin screw terminal type, 2.54-mm pitch connectors for connecting protective Earth
2. J2: 4-pin screw terminal type, 2.54-mm pitch connectors for analog outputs
3. J3: 8-pin screw terminal type, 2.54-mm pitch connectors for interfacing external analog inputs
4. J5: 50-pin connector for connecting SPI , I^2C, and power supply from the host controller

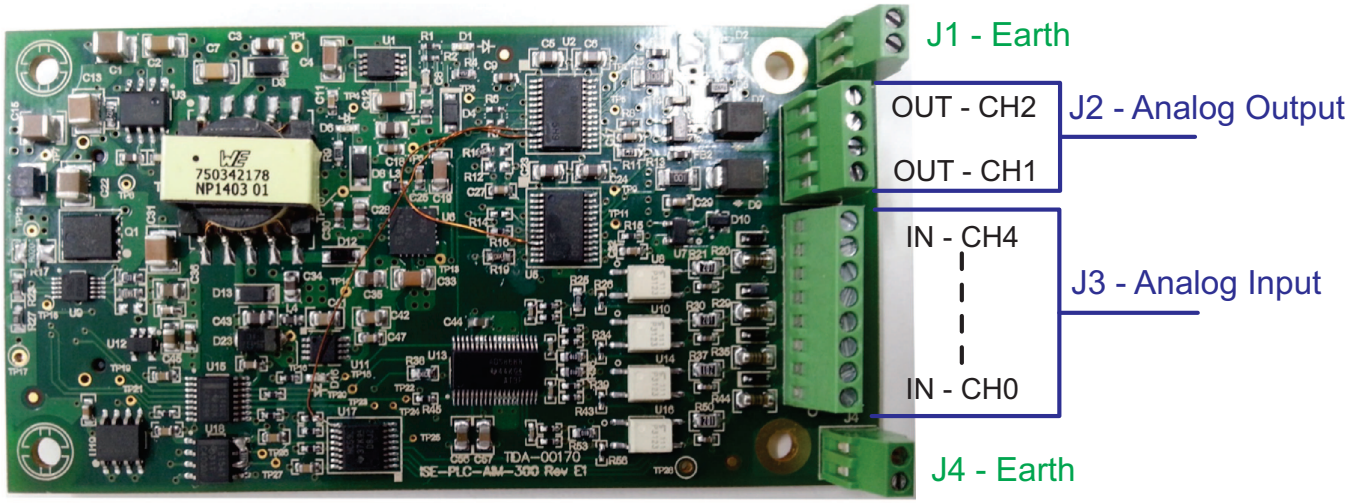


Figure 17. Board Top View

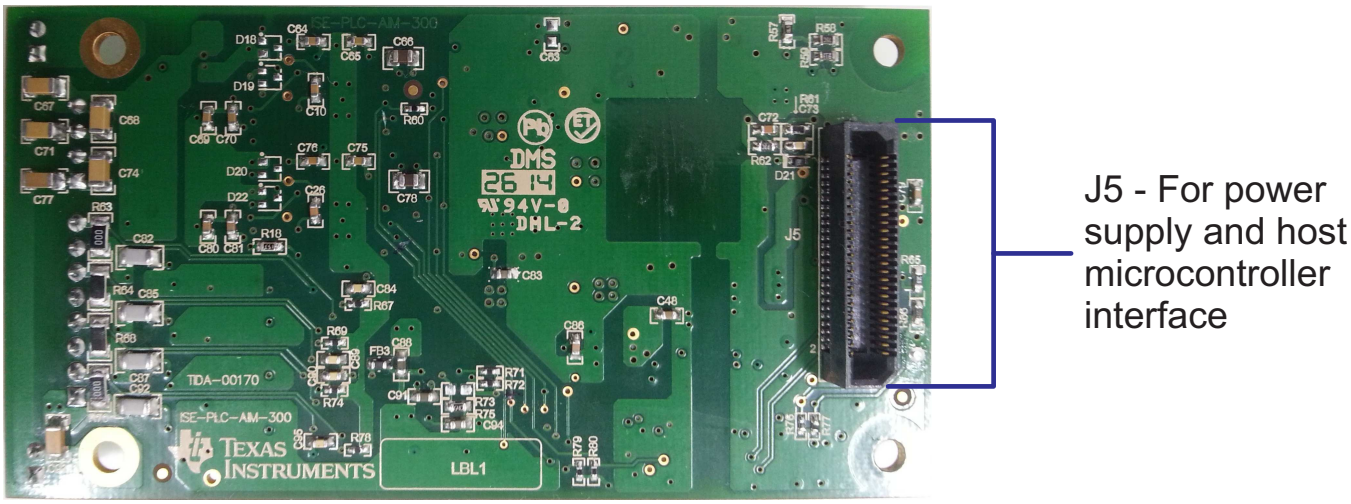


Figure 18. Board Bottom View

6 Test Setup

6.1 Hardware Test Setup

The TIVA C Series I/O Controller Platform (TIDA-00123) has the required connectors and the MCU to interface with the analog I/O Module. A 24-V power input to the module is supplied by the Tiva C Series I/O Controller Platform.

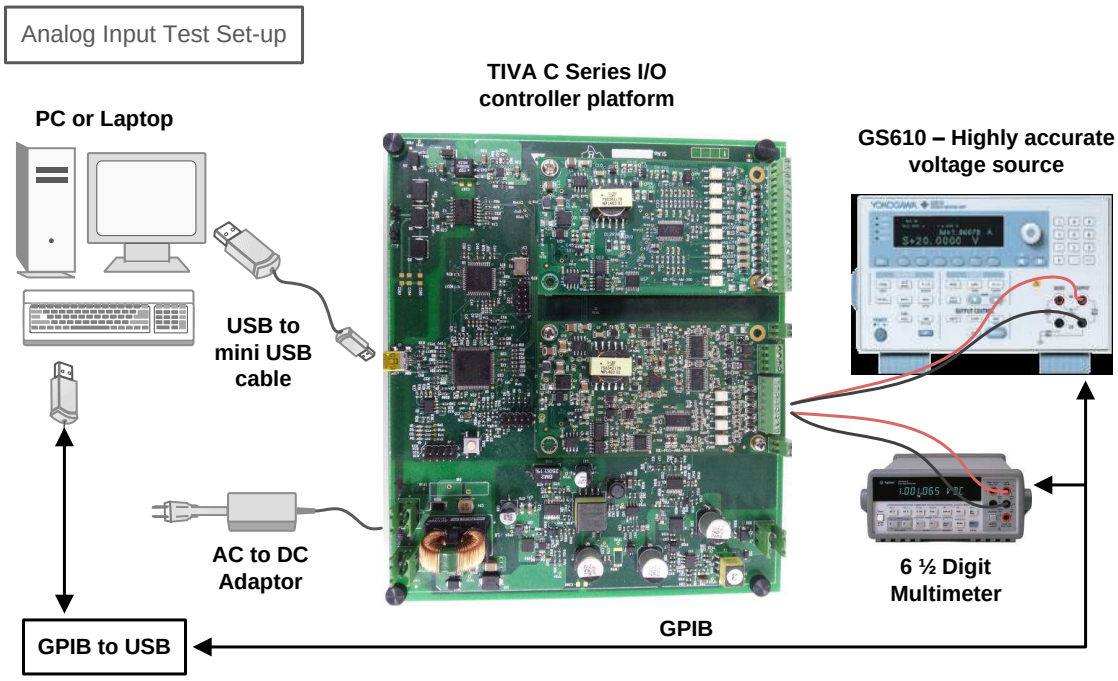


Figure 19. Analog Input Test Setup

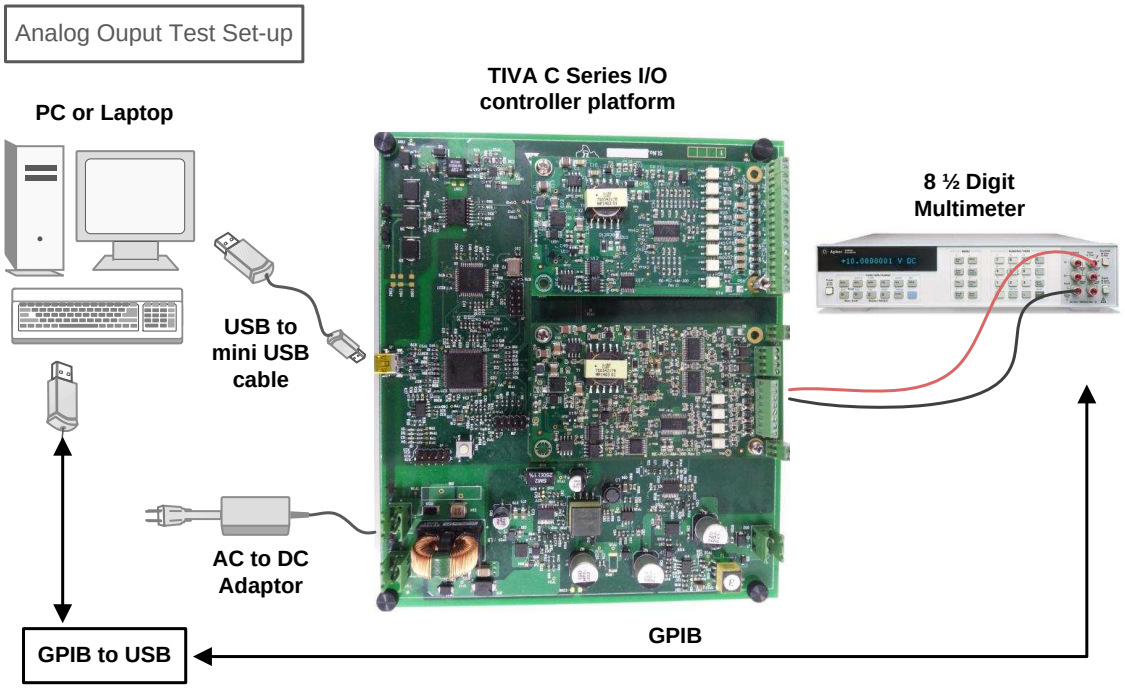


Figure 20. Analog Output Test Setup

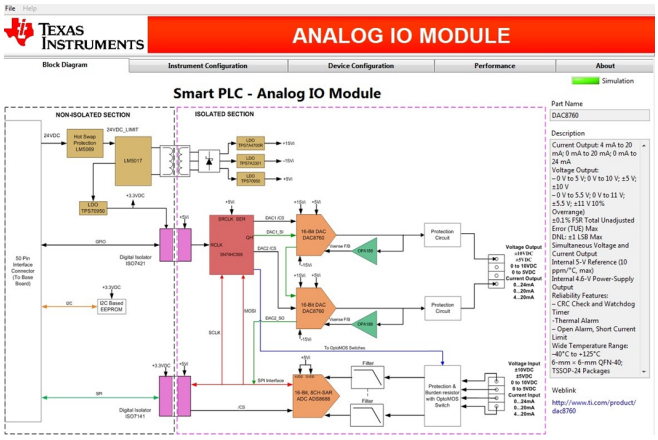


Figure 21. GUI to Demonstrate the Signal Chain Information

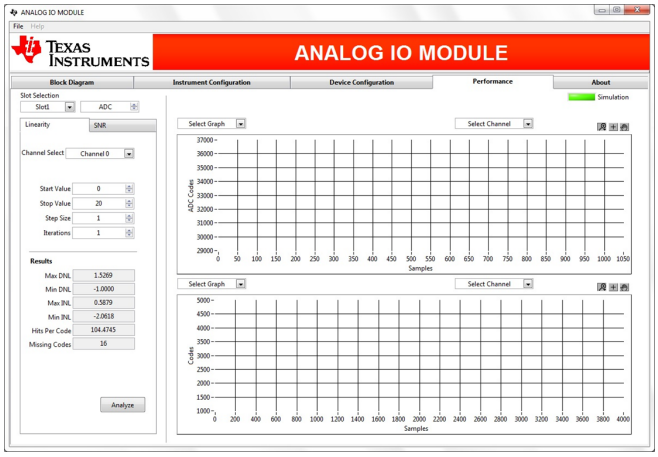


Figure 22. GUI to Demonstrate the Results

The complete signal chain performance can be evaluated using LabVIEW based GUI. The GUI on the PC connects to the Tiva C Series I/O Controller Platform through USB interface. The Tiva C Series I/O Controller Platform then controls the analog input card through an SPI interface. The setup has a precision signal generator (DS360, Stanford Research Systems), which feeds the analog input signal to the analog input module. The same signal is read by 6½ digit multimeter (DMM). The digital output generated is measured by the Tiva C Series I/O Controller Platform. The GUI does the post processing and computation of results. The GUI is LabVIEW based software. It can set the below functionalities:

- Configures all the registers in the ADS8688
- Configure channel for voltage or current input
- Reads the digitized data from the module
- Post processing of the data
- Result options: SNR, ENOB, DNL, and INL

Similarly, the analog output generated is measured by the 8½ DMM. The GUI does the computation of results. The GUI is a LabVIEW-based software that can set the following functionalities:

- Analog output channel: Two channels in each card
- Analog output type: Each analog output can be selected as voltage or current type
- ZERO error correction register
- Gain correction register
- Result options: DNL, INL, or TUE

7 Test Results

7.1 Typical Performance Characteristics

The overall accuracy depends on the performance of the different subsystems. The following results are for the integrated analog I/O module consisting of the ADC, DAC, power supply, filters, and protections. The offset error and gain error is reduced by applying a two-point linear calibration where one point is at 0 V and the second point is at full scale.

Analog Input Accuracy Test Plots

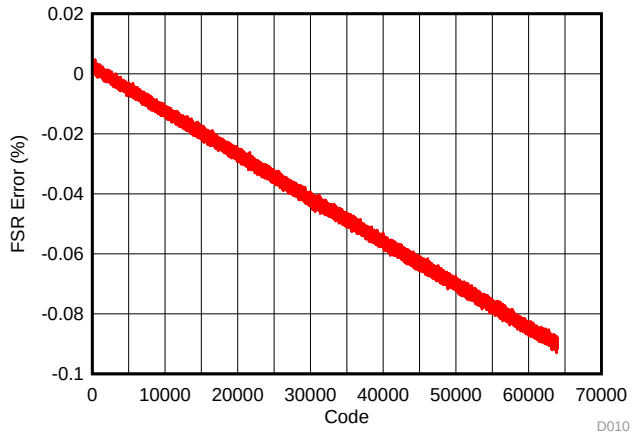


Figure 23. 0- to 5-V Range, Code versus FSR Error (Uncalibrated)

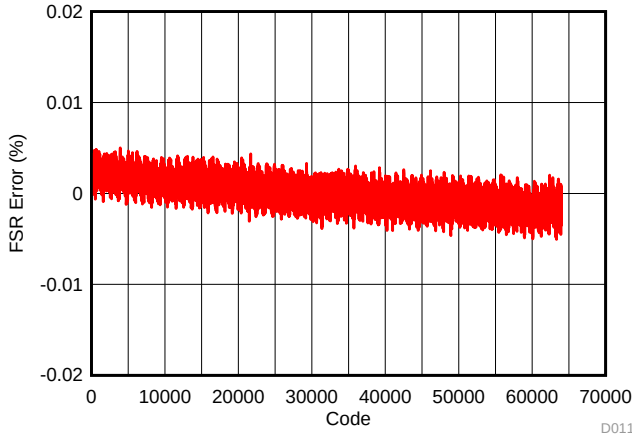


Figure 24. 0- to 5-V Range, Code versus FSR Error (Calibrated)

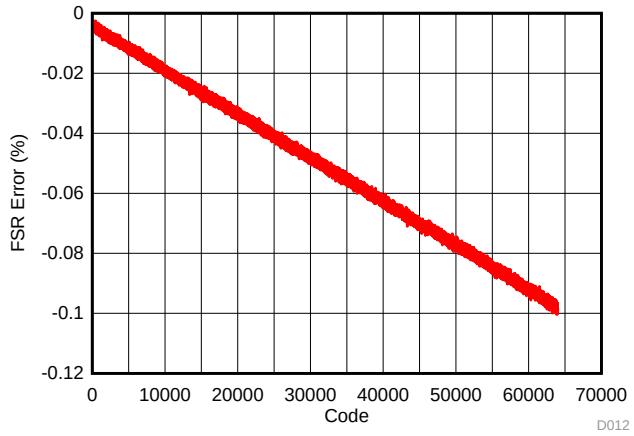


Figure 25. 0- to 10-V Range, Code versus FSR Error (Uncalibrated)

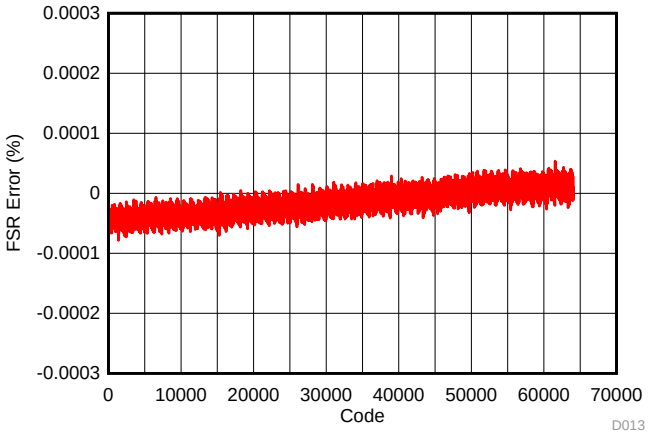


Figure 26. 0- to 10-V Range, Code versus FSR Error (Calibrated)

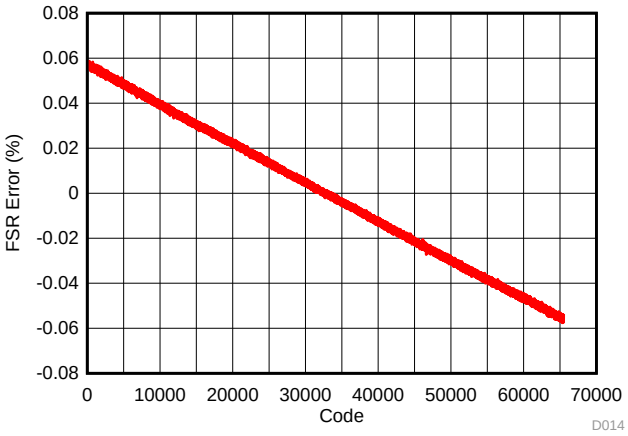


Figure 27. ±10-V Range, Code versus FSR Error (Uncalibrated)

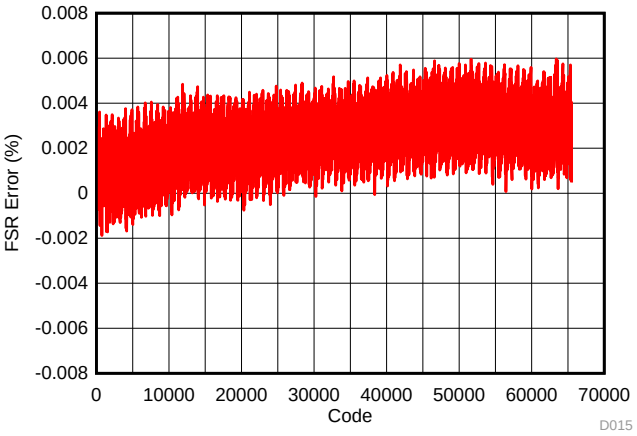


Figure 28. ±10-V Range, Code versus FSR Error (Calibrated)

7.2 Results Summary

Table 7. Measurement Result Summary of Analog Input Operation

SR. NO.	PARAMETER	MAX. FSR ERROR (%) (BEFORE CALIBRATION)		MAX. FSR ERROR (%) (AFTER CALIBRATION)	
1	0- to 5-V range	–0.093	0.0047	–0.005	0.005
2	0- to 10-V range	–0.1	0.9 × 10-6	–0.7 × 10-6	0.5 × 10-6
3	±10-V range	–0.0576	0.0588	–0.0019	0.006

Analog Output: Voltage Output Performance Graphs

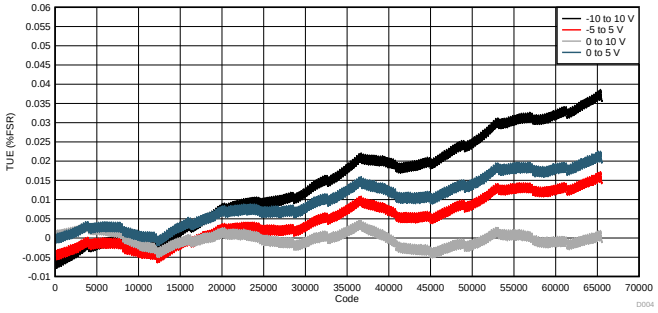


Figure 29. TUE (%FSR) versus Codes

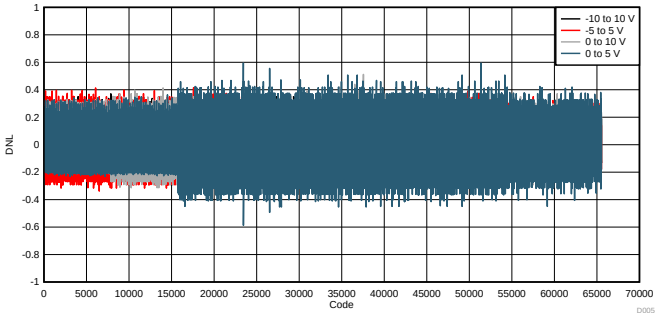


Figure 30. DNL versus Codes

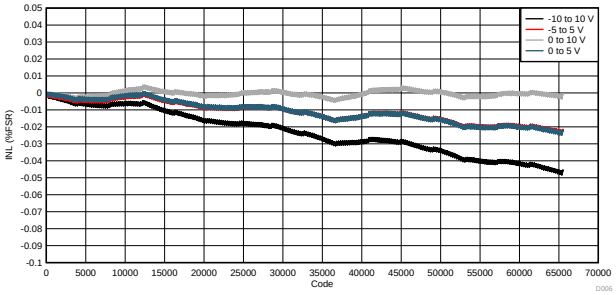


Figure 31. INL versus Codes

Analog Output: Current Performance Graphs

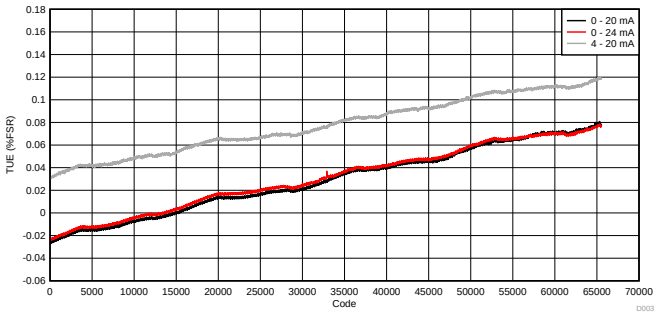


Figure 32. TUE (%FSR) versus Codes

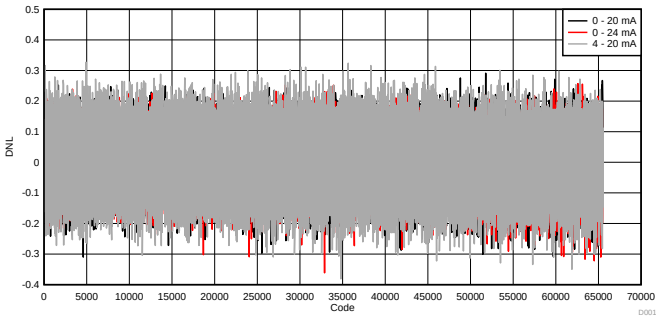


Figure 33. DNL versus Codes

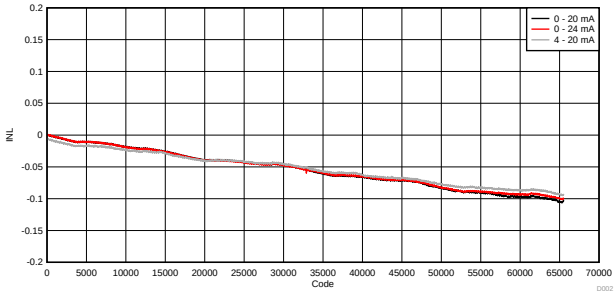


Figure 34. INL versus Codes

Table 8. Measurement Results of Analog Volatge Output Operation

SR. NO.	PARAMETER	±10 V	0 to 10 V	±5 V	0 to 5 V
1	TUE (%FSR) Max	0.038	0.035	0.017	0.019
2	TUE (%FSR) Min	–0.0083	–0.0019	–0.0064	–0.005
3	INL (%FSR) Max	0.00045	0.00851	0.00039	0.0047
4	INL (%FSR) Min	–0.04845	–0.0249	–0.024	–0.0055
5	DNL Max	0.381	0.587	0.415	0.511
6	DNAL Min	–0.555	–0.587	–0.473	–0.357

Table 9. Measurement Results of Analog Current Output Operation

SR. NO.	PARAMETER	4 to 20 mA	0 to 20 mA	0 to 24 mA
1	TUE (%FSR) Max	0.327	0.291	0.257
2	TUE (%FSR) Min	–0.532	–0.309	–0.361
3	INL (%FSR) Max	0	0.0007	0.0009
4	INL (%FSR) Min	–0.106	–0.106	–0.101
5	DNL Max	0.12	0.08	0.078
6	DNAL Min	0.024	–0.024	–0.024

7.3 Pre-Compliance Testing

The analog I/O module has been designed to meet standard EMC requirements for Industrial PLC application.

The following EMC tests have been performed.

Table 10. EMC Tests and Standards

TESTS	STANDARDS
ESD	IEC61000-4-2
EFT	IEC61000-4-4
Surge	IEC61000-4-5

Table 11. Criteria and performance as per IEC61131-2

CRITERIA	PERFORMANCE (PASS) CRITERIA
A	The analog I/O module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, analog I/O module must continue to operate as intended without manual intervention.
C	During the test loss of functions accepted, but no destruction of hardware or software. After the test, analog I/O module must continue to operate as intended automatically after a manual restart or power off/power on.

The targeted accuracy for Criteria A is

- Voltage input: ±0.2% full scale at 25°C
- Current input: ±0.2% full scale at 25°C

The next sections explain the test setup, procedures, and observations.

7.3.1 Test Setup

Figure 35. Pre-Compliance Test Setup

7.3.2 ESD: IEC61000-4-2

7.3.2.1 Test Level and Expected Performance

The ESD level at I/O connectors and the performance criteria expected are as follows:

Table 12. ESD Test Levels and Performance Criteria

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE
ESDIEC 61000-4-2	4-kV contact discharges – Level 2 8-kV air discharges – Level 3	Criteria B (After the test, the analog I/O module continued to operate as intended)

7.3.2.2 Description

Setup

The ESD is injected to the EUT in two ways: Contact discharge or air discharge.

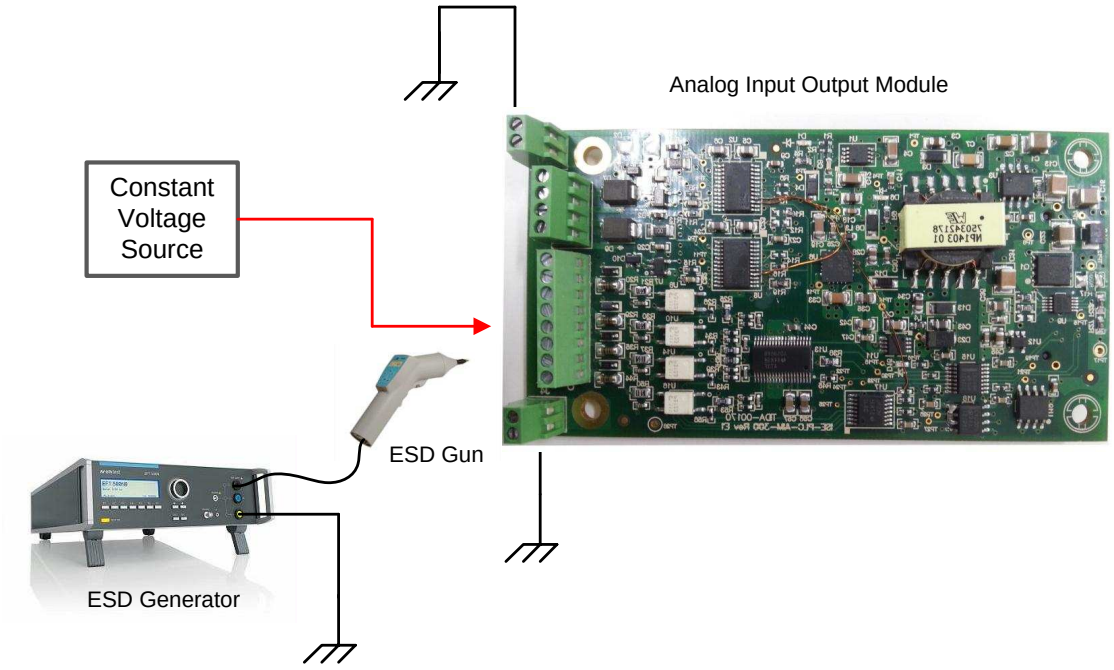


Figure 36. ESD Test Setup

Place the EUT on a horizontal coupling plane (HCP) of 160 × 80-cm dimensions on top of a wooden table 80-cm high and located above ground reference plane. Isolate the EUT and its attached cables from the HCP by a thin insulating support of 0.5-mm thick. Apply ESDs using an ESD gun directly (by contact or air discharges) or indirectly (by horizontal coupling plane). Monitor EUT operation after the test. Test the EUT in active mode using unshielded 3-m cables on I/O ports.

Analog input:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth, same as the test generator.
2. Power on the EUT.
   - The test software is configured to check the analog input for level with in a tolerance limit of 0.2%.
   - If the input level exceed the tolerance limit, the LED on the I/O controller toggles.
3. Set the voltage level to 3-V DC and current level.
4. Perform the ESD test as per the test levels mentioned in Table 13.
5. After testing the degradation, test the performance.
6. Repeat the test by changing the input voltage level to 6-V DC.

Analog output:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth, same as the ESD generator.
2. Power on the EUT.
   - The test software is configured to generate an output of 2.5 V and 7.5 V alternately for two seconds each.
   - The respective channel is checked before and after the test.
3. Perform the ESD test as per the test levels mentioned in Table 13.
4. After testing the degradation, test the performance.

7.3.2.3 Results

Table 13. ESD Test Results

TEST NO	TEST MODE	OBSERVATION
1	Air 2 kV	Pass
2	Air –2 kV	Pass
3	Air 4 kV	Pass
4	Air –4 kV	Pass
5	Air 6 kV	Pass
6	Air –6 kV	Pass
7	Air 8 kV	Pass
8	Air 8 kV	Pass
9	Contact 1 kV	Pass
10	Contact –1 kV	Pass
11	Contact 2 kV	Pass
12	Contact –2 kV	Pass
13	Contact 4 kV	Pass
14	Contact –4 kV	Pass
15	HCP 2 kV	Pass
16	HCP –2 kV	Pass
17	HCP 4 kV	Pass
18	HCP –4 kV	Pass
22	HCP –4 kV	Pass

7.3.3 EFT: IEC61000-4-4

Test Level and Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

Table 14. EFT Test Levels and Performance Criteria

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE
EFT/B IEC 61000-4-4	±2 kV at 5 kHz, 100kHz on signal ports	Criteria A

Description

Setup

Inject the burst signal on all cables together using a capacitive coupling clamp. Connect the EUT to auxiliary sources by unshielded cables. Set the lengths of the cables to 3 m and place the cables 10 cm above the reference plane. Test with the EUT placed 10 cm above the reference plane on insulating material, and with the EUT placed on the reference plane.

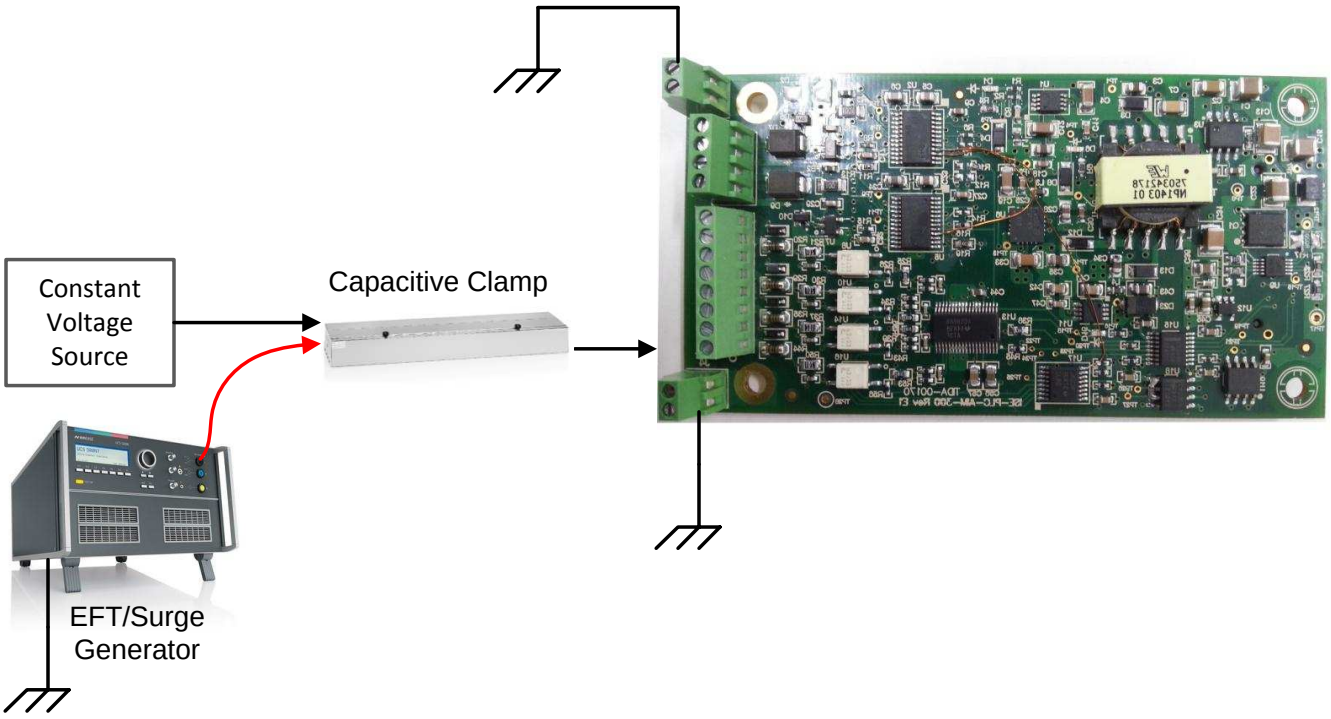


Figure 37. EFT Test Setup

Monitoring

Analog input:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth same as the test generator.
2. Power on the EUT.
   - The test software is configured to check the analog input for level with in a tolerance limit of 0.2%.
   - If the input level exceed the tolerance limit, the LED on the I/O controller toggles.
3. Set the voltage level to 3-V DC.
4. Perform the EFT test as per the test levels mentioned in Table 15.
5. After testing the degradation, test the performance.
6. Repeat the test by changing the input voltage level to 6-V DC.

Analog Output:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth same as the EFT generator.
2. Power on the EUT.
   - The test software is configured to generate an output of 2.5 V and 7.5 V alternately for two seconds each.
   - The respective channel is checked before and after the test.
3. Perform the EFT test as per the test levels mentioned in Table 15.
4. After testing the degradation, test the performance.

Results

Table 15. EFT Test Results

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV , 5 kHz	Pass
2	–0.5 kV , 5 kHz	Pass
3	1 kV , 5 kHz	Pass
4	–1 kV , 5 kHz	Pass
5	1.5 kV , 5 kHz	Pass
6	–1.5 kV , 5 kHz	Pass
7	2 kV , 5 kHz	Pass
8	–2 kV , 5 kHz	Pass
9	0.5 kV , 100 kHz	Pass
10	–0.5 kV , 100 kHz	Pass
11	1 kV , 100 kHz	Pass
12	–1 kV , 100 kHz	Pass
13	1.5 kV , 100 kHz	Pass
14	–1.5 kV , 100 kHz	Pass
15	2 kV , 100 kHz	Pass
16	–2 kV , 100 kHz	Pass

7.3.4 Surge: IEC61000-4-5

Test Level and Expected Performance

The common-mode Surge at I/O connectors and the performance criteria expected are as follows:

Table 16. Surge Test Levels and Performance Criteria

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE
Surge IEC 61000-4-5	±1-kV CM on signal ports	Criteria B (After the test, the analog I/O module continued to operate as intended without manual intervention)

Description

Setup

Place the EUT and analog I/O cable on non-conductive support 10 cm above a reference ground plane. Inject Surge into the analog I/O cable for testing through the coupling decoupling network. Monitor the EUT operation before and after the test.

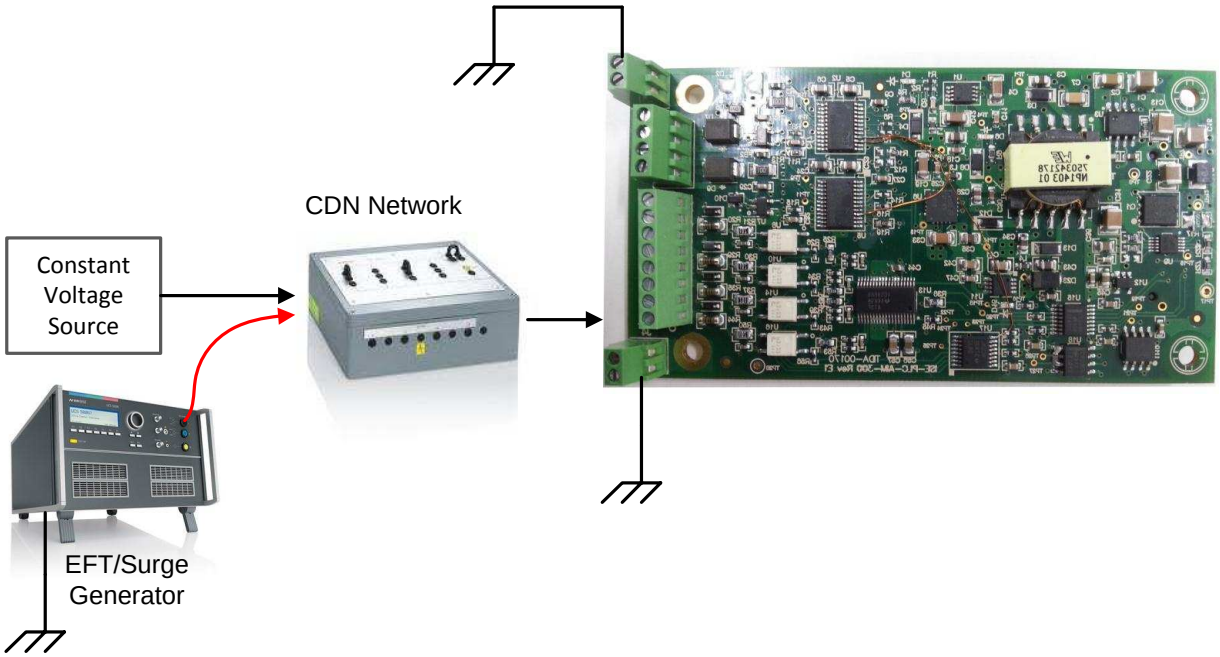


Figure 38. Surge Test Setup

Monitor the EUT operation after the test. Monitor all the four channels after the test by the MCU (on the I/O controller) and compare with a set value (equivalent of the external constant voltage or current source). The error should be within the accuracy as mentioned in Section 7.3.

Monitoring

Analog input:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth same as the test generator.
2. Power on the EUT.
   - The test software is configured to check the analog input for level with in a tolerance limit of 0.2%.
   - If the input level exceed the tolerance limit, the LED on the I/O controller toggles.
3. Set the voltage level to 3-V DC.
4. Perform the Surge test is performed as per the test levels mentioned in Table 17.
5. After testing the degradation, test the performance.
6. Conduct the test by changing the input voltage level to 6-V DC.

Analog output:

1. Connect the EUT as shown in Section 6. The shield pin is connected to local earth same as the Surge generator.
2. Power on the EUT.
   - The test software is configured to generate an output of 2.5 V and 7.5 V alternately for two seconds each.
   - The respective channel is checked before and after the test.
3. Perform the Surge test as per the test levels mentioned in Table 17.
4. After testing the degradation, test the performance.

Results

Table 17. Surge Test Results

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV	Pass
2	–0.5 kV	Pass
3	1 kV	Pass
4	–1 kV	Pass

8 References

1. AN-2292 Designing an Isolated Buck (Fly-Buck™) Converter (SNVA674B)
2. AN-2040 Output Voltage Clamping Using the LM5069 Hot Swap Controller (SNVA430B)
3. TIDA-00123 PLC I/O Module Front-End Controller Using a Tiva C Series ARM Cortex-M4 MCU (TIDU191)
4. TIDA-00118 16-Bit Analog Output Module Reference Design for Programmable Logic Controllers (PLCs) (TIDU189)

8.1 Terminology

Signal-to-Noise Ratio (SNR)
SNR is a measure that compares the level of a desired signal to the level of background noise. SNR is defined as the ratio of signal power to the noise power. The SNR specification provides information regarding the noise energy excluding the fundamental and harmonic energy present in the frequency spectrum for a particular input frequency. The SNR calculation usually integrates **noise till Nyquist frequency**.

$$SNR = \frac{P_{SIGNAL}}{P_{NOISE}} \tag{21}$$

$$SNR = 10\log_{10}\left[\frac{P_{SIGNAL}^{2}}{(\text{Sum of all harmonic amplitudes} - F_{IN} - DC)} \times 2\right] \tag{22}$$

Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)
DNL is the deviation between two analog values corresponding to adjacent input digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the DNL. DNL errors accumulate to produce a total INL. DNL and INL values are usually specified using one of the following units: LSB or %FSR.

Total Unadjusted Error (TUE)
TUE is measurement error without any gain or offset error compensations. TUE gives an exact measure of the system level inaccuracies. With the right choice of components and proper PCB layout, the need for factory calibration may be avoided, which can save time and costs during mass production.

$$TUE = \sqrt{(\text{Offset Error})^2 + (\text{Gain Error})^2 + (DNL)^2 + (INL)^2} \tag{23}$$

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00170.

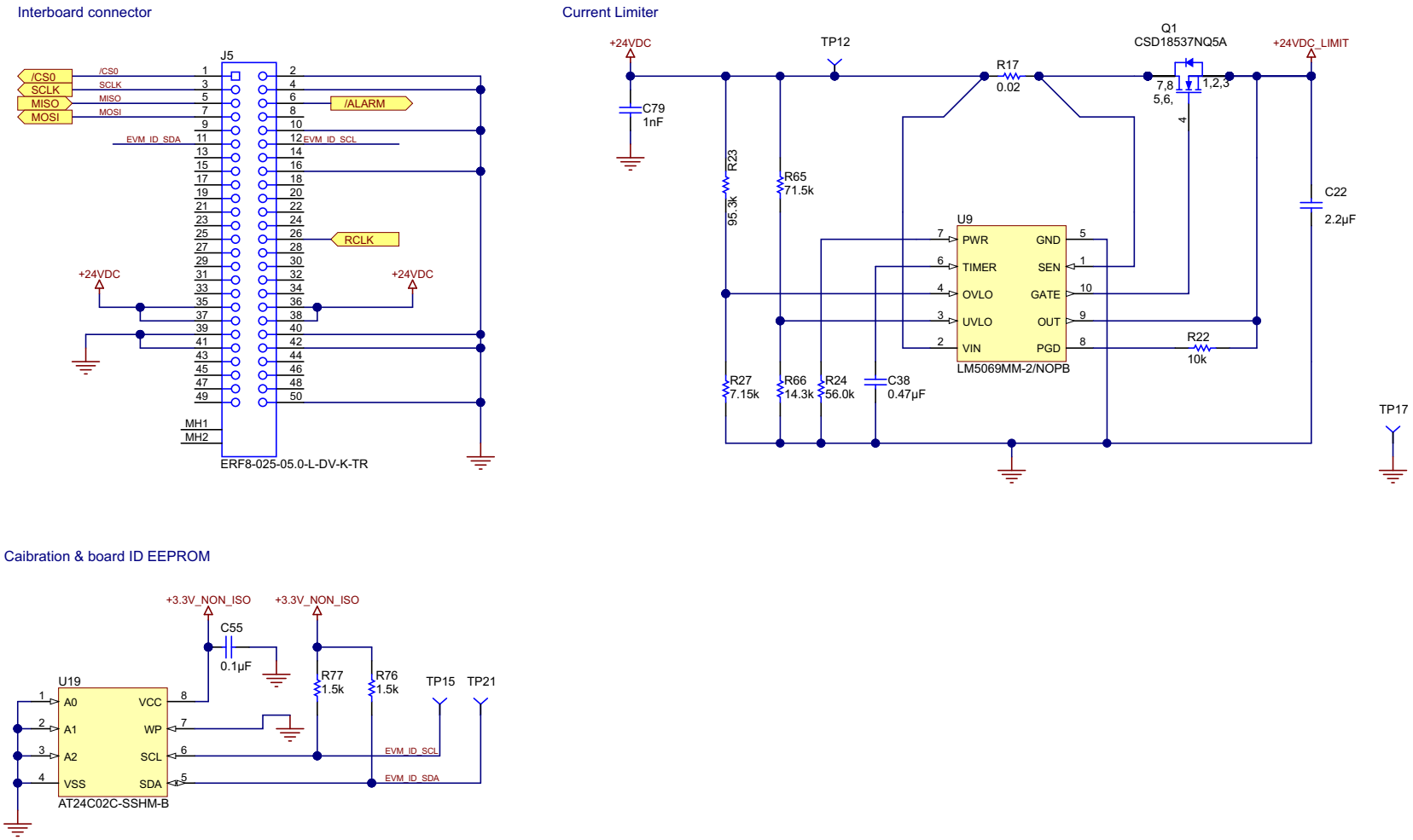


Figure 39. Inter-Board Connector, Inrush Current Limit, and EEPROM Schematic

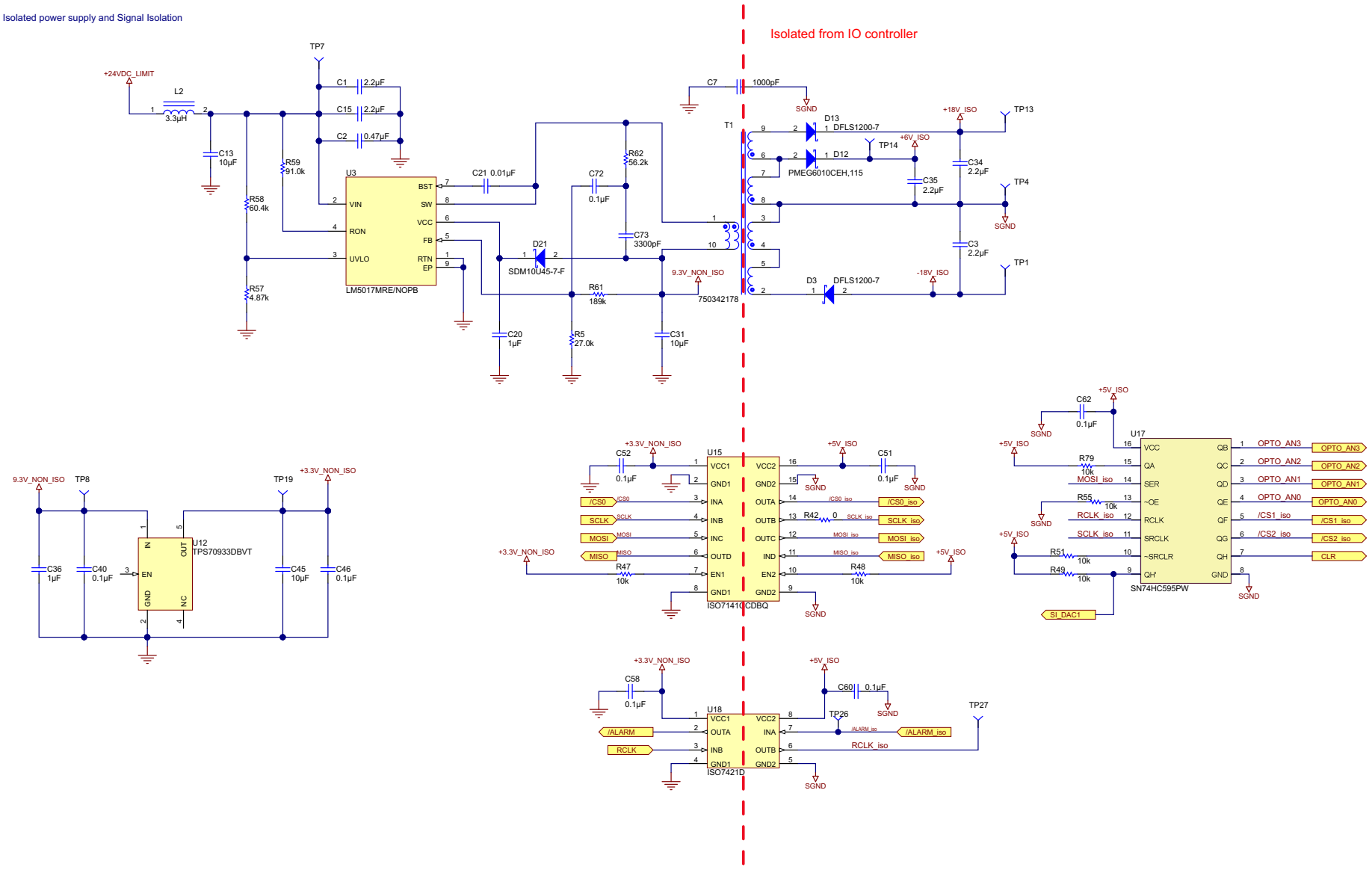


Figure 40. Isolated PS (Fly-Buck), Digital Isolation, and Shift Register Schematic

LDO

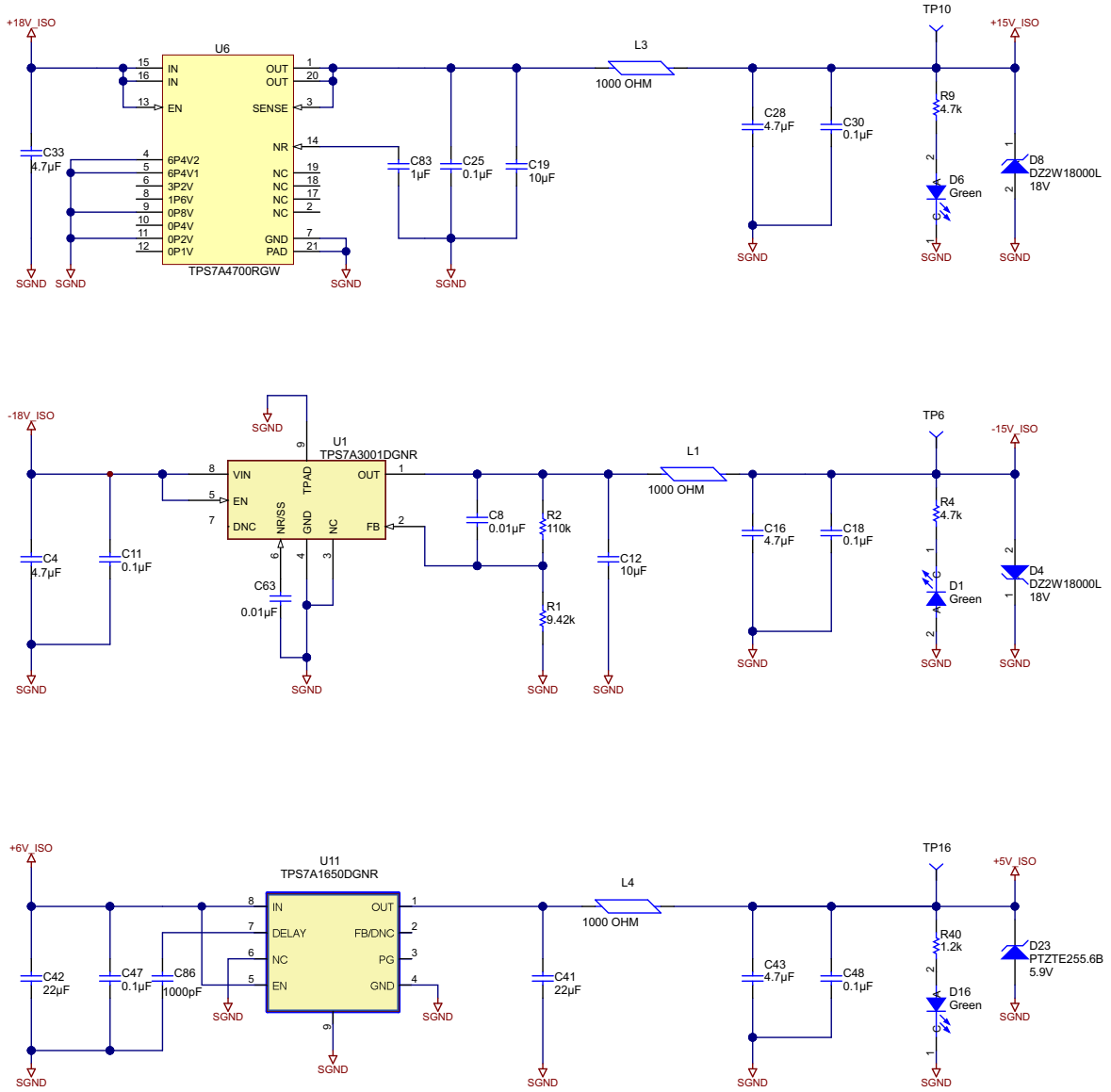


Figure 41. LDO Schematic

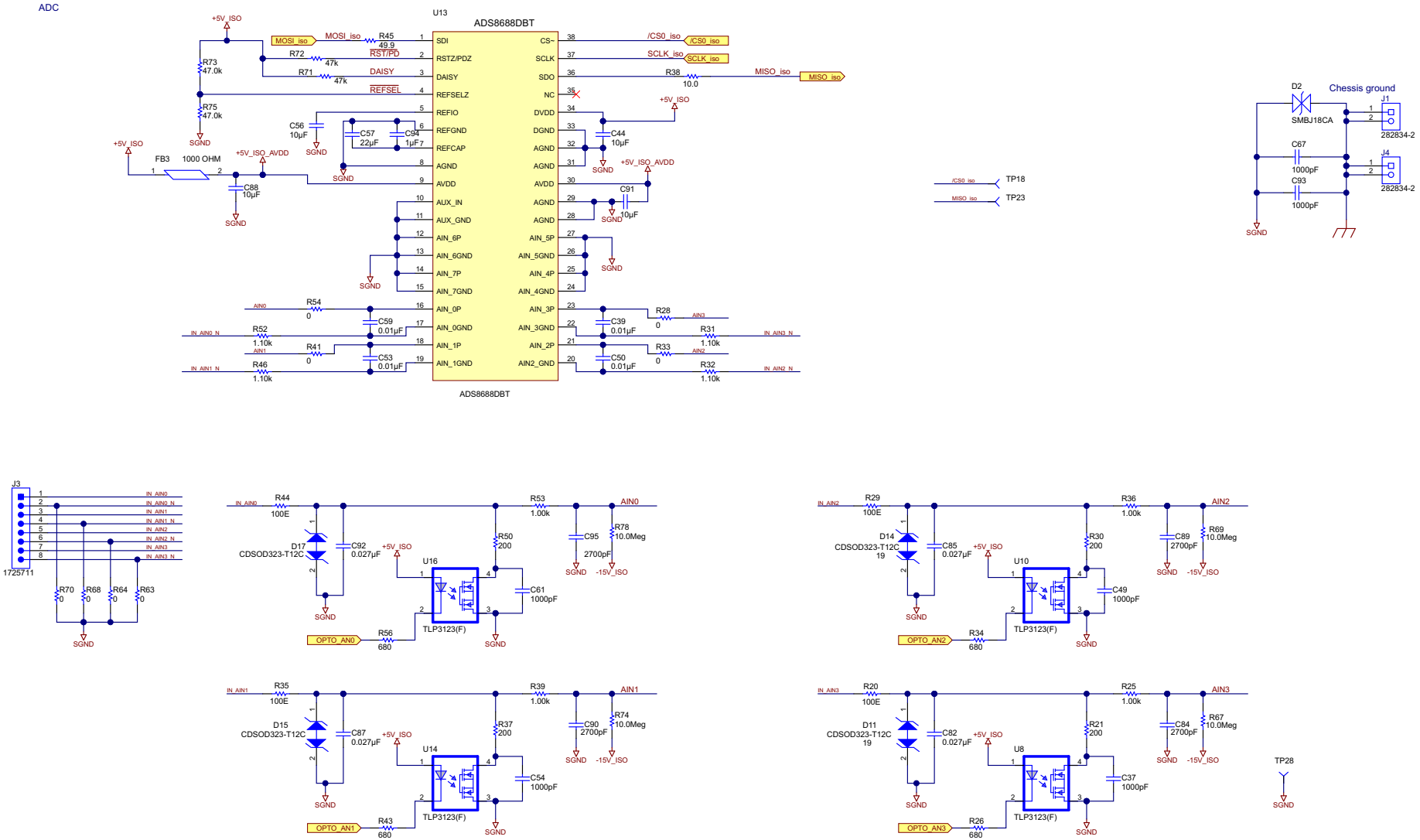


Figure 42. ADS8688 and Input Protection Schematic

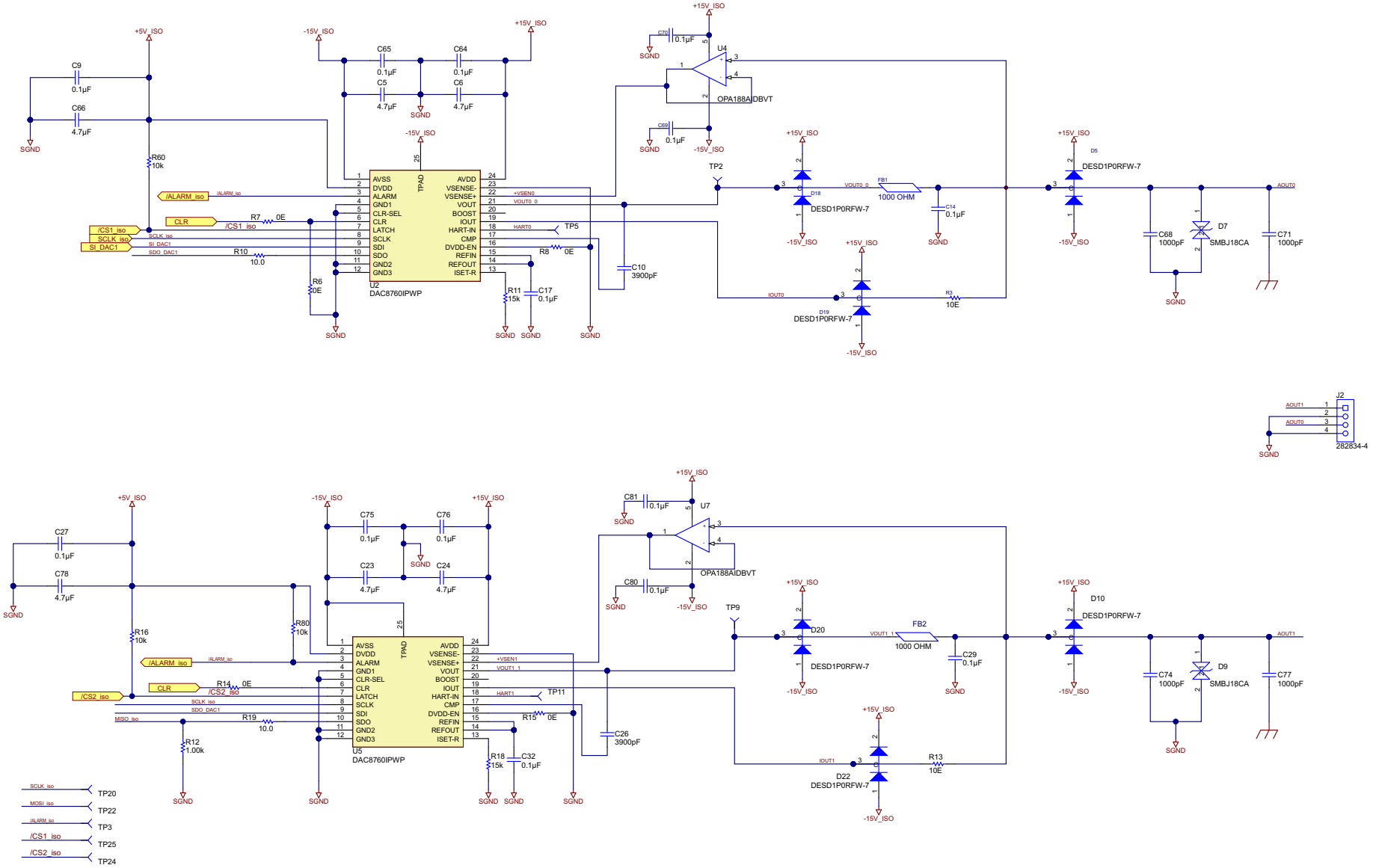


Figure 43. DAC8760 and Output Protection Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00170.

Table 18. BOM

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
1	C1, C15, C22	CAP, CERM, 2.2 µF, 100 V, ±10%, X7R, 1210	MuRata	GRM32ER72A225KA35L	3
2	C2	CAP, CERM, 0.47 µF, 100 V, ±10%, X7R, 1206	MuRata	GRM31MR72A474KA35L	1
3	C3, C34, C35	CAP, CERM, 2.2 µF, 25 V, ±10%, X7R, 0805	MuRata	GRM21BR71E225KA73L	3
4	C4, C33	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, 1206	MuRata	GRM31CR71H475KA12L	2
5	C5, C6, C16, C23, C24, C28, C43, C66, C78	CAP, CERM, 4.7 µF, 50 V, ±10%, X5R, 0805	TDK	C2012X5R1H475K125AB	9
6	C7, C67, C68, C71, C74, C77, C93	CAP, CERM, 1000 pF, 2 KV 10% X7R 1206	Johanson Dielectrics Inc	202R18W102KV4E	7
7	C8, C21	CAP, CERM, 0.01 µF, 100 V, ±5%, X7R, 0603	AVX	06031C103JAT2A	2
8	C9, C11, C14, C17, C18, C25, C27, C29, C30, C32, C47, C48, C64, C65, C69, C70, C75, C76, C80, C81	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	AVX	06035C104KAT2A	20
9	C10, C26	CAP, CERM, 3900 pF, 50 V, ±10%, X7R, 0603	MuRata	GRM188R71H392KA01D	2
10	C12, C19	CAP, CERM, 10 µF, 25 V, ±10%, X7R, 1206	MuRata	GRM31CR71E106KA12L	2
11	C13	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1
12	C20	CAP, CERM, 1 µF, 50 V, ±10%, X5R, 0603	MuRata	GRM188R61H105KAALD	1
13	C31	CAP, CERM, 10 µF, 35 V, ±20%, X7R, 1210	Taiyo Yuden	GMK325AB7106MM-T	1
14	C36	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	AVX	08055C105KAT2A	1
15	C37, C49, C54, C61	CAP, CERM, 1000 pF, 50 V, ±20%, X7R, 0402	TDK	C1005X7R1H102M	4
16	C39, C50, C53, C59	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0402	MuRata	GRM155R71H103KA88D	4
17	C40, C46, C51, C52, C55, C58, C60, C62	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	8
18	C41, C42	CAP, CERM, 22 µF, 16 V, ±20%, X5R, 0805	MuRata	GRM21BR61C226ME44	2
19	C44	CAP, CERM, 10 µF, 25 V, ±20%, X5R, 0603	TDK	C1608X5R1E106M080AC	1
20	C45, C56	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0805	AVX	0805YD106MAT2A	2
21	C57	CAP, CERM, 22 µF, 16 V, ±10%, X5R, 0805	TDK	C2012X5R1C226K125AC	1
22	C72	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 0603	MuRata	GRM188R72A104KA35D	1
23	C73	CAP, CERM, 3300 pF, 100 V, ±5%, X7R, 0603	AVX	06031C332JAT2A	1
24	C79	CAP, CERM, 1000 pF, 100 V, ±20%, X7R, 0603	AVX	06031C102MAT2A	1
25	C82, C85, C87, C92	CAP, CERM, 0.027 µF, 50 V, ±5%, C0G/NP0, 1206	MuRata	GRM3195C1H273JA01D	4
26	C83	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	TDK	C1608X7R1E105K080AB	1
27	C84, C89, C90, C95	CAP, CERM, 2700 pF, 100 V, ±5%, X7R, 0603	AVX	06031C272JAT2A	4
28	C86	CAP, CERM, 1000 pF, 100 V, ±5%, X7R, 0603	AVX	06031C102JAT2A	1

Table 18. BOM (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
29	C88, C91	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0603	Taiyo Yuden	EMK107BBJ106MA-T	2
30	C94	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	Taiyo Yuden	EMK107B7105KA-T	1
31	D1, D6, D16	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	3
32	D3, D13	Diode, Schottky, 200 V, 1 A, PowerDI123	Diodes Inc.	DFLS1200-7	2
33	D4, D8	Diode, Zener, 18 V, 1 W, SOD-123	Panasonic	DZ2W18000L	2
34	D5, D10	Diode, P-N, 70 V, 0.2 A, SOT-323	Diodes Inc	DESD1P0RFW-7	2
35	D7, D9	TVS 18-V, 600-W BI-DIR SMB	Littelfuse Inc	SMBJ18CA	2
36	D11, D14, D15, D17	Diode, TVS, Array, 19 V, SOD323	Bourns Inc.	CDSOD323-T12C	4
37	D12	Diode, Schottky, 60 V, 1 A, SOD-123F	NXP Semiconductor	PMEG6010CEH,115	1
38	D21	Diode, Schottky, 45 V, 0.1 A, SOD-523	Diodes Inc.	SDM10U45-7-F	1
39	D23	Diode Zener 5.9 V, 1 W PMDS	Rohm Semiconductor	PTZTE255.6B	1
40	FB1, FB2,FB3	Ferrite Chip 1000 Ω, 300 mA 0603	TDK Corporation	MMZ1608Y102B	2
41	L1, L3, L4	Ferrite Chip 1000 Ω, 300 mA 0603	TDK Corporation	MMZ1608B102C	4
42	J1, J4	Terminal Block, 2×1, 2.54 mm, TH	TE Connectivity	282834-2	2
43	J2	Receptacle, 100 mil, 4×1 TH	TE Connectivity	282834-4	1
44	J3	Terminal Block, 8×1, 2.54 mm, TH	Phoenix Contact	1725711	1
45	J5	Receptacle, 0.8 mm, 25×2, SMT	Samtec	ERF8-025-05.0-L-DV-K-TR	1
46	L2	Inductor, Chip, ±10%	EPCOS INC.	B82422H1332K	1
47	Q1	MOSFET, N-CH, 60 V, 50 A, SON 5x6mm	Texas Instruments	CSD18537NQ5A	1
48	R1	RES, 9.42 kΩ, 1%, 0.063 W, 0402	Vishay-Dale	TNPW04029K42BEED	1
49	R2	RES, 110 kΩ, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402110KFKED	1
50	R3, R13	RES, 10 Ω, 5%, 0.25 W, 1206	Vishay-Dale	CRCW120610R0JNEA	2
51	R4, R9	RES, 4.7 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06034K70JNEA	2
52	R5	RES, 27.0 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0727KL	1
53	R6, R8, R15, R28, R33, R41, R54	RES, 0 Ω, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	7
54	R10, R19, R38	RES, 10.0 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0FKEA	3
55	R11, R18	RES, 15 kΩ, 1/10 W 0.1% 0603	Vishay-Dale	RT0603BRB0715KL	2
56	R16, R47, R48, R49, R51, R55, R60, R79, R80	RES, 10 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0JNED	9
57	R17	RES, 0.02 Ω, 1%, 1 W, 1206	Susumu Co Ltd	PRL1632-R020-F-T1	1
58	R20, R29, R35, R44	RES 100 Ω .4 W 1% 0204 MELF	Vishay Beyschlag	MMA02040C1000FB300	4
59	R21, R30, R37, R50	RES, 200 Ω, 0.1%, 0.125 W, 0805	Susumu Co Ltd	RG2012P-201-B-T5	4
60	R22	RES, 10 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	1
61	R23	RES, 95.3 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060395K3FKEA	1

Table 18. BOM (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
62	R24	RES, 56.0 kΩ, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-563-B-T5	1
63	R25, R36, R39, R53	RES, 1.00 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	4
64	R26, R34, R43, R56	RES, 680 Ω, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402680RJNED	4
65	R27	RES, 7.15 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06037K15FKEA	1
66	R31, R32, R46, R52	RES, 1.10 kΩ, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04021K10FKED	4
67	R40	RES, 1.2 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K20JNED	1
68	R42	RES, 0 Ω, 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	1
69	R45	RES, 49.9 Ω, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	1
70	R57	RES, 4.87 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-074K87L	1
71	R58	RES, 60.4 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0760K4L	1
72	R59	RES, 91.0 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0791KL	1
73	R61	RES, 189 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD07189KL	1
74	R62	RES, 56.2 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0756K2L	1
75	R63, R64, R68, R70	RES 0.0 Ω .5 W Jump 1206 SMD	Vishay Dale	CRCW12060000Z0EAHP	4
76	R65	RES, 71.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060371K5FKEA	1
77	R66	RES, 14.3 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060314K3FKEA	1
78	R67, R69, R74, R78	RES, 10.0 MΩ, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210M0FKED	4
79	R71, R72	RES, 47 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040247K0JNED	2
80	R75	RES, 47.0 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0747KL	1
81	R76, R77	RES, 1.5 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED	2
82	T1	Transformer, 50 µH, SMT	Wurth Elektronik eiSos	750342178	1
83	U1	–36 V, –200 mA, Ultralow-Noise, Negative Linear Regulator	Texas Instruments	TPS7A3001DGNR	1
84	U2, U5	1-Channel, 16-Bit, Programmable Current/Voltage Output DAC for 4- to 20-mA Current Loop Applications	Texas Instruments	DAC8760IPWP	2
85	U3	100-V, 600-mA Constant On-Time Synchronous Buck Regulator, DDA0008B	Texas Instruments	LM5017MRE/NOPB	1
86	U4, U7	Precision, Low Noise, Rail-to-Rail Output, 36-V Zero-Drift Operational Amplifier	Texas Instruments	OPA188AIDBVT	2
87	U6	36-V, 1-A, 4.17-μV_{RMS}, RF LDO Voltage Regulator, RGW0020A	Texas Instruments	TPS7A4700RGW	1
88	U8, U10, U14, U16	PhotoRelay MOSFET 1A 4-SOP	Toshiba Semiconductor and Storage	TLP3123(F)	4
89	U9	Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	National Semiconductor	LM5069MM-2/NOPB	1
90	U11	IC, 60-V, 6-A IQ, 100-mA, LDO Voltage Regulator with Enable and Power-Good Functions	Texas Instruments	TPS7A1650DGNR	1
91	U12	IC REG LDO 3.3 V, 0.15 A SOT23-5	Texas Instruments	TPS70933DBVT	1

Table 18. BOM (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY
92	U13	16-bit 400 KSPS 8 Channel SAR ADC	Texas Instruments	ADS8688DBT	1
93	U15	4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	Texas Instruments	ISO7141CCDBQ	1
94	U17	IC, 8-Bit Shift Registers With 3-State Output Registers	Texas Instruments	SN74HC595PW	1
95	U18	Low-Power Dual Digital Isolators, D0008A	Texas Instruments	ISO7421D	1
96	U19	IC, EEPROM, 2KB, 1 MHZ, SOIC-8	Atmel	AT24C02C-SSHM-B	1

9.3 PCB Layout

The analog I/O module is implemented in four layers of PCB. For optimal design performance, follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Make additional considerations for providing robust EMC and EMI immunity. Place all protection elements as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, use low impedance, low-inductance traces along the output signal path and protection elements. Copper pours are used in place of traces whenever possible. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

9.3.1 Layout Guidelines

To achieve a high performance, follow these layout guidelines:

1. Use a common ground plane for both analog and digital.
2. Route all signals, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then, short both grounds to form a common ground plane.
3. Return the ADC ground pins to the ground plane through multiple vias (PTH).
4. Ensure that protection elements such as TVS diodes, capacitors are placed as close to connectors as possible to ensure that return current from high-energy transients does not cause damage to sensitive devices. Furthermore, use large and wide traces to ensure a low-impedance path for high-energy transients.
5. Place the decoupling capacitors close to supply pin of IC.
6. Use multiple vias for power and ground for decoupling caps.
7. Route the current sense resistor as Kelvin sense connection.
8. SPI lines: For signal integrity, place the termination resistances near to the source.
9. Place decoupling capacitors close to each AVDD's and AVSS's respective pins.
10. Place the reference capacitor close to the voltage reference input pin.

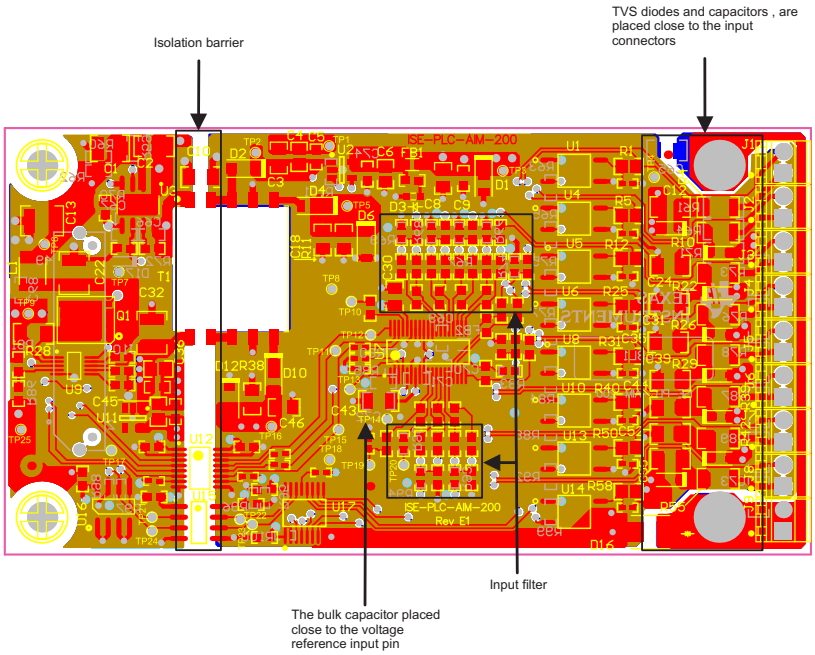


Figure 44. PCB Layout Guideline

9.3.2 Layout Prints

To download the layer plots, see the design files at TIDA-00170.

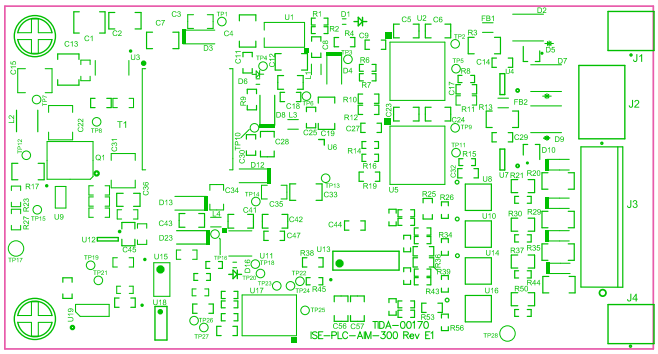


Figure 45. Top Overlay

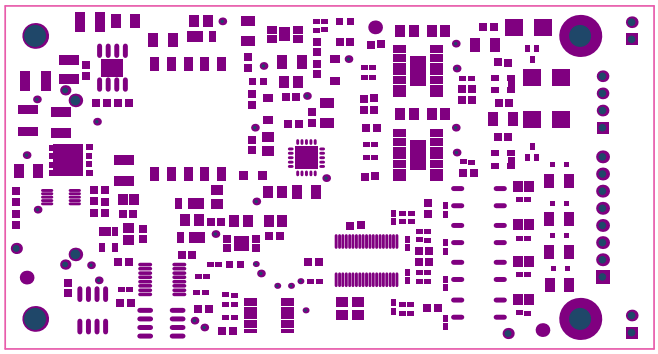


Figure 46. Top Solder Mask

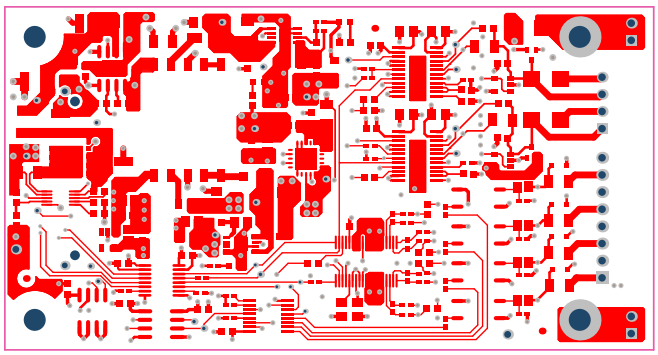


Figure 47. Top Layer

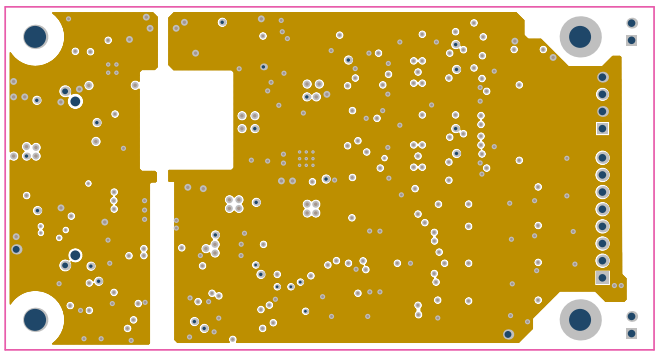


Figure 48. Layer 2

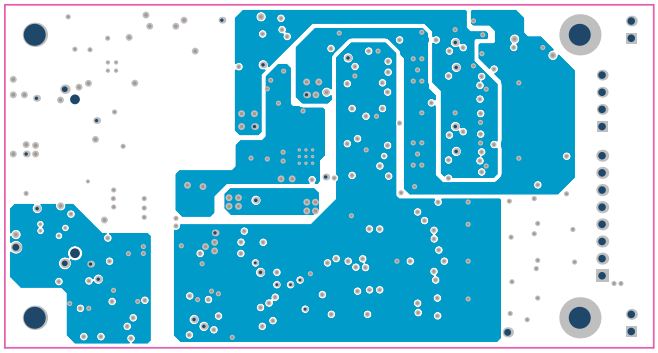


Figure 49. Layer 3

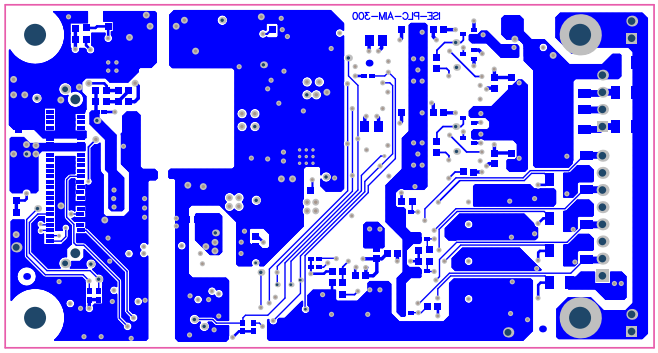


Figure 50. Bottom Layer

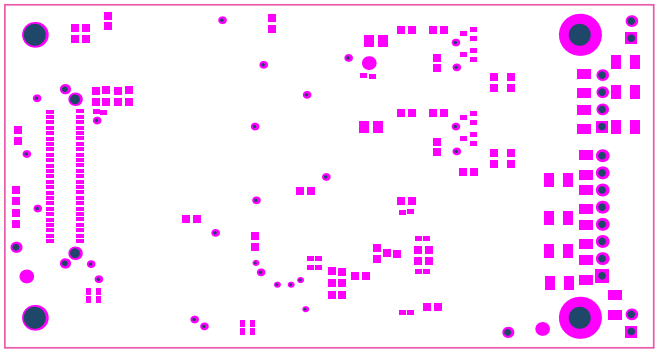


Figure 51. Bottom Solder Mask

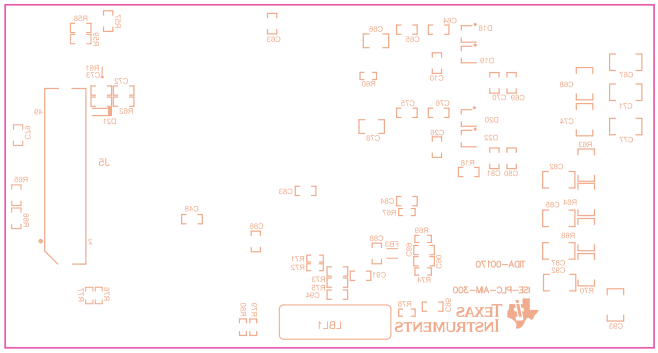
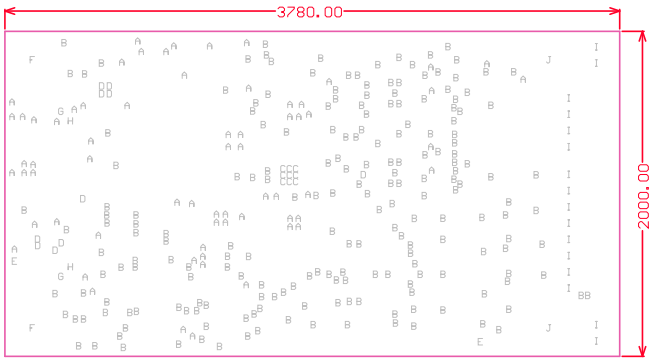


Figure 52. Bottom Overlay



Symbol	Hit Count	Tool Size	Plated	Hole Type
C	9	8mil (0.203mm)	PTH	Round
D	10	12mil (0.305mm)	PTH	Round
B	202	16mil (0.406mm)	PTH	Round
A	67	20mil (0.508mm)	PTH	Round
G	2	33mil (0.838mm)	PTH	Round
E	2	40mil (1.016mm)	PTH	Round
I	16	43.307mil (1.1mm)	PTH	Round
H	2	57.087mil (1.45mm)	NPTH	Round
J	2	128mil (3.251mm)	PTH	Round
F	2	128mil (3.251mm)	NPTH	Round
	314 Total			

Drill Table
FOR 8MIL DRILL +0/-8MIL
FOR 12MIL DRILL +0/-12MIL
FOR 16MIL DRILL +0/-16MIL

Figure 53. Drill Drawing

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00170.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00170.

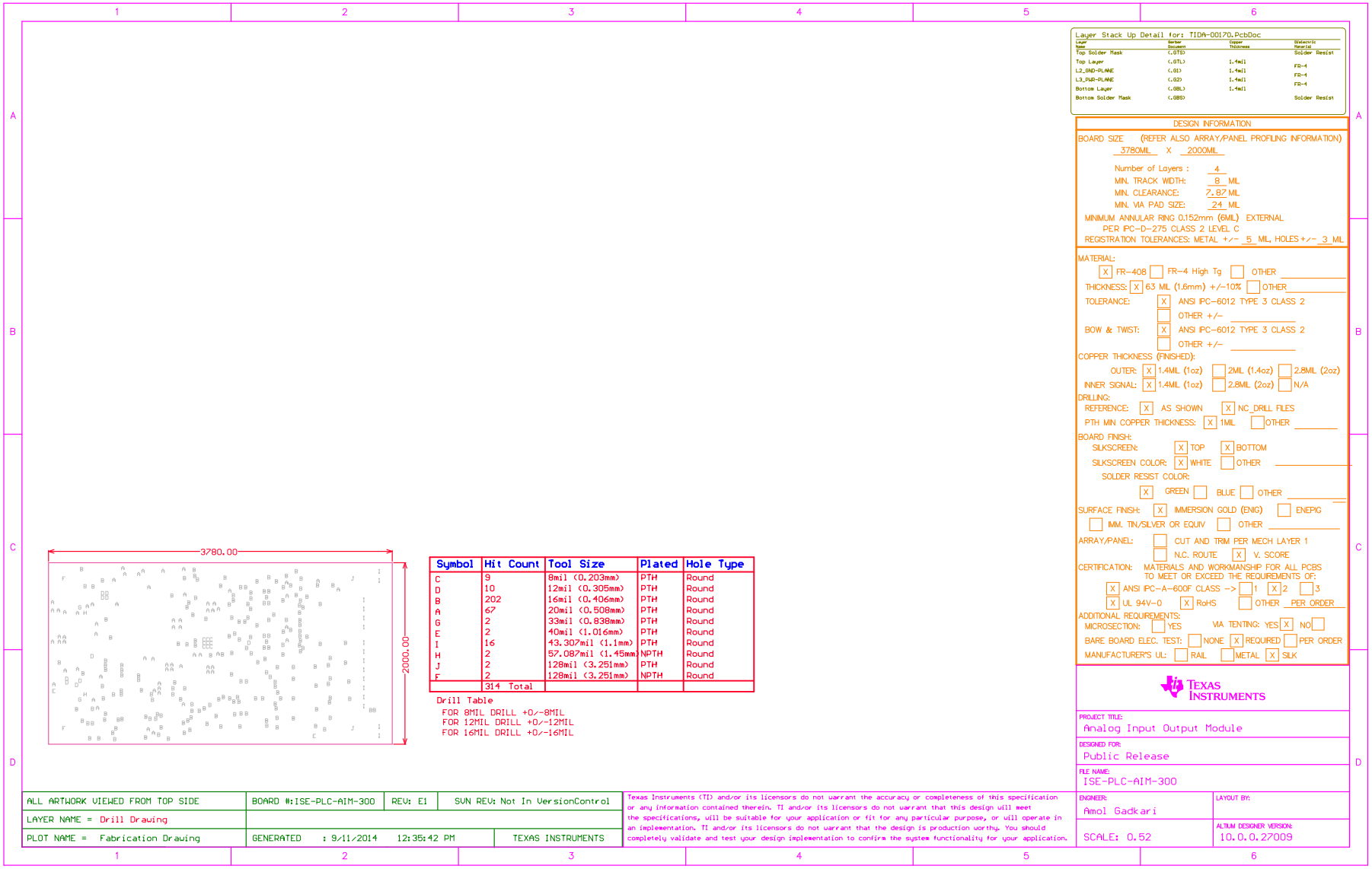


Figure 54. Fabrication Drawing

9.6 Software Files

To download the software files, see the design files at TIDA-00170.

10 About the Author

AMOL GADKARI is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Amol has eight years of experience in mixed signal board design, analog circuit designs, and EMC-protection circuit design. He can be reached at a-gadkari@ti.com.

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