

PMP7208RevB1 (16325) Test Results

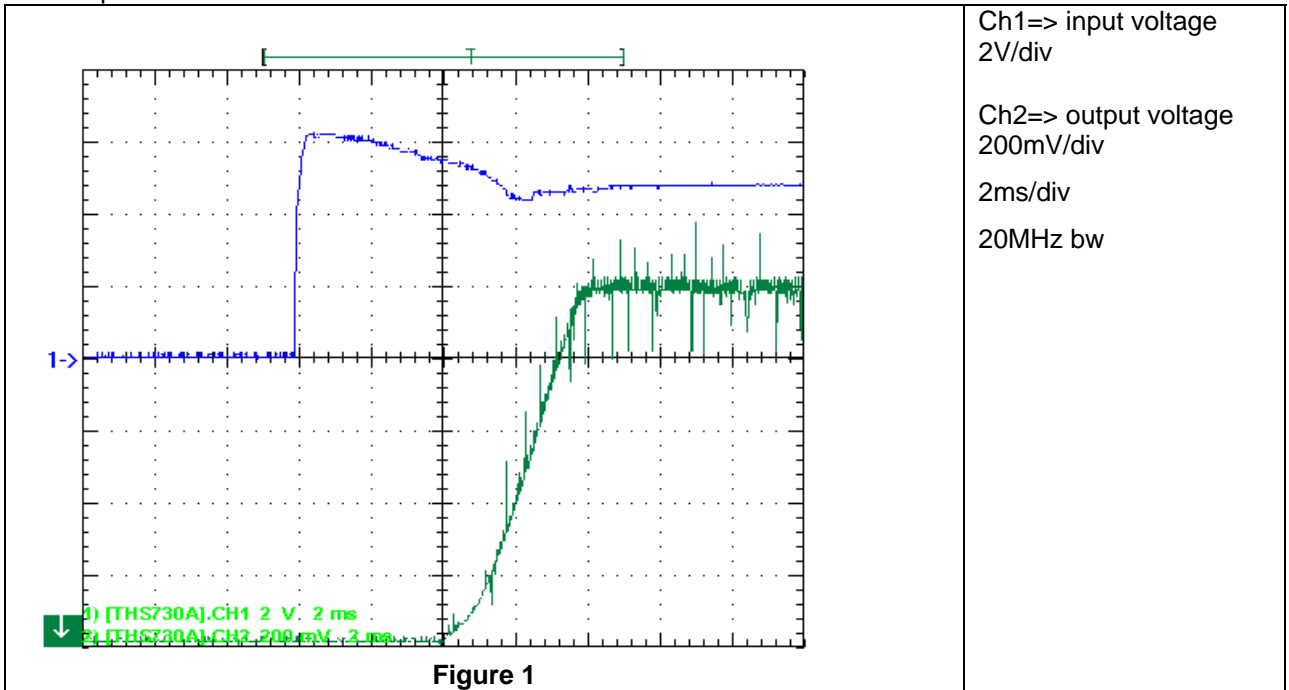
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Topology: Buck

Device: TPS40303 + 3x CSD16325Q5

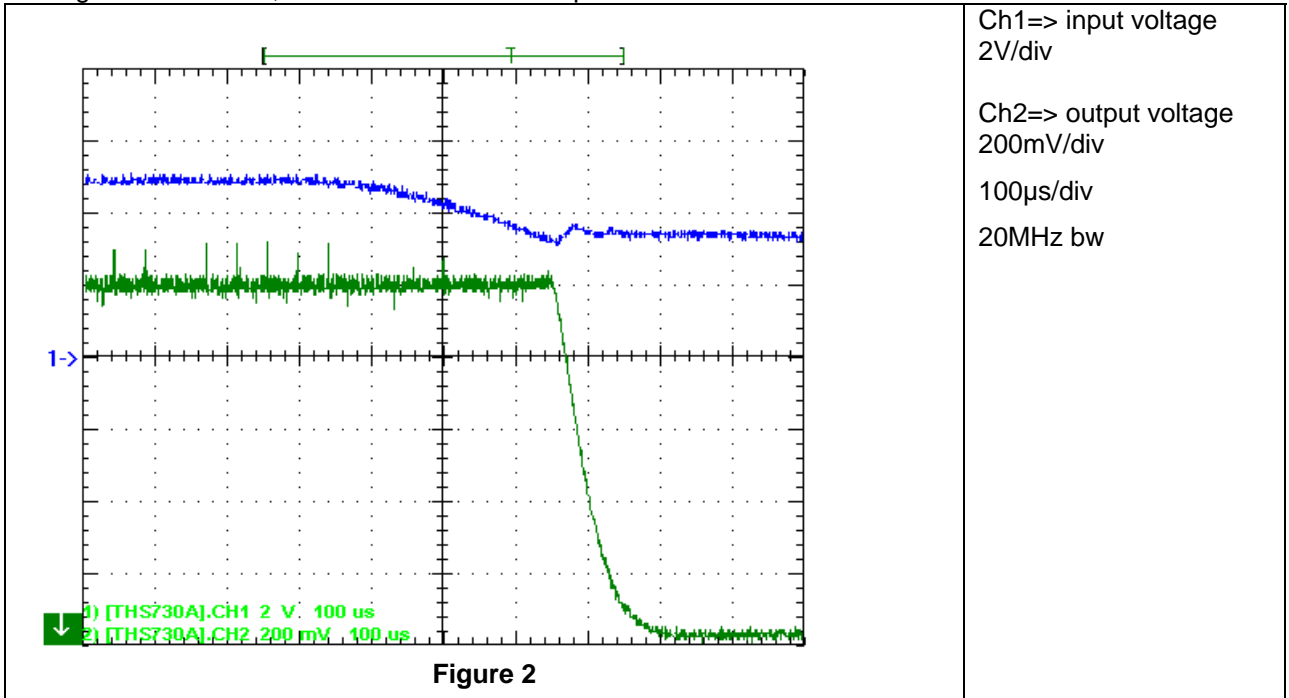
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 5V, with 25A load at the output.



2 Shutdown

The shutdown waveform is shown in the Figure 2 (the power supply was switched off). The input voltage was set at 5V, with 25A load on the output.



3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 5V. Input voltage was measured at C3 and the output voltage at C16

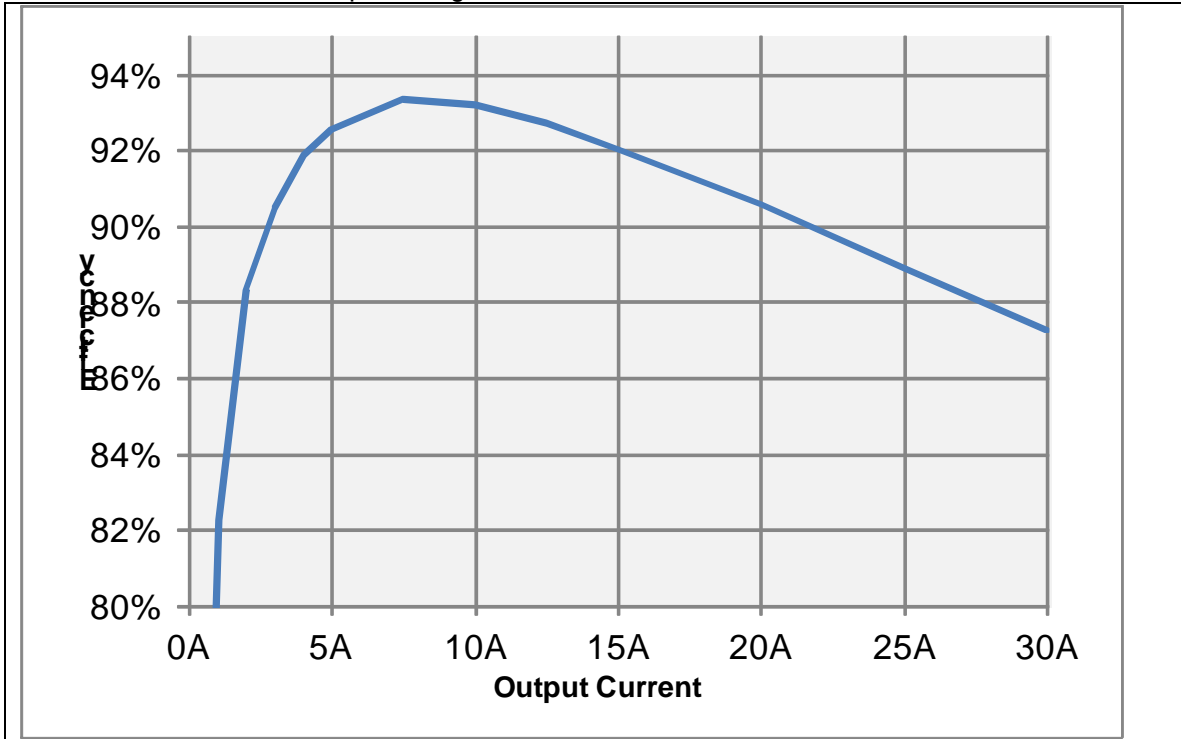


Figure 3

4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The input voltage was set to 5V. The output voltage was measured at J2-1 (VOUT) and **TP102 (AGND)**.

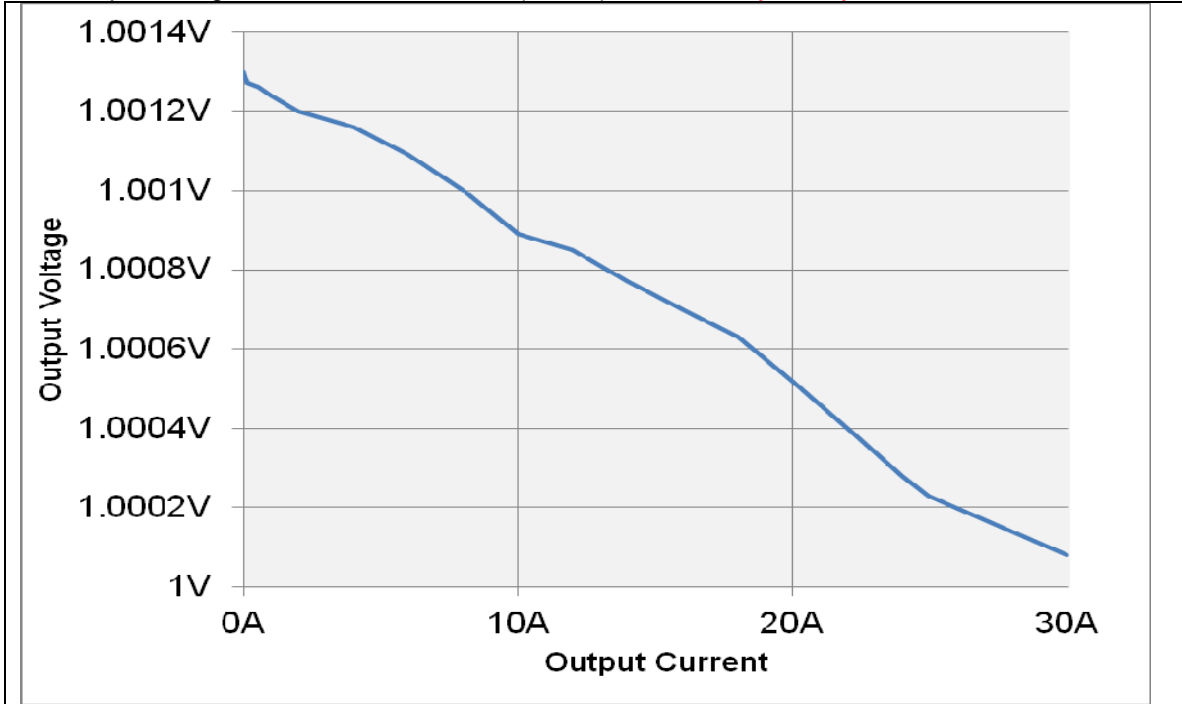
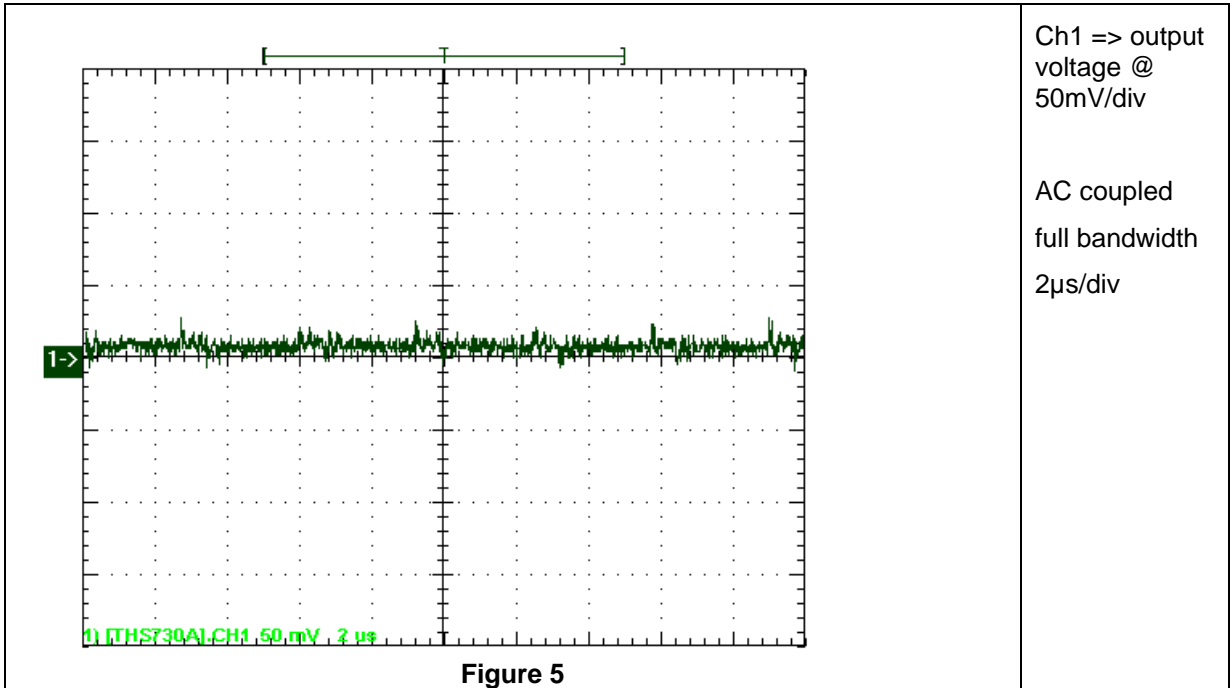


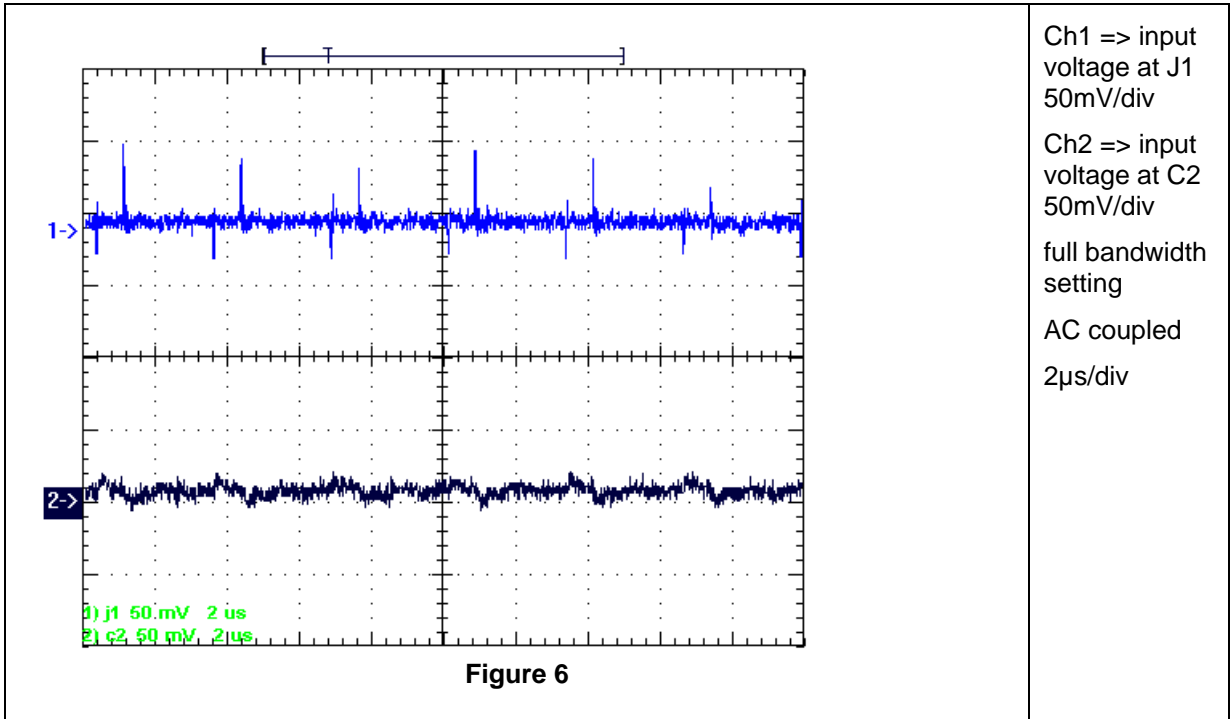
Figure 4

5 Ripple Voltage

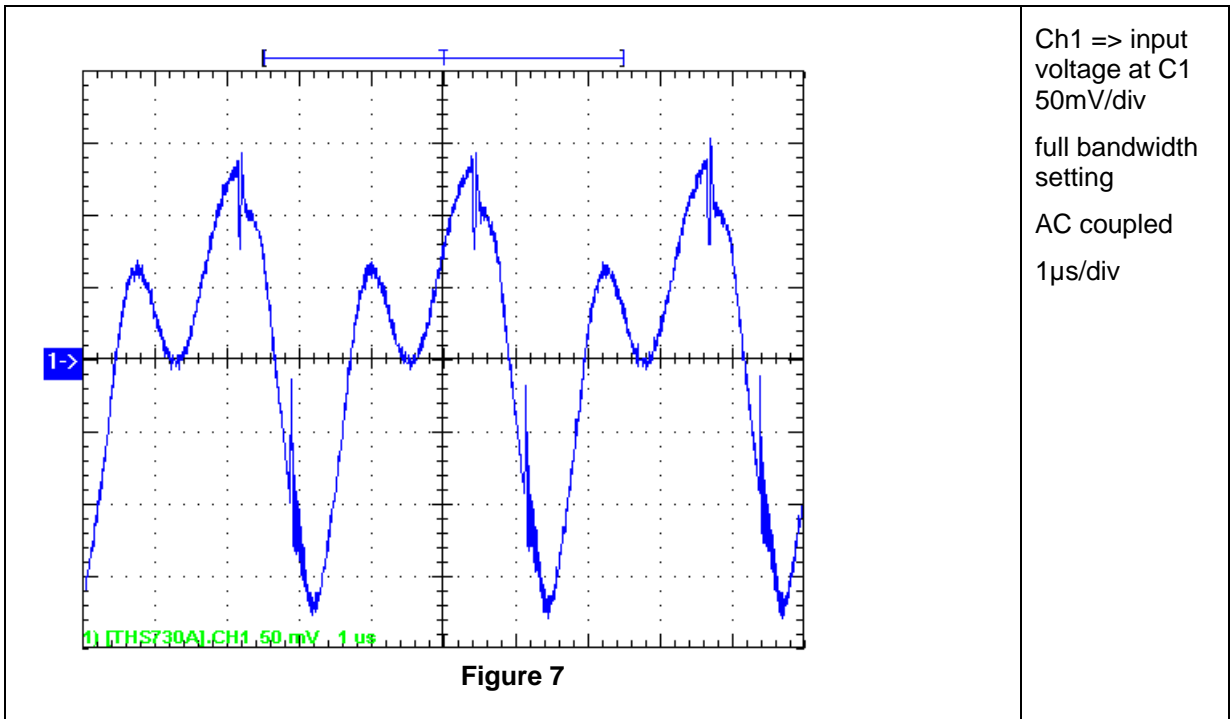
The output ripple voltage is shown in Figure 5. The image was taken with 25A load 5V at the input.



The input ripple voltage is shown in Figure 6. The image was taken with 25A load 5V at the input. The two waveforms were captured separately.



The input ripple voltage is shown in Figure 7. The image was taken with 25A load 5V at the input.



6 Control Loop Frequency Response

Figure 8 shows the loop response with 25A load and 5V input. The ground connection should be **analog power ground (TP102)**.

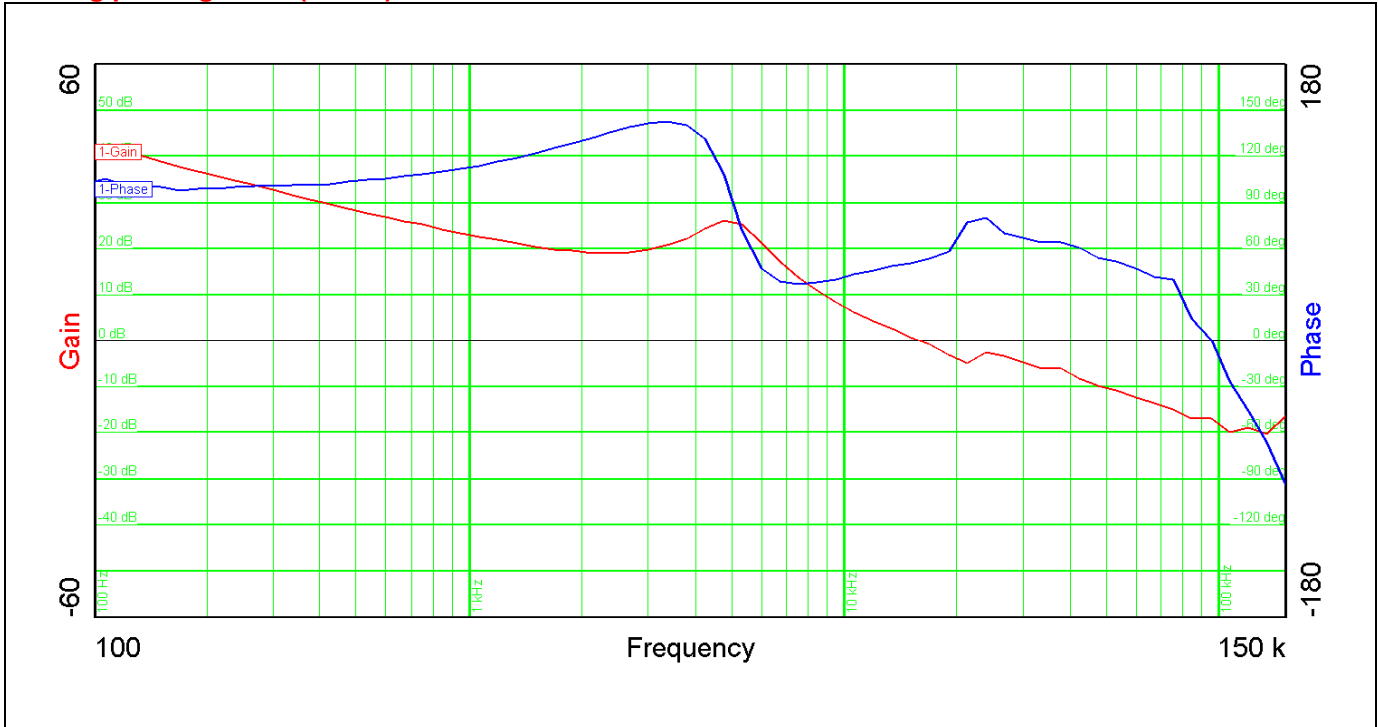


Figure 8

Table 1 summarizes the results from Figure 8

Input Voltage	5V
Bandwidth (kHz)	15.88
Phasemargin	52°
slope (20dB/decade)	-1.88
gain margin (dB)	-17
slope (20dB/decade)	-3
freq (kHz)	95.3

Table 1

7 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 12.5A to 25A with 400Hz frequency. The input voltage was set to 5V

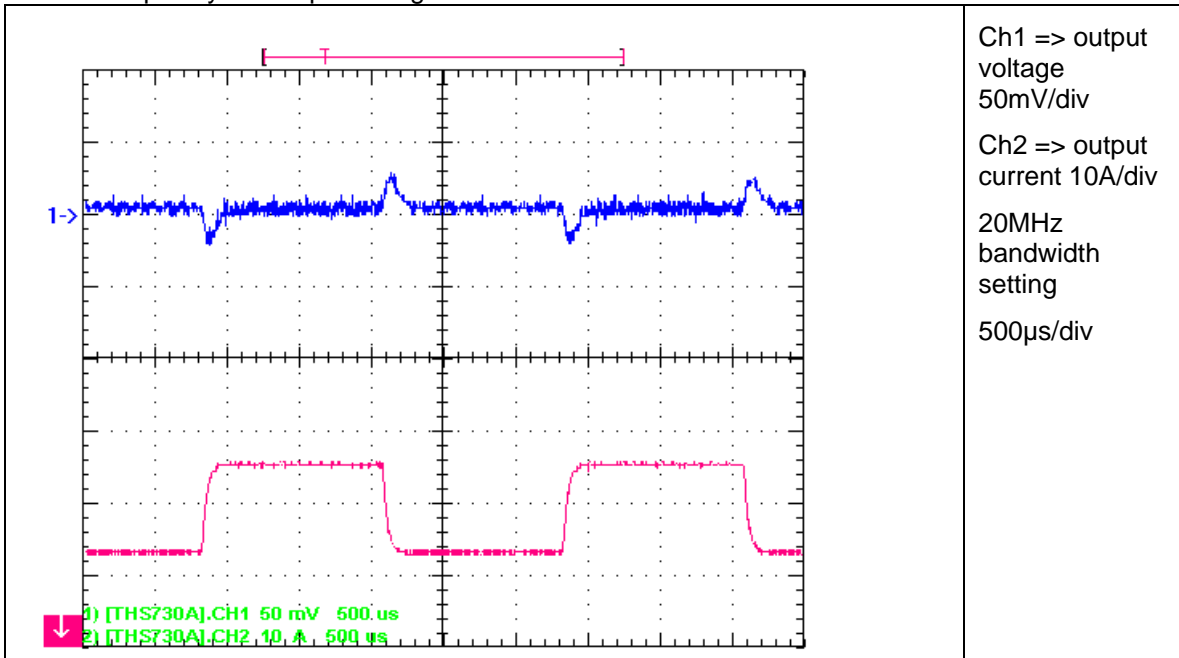


Figure 9

After modifying the loop (R3=28kOhm, C9=1nF, C13=33pF) this measurement was repeated. The result is shown in Figure 10.

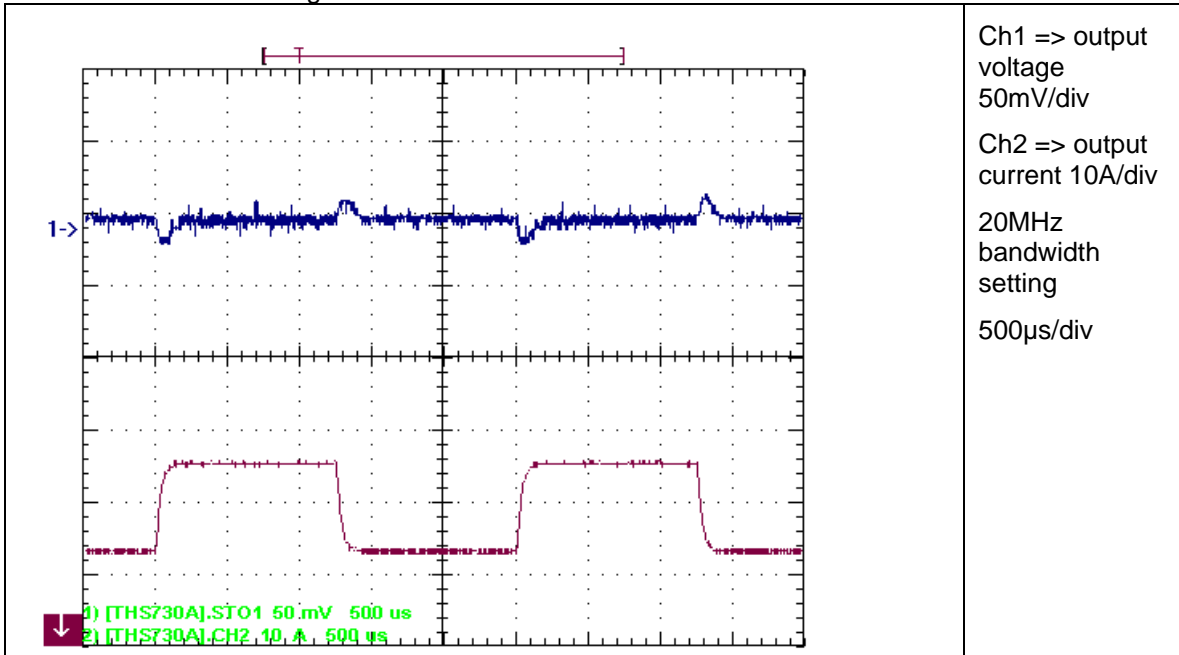


Figure 10

Then the load step were increased. The load current was switched between 10A and 30A. This is shown in Figure 11.

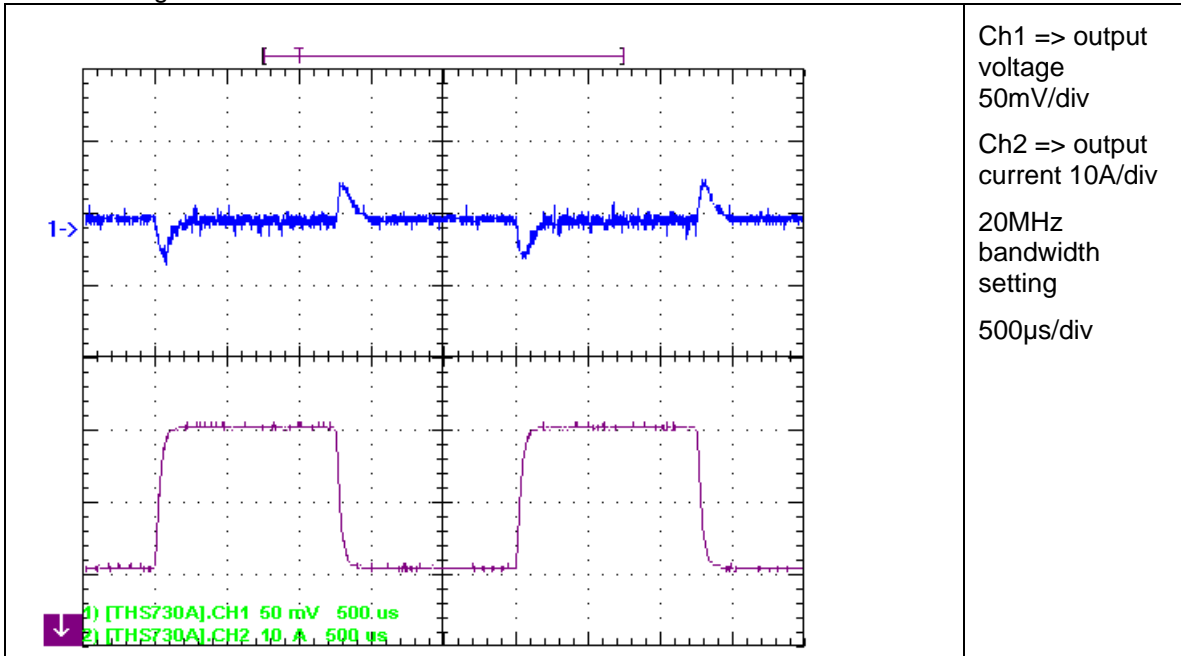


Figure 11

8 Miscellaneous Waveforms

8.1 Switchnode (Q2)

With input voltage set to 5V and 25A lout results in the waveform shown in Figure 12

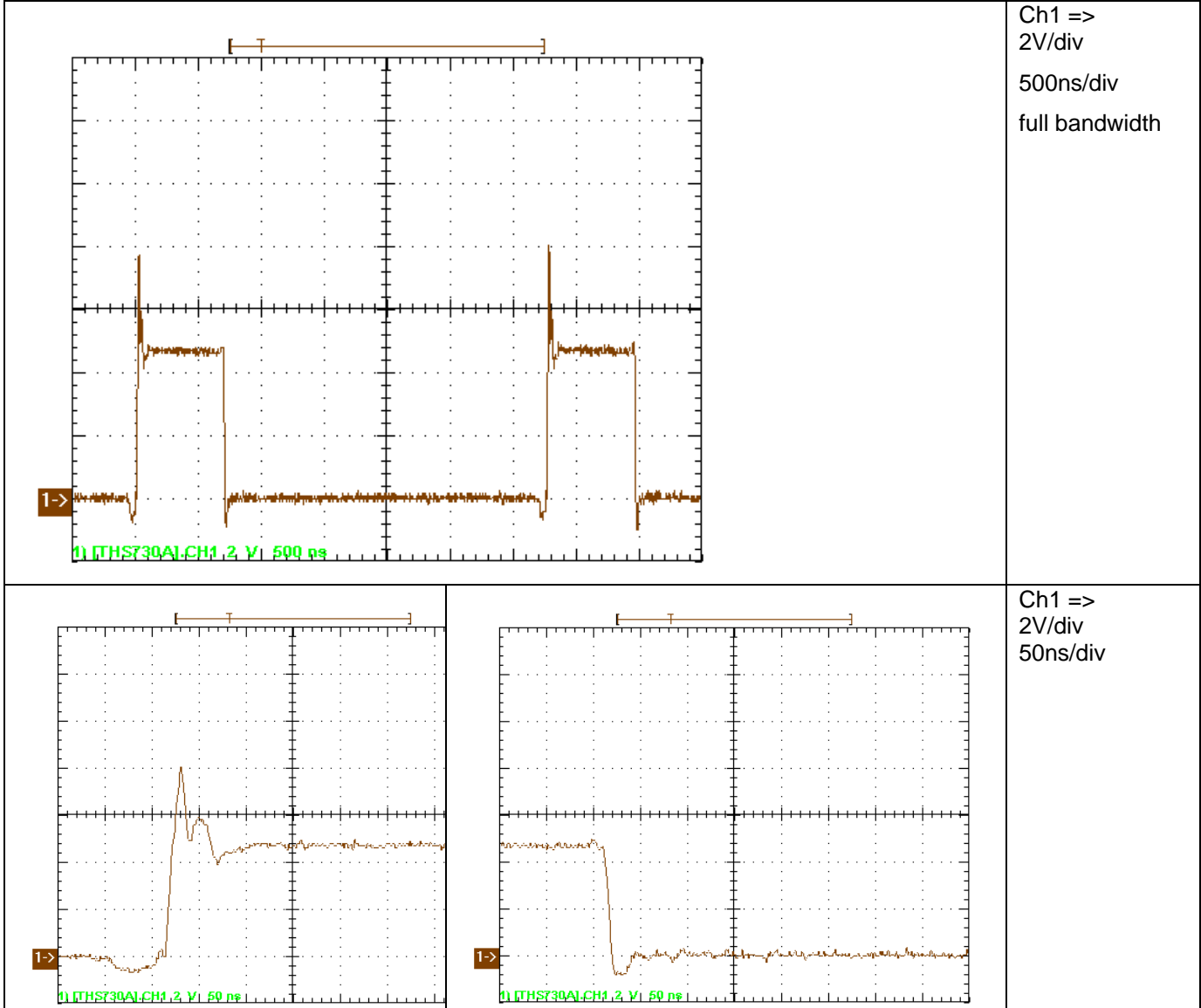


Figure 12

8.2 Switchnode (Q3)

With input voltage set to 5V and 25A lout results in the waveform shown in Figure 12

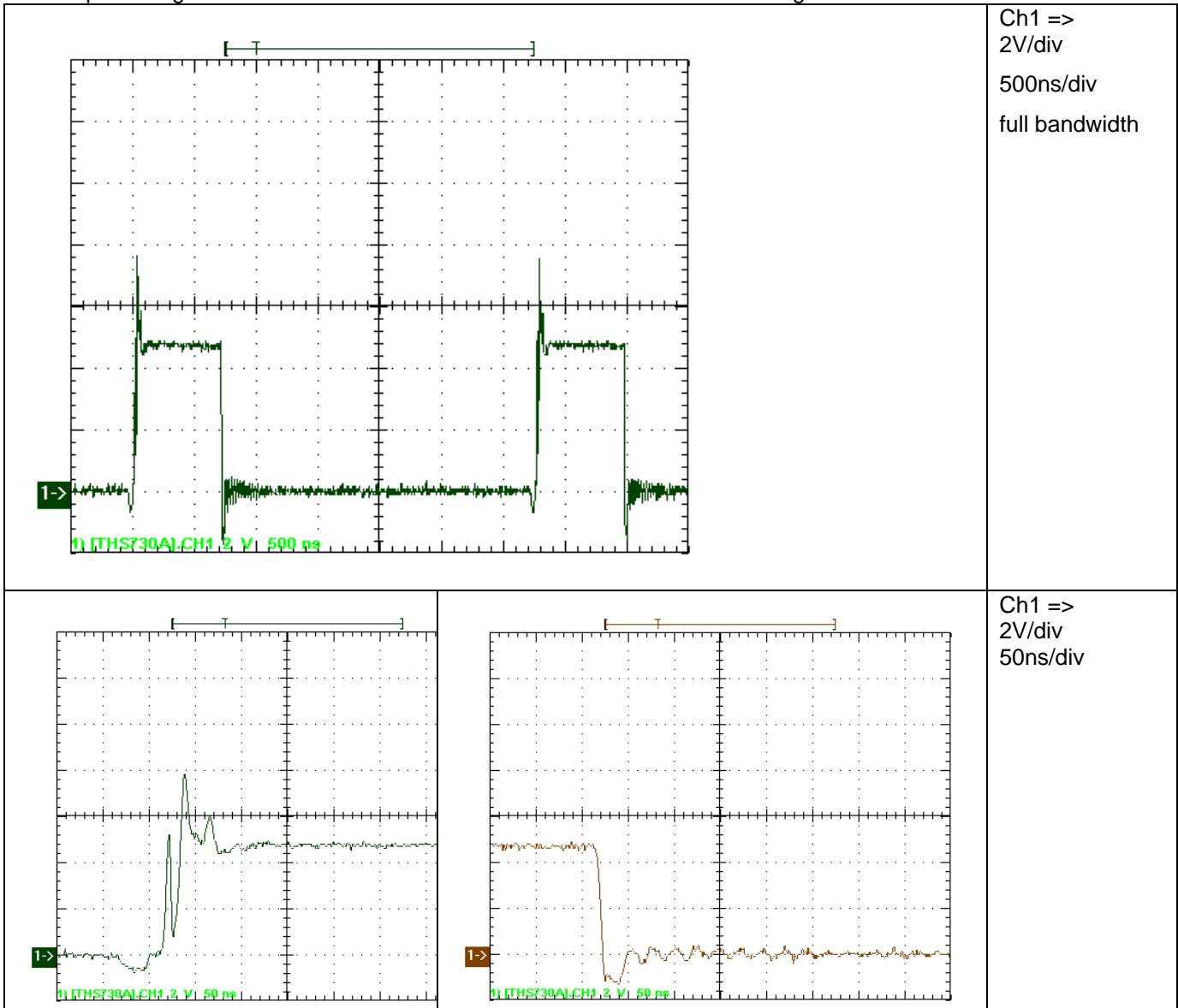


Figure 13

8.3 Low Side FET Gate (Q2) to GND

With input voltage set to 5V and 25A Iout results in the waveform shown in Figure 14

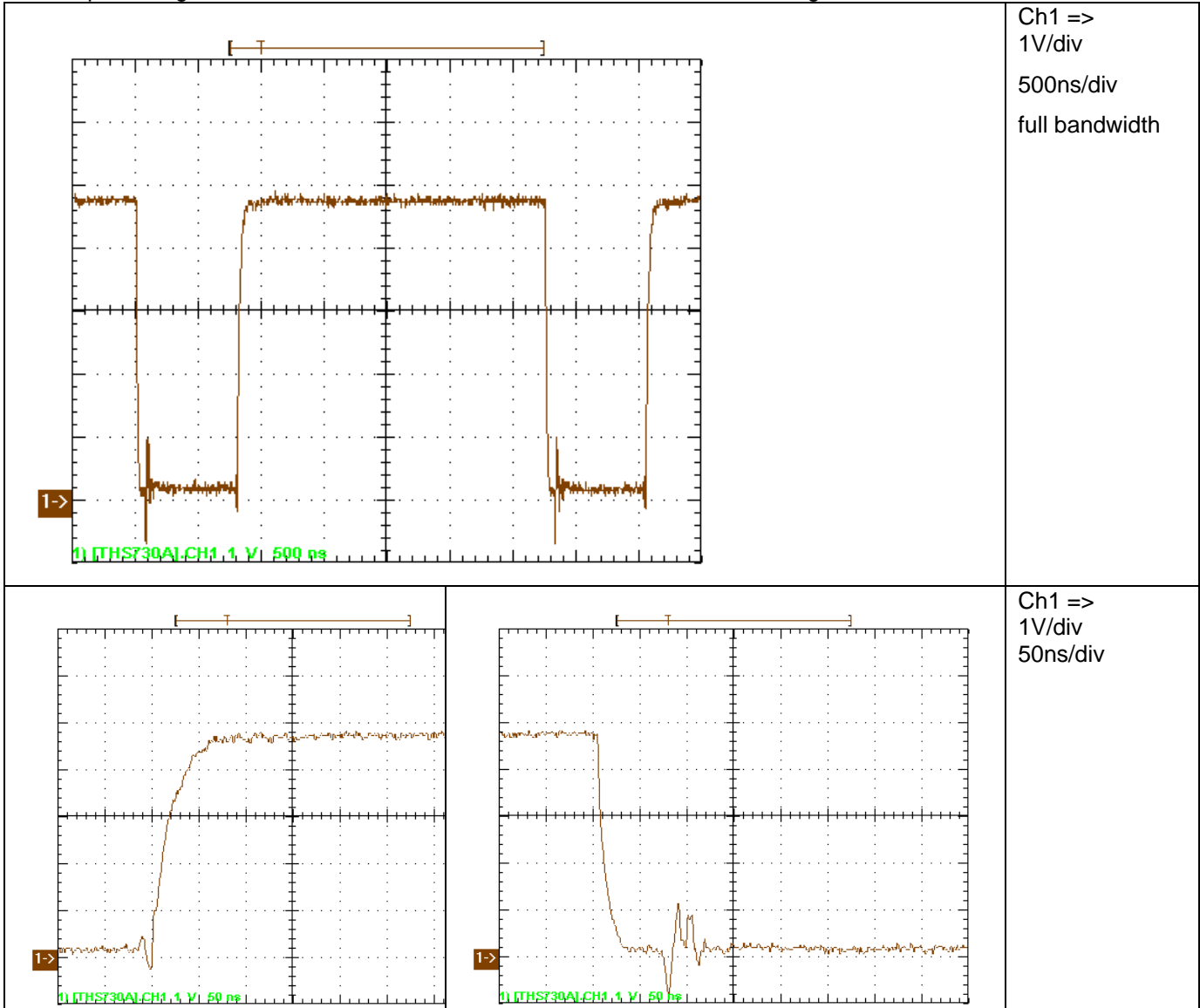


Figure 14

8.4 Low Side FET Gate (Q3) to GND

With input voltage set to 5V and 25A Iout results in the waveform shown in Figure 14

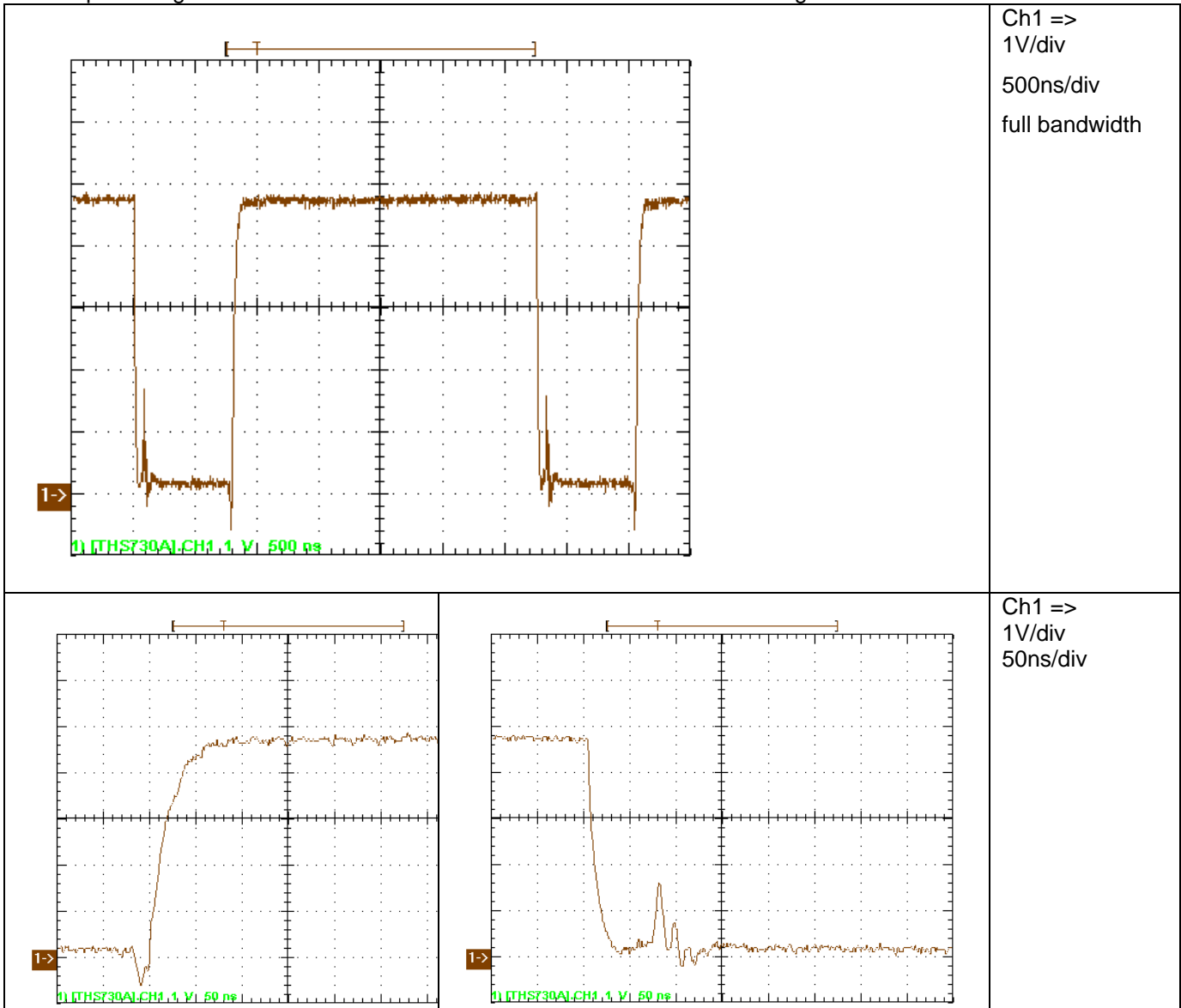


Figure 15

8.5 Hi Side FET Drain to switch node (Q1)

With input voltage set to 5V and 25A lout results in the waveform shown in Figure 16

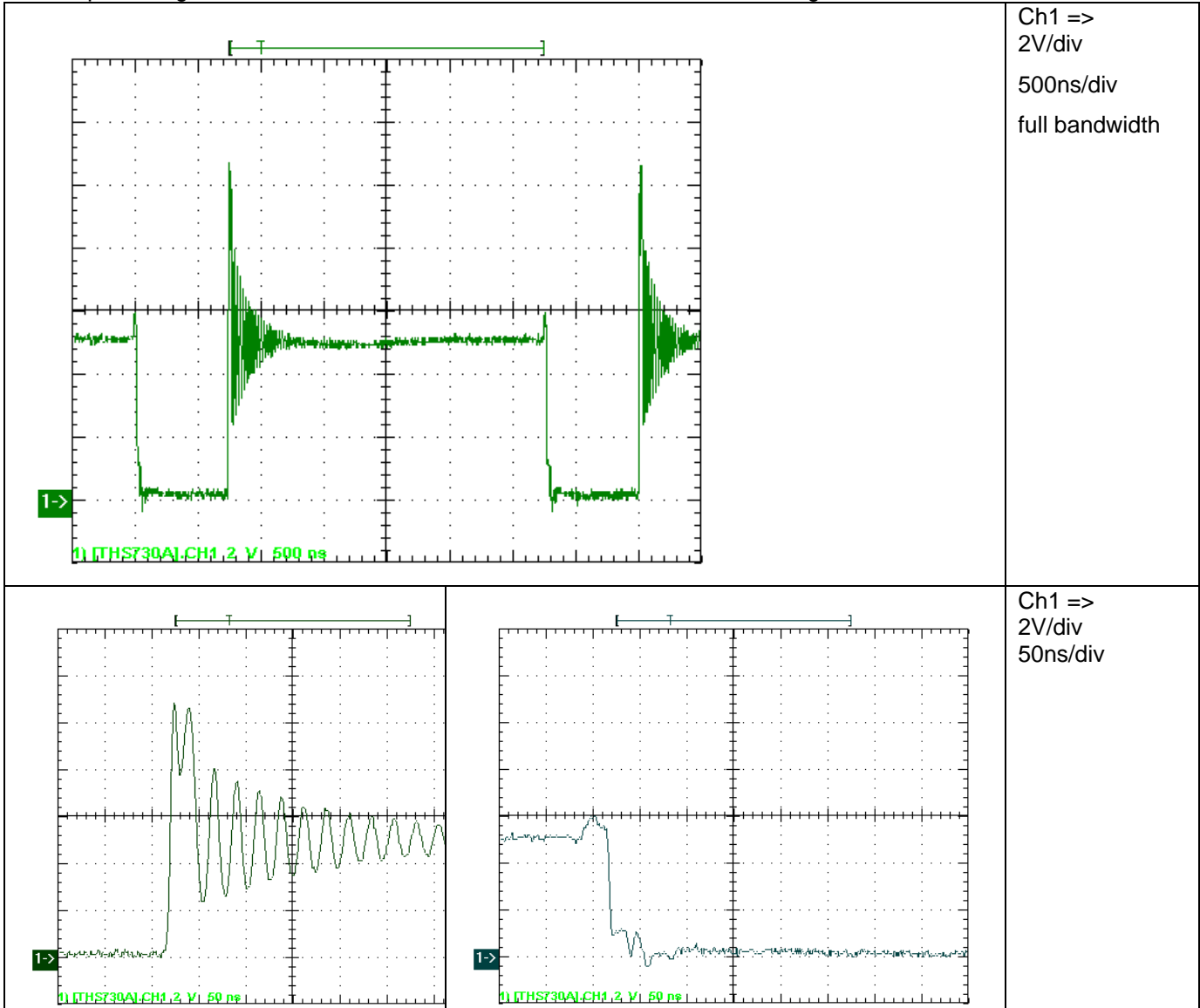


Figure 16

8.6 Hi Side FET Gate to switchnode

With input voltage set to 5V and 25A lout results in the waveform shown in Figure 17

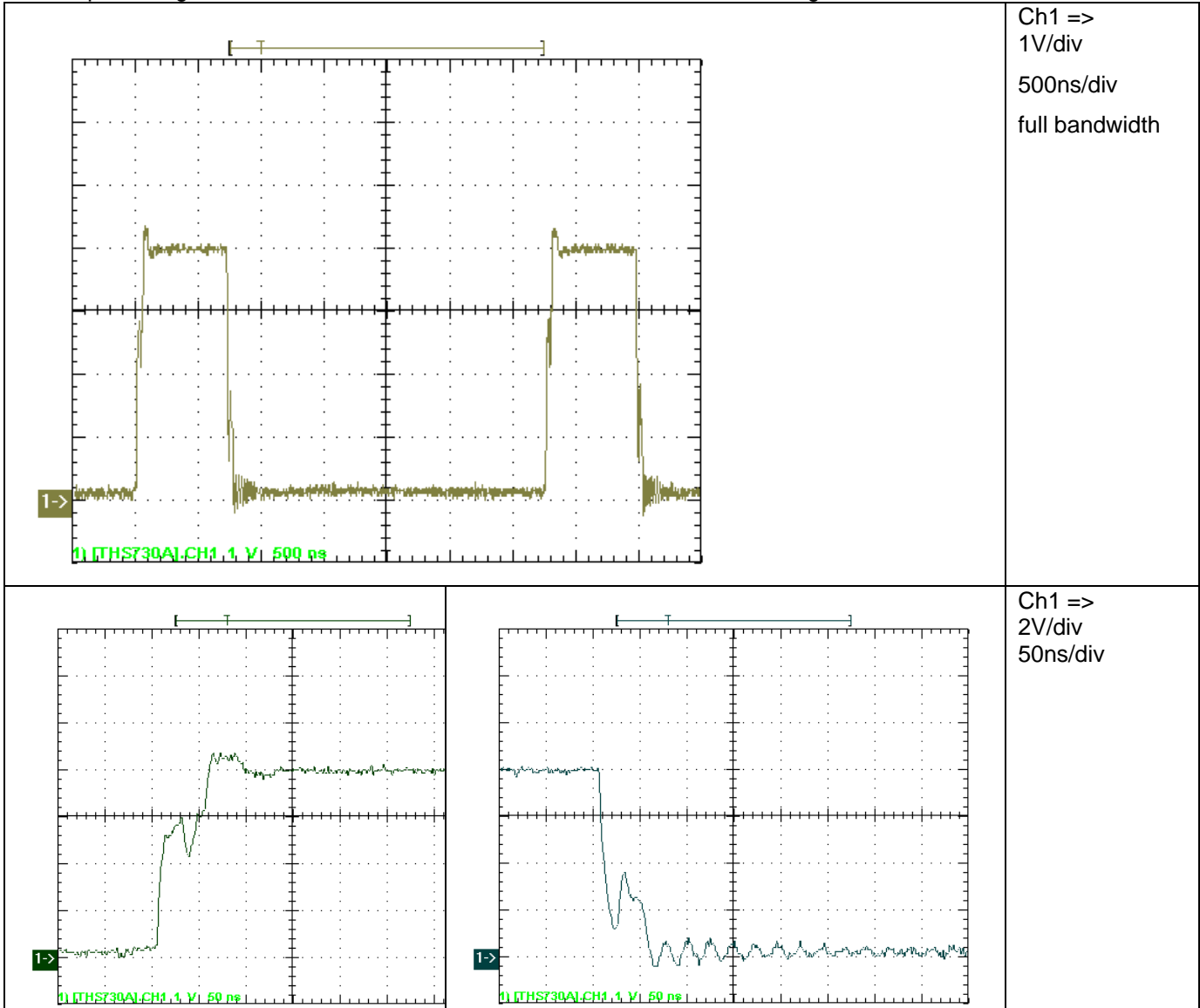


Figure 17

9 Thermal Image

Figure 18 shows the thermal image of the circuit at 30A.

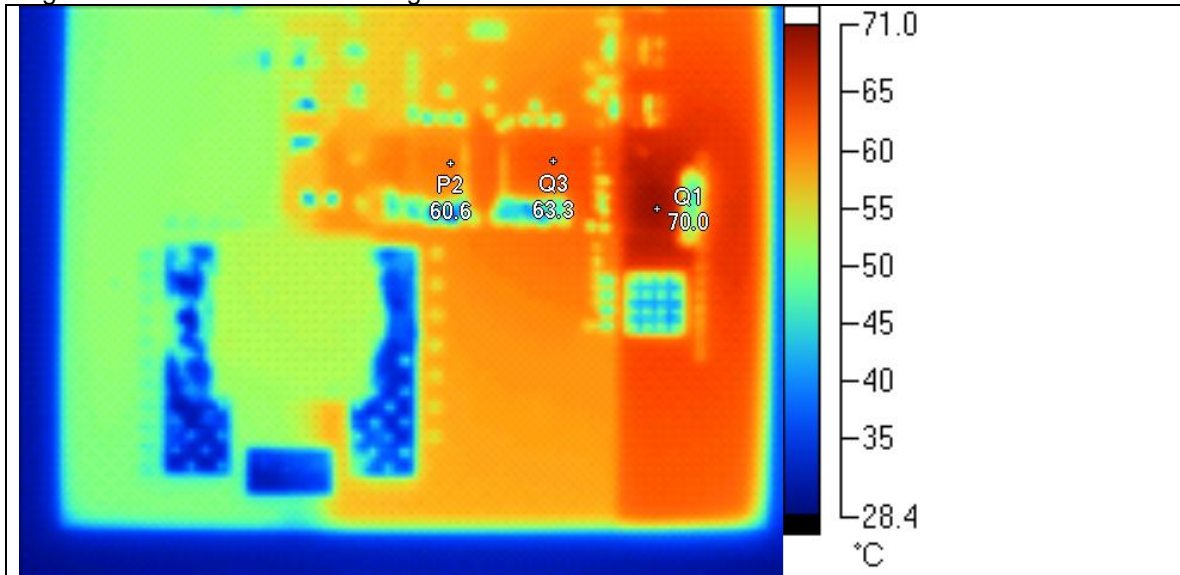


Figure 18

Name	Temperature
Q1	70.0°C
Q3	63.3°C
Q2	60.6°C

Table 2

PMP7208RevB1 (16325) Test Results

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