

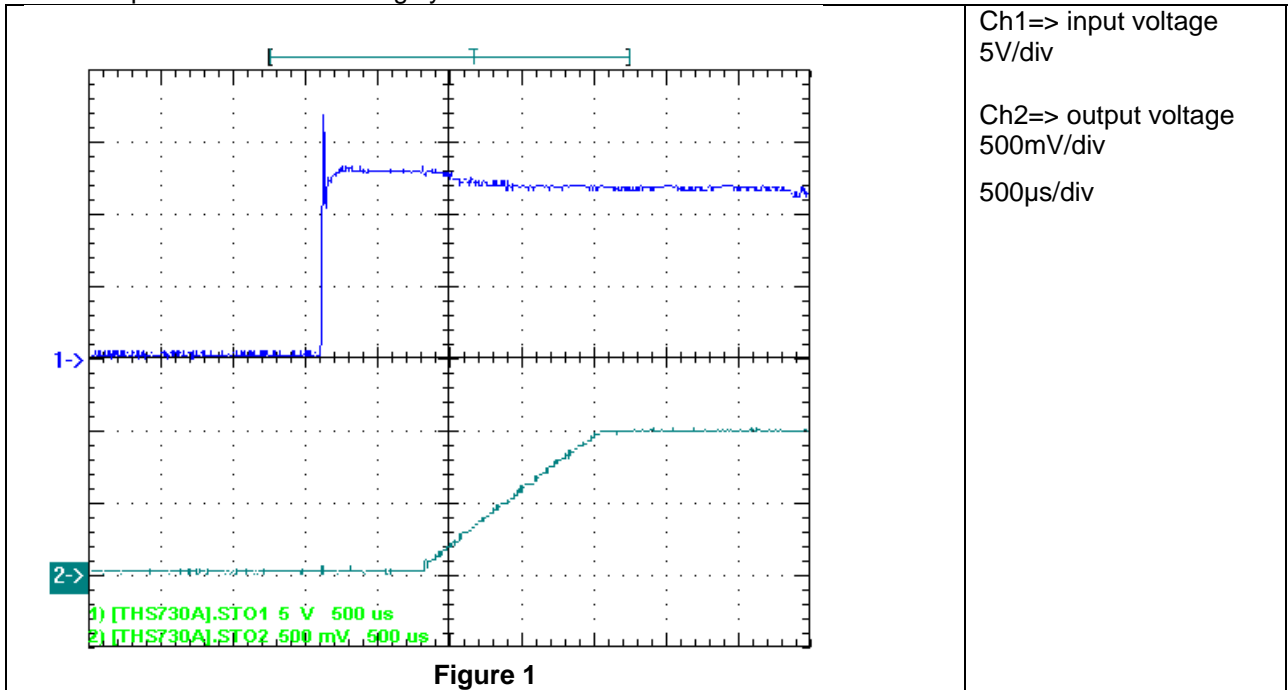
PMP8670RevA2 Test Results

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Topology: Sync Buck
Device: TPS53014, HS CSD17327Q5A, LS CSD17301Q5A

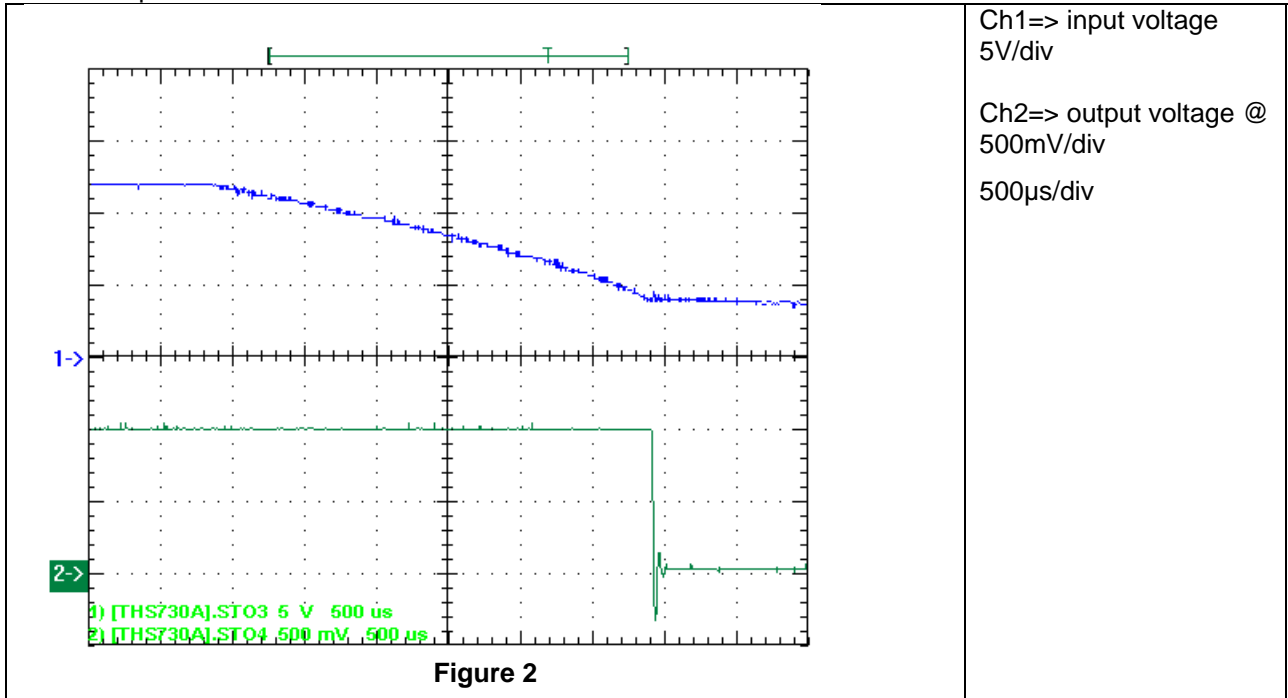
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 12V, with 12A load at the output. Soft start time roughly 1ms:



2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 48V, with 8A load on the output.



3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 12V

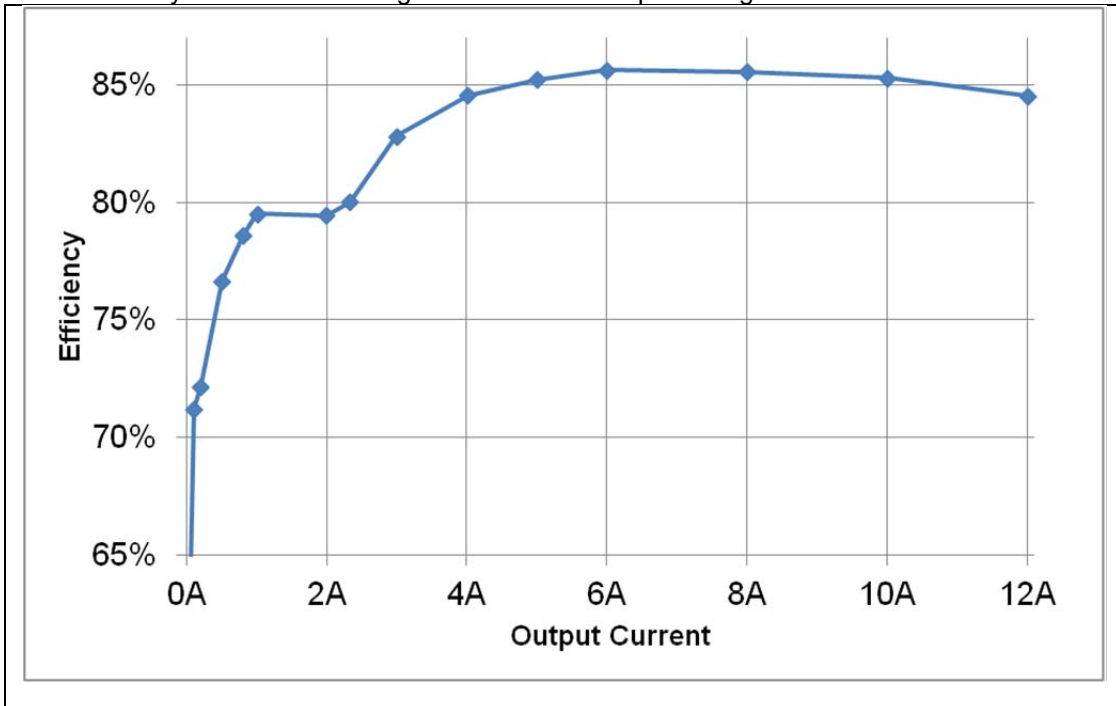


Figure 3

4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The input voltage was set to 12V.

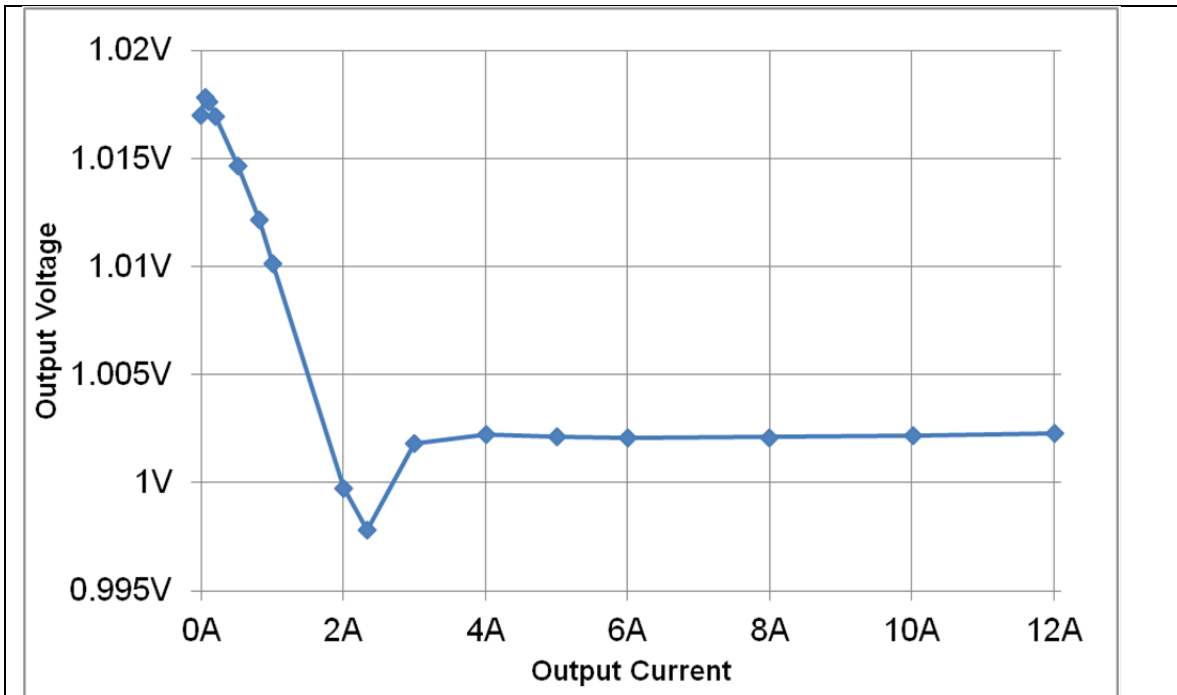
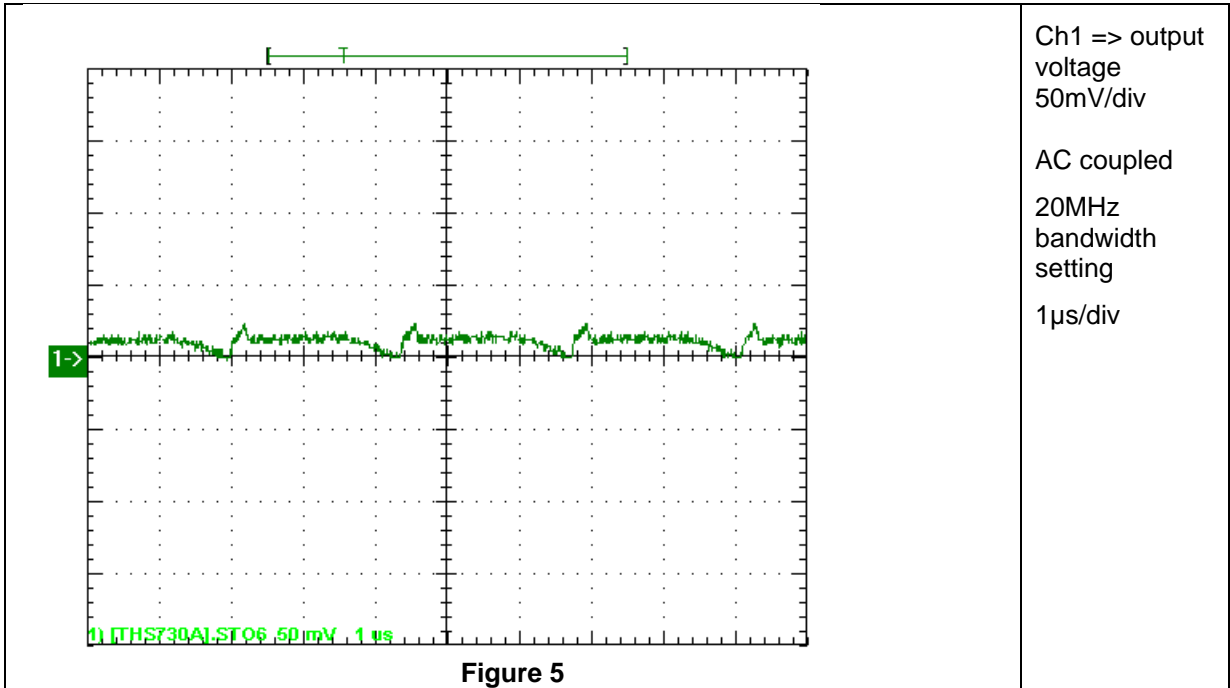


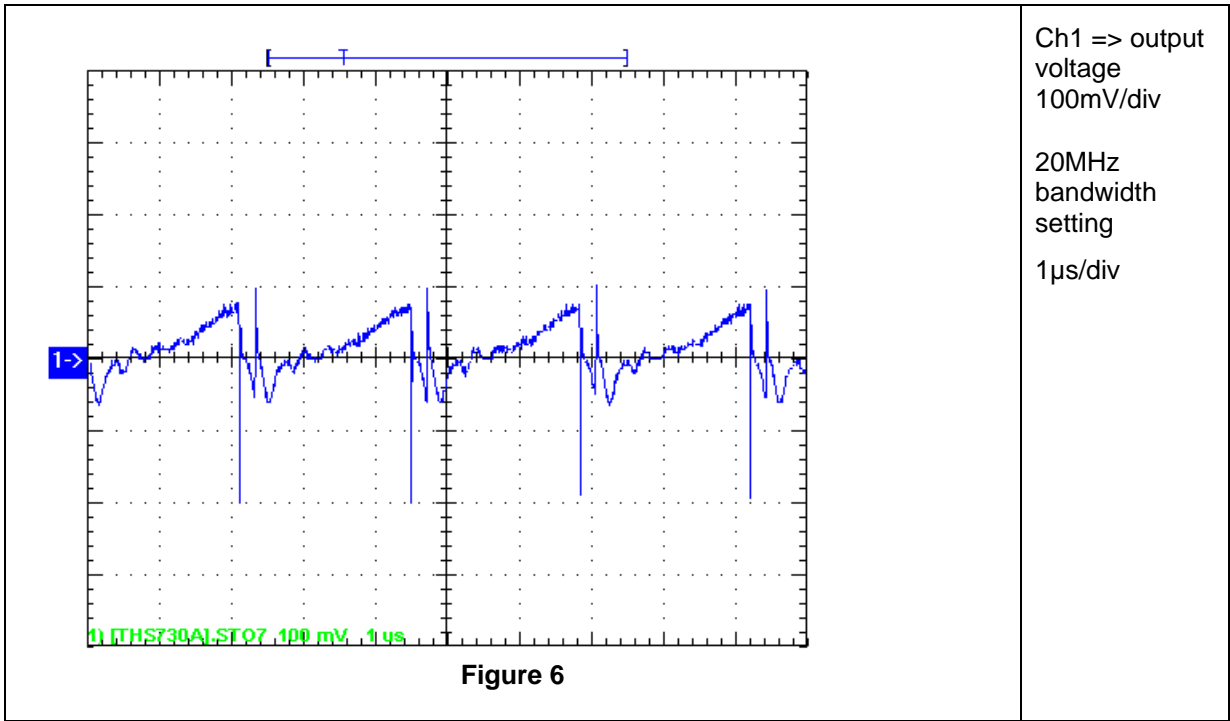
Figure 4

5 Ripple Voltage

The output ripple voltage is shown in Figure 5. The image was taken with a 12A load 12V at the input.



The input ripple voltage is shown in Figure 6. The image was taken with a 12 A load 12V at the input.



6 Load Transients

The

Figure 7 shows the response to load transients. The load is switching from 2A to 12A with 400Hz frequency. The input voltage was set to 12V; DCAP2 shows no response on 10A transients:

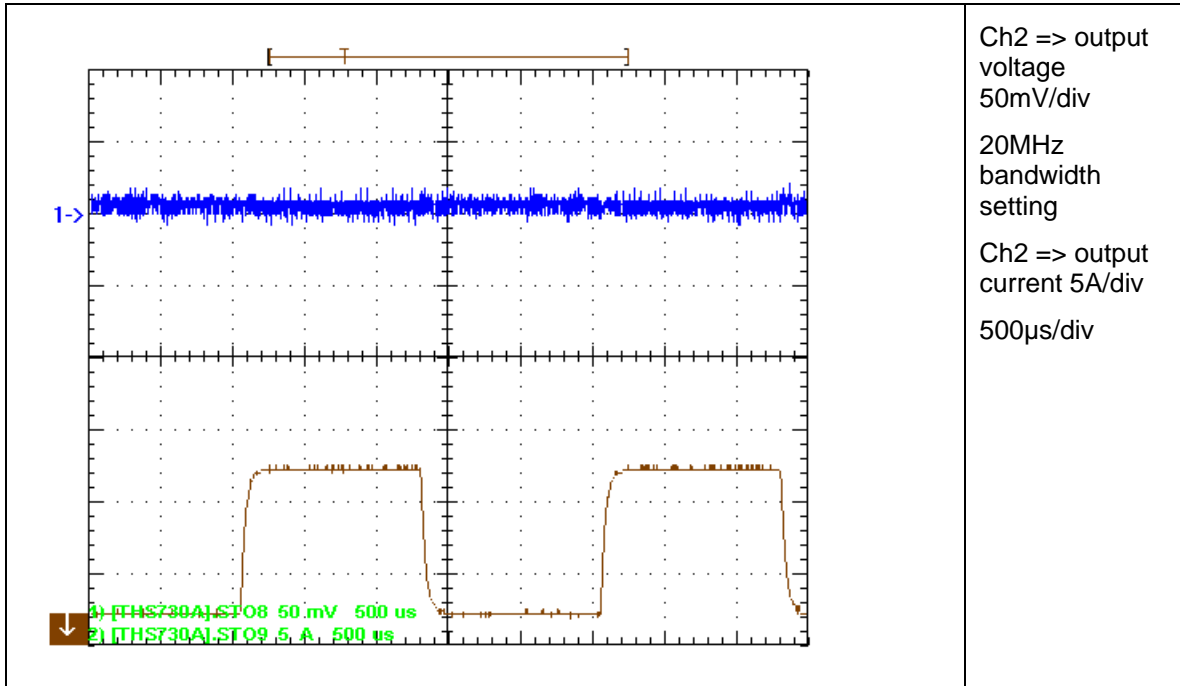


Figure 7

7 Miscellaneous Waveforms

7.1 Switch node (Low Side FET)

With input voltage set to 12V and 12A I_{out} results in the waveform shown in Figure 8, RC snubber and bootstrap resistor was implemented to reduce overshoot and ringing:

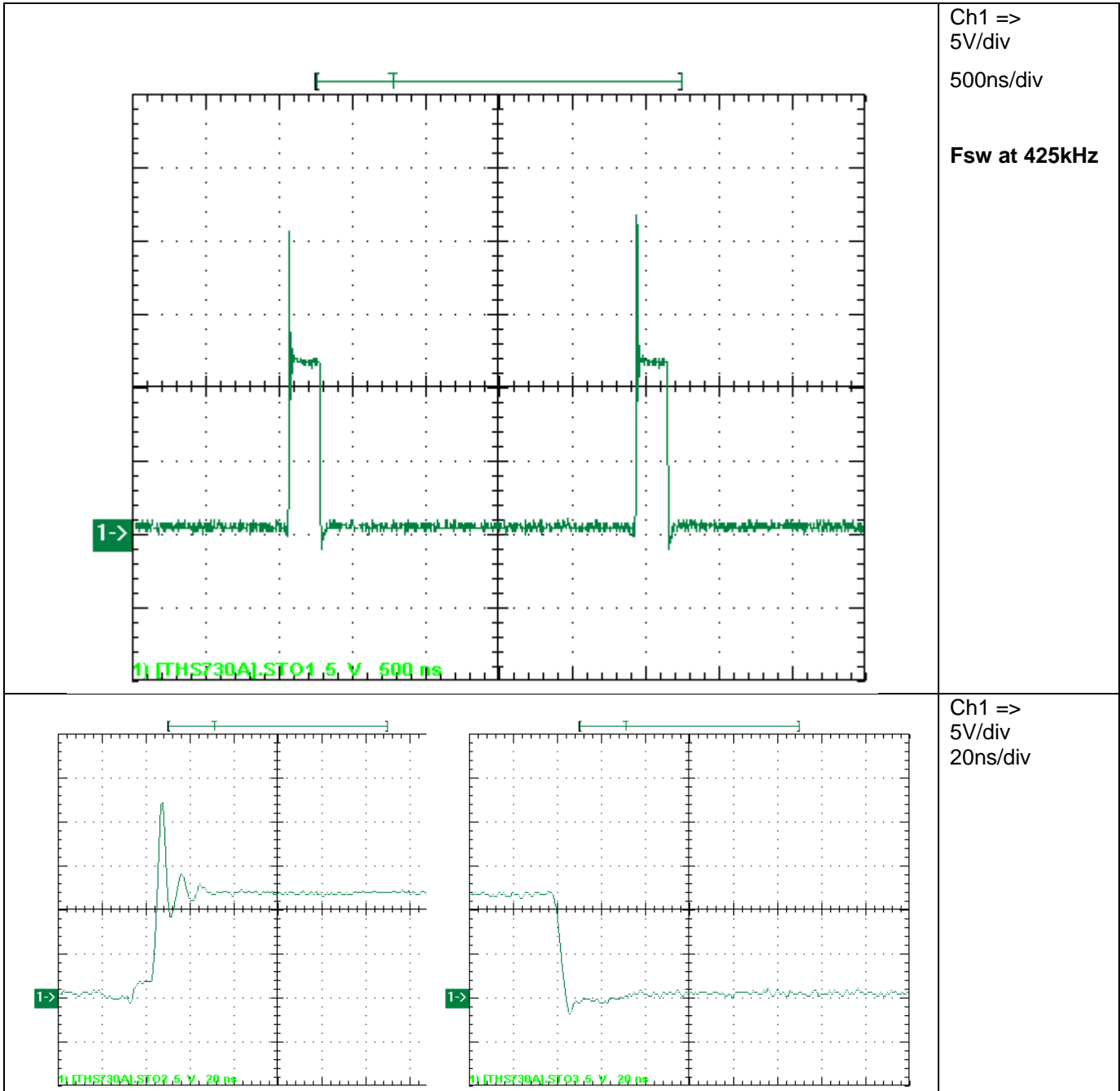


Figure 8

7.2 Gate of Low side MOS-FET

With input voltage set to 12V and 12A lout results in the waveform shown in Figure 8.

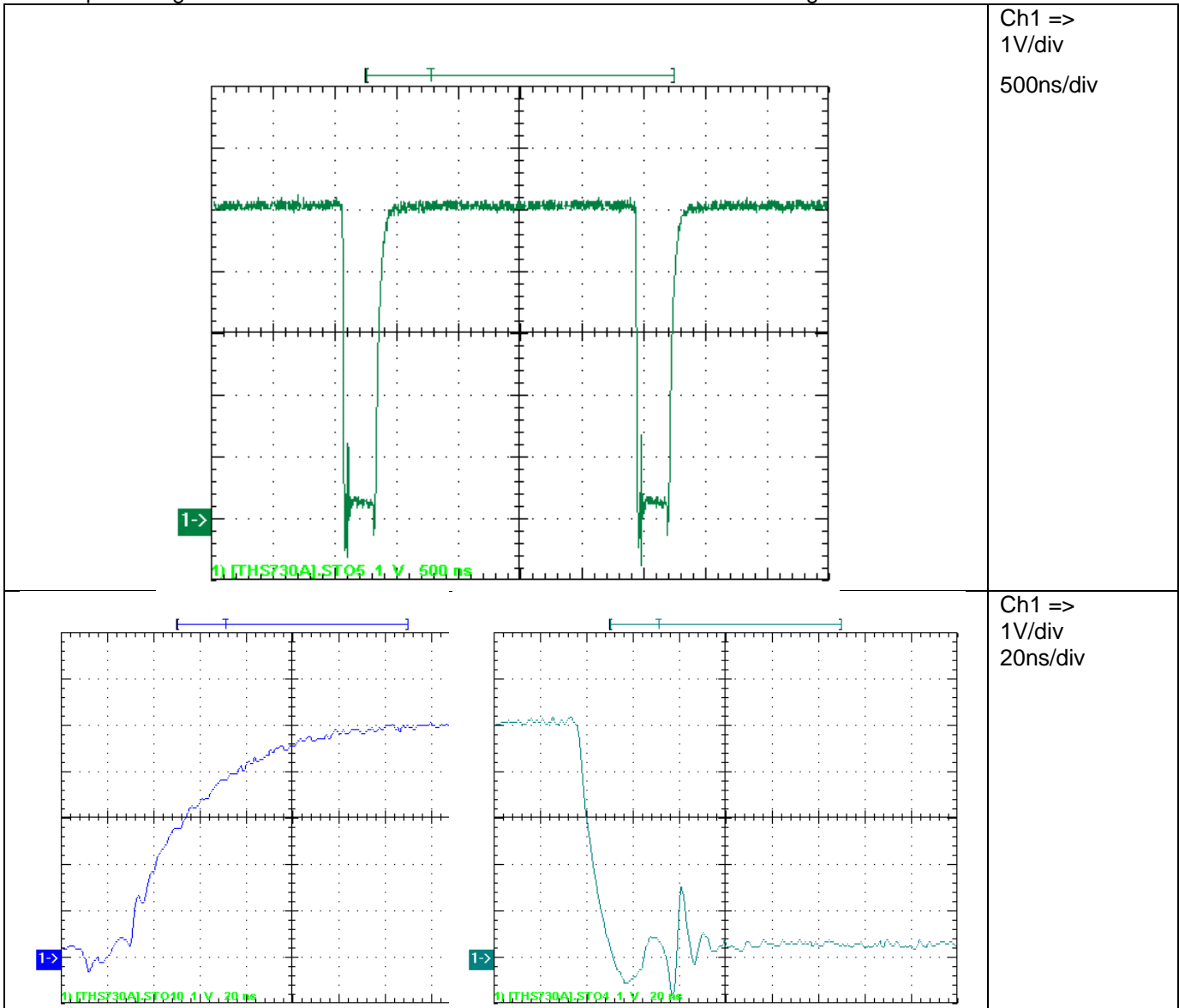


Figure 9

7.3 Hi Side MOS FET

The waveform is shown in **Figure 10**.(the same setup as above)

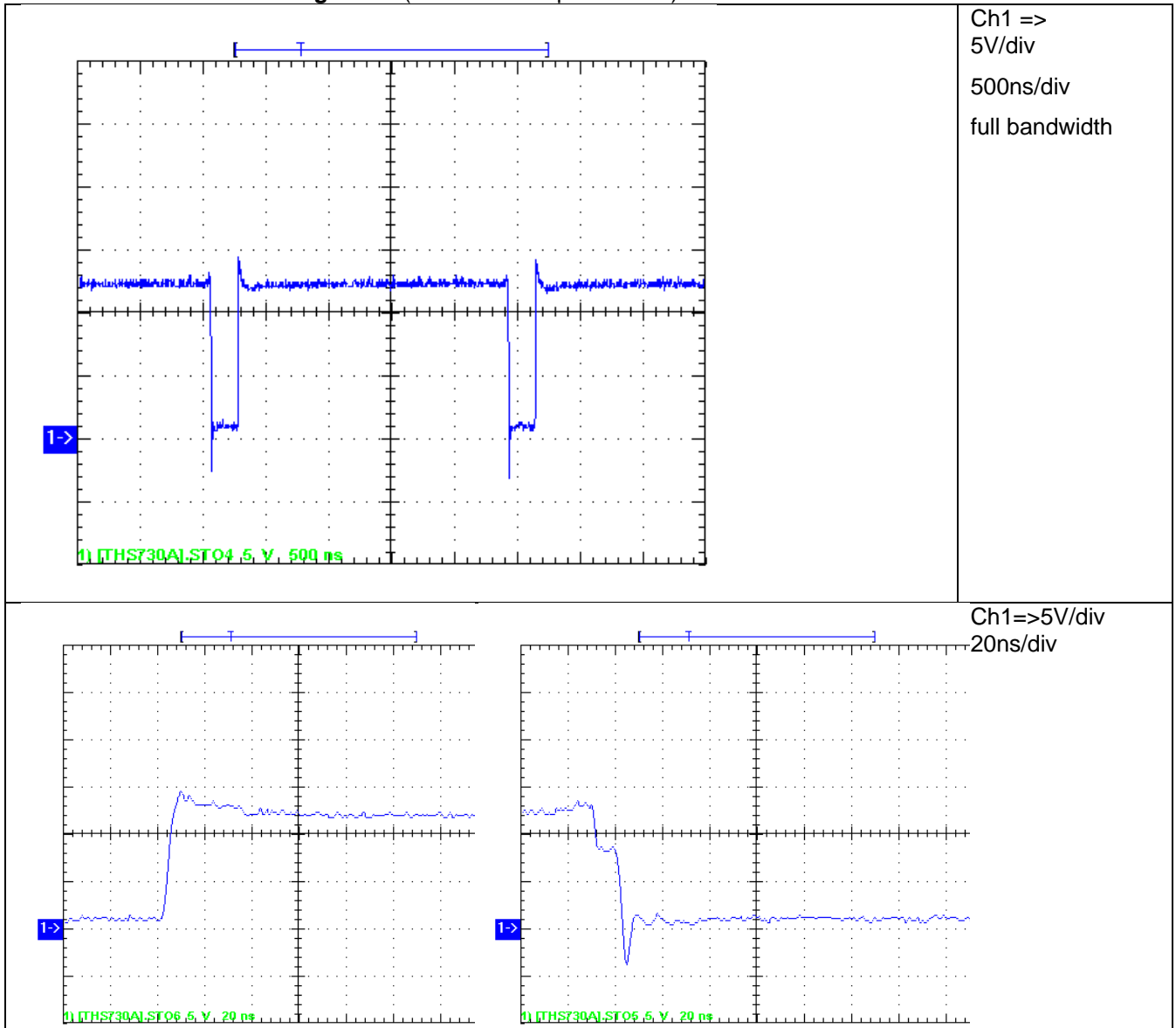


Figure 10

7.4 Hi Side MOS FET Gate

The waveform of gate is shown in Figure 11. BootR=0; GateR=10Ohms

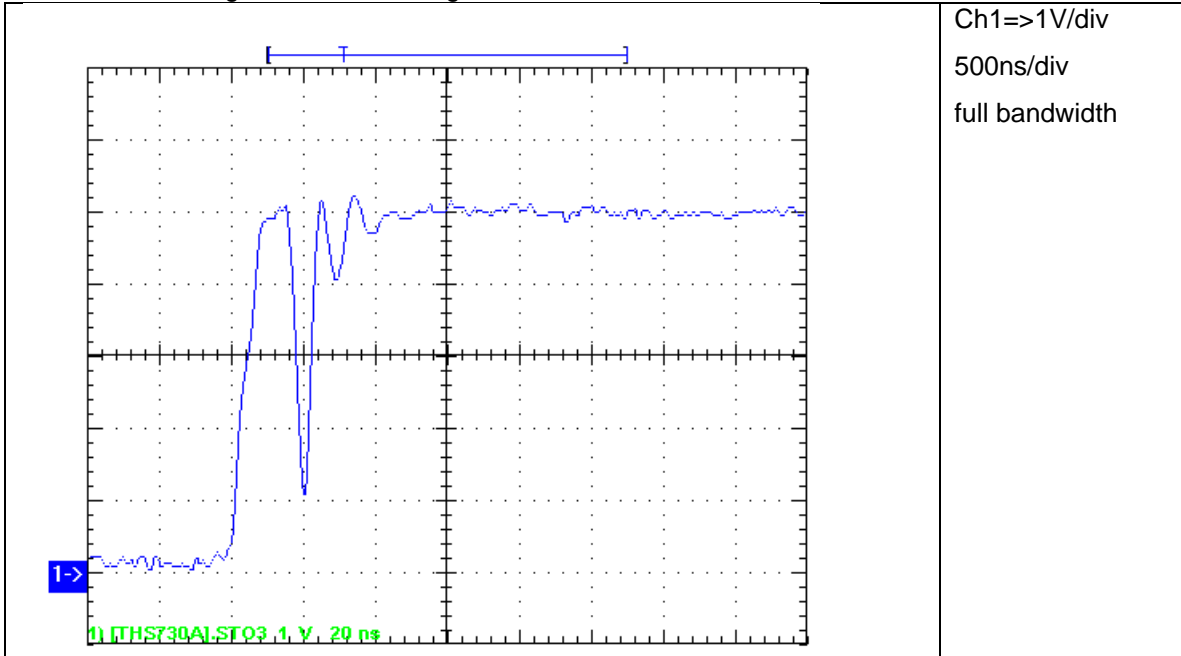


Figure 11

The waveform of gate is shown in Figure 12. BootR=3R3; GateR=10Ohms

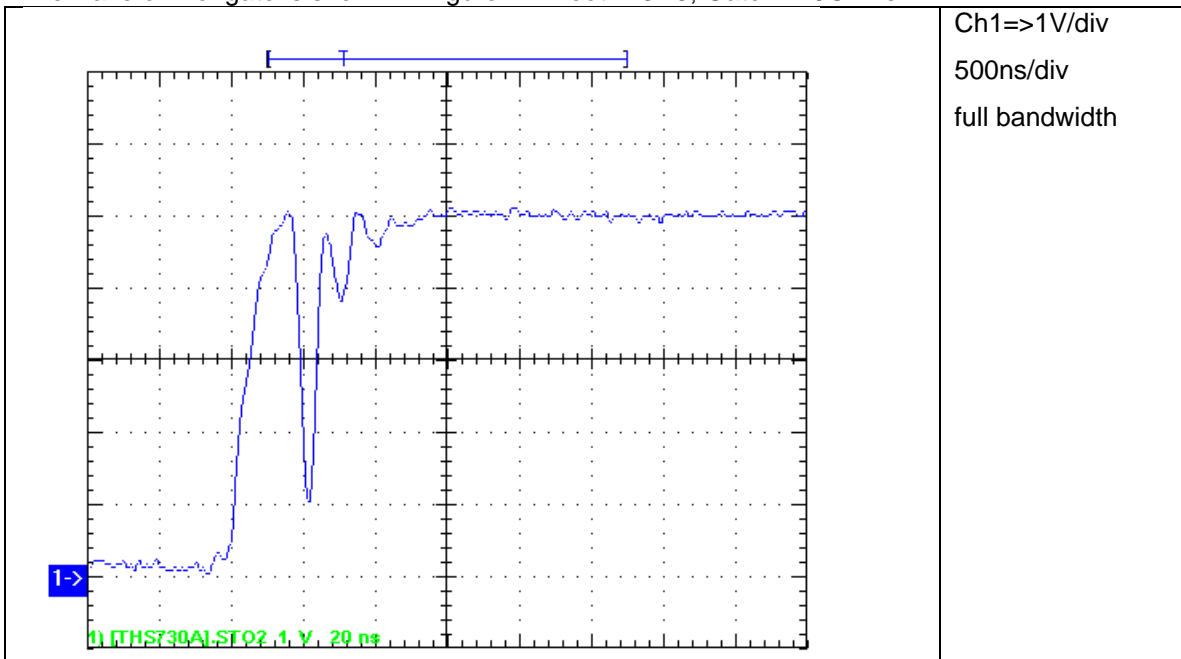


Figure 12

The waveform of gate is shown in Figure 13. BootR=3R3; GateR=10Ohms

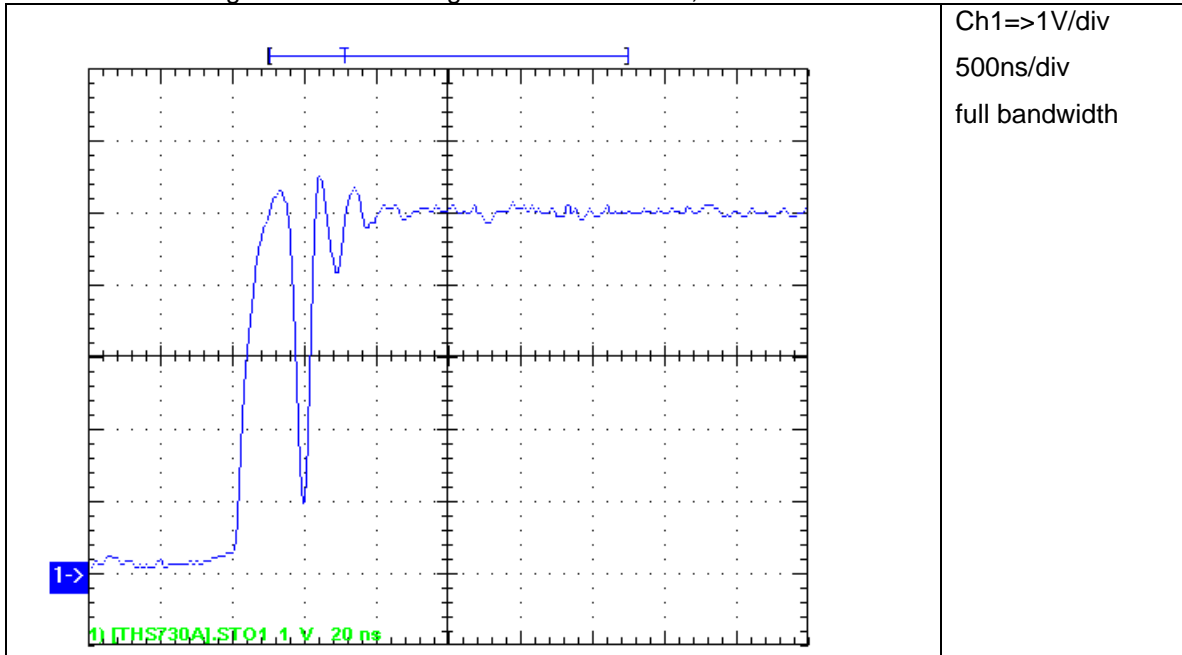


Figure 13

The waveform of gate is shown in **Figure 14**. BootR=3R3; GateR=0Ohms

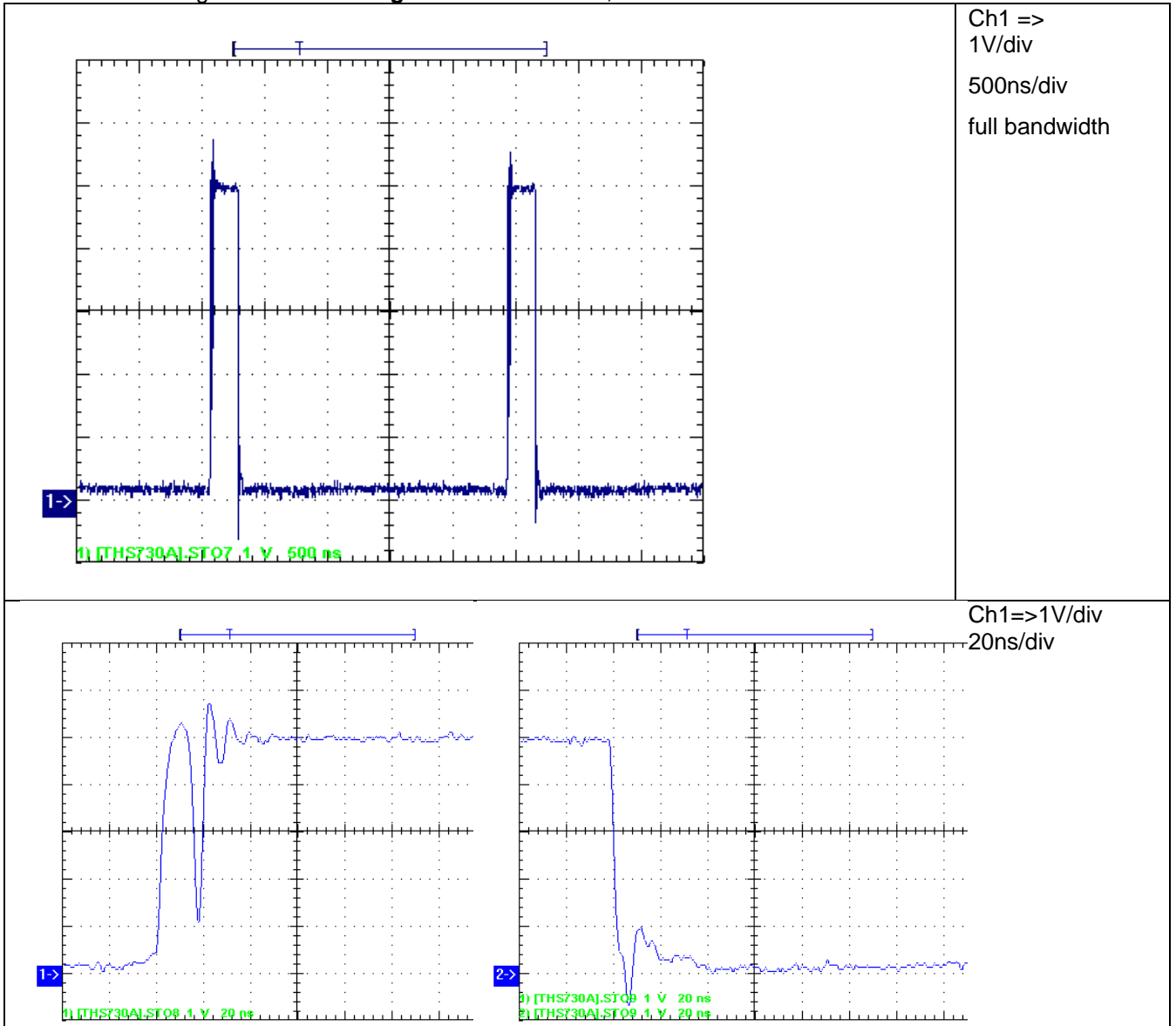


Figure 14

8 Thermal Image

Figure 15 shows the thermal image at 12V input and 12A output; design is thermally balanced, temperature rise at semiconductors is below 40K:

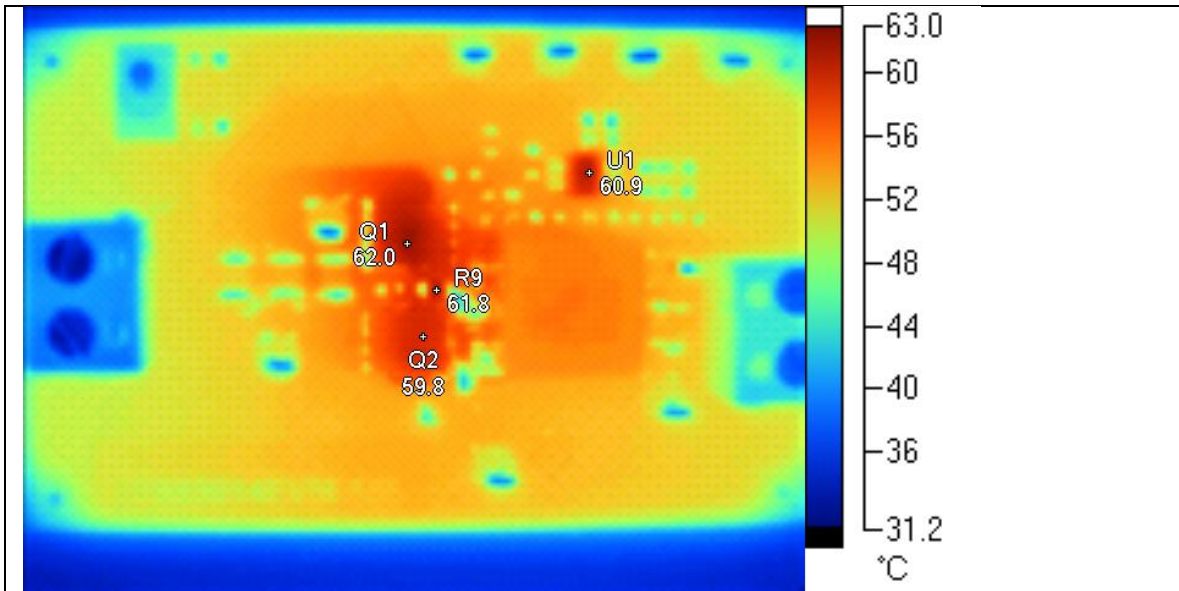


Figure 15

Name	Temperature
Q1	62.0°C
U1	60.9°C
R9	61.8°C
Q2	59.8°C

Table 1

PMP8670RevA2 Test Results

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