

Xilinx Virtex UltraScale FPGA Power Solution (PMP9475)



System Description

The PMP9475 reference design provides all the power supply rails necessary to power Xilinx's Virtex UltraScale family of FPGAs. It features a UCD90120A for flexible power up and power down sequencing as well as voltage monitoring, current monitoring, and voltage margining through the PMBus interface. This design uses a 12V input.

Featured Applications

- FPGA

Design Resources

- Block Diagram and Schematic
- Test Data
- Gerber Files
- Design Files
- Bill of Materials

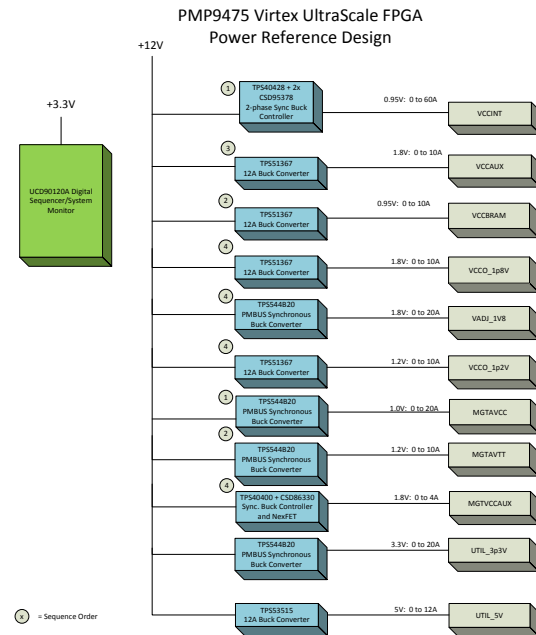
Design Features

- 12V Input Voltage
- Provides all the power supply rails needed to power a Xilinx Virtex UltraScale FPGA
- Power-up and power-down sequencing
- PMBUS compatible interface
- Low cost discrete IC design

Design Photo



Block Diagram



Jump start system design and speed time to market

Comprehensive designs include schematics or block diagrams, BOMs, design files and test reports by experts with deep system and product knowledge. Designs span TI's portfolio of analog, embedded processor and connectivity products and supports a board range of applications including industrial, automotive, medical, consumer, and more. To explore the designs, go to <http://www.ti.com/tidesigns>

Xilinx Virtex UltraScale FPGA Power Solution (PMP9475)



Associated Part Numbers

<u>Part Number</u>	<u>Part Description</u>
TPS40428	Stackable PMBus synchronous buck converter with a driverless controller. It can be configured for dual output or 2-phase operation. Input voltage ranges from 5 to 12V and can support load current up to 120A.
CSD95378BQ5M	Synchronous buck NexFET smart power stage with TAO offset. Has a continuous operating current capability of 60A.
TPS51367	Synchronous buck converter based on DCAP-2 control topology. Input voltage ranges from 3 to 22V and has an output current of 12A.
TPS544B20	Non-isolated DC-DC SWIFT converter that is PMBus compatible and capable of high-frequency operation. Input voltage ranges from 4.5 to 18V and has an output current of 20A.
TPS40400	Synchronous buck controller that operates from a nominal 3 to 20V supply. It is an analog PWM controller that allows programming and monitoring via the PMBus interface.
CSD86330Q3D	Synchronous buck NexFET power block MOSFET pair designed for applications offering high current, efficiency, and frequency capability with a 5V gate drive.
TPS53515	Synchronous buck SWIFT converter. Input voltage ranges from 1.5 to 18V and has a continuous output current of 12A.
UCD90120A	12-rail PMBus/I2C addressable power-supply sequencer and monitor with ACPI support.
INA333	Low power, precision instrumentation amplifier with excellent accuracy.

Design Considerations:

The design goal is to provide a full solution to power a Xilinx Virtex UltraScale FPGA; including core, transceiver, auxiliary, and I/O power. The design must also provide power up and power down sequencing, voltage and current monitoring, and voltage margining through a PMBus interface.

Core Supply –

The core supply required 0.95V at 60A. The TPS40428 two phase driverless controller was used with 2xCSD95378 NexFET smart power stages. A 2 phase design was used to reduce the output voltage ripple and keep the power dissipation manageable without an external heat sink. A PMBus interface allowed telemetry functions such as voltage and current reporting as well as flexibility with voltage margining.



Jump start system design and speed time to market

Comprehensive designs include schematics or block diagrams, BOMs, design files and test reports by experts with deep system and product knowledge. Designs span TI's portfolio of analog, embedded processor and connectivity products and supports a board range of applications including industrial, automotive, medical, consumer, and more. To explore the designs, go to <http://www.ti.com/tidesigns>

Xilinx Virtex UltraScale FPGA Power Solution (PMP9475)



Transceiver Power Supplies –

The transceiver supplies were designed with low output noise in mind, limiting the voltage ripple to <10mV. MGTAVCC required 1.0V at 20A, MGTAVTT required 1.2V at 10A, and MGTVCCAUX required 1.8V at 4A. TPS544B20 was chosen for MGTAVCC and MGTAVTT since it's a 20A integrated MOSFET step down converter with internal current sense. This eliminated the need to use an external sense resistor to monitor current which in turn reduces loss since the resistor is not there to dissipate extra power. TPS40400 controller along with a CSD86330 MOSFET was chosen for MGTVCCAUX since it provides all the necessary PMBUS telemetry and can meet all the necessary specifications along with providing a lower cost. An external sense resistor is still needed with this option but since it's only running 4A, the losses are much smaller than the other two rails.

I/O Power Supplies –

A combination of TPS544B20, TPS51367, and TPS53315 were used to provide the remaining power supply rails for this system. These ICs feature integrated MOSFETs and require minimal external components. These power supply rails were designed to keep output ripple at a minimum and DC & AC errors <3%.

Telemetry, Sequencing, and Margining –

A UCD90120A system health monitor is used to provide flexible power up and down sequencing, voltage monitoring, current reporting, and voltage margining for the entire set of power supply rails. This device is interfaced through PMBus to TI's Digital Fusion GUI to allow for easy configuration.



Jump start system design and speed time to market

Comprehensive designs include schematics or block diagrams, BOMs, design files and test reports by experts with deep system and product knowledge. Designs span TI's portfolio of analog, embedded processor and connectivity products and supports a board range of applications including industrial, automotive, medical, consumer, and more. To explore the designs, go to <http://www.ti.com/tidesigns>

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.