PMP10051RevB Test Results

Topology: SEPIC
Device: TPS61175

Unless otherwise mentioned all measurements were done with 6.3V at the input and full load at each output applied.

Static measurements:

Switching frequency Fsw 360kHz;

Load resistors:

R1 = 68.20 Ohms
R2 = 13.99 kOhm
R3 = 68.17 Ohm
R4 = 12.08 kOhm

1 Startup

The startup waveform is shown in the Figure 1.

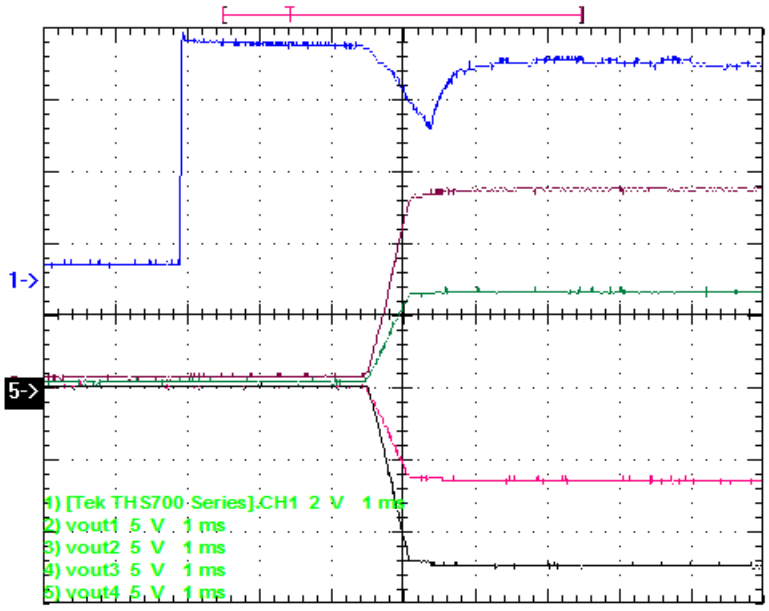


Figure 1

Ch1=> input voltage 2V/div

Ch2-5=> output voltage 5V/div (full

1ms/div

20MHz bw

2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 3V, with 1.2A load on the output. The power supply was disconnected**.**

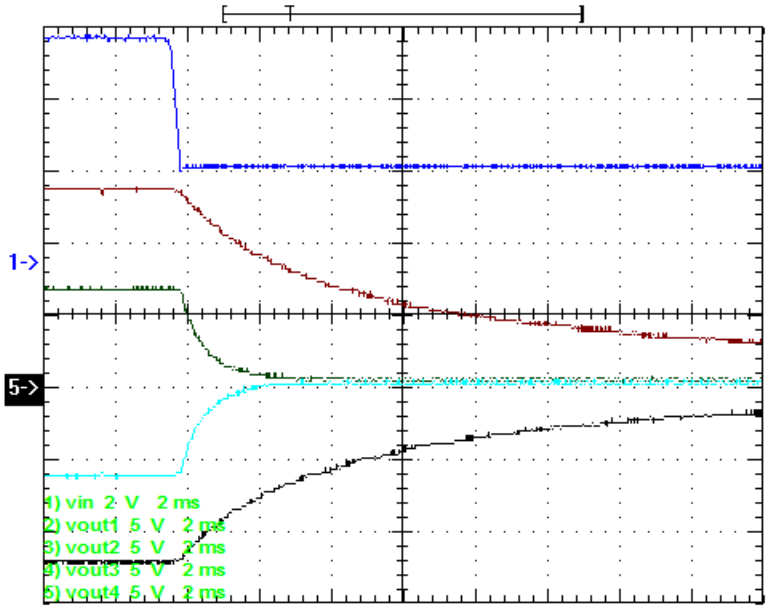


Figure 2

Ch1=> input voltage 2V/div

Ch2-5=> output voltage 5V/div (full load)

2ms/div

20MHz bw

3 Efficiency

The efficiencies are shown in the Table 1 below.

VIN	IIN	VOUT1	VOUT2	VOUT3	VOUT4	Eff
3.01	0.4996	6.6702	13.509	6.5771	12.75	0.87
6.302	0.2354	6.6758	13.511	6.6263	12.72	**0.89**
13.21	0.1181	6.6772	13.503	6.6485	12.75	0.85

Table 1

results in converter power losses of 163mW at nominal input voltage 6.3V

4 Output Ripple Voltage

The output ripple voltage is shown in Figure 3, <1%

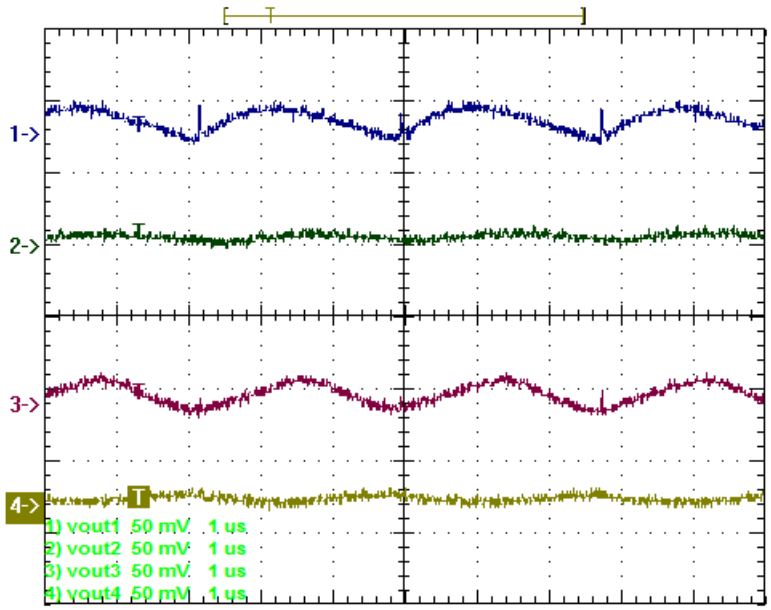


Figure 3

Ch1 => output voltage1

Ch2 => output voltage2

Ch3 => output voltage3

Ch4 => output voltage 4

50mV/div

AC coupled

20MHz bw

1µs/div

5 Input Ripple Voltage

The input ripple voltage is shown in Figure 4.

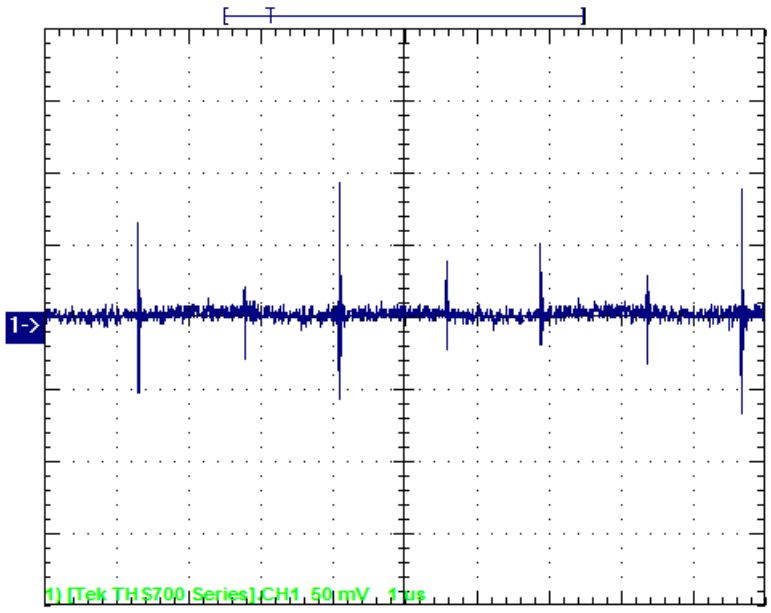


Figure 4

Ch1 => input voltage

50mV/div

AC coupled

full bw

1µs/div

6 Control Loop Frequency Response

Figure 5 shows the loop response. Full-load applied. The input voltage was set to 3V.

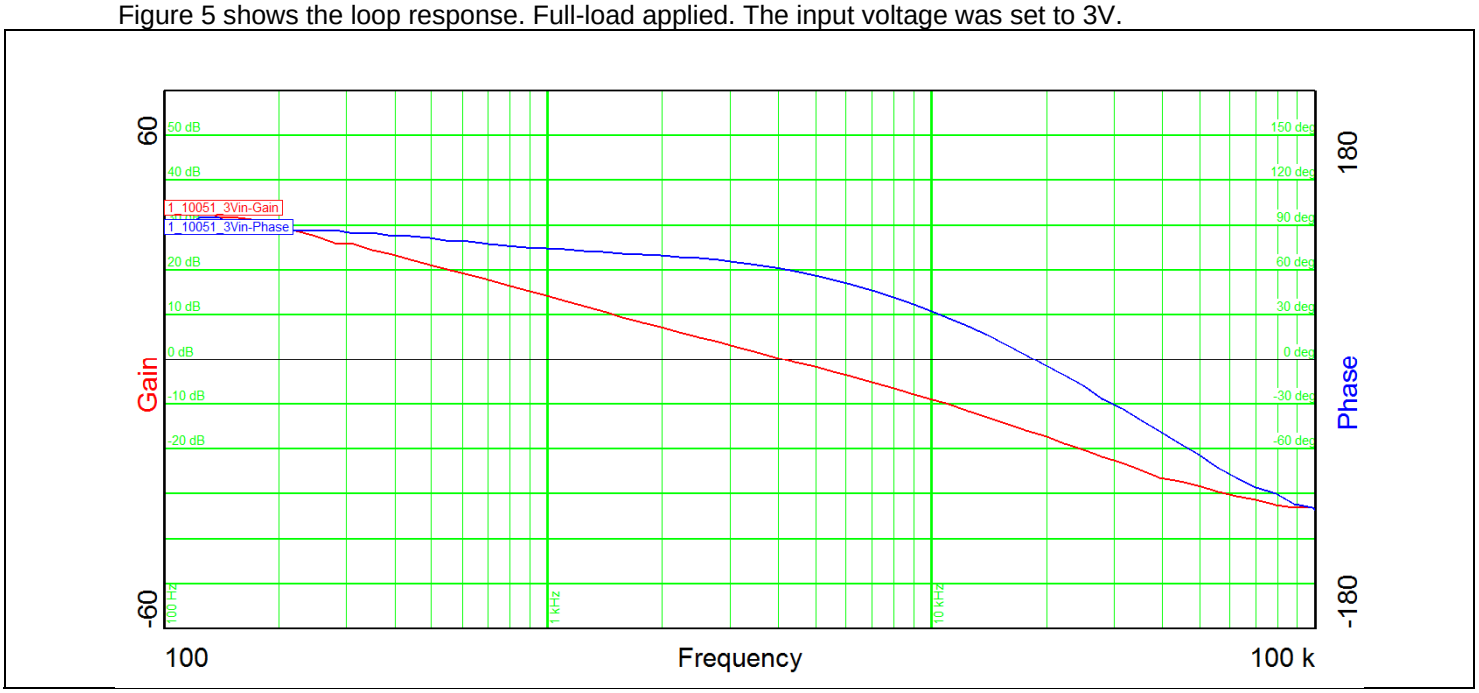


Figure 5

Figure 6 shows the loop response. Full-load applied. The input voltage was set to 6.3V.

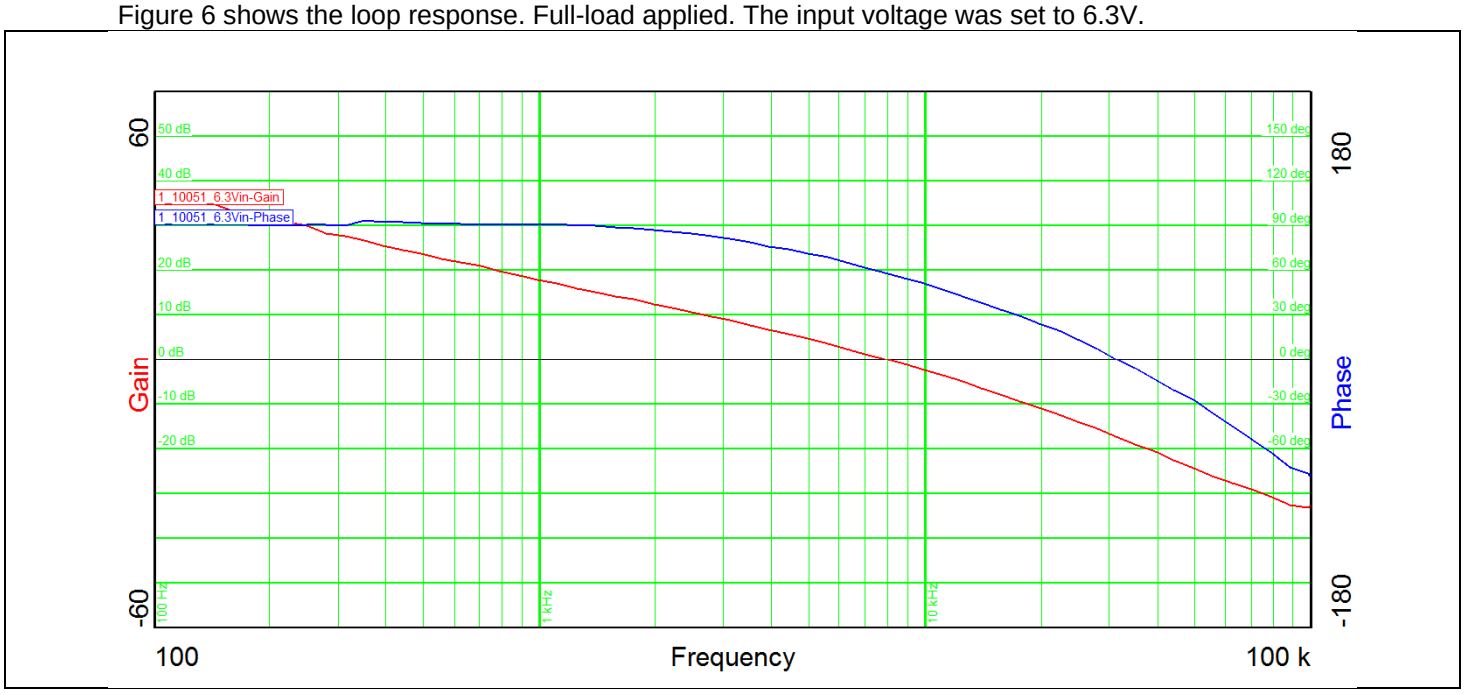


Figure 6

Figure 7 shows the loop response. Full-load applied. The input voltage was set to 13.2V.

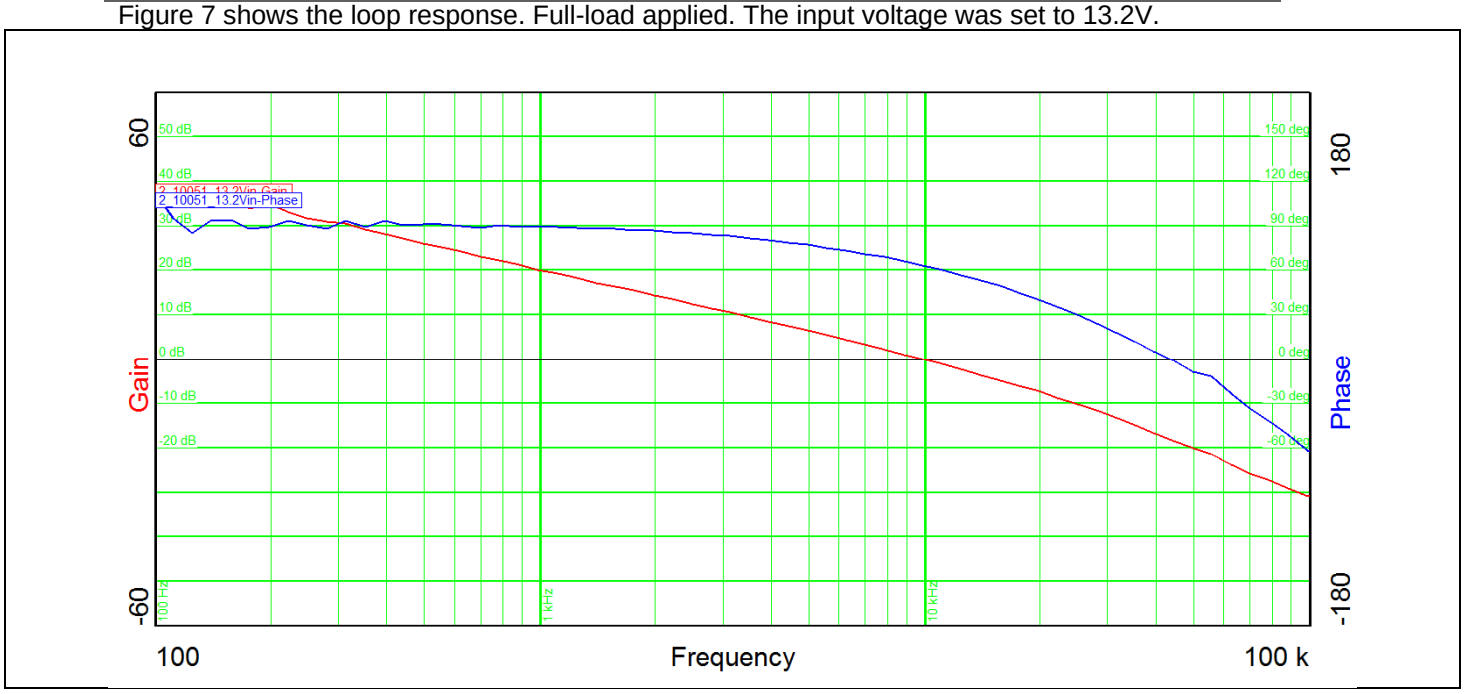


Figure 7

Table 1 summarizes the results from Figure 5 Figure 6 and Figure 7.

Vin	3V	6.3V	13.2V
Bandwidth (kHz)	4.158	7.96	9.93
Phase margin	60.1°	58.1°	63°
slope (20dB/decade)	-1.1	-1.23	-1.16
gain margin (dB)	-16.5	-17.5	-18.1
slope (20dB/decade)	-1.43	-1.75	-1.77
freq (kHz)	18.6	31.6	43.5

Table 1

7 Output Voltages at different load conditions

The table below shows the voltage measurements at different load conditions. The fields which are filled with blue means full load is applied.

This is a **WORST CASE** analysis full load (jumper set = 1) / zero load (jumper off = 0):

Jmp11	Jmp21	Jmp31	Jmp41	U11	U21	-U31	-U41
0	0	0	0	**6.673**	**13.486**	**6.739**	**12.81**
0	0	0	1	6.6867	13.615	6.7985	6.023
0	0	1	0	6.6867	13.575	2.3	12.64
0	0	1	1	6.67	14.424	2.4	7.032
0	1	0	0	6.68	6.78	6.809	12.89
0	1	0	1	6.71	6.1	6.837	5.444
0	1	1	0	6.674	9.7	4.63	12.52
0	1	1	1	6.674	9.24	4.28	8.334
1	0	0	0	6.676	16.017	8.861	16.77
1	0	0	1	6.675	15.233	8.232	12.85
1	0	1	0	6.676	16.76	6.627	16.79
1	0	1	1	6.675	16.225	6.626	12.73
1	1	0	0	6.674	13.513	8.855	16.04
1	1	0	1	6.674	13.509	8.855	12.84
1	1	1	0	6.674	13.508	6.625	16.16
1	1	1	1	**6.674**	**13.503**	**6.625**	**12.72**

Due to the peak detection of the flyback rectifier this multi output sepic will NOT work properly if an output is NOT loaded. The deviation itself depends on coupling of the transformer and load scenario. **See the load scenario approx. 33mA / 67mA / 100mA at V1 and –V3**;
V2 and V4 loaded w/ 1mA; to avoid zero load condition each output could be preloaded w/ a small bias resistor:

Load 11	**Load 31**	**V11 (+6V7)**	**V21 (+14V)**	**V31 (-6V7)**	**V41 (-12V)**	**Vin (V)**	**Iin (mA)**	**Effcy (%)**
1/3	1/3	6.675	**13.414**	-6.648	-12.565	6.296	84.3	86.6%
1/3	2/3	6.677	13.417	-6.608	-12.567	6.305	123.9	86.0%
1/3	3/3	6.676	13.415	**-6.573**	**-12.556**	6.310	159.1	87.4%
2/3	1/3	6.676	13.479	-6.687	-12.660	6.313	125.0	86.2%
2/3	2/3	6.676	13.484	-6.644	-12.650	6.311	161.7	87.6%
2/3	3/3	6.676	13.478	-6.606	-12.618	6.304	197.5	88.5%
3/3	1/3	6.676	**13.525**	**-6.709**	**-12.717**	6.310	162.4	87.8%
3/3	2/3	6.676	13.502	-6.659	-12.680	6.300	198.6	89.1%
3/3	3/3	6.676	13.513	-6.625	-12.651	6.298	235.0	89.4%

The load variation 33mA / 67mA / 100mA resulted in:

V21, +14V = 13.414V ... 13.525V, **du = 111mV**
V31, -6.7V = -6.573V .. -6.709V, **du = 136mV**, referred to V11 +6.676V: **-103mV / +33mV**
V41, -12V = -12.556V .. -12.717V, **du = 161mV**

An improved transformer w/ multifilar windings will improve cross regulation further.
V31 range could be balanced slightly by Schottky w/ bigger Vf at output V11.

Miscellaneous Waveforms

The waveform of the voltage on switchnode (drain to gnd) is shown in Figure 8.

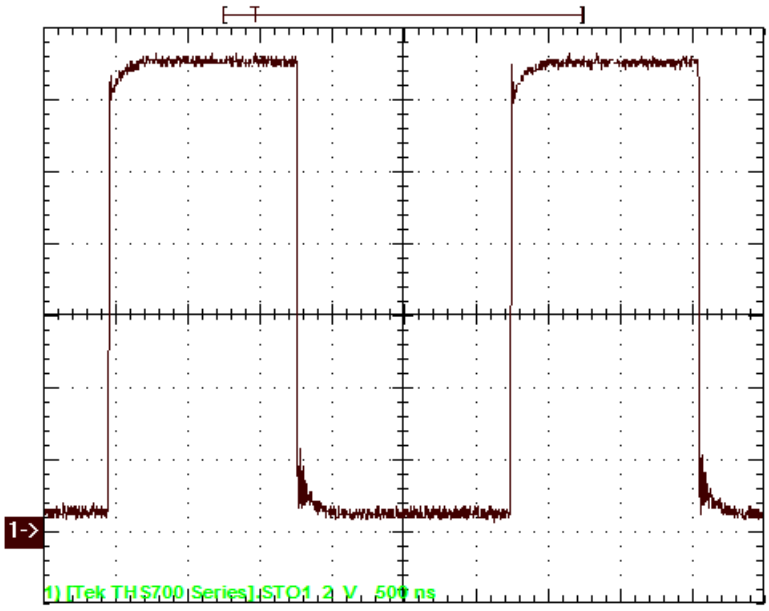
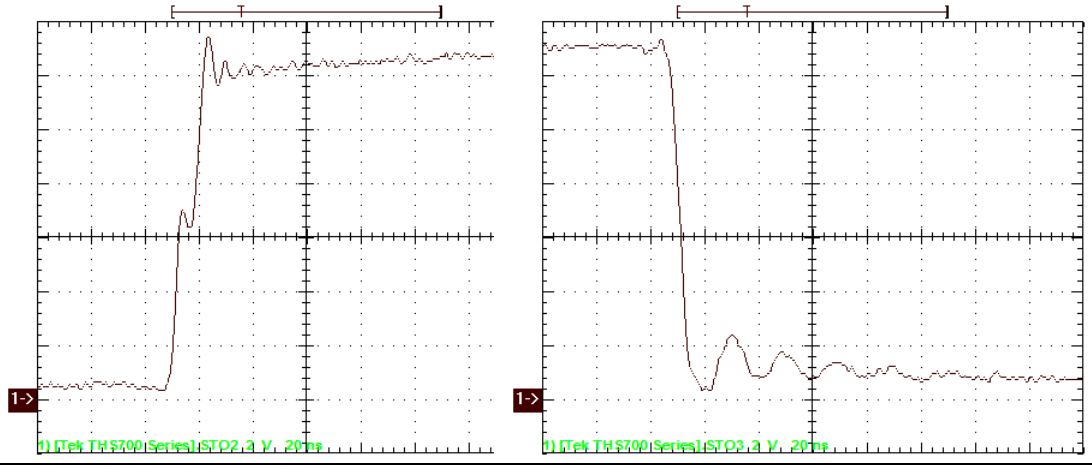
	Ch1 => 2V/div 500ns/div full bandwidth
	Ch1 => 2V/div 50ns/div

Figure 8

The waveform of the voltage on switchnode (anode D1 to gnd) is shown in Figure 9.

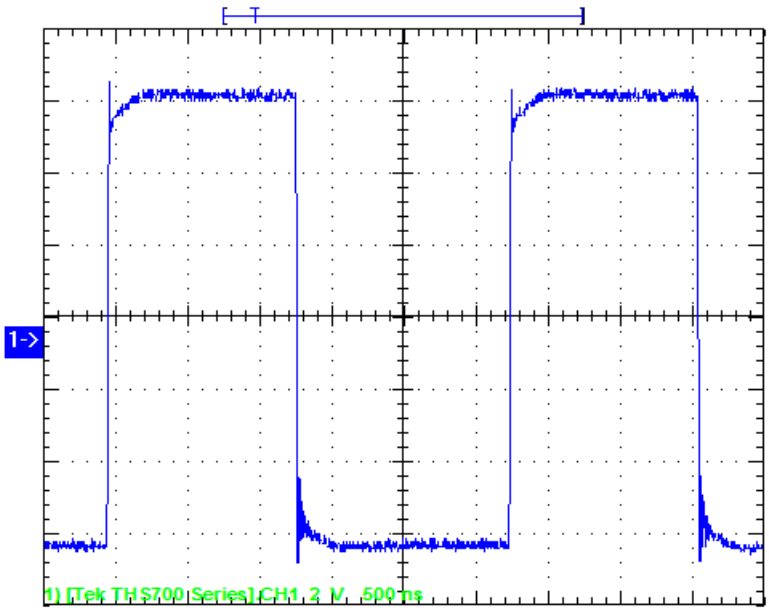
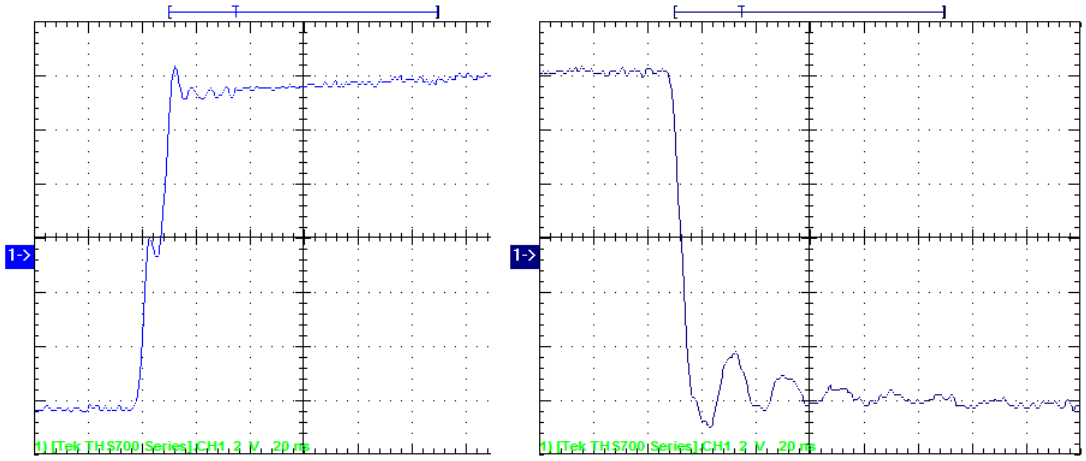
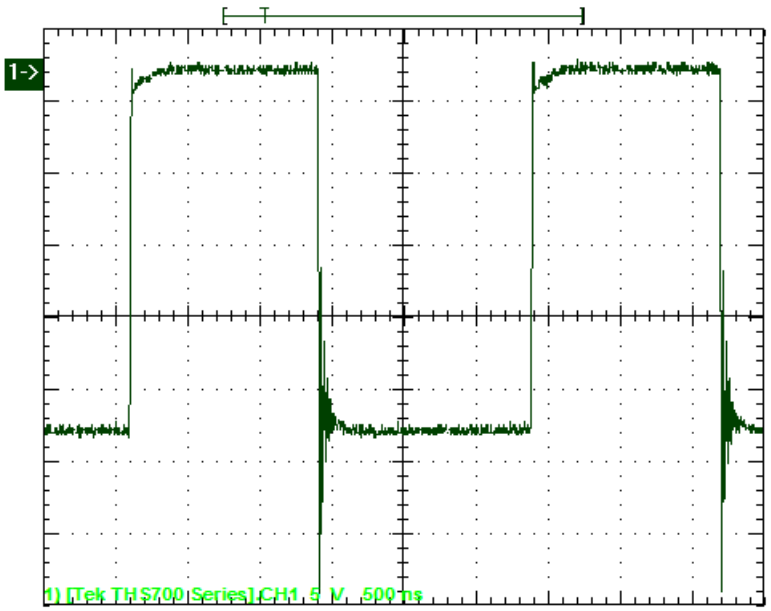
	Ch1 => 2V/div 500ns/div full bandwidth
	Ch1 => 2V/div 50ns/div

Figure 9

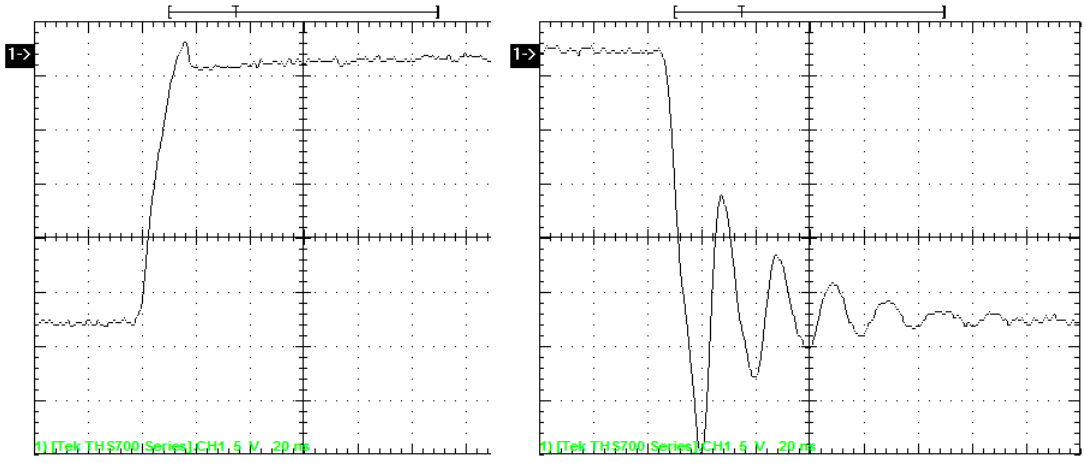
The waveform of the voltage on diode D2 (referenced to VOUT2) is shown in Figure 10.



Ch1 =>
5V/div

500ns/div

full bandwidth



Ch1 =>
5V/div
50ns/div

Figure 10

The waveform of the voltage on switchnode (cathode D3 to GND) is shown in Figure 11.

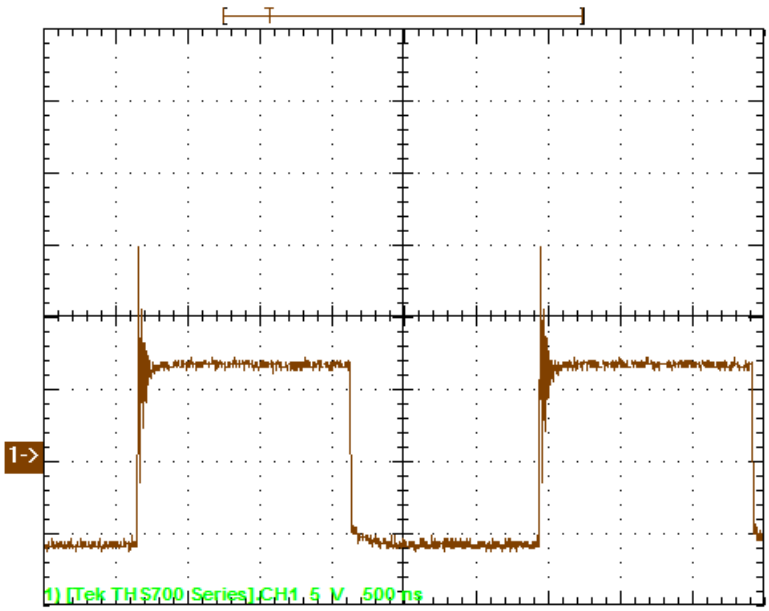
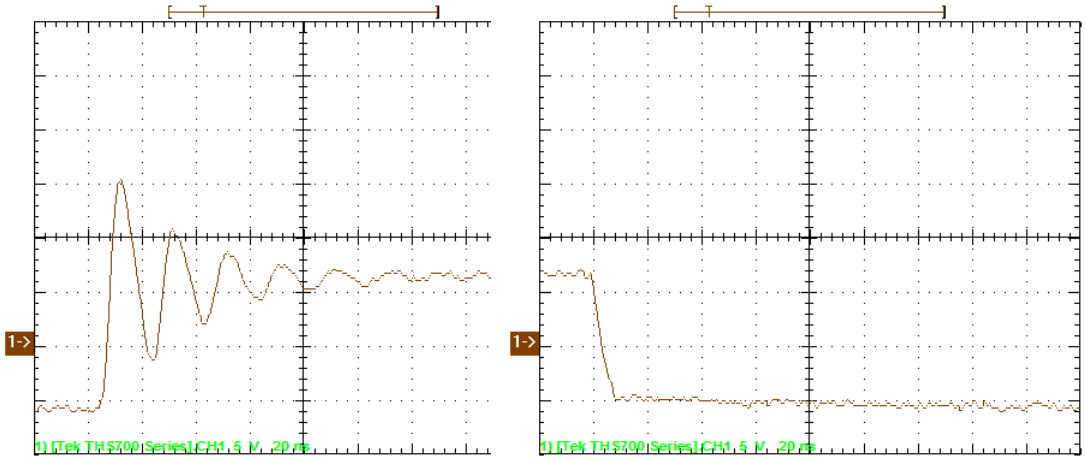
	Ch1 => 5V/div 500ns/div full bandwidth
	Ch1 => 5V/div 50ns/div

Figure 11

The waveform of the voltage on switchnode (cathode D41 to GND) is shown in Figure 12.

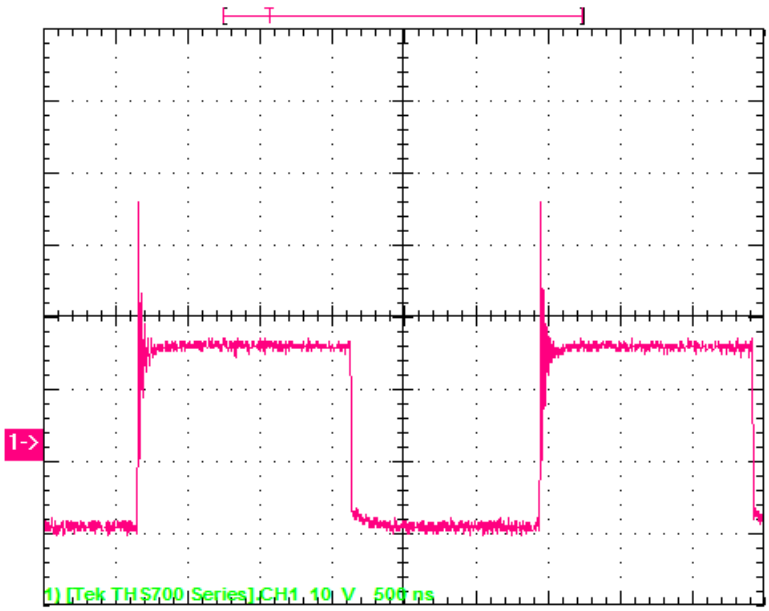
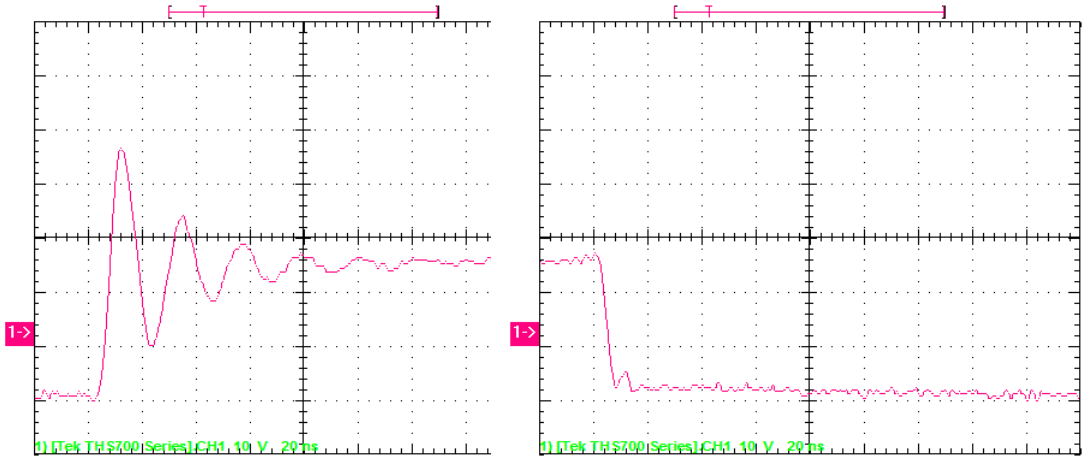
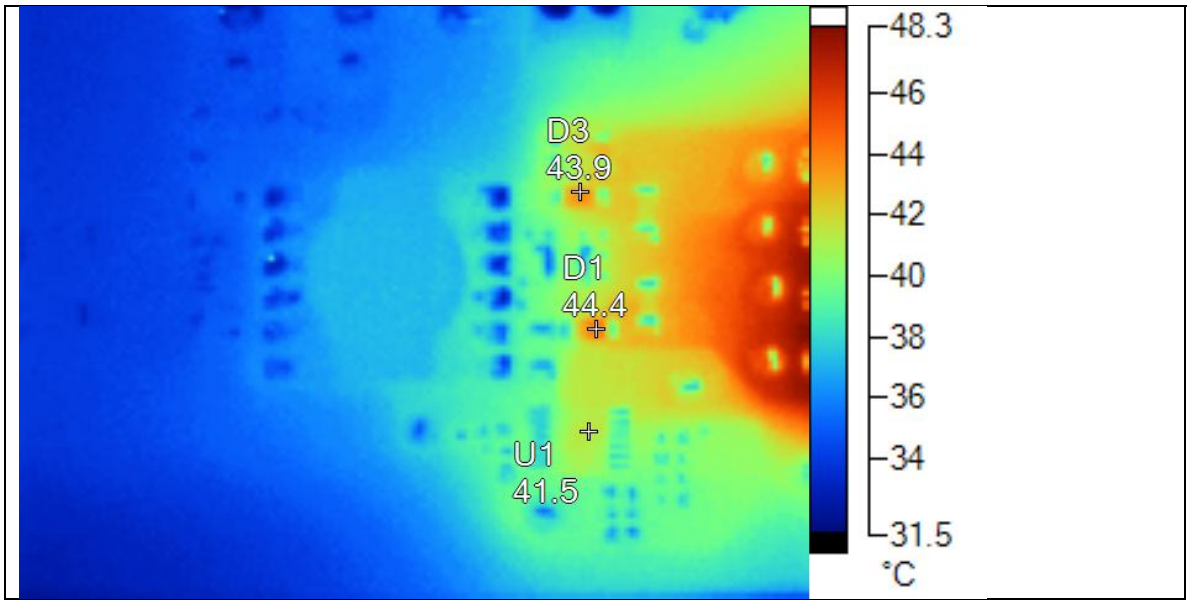
	Ch1 => 10V/div 500ns/div full bandwidth
	Ch1 => 10V/div 50ns/div

Figure 12

8 Thermal Image



Load resistors at output 1 and 3 (right handed) are radiating to the power stage;
The rectifiers and the controller are below 50c at 23c ambient temperature.
The losses at output 2 and output 4 are minor, total converter losses are 163mW.

Name	Temperature
D3	43.9°C
D1	44.4°C
U1	41.5°C

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