**TI Designs – Precision: Verified Design**

**±1A Single-Supply Low-Side Current Sensing Solution Reference Design**

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**Circuit Description**

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from -1 A to 1 A. The linear range of the output is from 110 mV to 3.19 V. The design utilizes the OPA2313 configured as a difference amplifier and reference voltage buffer.

**Design Resources**

Design Archive
- TINA-TI™
- OPA2313

All Design files
- SPICE Simulator
- Product Folder

Ask The Analog Experts
- WEBENCH® Design Center
- TI Designs – Precision Library

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 3.3 V
- Input: -1 A to +1 A
- Output: 110 mV to 3.19 V
- Maximum Shunt Voltage: ±100 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

<table>
<thead>
<tr>
<th>Total Unadjusted Error (%)</th>
<th>Goal</th>
<th>Simulated (typ)</th>
<th>Calculated (typ)</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>±1.0%</td>
<td>±0.893%</td>
<td>±0.53%</td>
<td>±0.621%</td>
</tr>
</tbody>
</table>

![Output Voltage vs. Load Current](image)

Figure 1: Measured Transfer Function
2 Theory of Operation

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of the bus voltage, \( V_{BUS} \). When sensing bidirectional currents, a reference voltage must be added to differentiate between positive and negative currents. Figure 2 depicts a general circuit topology for a low side, bidirectional current sensing solution. This topology is particularly useful when cost is a priority at the expense of accuracy and printed circuit board (PCB) space.

The shunt voltage \( V_{SHUNT} \) is created by the load current \( (I_{LOAD}) \) flowing through the shunt resistor \( R_{SHUNT} \). \( V_{SHUNT} \) is amplified by an op amp (U1A) according to the gain set by the ratio of \( R_4 \) to \( R_3 \). To achieve the transfer function in Equation (1) and to minimize errors as described in Table 2, set \( R_4=R_2 \) and \( R_3=R_1 \).

To provide the reference voltage in this design, divide down the supply voltage \( (V_{CC}) \) using \( R_5 \) and \( R_6 \). The reference voltage is then buffered using an op amp (U1B).

![Figure 2: Design Schematic](image)

Equation (1) depicts the ideal transfer function for the schematic shown in Figure 2.

\[
V_{OUT} = V_{SHUNT} \times \text{Gain}_{\text{Diff}_-\text{Amp}} + V_{REF} 
\]

(1)

Where

\[
V_{SHUNT} = I_{LOAD} \times R_{SHUNT} 
\]

(2)

\[
\text{Gain}_{\text{Diff}_-\text{Amp}} = \frac{R_4}{R_3} 
\]

(3)

\[
V_{REF} = V_{CC} \times \left( \frac{R_6}{R_5 + R_6} \right) 
\]

(4)
2.1 Error Analysis

There are two types of errors introduced by the circuit in Figure 2: offset and gain. To obtain more information about these types of errors, please refer to TIPD129. Table 2 lists the error sources and their respective type(s).

<table>
<thead>
<tr>
<th>Error Source</th>
<th>Description</th>
<th>Error Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shunt resistor</td>
<td>Shunt resistor tolerance</td>
<td>Gain</td>
</tr>
<tr>
<td>Difference Amplifier</td>
<td>U1A and R1-R4 create a difference amplifier. The ratios of R2/R1 and R4/R3 introduce a gain error. The absolute value of the ratios introduce a gain error and the matching of the ratios determine the CMRR performance, which translates to an offset error.</td>
<td>Offset &amp; Gain</td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>The accuracy of the voltage divider created by R5 and R6 yields an offset error.</td>
<td>Offset</td>
</tr>
</tbody>
</table>

These errors ultimately combine and are measured at the output as gain and offset errors. It is common to combine them using the root sum squared (RSS) method. This method is used when combining errors with a normal distribution, thereby yielding typical total error. For a worst-case total error, simply add all error terms directly.
3 Component Selection

3.1 Shunt Resistor (R_{SHUNT})

As shown in Figure 2, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, it may cause issues when interfacing with systems whose ground potential is truly 0 V. If the value of V_{SHUNT} is too negative, it may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore it is important to limit the voltage across the shunt resistor. Equation (5) calculates the maximum value of R_{SHUNT} given a maximum shunt voltage of 100 mV.

\[ R_{SHUNT(MAX)} = \frac{|V_{SHUNT(MAX)}|}{|I_{LOAD(MAX)}|} = \frac{100 \text{mV}}{1 \text{A}} = 100 \Omega \]  

(5)

Since cost is a priority in this design, a shunt resistor with 0.5% tolerance was selected.

3.2 Operational Amplifiers

The shunt voltage in this design can range from -100 mV to +100 mV. It is divided down by R_1 and R_2. The op amp configured as a difference amplifier (U1A) must have an input common-mode that includes this voltage range. Therefore an op amp with rail-to-rail input (RRI) that extends below GND is recommended. The output swing of the amplifier should also be rail-to-rail output (RRO) to maximize the dynamic range of the system. A CMOS op amp is suggested because the supply voltage is 3.3 V. The supply-splitter op amp (U1B) should have low offset voltage. Since there are 2 op amps in this design, a dual package minimizes the required area.

This design utilizes the OPA2313 because it is a RRI/O CMOS device. In addition, the cost vs. performance of the device is excellent.

3.3 Reference Voltage Resistors (R5-R6)

Since the load current range is symmetric (-1 A to 1 A), the resistors that divide down the supply voltage should be equal so that the reference voltage is mid supply (1.65 V). Since cost is a priority in this design, the tolerance should be consistent with the shunt resistor tolerance (0.5%). Finally, select resistors that are large enough to meet the system’s power consumption requirement. For this design, 10 kΩ resistors were chosen.

3.4 Difference Amplifier Gain Setting Resistors (R1-R4)

Equations (6) and (7) show the input common-mode and output voltage range of the OPA2313 given a 3.3V supply.

\[-200 \text{mV} < V_{CM} < 3.5 \text{V} \]  

(6)

\[100 \text{mV} < V_{OUT} < 3.2 \text{V} \]  

(7)

The gain is calculated as shown in Equation (8).

\[ \text{Gain}_{\text{Diff Amp}} = \frac{V_{OUT_{MAX}} - V_{OUT_{MIN}}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2 \text{V} - 100 \text{mV}}{100 \Omega \times (1 \text{A} - (-1 \text{A}))} = 15.5 \frac{\text{V}}{\text{V}} \]  

(8)

The resistor value selected for R_1 and R_3 was 1 kΩ. The resistor value selected for R_2 and R_4 was 15.4 kΩ, which is the nearest 0.1% value to the ideal value of 15.5 kΩ. Therefore the ideal gain of the difference amplifier is 15.4 V/V.
4 Simulation

4.1 Transfer Function

Figure 3 shows the TINA-TI™ schematic used to simulate the dc transfer function.

Figure 3: TINA-TI™ Transfer Function Schematic

Figure 4 depicts the simulated dc transfer function results using nominal component values.

Figure 4: Simulated Nominal Output Voltage vs. Load Current
These results correlate with the ideal minimum and maximum output voltages as calculated in Equations (9) and (10).

\[ V_{\text{OUT}_\text{MIN}} = -100\text{mV} \times 15.4 \frac{V}{V} + 1.65V = 110\text{mV} \]  
(9)

\[ V_{\text{OUT}_\text{MAX}} = 100\text{mV} \times 15.4 \frac{V}{V} + 1.65V = 3.19V \]  
(10)

\[ V_{\text{OUT}(V) \text{ at } -1A} = 119.481035 \text{mV} \pm 3.424383 \text{mV} \]

\[ V_{\text{OUT}(V) \text{ at } 0A} = 1.659374 \text{V} \pm 2.215354 \text{mV} \]

\[ V_{\text{OUT}(V) \text{ at } 1A} = 3.199267 \text{V} \pm 3.608592 \text{mV} \]

4.2 Monte Carlo Simulation Error Analysis

To analyze error due to the op amps, tolerance of RSHUNT, the difference amplifier resistors R1-R4, and the reference voltage divider resistors R5-R6, a 1,000 point Monte-Carlo simulation was run at -1 A and 1 A input currents. The results of the Monte-Carlo simulation are shown in Table 3.

Table 3. DC Transfer Results from Calibrated Monte-Carlo Analysis

<table>
<thead>
<tr>
<th>Average (µ)</th>
<th>Std. Dev. (σ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT (V) at -1A</td>
<td>119.481035m</td>
</tr>
<tr>
<td>VOUT (V) at 0A</td>
<td>1.659374</td>
</tr>
<tr>
<td>VOUT (V) at 1A</td>
<td>3.199267</td>
</tr>
</tbody>
</table>

Using the mean (µ) and standard deviation (σ) from the Monte-Carlo simulation, a prediction of the typical (±1σ) offset error is calculated using Equation (12).

\[ \text{OffsetError(\%)}_{\text{TYP \_ SIM}} = \left( \frac{\mu \pm 1\sigma}{1.65} - 1 \right) \times 100 = 0.7\% \]  
(11)

Similarly, a prediction of the typical gain error is calculated below.

\[ \text{GE(\%)}_{\text{TYP \_ SIM}} = \left( \frac{\mu + 1\sigma}{2 \times 1.54} - 1 \right) \times 100 = 0.22\% \]  
(12)

4.3 DC Sweep Error Analysis

In addition to the Monte Carlo simulation, worst-case dc sweeps of the circuit in Figure 3 were simulated while varying the resistors within their typical values (±1σ), which is 1/3 of their given tolerance. For example, resistors with a tolerance of 0.1% were change to 0.033%. The typical offset error was simulated to be 0.86% and the gain error was 0.24%. These results correlate well with the Monte Carlo simulation.

4.4 Simulated Results Summary

Table 4 compares the simulation results with the design goals.

Table 4. Design Goals with Simulated Performance

<table>
<thead>
<tr>
<th>Goal</th>
<th>Simulated-MC</th>
<th>Simulated-DC Sweep</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Error</td>
<td>0.7%</td>
<td>0.86%</td>
</tr>
<tr>
<td>Gain Error</td>
<td>0.22%</td>
<td>0.24%</td>
</tr>
<tr>
<td>Total Error</td>
<td>±1%</td>
<td>0.734% (RSS)</td>
</tr>
</tbody>
</table>
5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

Figure 5 depicts the printed circuit board (PCB) layout. The traces for the shunt voltage are balanced and short. Wide, short traces were used for the load current path to minimize impedance. All other standard PCB layout practices were observed.

![Figure 5: PCB Layout](image-url)
6 Verification & Measured Performance

6.1 Transfer Function

The output voltage was measured while sweeping the input current from -1 A to 1 A. Five boards were assembled and measured. The transfer function measurement for Board 1 is shown in Figure 6 while the remaining results can be found in Appendix C.

\[ y = 1.5397x + 1.6443 \]

**Figure 6: Measured Output Voltage vs. Load Current (Board #1)**

The ideal circuit gain (which is the product of the shunt gain, 0.1, and difference amplifier gain, 15.4) is 1.54V/V. The ideal offset voltage is equal to the reference voltage, or 1.65V. Using a straight-line approximation for the results yields the measured gain and offset as shown in Figure 6. The gain and offset error for board #1 is calculated below.

\[
\text{Offset Error(\%)}_{\text{MEAS \_BOARD1}} = \frac{1.6443 - 1.65}{1.65} \times 100 = -0.343\%
\]  
\[
\text{GE(\%)}_{\text{MEAS \_BOARD1}} = \frac{1.5397 - 1.54}{1.54} \times 100 = -0.022\%
\]
6.2 Measured Results Summary

The measured results are summarized in Table 5.

Table 5. Measured Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>GE(%)</th>
<th>Offset Error (%)</th>
<th>RSS Total Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board 1</td>
<td>-0.022</td>
<td>-0.343</td>
<td>0.344</td>
</tr>
<tr>
<td>Board 2</td>
<td>-0.011</td>
<td>-0.146</td>
<td>0.146</td>
</tr>
<tr>
<td>Board 3</td>
<td>-0.084</td>
<td>0.026</td>
<td>0.088</td>
</tr>
<tr>
<td>Board 4</td>
<td>0.029</td>
<td>0.448</td>
<td>0.449</td>
</tr>
<tr>
<td>Board 5</td>
<td>-0.010</td>
<td>0.621</td>
<td>0.621</td>
</tr>
</tbody>
</table>
7 Modifications

The most significant error contribution is the offset error due to the reference voltage divider accuracy and op amp offset voltage. In order to minimize this error, consider using resistors with a tighter tolerance. Alternate op amps with less offset voltage are listed below. Note that the input common-mode range for the alternate op amps is less than the OPA2313. Therefore it is suggested to limit the shunt voltage to no more than 50 mV below the negative rail for design margin.

Table 6: Alternate Op Amps

<table>
<thead>
<tr>
<th>Op Amp</th>
<th>Vos @ 25ºC (max, µV)</th>
<th>Vcm(min)</th>
<th>Vcm(max)</th>
<th>Output Swing to Supply (mV)</th>
<th>BW (typ, MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2313</td>
<td>2500 (V-)0.2 (V+)0.2</td>
<td>100</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2317</td>
<td>90 (V-)0.1 (V+)0.1</td>
<td>100</td>
<td>0.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2320</td>
<td>150 (V-)0.1 (V+)0.1</td>
<td>35</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2330</td>
<td>50 (V-)0.1 (V+)0.1</td>
<td>100</td>
<td>0.35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2333</td>
<td>10 (V-)0.1 (V+)0.1</td>
<td>50</td>
<td>0.35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2365</td>
<td>200 (V-)0.1 (V+)0.1</td>
<td>20</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPA2376</td>
<td>25 (V-)0.1 (V+)0.1</td>
<td>30</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In order to decrease gain error, consider either resistors with a tighter tolerance or a RRI/O instrumentation amplifier (e.g. INA326). For solutions that require low-drift, consider using a current shunt monitor and dual-output reference (e.g. TIPD156) because all resistors are integrated in the package and will drift together.

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments’ difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University’s Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

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9 Acknowledgements & References

The authors would like to thank Collin Wells for his technical contributions.

A.1 Electrical Schematic

Figure A-1: Electrical Schematic
### A.2 Bill of Materials

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>DigiKey Part Number</th>
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<td>Red</td>
<td>Test Point, TH, Compact, Red</td>
<td>Keystone</td>
<td>5005</td>
<td>500SK-ND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Black</td>
<td>Test Point, TH, Compact, Black</td>
<td>Keystone</td>
<td>5006</td>
<td>5006K-ND</td>
</tr>
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<td>1</td>
<td>Vout</td>
<td>White</td>
<td>Test Point, Compact, White, TH</td>
<td>Keystone</td>
<td>5007</td>
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<td>Orange</td>
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<td>5008</td>
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<td>RMCF0603FT10K0</td>
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<td>U94, U95, U96, U97</td>
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<td>PM555 440 0025 PH</td>
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<td>296-35004-ND</td>
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<td>TPSC106K025R0500</td>
<td>478-1762-1-ND</td>
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Appendix B.

B.1 Error Analysis

The transfer function for this design is given in Equation (15).

\[ V_{\text{OUT}} = V_{\text{SHUNT}} \times \text{Gain} + V_{\text{REF}} \]  \hfill (15)

Equation (16) is the transfer function in terms of circuit voltages, currents, and components. This equation aids in understanding the error analysis.

\[ V_{\text{OUT}} = I_{\text{LOAD}} \times R_{\text{SHUNT}} \times \frac{R_4}{R_3} + \left( V_{\text{CC}} \times \left( \frac{R_6}{R_5 + R_6} \right) \right) \]  \hfill (16)

B.1.1 Offset Errors

The reference voltage supplied by the resistor divider (R_5 and R_6) and U1B will introduce an offset error. Given a tolerance of ±0.5% for the resistors, supply voltage (V_{\text{CC}}) of 3.3V, and ideal dividing ratio of ½, the maximum offset voltage due to R_5 and R_6 is calculated in Equation (17).

\[ V_{\text{OS,R5R6,MAX}} = V_{\text{CC}} \times \left( \text{IdealRatio} - \frac{1\pm 0.5\%}{(1\pm 0.5\%) + (1\pm 0.5\%)} \right) = \pm 8.25 \text{mV} \]  \hfill (17)

This error calculation represents the worst-case scenario. Assuming the resistor values observe a Gaussian 6σ (±3σ) distribution, dividing the tolerance by 3 will yield a typical error analysis (±1σ). This result is calculated in Equation (18).

\[ V_{\text{OS,R5R6,TYP}} = V_{\text{CC}} \times \left( \text{IdealRatio} - \frac{1\pm 0.167\%}{(1\pm 0.167\%) + (1\pm 0.167\%)} \right) = \pm 2.76 \text{mV} \]  \hfill (18)

In addition to the offset due to R_5 and R_6, the op amps U1A and U1B have typical offset voltages of ±0.5mV (±2.5mV maximum).

\[ V_{\text{OS,U1,TYP}} = \pm 0.5 \text{mV} \]  \hfill (19)

\[ V_{\text{OS,U1,MAX}} = \pm 2.5 \text{mV} \]  \hfill (20)
The CMRR performance of the op amp U1A also introduces an offset error. Equations (21) and (22) calculate the typical and maximum offset errors introduced by the OPA313 given a common-mode voltage near zero. For more information on this calculation, please refer to Part III of the Current Sensing Fundamentals article series.

\[
V_{OS\_U1A\_CMRR\_TYP} = 1.65V \times \left( \frac{1}{\frac{85}{20}dB} \right) = \pm 97.8\mu V
\]

\[
V_{OS\_U1A\_CMRR\_MAX} = 1.65V \times \left( \frac{1}{\frac{70}{20}dB} \right) = \pm 0.52mV
\]

Finally, the CMRR performance of the difference amplifier also introduces an offset error. The CMRR performance of a discrete difference amplifier can be calculated using Equation (23). [1]

\[
CMRR_{db} = 20\log_{10} \left( \frac{1 + \text{Gain}}{4 \times \frac{R_{\text{tolerance}}}{100}} \right)
\]

The worst-case CMRR performance of the difference amplifier in a gain of 15.4 V/V using 0.1% resistors is 72.25 dB. The typical CMRR is 81.8 dB (calculated using 0.033% resistors).

The common-mode voltage of the difference amplifier (defined as the average voltage at the input pins) can range from -50 mV to 50 mV. Therefore, the offset voltage due to the difference amplifier CMRR is calculated in Equations (24) and (25).

\[
V_{OS\_DA\_TYP} = \pm 50mV \times \left( \frac{1}{\frac{81.8}{20}dB} \right) = \pm 4.1\mu V
\]

\[
V_{OS\_DA\_MAX} = \pm 50mV \times \left( \frac{1}{\frac{72.25}{20}dB} \right) = \pm 12.2\mu V
\]

Table 7 summarizes the offset voltage errors.

<table>
<thead>
<tr>
<th></th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor Divider</td>
<td>±2.76mV</td>
<td>±8.25mV</td>
</tr>
<tr>
<td>U1A &amp; U1B</td>
<td>±0.5mV</td>
<td>±2.5mV</td>
</tr>
<tr>
<td>U1A CMRR</td>
<td>±97.8μV</td>
<td>±0.52mV</td>
</tr>
<tr>
<td>Difference Amp CMRR</td>
<td>±4.1μV</td>
<td>±12.2μV</td>
</tr>
</tbody>
</table>
The offset voltages due to the resistor divider (R5 and R6) and the offset voltage of U1B add directly to the output of U1A. The remaining offset voltages are referred to the output of the circuit (RTO) by multiplying by the gain of the difference amplifier (15.4V/V). Therefore we can calculate the total offset error referred to the output as shown in Equation (26). The typical and maximum offset voltages referred to the output are depicted in Equations (27) and (28).

\[
V_{OS\_Total\_RTO} = \sqrt{V_{OS\_R5R6}^2 + V_{OS\_U1B}^2 + (Gain \times V_{OS\_U1A})^2 + (Gain \times V_{OS\_U1A\_CMRR})^2 + (Gain \times V_{OS\_DA})^2}
\]

\[
V_{OS\_Total\_RTO\_Typ} = \pm 8.33\text{mV}
\]

\[
V_{OS\_Total\_RTO\_Max} = \pm 40.23\text{mV}
\]

Given an ideal offset voltage of 1.65V, the offset typical and maximum offset errors are calculated below.

\[
\text{OffsetError(\%)}_{Typ\_Calc} = \frac{\pm 8.33\text{mV}}{1.65} \times 100 = 0.5\%
\]

\[
\text{OffsetError(\%)}_{Max\_Calc} = \frac{\pm 40.23\text{mV}}{1.65} \times 100 = 2.44\%
\]

The calculated typical offset error correlates well with the simulated results (0.7% and 0.86%). The calculated maximum offset error is larger than the simulated results because the amplifier simulation models only model the typical offset error.
Gain Errors

The shunt resistor, \( R_{\text{SHUNT}} \), introduces a gain error. In this design, the tolerance of \( R_{\text{SHUNT}} \) is 0.5%. Also, any mismatch in the gain setting resistors of the difference amplifier (\( R_4 \) and \( R_3 \)) introduce gain error. Since they each have a tolerance of 0.1% (\( \varepsilon = 0.001 \)), the worst-case gain error introduced by the gain-setting resistors of the difference amplifier is approximately 0.2% as calculated in Equation (31).

\[
GE_{\text{Diff Amp}}(\%) = \left( 1 - \frac{1 + \varepsilon}{1 - \varepsilon} \right) \times 100 = 0.2002\% \approx 0.2\%
\] (31)

The following equations calculate the typical (using 1/3 of the resistor tolerance) and maximum gain error expected for this design.

\[
GE_{\text{TYP}} = \sqrt{0.167^2 + 0.07^2} = 0.18\%
\] (32)

\[
GE_{\text{MAX}} = \sqrt{0.5^2 + 0.2^2} = 0.54\%
\] (33)

Total Error

The total error, including both offset and gain errors, is calculated in Equations (34) and (35).

\[
\text{Error}_{\text{Total TYP}} = \sqrt{\text{OffsetError}_{\text{TYP}}^2 + GE_{\text{TYP}}^2} = 0.53\%
\] (34)

\[
\text{Error}_{\text{Total MAX}} = \sqrt{\text{OffsetError}_{\text{MAX}}^2 + GE_{\text{MAX}}^2} = 2.5\%
\] (35)
Appendix C.

C.1 Board #2

Output Voltage vs. Load Current

\[ y = 1.5398x + 1.6476 \]

C.2 Board #3

Output Voltage vs. Load Current

\[ y = 1.5387x + 1.6504 \]
C.3 Board #4

![Output Voltage vs. Load Current](chart.png)

\[ y = 1.5404x + 1.6574 \]

C.4 Board #5

![Output Voltage vs. Load Current](chart.png)

\[ y = 1.5399x + 1.6602 \]
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