LM5121
Wide Input Synchronous Boost Controller with Disconnection Switch Control

TI reference design number: PMP9297 Rev B

Input: 34.5V - 37.5V
Output 1: 38V @ 4A
Output 2: 52V @ 3A

DC–DC Converter Test Results
# Table of Contents

1. Circuit Description ........................................................................................................... 4
2. Fabrication ......................................................................................................................... 4
3. Efficiency ........................................................................................................................... 6
4. Thermal ............................................................................................................................... 8
   Top View ............................................................................................................................ 8
5. Power Up ............................................................................................................................ 9
   5.1 Power Up at 34.5V Input – No Load  Power Up at 34.5V Input – 4A Load ............... 9
   Output 1 38V ................................................................................................................ 9
   5.2 Power Up at 37.5V Input – No Load  Power Up at 37.5V Input – 4A Load ............... 9
   Output 1 38V ................................................................................................................ 9
   5.3 Power Up at 34.5V Input – No Load  Power Up at 34.5V Input – 3A Load ............... 10
   Output 2 52V ................................................................................................................ 10
   5.4 Power Up at 37.5V Input – No Load  Power Up at 37.5V Input – 3A Load ............... 10
   Output 2 52V ................................................................................................................ 10
6. Switch Node Voltage and Output Ripple Voltage ........................................................... 11
   6.1 35V input –38V Output 4A load ............................................................................. 11
   Output 1 38V ................................................................................................................ 11
   6.2 35V input –52V Output 3A load ............................................................................. 11
   Output 2 52V ................................................................................................................ 11
7. Transient Response ........................................................................................................... 12
   7.1 34.5V Input – 2A to 4A, 100mA/µs, 100 Hz, 50% duty cycle, 38V out. ................. 12
   Output 1 38V ................................................................................................................ 12
   7.2 37.5V Input – 2A to 4A, 100mA/µs, 100 Hz, 50% duty cycle, 38V out. ................. 12
   Output 1 38V ................................................................................................................ 12
   7.3 34.5V Input – 1.5A to 3A, 100mA/µs, 100 Hz, 50% duty cycle, 52V out. .............. 13
   Output 2 52V ................................................................................................................ 13
   7.4 37.5V Input – 1.5A to 3A, 100mA/µs, 100 Hz, 50% duty cycle, 52V out. .............. 13
   Output 2 52V ................................................................................................................ 13
8. Current Limit Tests ............................................................................................................ 14
   8.1 34.5V input - No Load  34.5V input – 4A Load ......................................................... 14
   Output 1 38V ................................................................................................................ 14
   8.2 37.5V input - No Load  37.5V input - 4A Load ......................................................... 14
   Output 1 38V ................................................................................................................ 14
   8.3 34.5V input – No Load  34.5V input – 3 A Load ....................................................... 15
   Output 2 52V ................................................................................................................ 15
   8.4 37.5V input – No Load  37.5V input – 3A Load ....................................................... 15
   Output 2 52V ................................................................................................................ 15
9. Short Circuit Tests (I OUT Monitored) ........................................................................... 16
   9.1 34.5V input - No Load  34.5V input – 4A Load ......................................................... 16
   Output 1 38V ................................................................................................................ 16
   9.2 37.5V input - No Load  37.5V input - 4A Load ......................................................... 16
   Output 1 38V ................................................................................................................ 16
9.3 34.5V input – No Load 34.5V input – 3 A Load ........................................... 17
Output 2 52V ................................................................. 17
9.4 37.5V input – No Load 37.5V input – 3A Load ........................................... 17
Output 2 52V ................................................................. 17
10. Short Circuit Tests (I IN Monitored) ............................................................. 18
10.1 34.5V input - No Load 34.5V input – 4A Load ........................................... 18
Output 1 38V ................................................................. 18
10.2 37.5V input - No Load 37.5V input - 4A Load ........................................... 18
Output 1 38V ................................................................. 18
10.3 34.5V input – No Load 34.5V input – 3 A Load ........................................... 19
Output 2 52V ................................................................. 19
10.4 37.5V input – No Load 37.5V input – 3A Load ........................................... 19
Output 2 52V ................................................................. 19
11. Power Up into a Short Circuit ................................................................. 20
11.1 34.5V input 37.5V input ......................................................... 20
Output 1 38V ................................................................. 20
11.2 34.5V input 37.5V input ......................................................... 20
Output 2 52V ................................................................. 20
12. UVLO into a Short Circuit ................................................................. 21
12.1 34.5V input - 4 Load 37.5V input – 4A Load ........................................... 21
Output 1 38V ................................................................. 21
12.2 34.5V input – 3A load 37.5V input – 3 A Load ........................................... 21
Output 2 52V ................................................................. 21
13. Short Circuit Recovery (UVLO) ............................................................. 22
13.1 34.5V input - No Load 34.5V input – 4A Load ........................................... 22
Output 1 38V ................................................................. 22
13.2 37.5V input - No Load 37.5V input - 4A Load ........................................... 22
Output 1 38V ................................................................. 22
13.3 34.5V input – No Load 34.5V input – 3 A Load ........................................... 23
Output 2 52V ................................................................. 23
13.4 37.5V input – No Load 37.5V input – 3A Load ........................................... 23
Output 2 52V ................................................................. 23
1. Circuit Description

PMP9297 is a dual channel synchronous boost for GaN audio amplifier applications. It converts 35V input to an adjustable 38V to 55V output at 150W per channel. The solution size fits in a 45mm x 34 mm board area. Additional input and output bulk capacitors are included outside of the solution size area. This design uses TLP0202 dual channel digital pot to program the output voltages via SPI bus. Output current monitoring is done using LMP8481-S high-side current sense amplifiers. NTC thermistors allow temperature measurement of the High-side MOSFETs.

2. Fabrication

The dual LM5121 boost circuit was built on PMP9297 Rev A printed circuit board. This is a four layer board with overall dimensions of 7.45” (189mm) x 3.45” (87mm). The copper weight is 1oz on the outer layer and 0.5oz on the inner layers. The overall solution size per channel is 1.3” (34mm) x 0.89” (22.5mm).
3. Efficiency

3.1 LM5121Boost Efficiency Data
### 3.2 LM5121 38V out Efficiency

<table>
<thead>
<tr>
<th>Vin (V)</th>
<th>Iin (A)</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>Efficiency (%)</th>
<th>Pin (W)</th>
<th>Pout (W)</th>
<th>Losses (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>34.999</td>
<td>0.066</td>
<td>38.404</td>
<td>0.000</td>
<td>0.18%</td>
<td>2.321</td>
<td>0.004</td>
<td>2.317</td>
</tr>
<tr>
<td>34.999</td>
<td>0.066</td>
<td>38.405</td>
<td>0.000</td>
<td>0.12%</td>
<td>2.323</td>
<td>0.003</td>
<td>2.320</td>
</tr>
<tr>
<td>34.998</td>
<td>0.334</td>
<td>38.404</td>
<td>0.247</td>
<td>81.34%</td>
<td>11.680</td>
<td>9.501</td>
<td>2.180</td>
</tr>
<tr>
<td>34.998</td>
<td>0.619</td>
<td>38.400</td>
<td>0.502</td>
<td>88.96%</td>
<td>21.655</td>
<td>19.264</td>
<td>2.391</td>
</tr>
<tr>
<td>34.998</td>
<td>0.900</td>
<td>38.398</td>
<td>0.756</td>
<td>92.18%</td>
<td>31.484</td>
<td>29.022</td>
<td>2.462</td>
</tr>
<tr>
<td>34.998</td>
<td>1.177</td>
<td>38.396</td>
<td>1.010</td>
<td>94.11%</td>
<td>41.204</td>
<td>38.775</td>
<td>2.429</td>
</tr>
<tr>
<td>34.998</td>
<td>1.455</td>
<td>38.395</td>
<td>1.264</td>
<td>95.26%</td>
<td>50.937</td>
<td>48.523</td>
<td>2.414</td>
</tr>
<tr>
<td>34.997</td>
<td>1.734</td>
<td>38.394</td>
<td>1.518</td>
<td>96.04%</td>
<td>60.682</td>
<td>58.278</td>
<td>2.404</td>
</tr>
<tr>
<td>34.997</td>
<td>2.012</td>
<td>38.392</td>
<td>1.772</td>
<td>96.62%</td>
<td>70.413</td>
<td>68.032</td>
<td>2.381</td>
</tr>
<tr>
<td>34.997</td>
<td>2.290</td>
<td>38.391</td>
<td>2.026</td>
<td>97.04%</td>
<td>80.156</td>
<td>77.786</td>
<td>2.370</td>
</tr>
<tr>
<td>34.997</td>
<td>2.569</td>
<td>38.389</td>
<td>2.280</td>
<td>97.37%</td>
<td>89.894</td>
<td>87.534</td>
<td>2.360</td>
</tr>
<tr>
<td>34.997</td>
<td>2.848</td>
<td>38.388</td>
<td>2.534</td>
<td>97.62%</td>
<td>99.658</td>
<td>97.286</td>
<td>2.372</td>
</tr>
<tr>
<td>34.997</td>
<td>3.126</td>
<td>38.387</td>
<td>2.788</td>
<td>97.82%</td>
<td>109.410</td>
<td>107.020</td>
<td>2.390</td>
</tr>
<tr>
<td>34.996</td>
<td>3.405</td>
<td>38.385</td>
<td>3.042</td>
<td>97.98%</td>
<td>119.170</td>
<td>116.760</td>
<td>2.410</td>
</tr>
<tr>
<td>34.996</td>
<td>3.685</td>
<td>38.384</td>
<td>3.296</td>
<td>98.12%</td>
<td>128.951</td>
<td>126.521</td>
<td>2.430</td>
</tr>
<tr>
<td>34.996</td>
<td>3.964</td>
<td>38.382</td>
<td>3.551</td>
<td>98.23%</td>
<td>138.742</td>
<td>136.280</td>
<td>2.461</td>
</tr>
<tr>
<td>34.996</td>
<td>4.244</td>
<td>38.381</td>
<td>3.805</td>
<td>98.31%</td>
<td>148.527</td>
<td>146.024</td>
<td>2.504</td>
</tr>
<tr>
<td>34.996</td>
<td>4.524</td>
<td>38.379</td>
<td>4.059</td>
<td>98.39%</td>
<td>158.318</td>
<td>155.763</td>
<td>2.555</td>
</tr>
<tr>
<td>34.996</td>
<td>4.804</td>
<td>38.377</td>
<td>4.312</td>
<td>98.44%</td>
<td>168.123</td>
<td>165.507</td>
<td>2.616</td>
</tr>
<tr>
<td>34.996</td>
<td>5.085</td>
<td>38.377</td>
<td>4.566</td>
<td>98.49%</td>
<td>177.941</td>
<td>175.247</td>
<td>2.694</td>
</tr>
</tbody>
</table>

### 3.3 LM5121 52V out Efficiency

<table>
<thead>
<tr>
<th>Vin (V)</th>
<th>Iin (A)</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>Efficiency (%)</th>
<th>Pin (W)</th>
<th>Pout (W)</th>
<th>Losses (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>34.999</td>
<td>0.066</td>
<td>51.419</td>
<td>0.000</td>
<td>1.04%</td>
<td>2.324</td>
<td>0.024</td>
<td>2.299</td>
</tr>
<tr>
<td>34.999</td>
<td>0.066</td>
<td>51.419</td>
<td>0.000</td>
<td>0.54%</td>
<td>2.316</td>
<td>0.013</td>
<td>2.303</td>
</tr>
<tr>
<td>34.999</td>
<td>0.426</td>
<td>51.418</td>
<td>0.247</td>
<td>85.29%</td>
<td>14.912</td>
<td>12.719</td>
<td>2.193</td>
</tr>
<tr>
<td>34.998</td>
<td>0.813</td>
<td>51.413</td>
<td>0.501</td>
<td>90.66%</td>
<td>28.437</td>
<td>25.781</td>
<td>2.656</td>
</tr>
<tr>
<td>34.998</td>
<td>1.192</td>
<td>51.410</td>
<td>0.756</td>
<td>93.12%</td>
<td>41.711</td>
<td>38.842</td>
<td>2.870</td>
</tr>
<tr>
<td>34.998</td>
<td>1.565</td>
<td>51.409</td>
<td>1.010</td>
<td>94.75%</td>
<td>54.786</td>
<td>51.908</td>
<td>2.878</td>
</tr>
<tr>
<td>34.998</td>
<td>1.940</td>
<td>51.408</td>
<td>1.264</td>
<td>95.69%</td>
<td>67.887</td>
<td>64.964</td>
<td>2.923</td>
</tr>
<tr>
<td>34.998</td>
<td>2.315</td>
<td>51.407</td>
<td>1.518</td>
<td>96.30%</td>
<td>81.012</td>
<td>78.013</td>
<td>2.999</td>
</tr>
<tr>
<td>34.998</td>
<td>2.689</td>
<td>51.406</td>
<td>1.772</td>
<td>96.77%</td>
<td>94.111</td>
<td>91.072</td>
<td>3.039</td>
</tr>
<tr>
<td>34.998</td>
<td>3.064</td>
<td>51.406</td>
<td>2.026</td>
<td>97.10%</td>
<td>107.248</td>
<td>104.142</td>
<td>3.105</td>
</tr>
<tr>
<td>34.998</td>
<td>3.440</td>
<td>51.405</td>
<td>2.280</td>
<td>97.33%</td>
<td>120.402</td>
<td>117.185</td>
<td>3.217</td>
</tr>
<tr>
<td>34.998</td>
<td>3.816</td>
<td>51.404</td>
<td>2.534</td>
<td>97.53%</td>
<td>133.567</td>
<td>130.265</td>
<td>3.302</td>
</tr>
<tr>
<td>34.998</td>
<td>4.193</td>
<td>51.403</td>
<td>2.788</td>
<td>97.64%</td>
<td>146.755</td>
<td>143.292</td>
<td>3.463</td>
</tr>
<tr>
<td>34.998</td>
<td>4.571</td>
<td>51.403</td>
<td>3.042</td>
<td>97.75%</td>
<td>159.968</td>
<td>156.361</td>
<td>3.606</td>
</tr>
<tr>
<td>34.998</td>
<td>4.949</td>
<td>51.402</td>
<td>3.296</td>
<td>97.81%</td>
<td>173.205</td>
<td>169.418</td>
<td>3.788</td>
</tr>
<tr>
<td>34.997</td>
<td>5.328</td>
<td>51.402</td>
<td>3.550</td>
<td>97.87%</td>
<td>186.451</td>
<td>182.480</td>
<td>3.971</td>
</tr>
<tr>
<td>34.997</td>
<td>5.707</td>
<td>51.401</td>
<td>3.804</td>
<td>97.89%</td>
<td>199.731</td>
<td>195.524</td>
<td>4.207</td>
</tr>
<tr>
<td>34.997</td>
<td>6.087</td>
<td>51.401</td>
<td>4.058</td>
<td>97.92%</td>
<td>213.021</td>
<td>208.589</td>
<td>4.431</td>
</tr>
<tr>
<td>34.997</td>
<td>6.468</td>
<td>51.400</td>
<td>4.312</td>
<td>97.92%</td>
<td>226.362</td>
<td>221.647</td>
<td>4.715</td>
</tr>
</tbody>
</table>
4. Thermal

4.1 Steady State Temperature - 35V in, 52V out, 3A load each channel

*Top View*
5. Power Up

5.1 Power Up at 34.5V Input – No Load

Output 1 38V
Channel 1 VIN
Channel 2 VOUT
Channel 4 IIN

5.2 Power Up at 37.5V Input – No Load

Output 1 38V
Channel 1 VIN
Channel 2 VOUT
Channel 4 IIN
5.3 Power Up at 34.5V Input – No Load

Power Up at 34.5V Input – 3A Load

Output 2 52V
Channel 1 VIN
Channel 2 VOUT
Channel 4 IIN

5.4 Power Up at 37.5V Input – No Load

Power Up at 37.5V Input – 3A Load

Output 2 52V
Channel 1 VIN
Channel 2 VOUT
Channel 4 IIN
6. Switch Node Voltage and Output Ripple Voltage

6.1 35V Input –38V Output 4A load

![Graph](image1)

**Output 1 38V**
Less than 260mV p-p Ripple
Channel 1 VSW
Channel 2 VOUT

6.2 35V Input –52V Output 3A load

![Graph](image2)

**Output 2 52V**
Less than 1.4V p-p Ripple
Channel 1 VSW
Channel 2 VOUT
7. Transient Response

7.1 34.5V Input – 2A to 4A, 100mA/µs, 100 Hz, 50% duty cycle, 38V out.

![Graph](image)

Cursors indicate ~550mV maximum deviation.

**Output 1 38V**

Channel 2 VOUT
Channel 4 IOUT

7.2 37.5V Input – 2A to 4A, 100mA/µs, 100 Hz, 50% duty cycle, 38V out.

![Graph](image)

Cursors indicate ~465mV maximum deviation.

**Output 1 38V**

Channel 2 VOUT
Channel 4 IOUT
7.3 34.5V Input – 1.5A to 3A, 100mA/µs, 100 Hz, 50% duty cycle, 52V out.

Cursors indicate ~1V maximum deviation.

**Output 2 52V**

Channel 2 VOUT
Channel 4 IOUT

7.4 37.5V Input – 1.5A to 3A, 100mA/µs, 100 Hz, 50% duty cycle, 52V out.

Cursors indicate ~825mV maximum deviation.

**Output 2 52V**

Channel 2 VOUT
Channel 4 IOUT
8. Current Limit Tests

This test was conducted by load stepping to an over current condition.

8.1 34.5V input - No Load  34.5V input – 4A Load

Output 1 38V

Channel 2 VOUT
Channel 4 IOUT

8.2 37.5V input - No Load  37.5V input - 4A Load

Output 1 38V

Channel 2 VOUT
Channel 4 IOUT
8.3  34.5V input – No Load

8.4  37.5V input – No Load
9. Short Circuit Tests (I OUT Monitored)

This test was conducted by applying a short to the output.

9.1  34.5V input - No Load  34.5V input – 4A Load

Output 1 38V
Channel 2 VOUT
Channel 4 IOUT

9.2  37.5V input - No Load  37.5V input - 4A Load

Output 1 38V
Channel 2 VOUT
Channel 4 IOUT
9.3  34.5V input – No Load

34.5V input – 3 A Load

Output 2 52V

Channel 2 VOUT
Channel 4 IOUT

9.4  37.5V input – No Load

37.5V input – 3A Load

Output 2 52V

Channel 2 VOUT
Channel 4 IOUT
10. Short Circuit Tests (I IN Monitored)

This test was conducted by applying a short to the output. A differential probe was placed across the current sense resistor and VDS was also measured.

10.1 34.5V input - No Load

34.5V input – 4A Load

Output 1 38V

Channel 2 VDS
Channel 4 IIN

10.2 37.5V input - No Load

37.5V input - 4A Load

Output 1 38V

Channel 2 VDS
Channel 4 IIN
10.3 34.5V input – No Load

Output 2 52V

Channel 2 VDS
Channel 4 IIN

10.4 37.5V input – No Load 37.5V input – 3A Load

Output 2 52V

Channel 2 VDS
Channel 4 IIN
11. Power Up into a Short Circuit

This test was conducted by powering up into a short condition. Latch off.

<table>
<thead>
<tr>
<th>11.1</th>
<th>34.5V input</th>
<th>37.5V input</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Graph 1" /></td>
<td><img src="image2" alt="Graph 2" /></td>
<td></td>
</tr>
</tbody>
</table>

**Output 1 38V**

Channel 2 VOUT
Channel 4 IOUT

<table>
<thead>
<tr>
<th>11.2</th>
<th>34.5V input</th>
<th>37.5V input</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3" alt="Graph 3" /></td>
<td><img src="image4" alt="Graph 4" /></td>
<td></td>
</tr>
</tbody>
</table>

**Output 2 52V**

Channel 2 VOUT
Channel 4 IOUT
12. UVLO into a Short Circuit

Under voltage lock out was toggled to ground to restart into a short circuit. A differential probe was placed across the current sense resistor and VDS was also measured.

<table>
<thead>
<tr>
<th>12.1</th>
<th>34.5V input - 4 Load</th>
<th>37.5V input – 4A Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output 1 38V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Channel 2 VDS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Channel 4 IIN</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>12.2</th>
<th>34.5V input – 3A load</th>
<th>37.5V input – 3 A Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output 2 52V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Channel 2 VDS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Channel 4 IIN</td>
<td></td>
</tr>
</tbody>
</table>
13. Short Circuit Recovery (UVLO)

Under voltage lock out was toggled to ground to restart after short circuit.

13.1 34.5V input - No Load  
34.5V input – 4A Load

13.2 37.5V input - No Load  
37.5V input - 4A Load

Output 1 38V

Channel 2 VOUT
Channel 4 IOUT
13.3 34.5V input – No Load  
34.5V input – 3 A Load  

Output 2 52V  
Channel 2 VOUT  
Channel 4 IOUT  

13.4 37.5V input – No Load  
37.5V input – 3A Load  

Output 2 52V  
Channel 2 VOUT  
Channel 4 IOUT
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that have specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer’s risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.