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This design was tested at 210A peak and 160A steady state output current. For 4 phases that is 52.5A peak per phase. The TPS40428 only allows current fault threshold to be set at 50A. To avoid faults at or near max load, the current sense gain was increased from 500uOhms, the standard for CSD95378B Smart Power to 700uohms to make the TPS40428 think current was actually 30% less and avoid faults being triggered at or near peak loads.

The CSD95378B power stage is rated for up to 90A peak.

The TPS40428 controller current sense input is rated to 600mV max when operated in Smart Power mode. At the 50A threshold with 700uohms setting, the actual peak current will be 70A which is well under the CSD95378B max rating. The voltage on the TPS40428 controller current sense input will be this 70A times 5mV/A or 350mV, well within the 600mV limit.

For applications in which peak electrical current is 150A or less this current sense gain change is not needed. General “best practice” is to set current limit fault threshold at 130 to 150 percent of max application current.

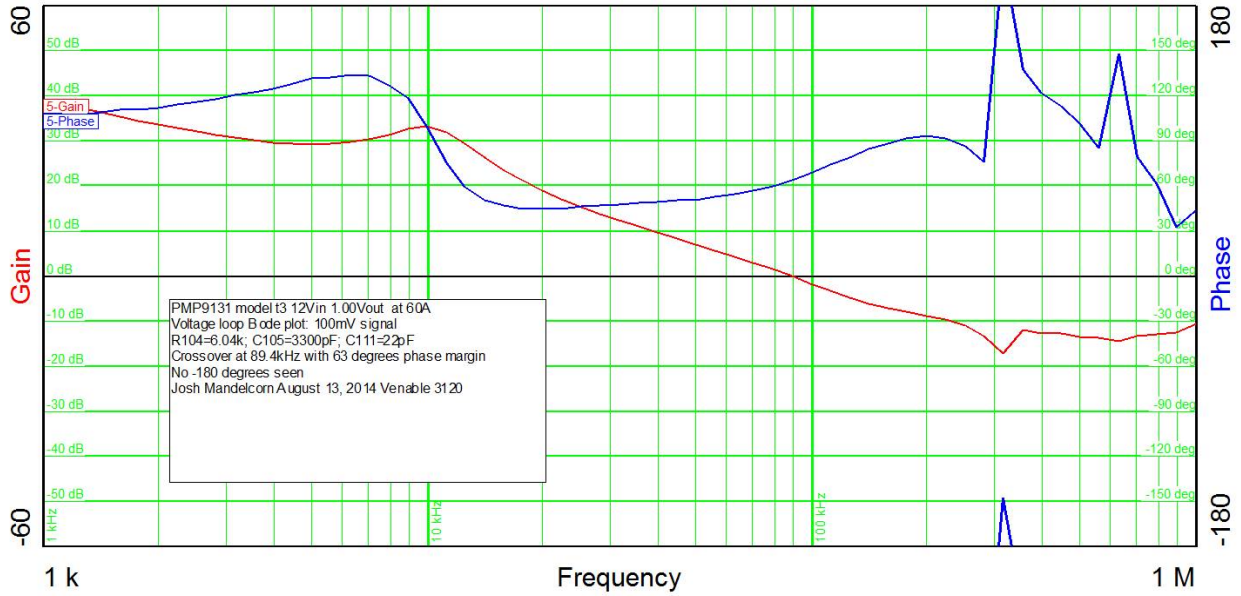
Testing was done on model t1, which was then shipped to customer. Control was finalized afterwards to improve dynamic response, and tests in performance areas that could be affected by control loop were repeated on model t3 here and are shown in this report. They include Bode plot, step load & load dump response, output ripple and start up. Dynamic load tester was not changed. Hence, waveforms from model t1 were used for details of step load / load dump on pages 5 & 6.

Efficiency and Losses: **model t1**: 12Vin, Vout set at 1.0V
Close in Vin & Vout senses, 12V 5" fan to give about 200 LFM or 1 M/S airflow

Vin Volts	Iin A	Vout Volts	Iout A	% Effi ciency	Losses in W
12.06	0.039	off			
12.121	15.646	1.019	160.32	86.1	26.279
12.023	13.385	1.0183	138.84	87.9	19.547
12.05	12.61	1.018	132.04	88.5	17.534
12.035	11.37	1.0175	120.00	89.2	14.738
12.04	9.343	1.016	100.00	90.3	10.890
12.035	7.398	1.015	80.00	91.2	7.835
12.06	5.512	1.014	60.00	91.5	5.635
12.03	3.705	1.0125	40.00	90.9	4.071
12.05	1.900	1.011	20.00	88.3	2.675
12.01	1.027	1.011	10.00	82.0	2.224
12.07	0.178	1.010	0	0.0	2.148

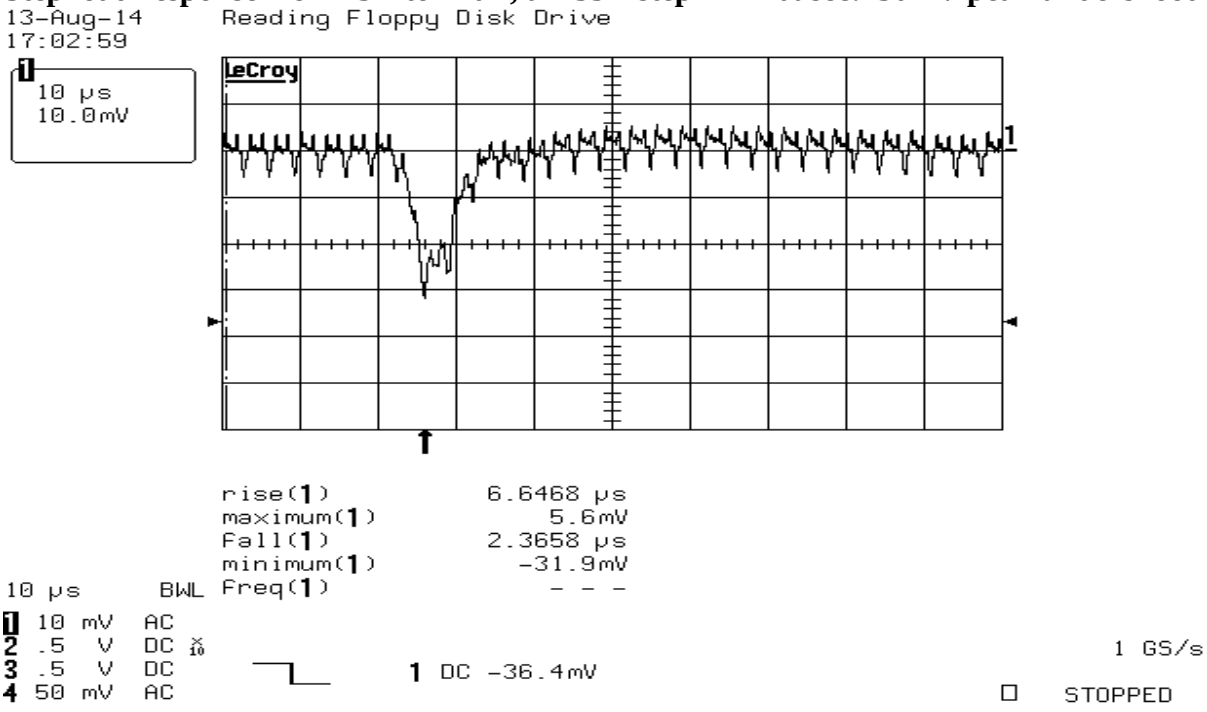
Model t1:
307kHz dropping to 305.5kHz when running at 160A and hot
Current sense changed to 0.7mOhms from 0.5mOhms to allow >50A per phase:

Bode plot of Voltage control loop 12Vin 1.0Vout at 60A: **model t3**

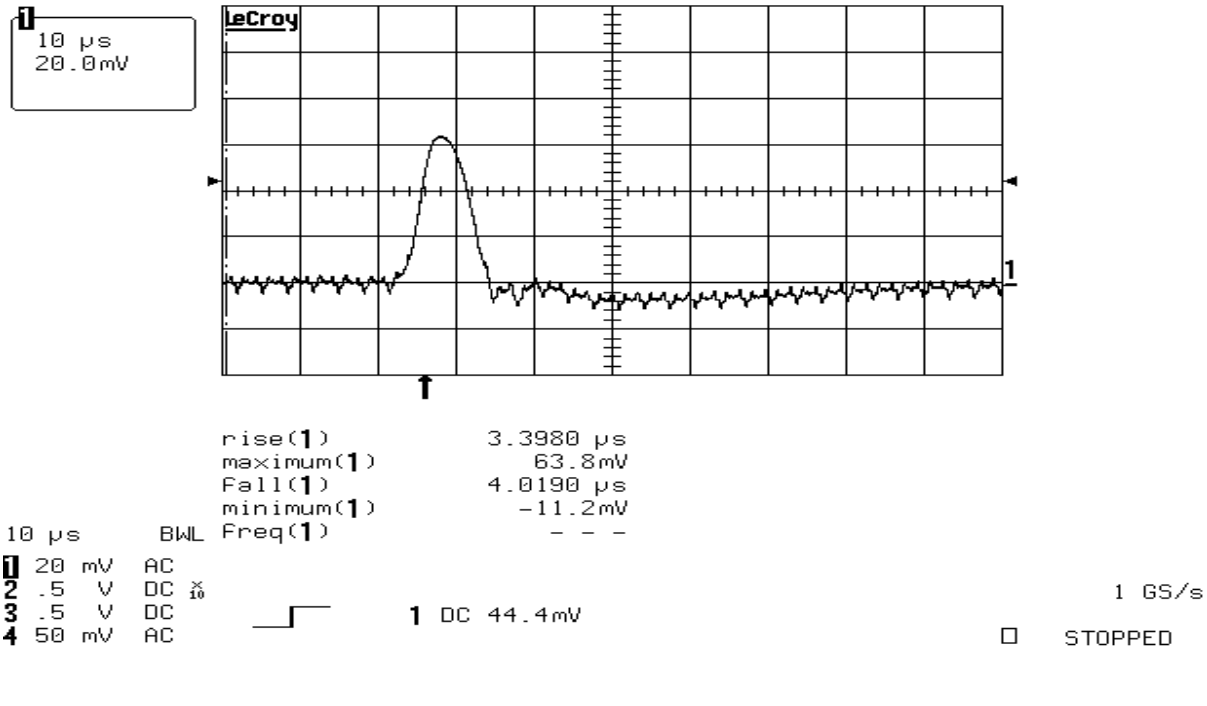


Model t3 with 210nH inductors and loop adjusted to 90kHz crossover: 1.0Vout
Output caps: 10x 470uF 9mOhms plus 8x 100uF 6.3V 1210 sized ceramics
The 75A static load is an external load bank, the 135A dynamic load is on the board. See page 4 of the schematic.

Step load response from 75A to 210A, a 135A step in ~ 10usec: 30mV peak undershoot

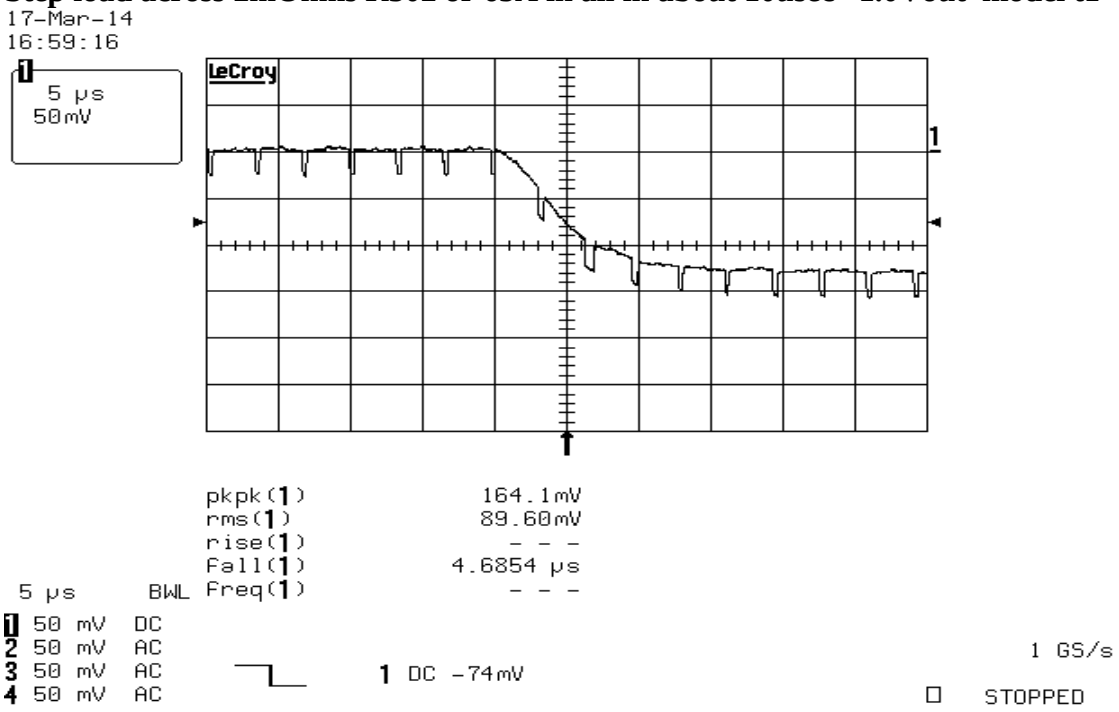


Load dump from 210A to 75A 12.0Vin; a 135A Dump in ~4usec 60mV overshoot



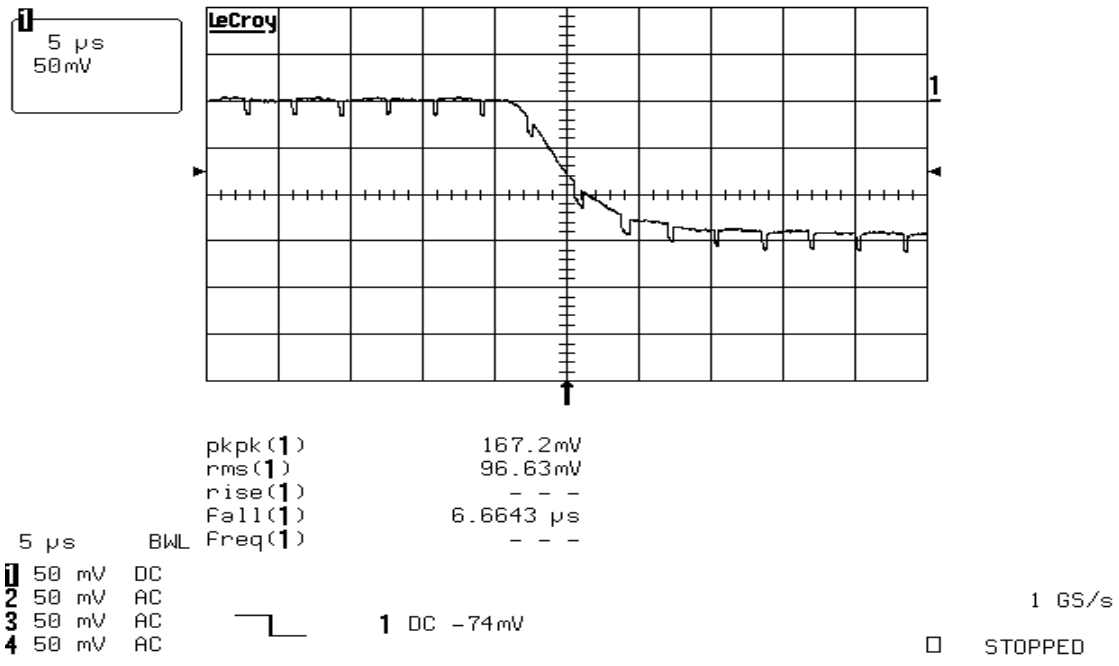
Waveforms across resistors in dynamic load bank used to calculate step load current and speed: There are two resistor paths from Vout; R302 and R301. Hence, the total load step is the sum of both. Here scope ground on Vout side of resistor.

Step load across 2mOhms R302 or 65A in all in about 10usec 1.0Vout model t1



q

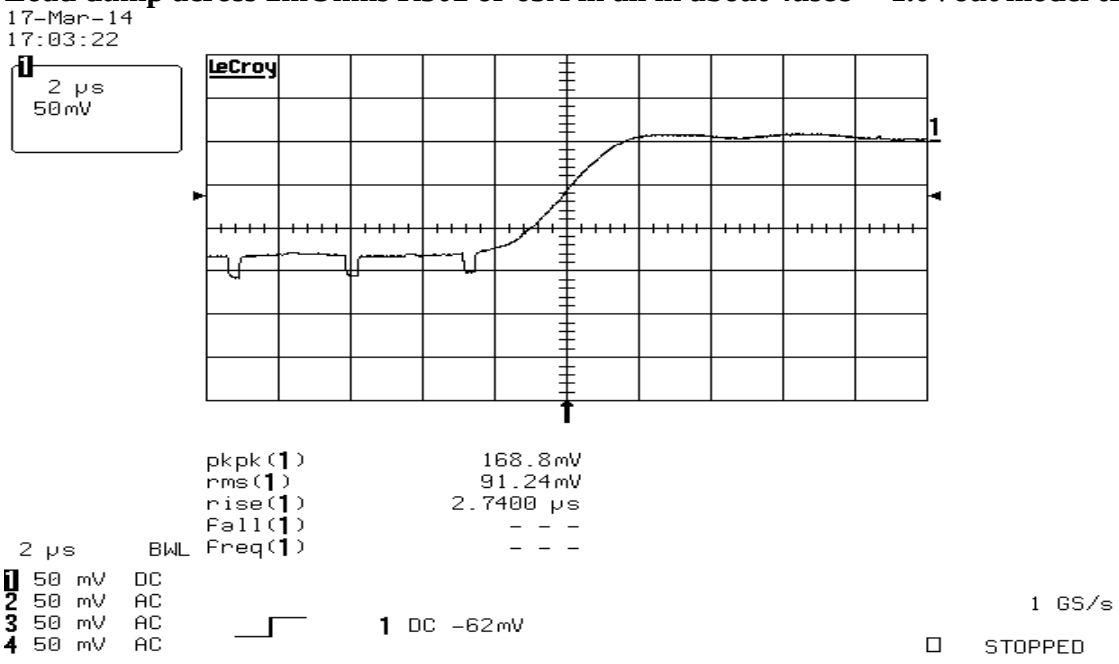
Step load across 2mOhms R301 or 70A in all in about 10usec



Load strings are in parallel driven by same FET: Hence, 135A in ~10usec

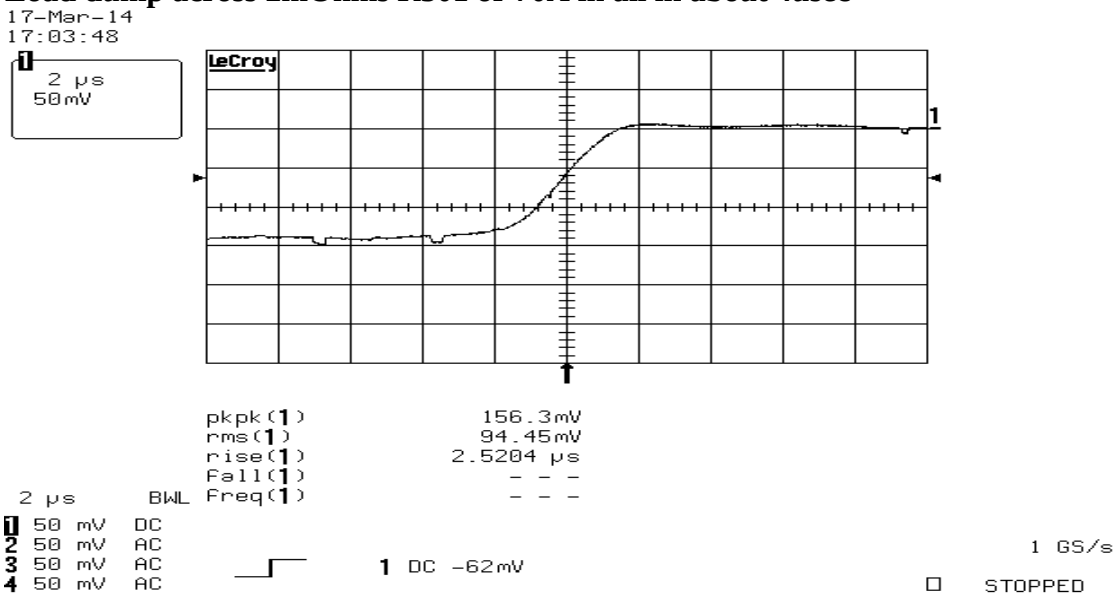
Waveforms across resistors in dynamic load bank used to calculate load dump current and speed: There are two resistor paths from Vout; R302 and R301. Hence, the total load dump is the sum of both. Here scope ground on Vout side of resistor.

Load dump across 2mOhms R302 or 65A in all in about 4usec 1.0Vout model t1



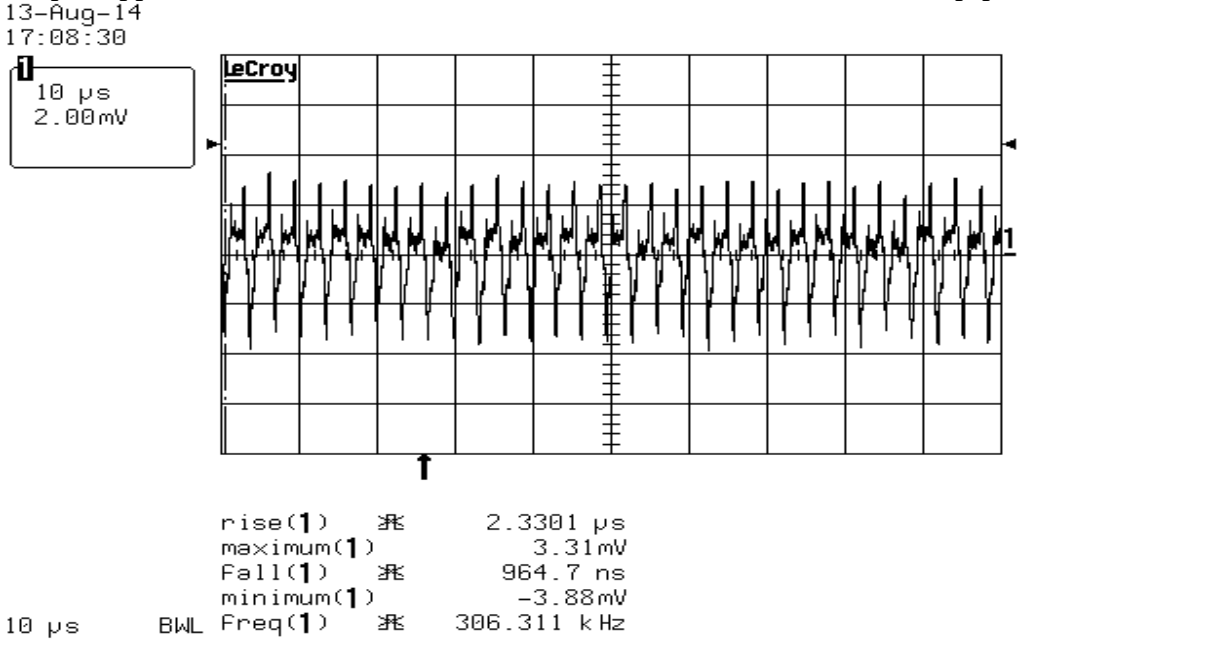
q

Load dump across 2mOhms R301 or 70A in all in about 4usec



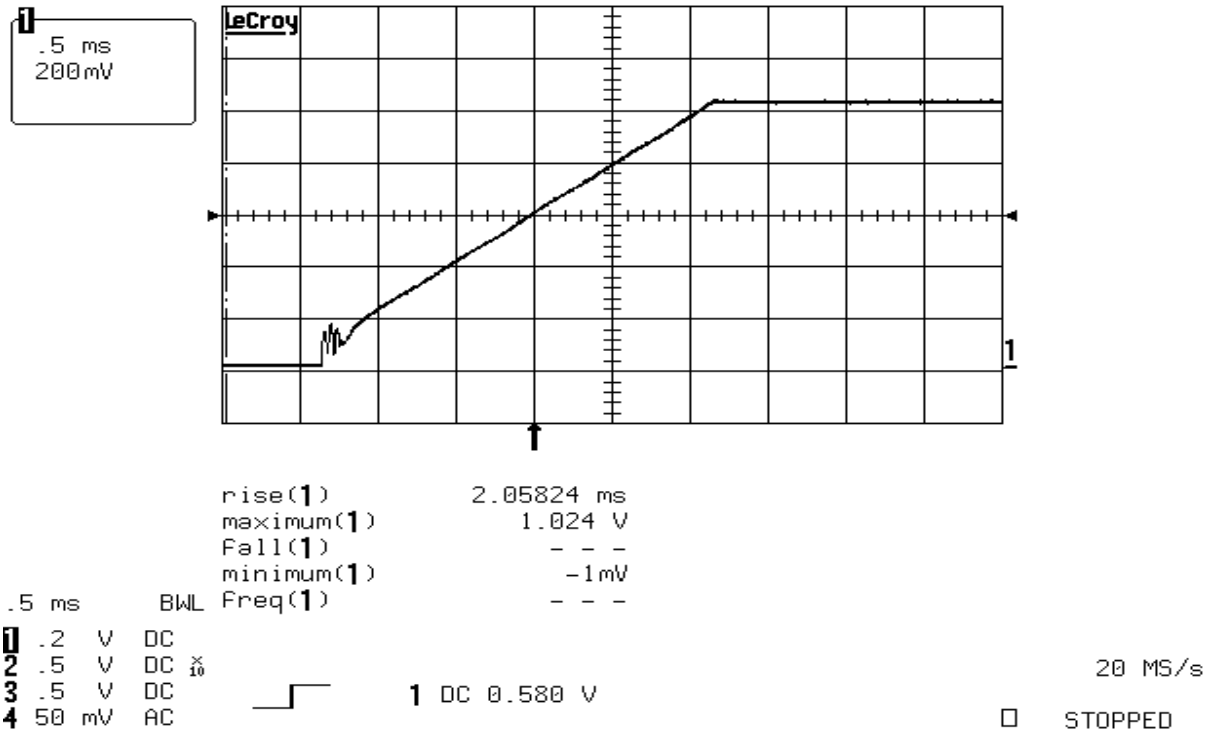
Load strings are in parallel driven by same FET: Hence, 135A in ~4usec

Output ripple at 12.0Vin and 139A off 1.0Vout at C128: **model t3** 7.2mV p-p 20MHz BW

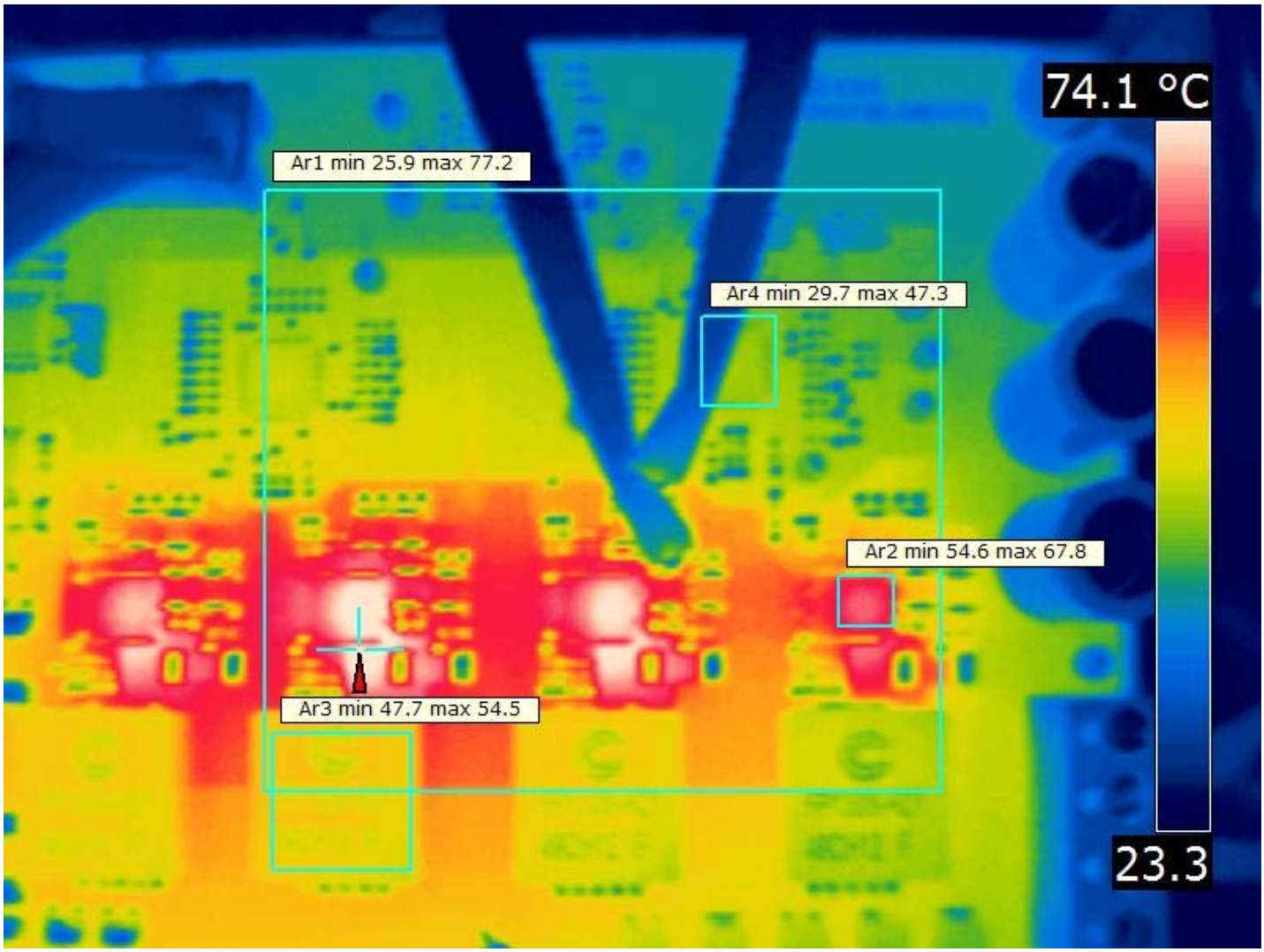


Qq

Start up with no pre bias: **model t3** 1.0Vout

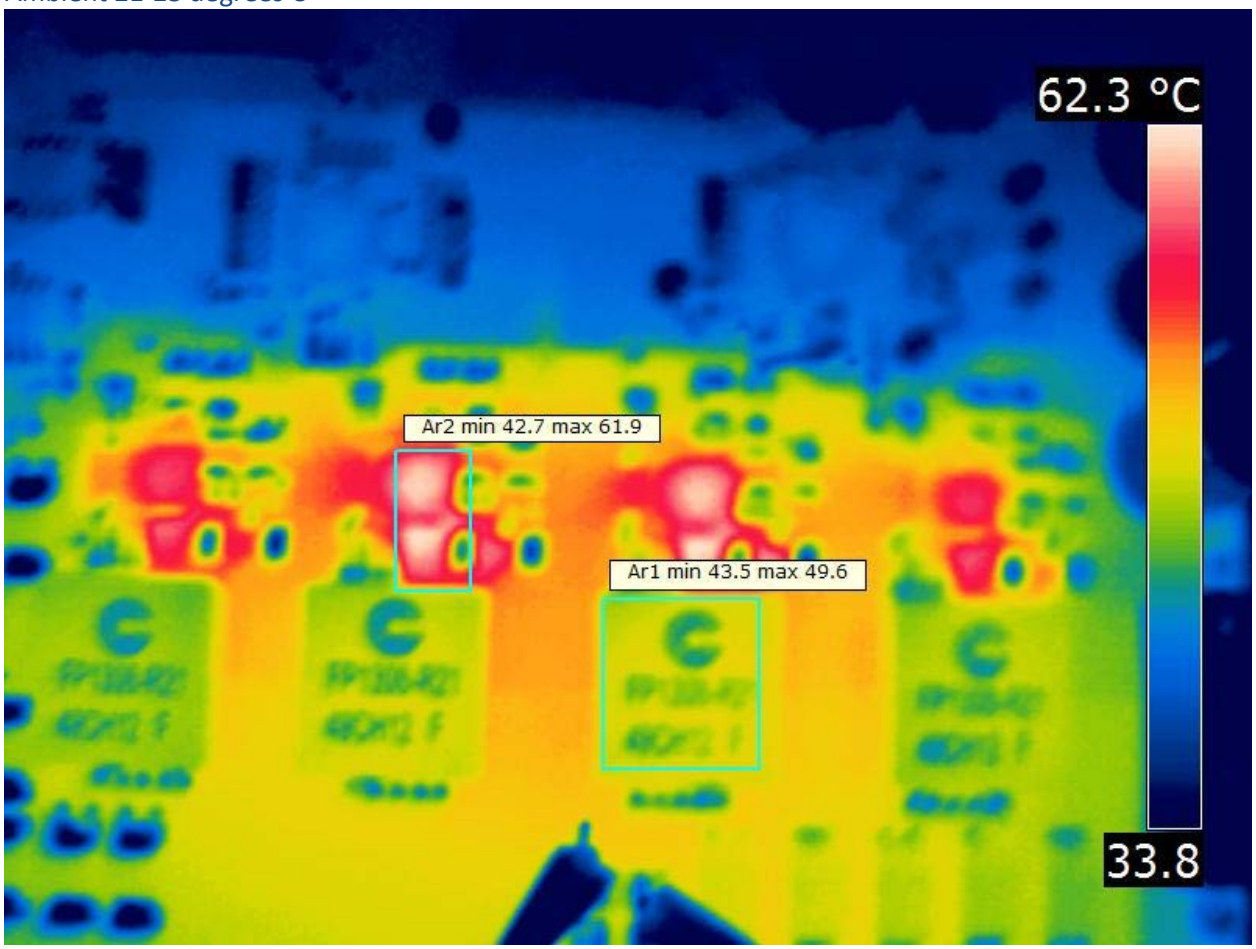


Thermal Image:
PMP9131 1.0V **160A** off 12.1Vin 305.5kHz / phase **model t1**
Strong 5" fan 12Vin 6" away on right side of model: 200 to 400 LFM estimated
Ambient ~22 deg. C; hotspot PWB path from third Q
Q Surfaces from fan & U102: 68; 74.5; 76.4; 71.7
Inductor tops 49, 53, 55, 54
Snubbers: 60, 69, 71, 68
Controllers TPS40428s 47 & 50



Qq

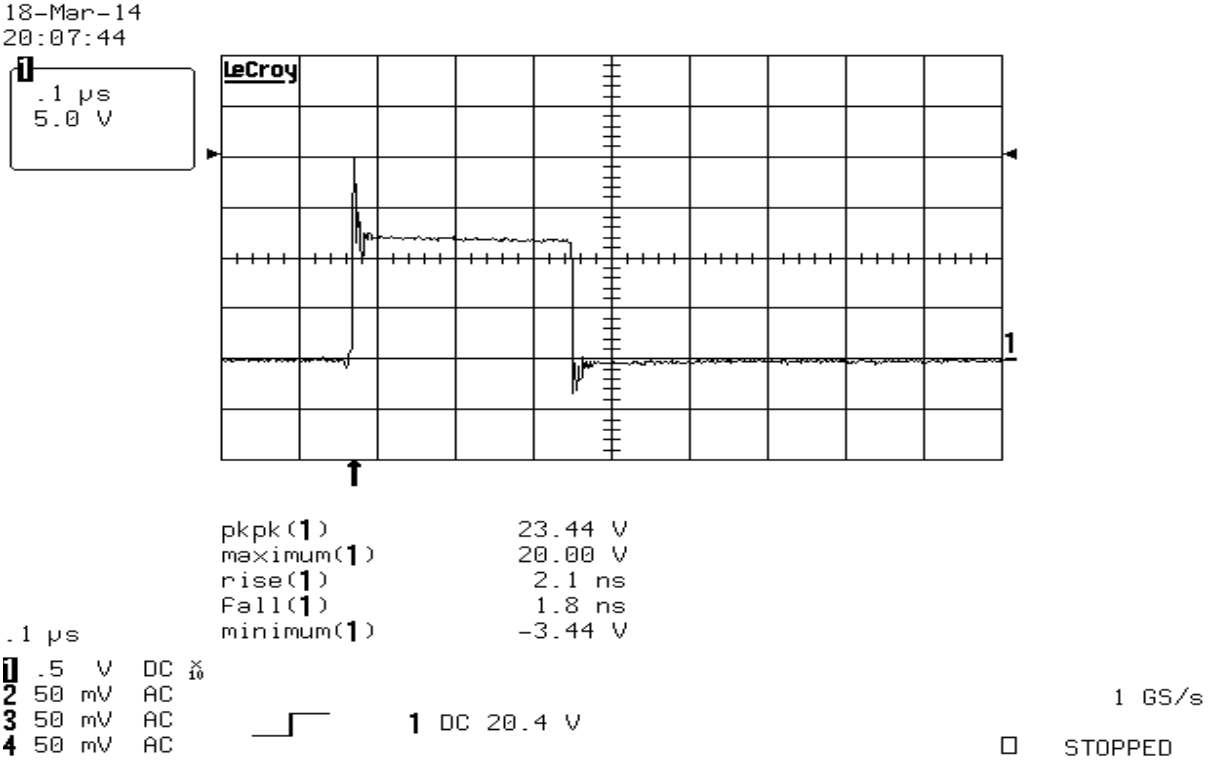
PMP9131 12Vin 1.0vout **132A** ~200 LFM airflow **model t1:** Lower current than previous page, but also slower fan speed to approximate 200 LFM. Fan is also to the right of model.
17.5W on PCB / assy
FETs & nearby PCB 58 to 62 degrees C
Inductor tops 48 to 50
Ambient 21-23 degrees C



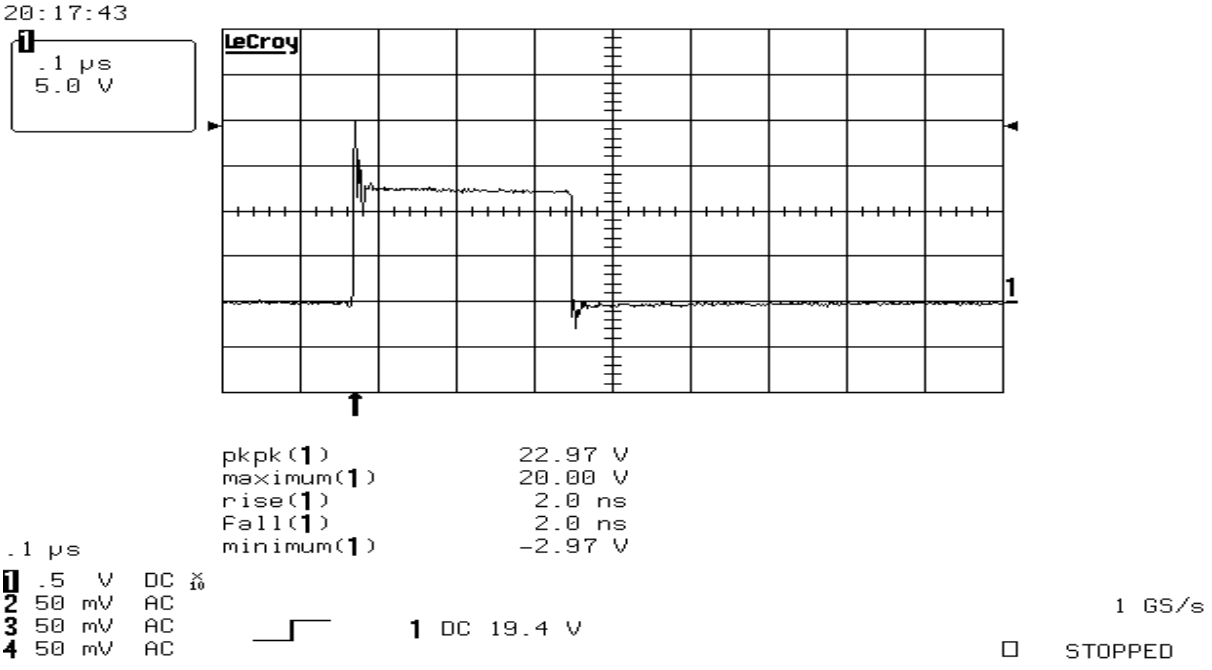
Qq

Major waveforms: **model t1**

12vin load stepped from 45A to 180A & back. Scope trigger increased slowly to capture highest peak of 20.0V: channel 2 shown (U103 pin 6 VSW). Same 20V seen on channels 1 & 3. Channel 4 max was 19V.



12Vin: load stepped from 75Ato 210A & back. Scope trigger increased slowly to capture highest peak of 20.0V: channel 1 shown (U102 pin 6 VSW). Same 20V seen on channels 2 & 3. Channel 4 max was 19V.



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