TI Designs
40 V to 400 V Uni-directional Current/Voltage/Power Monitoring Reference Design

TEXAS INSTRUMENTS

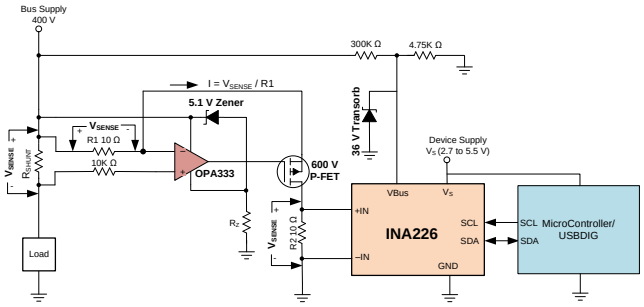
Design Overview

This verified design can accurately measure current, voltage and power on a bus as high as 400 V using an I2C- or SMBUS-compatible interface. This design is targeted towards industrial applications where there is a need to measure system current accurately with bus voltages greater than 40 Volts such as Solar inverters, HEV/EV systems and Source generation for AC/DC electronic loads and power sources. This is a low cost non-isolated solution for high voltage current monitoring. It uses INA226 and OPA333 along with a 600-V P-FET transistor.

Design Resources

TIDA-00528	Design Folder
INA226	Product Folder
OPA333	Product Folder
INA226EVM	Tools Folder

Block Diagram



Design Features

- Supports Bus Voltages between 40 Volts and 400 Volts
- Current, Voltage and Power Monitor
- I2C-/SMBUS-compatible interface
- High accuracy
- Low cost

Featured Applications

- > 40 V common mode current sensing
- Telecom
- Wireless infrastructure
- Servers
- Test and Measurements
- Smart grid and energy

Board Image

CAUTION: This PCB operates at high voltages and currents which can result in hazardous electrical shock. Please make sure you understand and follow all necessary safety precautions prior to building and operating.

1 Key System Specifications

PARAMETER	SPECIFICATIONS and FEATURES	DETAILS
Operating Bus Voltage range	40 V to 400 V	Section 2
Accuracy at Full scale	<1%	Section 8.1
Operating temperature	+25°C	
Wired Interface from Current Shunt to Application Processor	I^2C Compatible	Section 2
Form Factor	67.8 mm x 93 mm square PCB	Section 5.1

Figure 1: Key System Specification of 40-400V Current Sense Monitor Reference Design

2 System Description

Current shunt monitors sense differential voltages developed across a sense resistor (V_{SENSE}) to monitor system load currents. Sensing load currents at the bus (High-side) offers the benefit of sensing load shorts to ground vs. sensing on the low-side. Often sensing load currents at bus voltages greater than 40 volts is needed. The INA226 from Texas Instruments cannot exceed a bus supply voltage of 36V. To that end, this design explores one possible solution for achieving current sensing at bus voltages as high as 400 V without significant loss in accuracy.

This TI design demonstrates a simple, non-isolated technique using a precision opamp and a high voltage P-FET to extend the common mode voltage of a current sense amplifier up to 400 V. With minor component changes this design can be optimized for any voltage ranging from 40 to 400 Volts.

3 Block Diagram

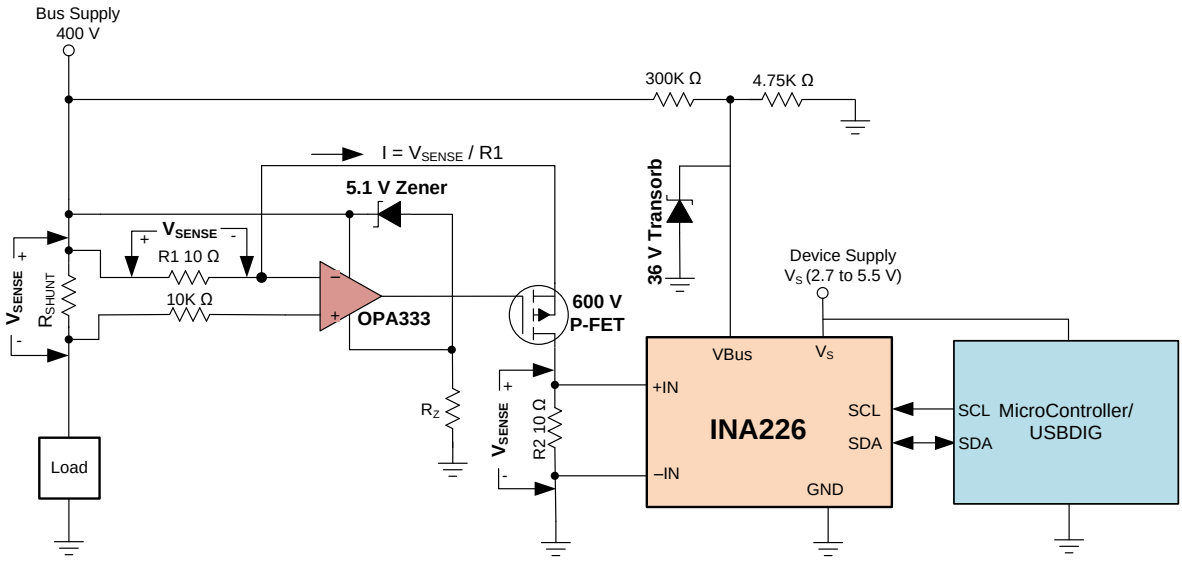


Figure 2: 400 V Current/Voltage/Power Monitor Block Diagram

3.1 Highlighted Products

400V Unidirectional Current/Voltage/Power Monitor TI design feature the following devices:

- INA226
  - High-Side or Low-Side, Bi-Directional Current and Power Monitor with I2C Compatible Interface
- OPA333
  - 1.8-V, microPower, CMOS, Zero-Drift Series High Voltage Operational Amplifier

For more information on each of these devices, see the respective product folders at www.ti.com

3.1.1 INA226

3.1.1.1 INA226 Description

The INA226 is a current shunt and power monitor with an I2C™- or SMBUS-compatible interface. The device monitors both a shunt voltage drop and bus voltage. Programmable calibration value, conversion times and averaging, combined with an internal multiplier enable direct readouts of current in Amperes and power in Watts.

The INA226 senses current on common-mode bus voltages that can vary from 0 V to 36 V, independent of the supply voltage. The device operates from a single 2.7-V to 5.5-V supply, drawing a

typical of 330 µA of supply current. The device is specified over the operating temperature range between –40°C and 125°C and features up to 16 programmable addresses on the I2C-compatible interface.

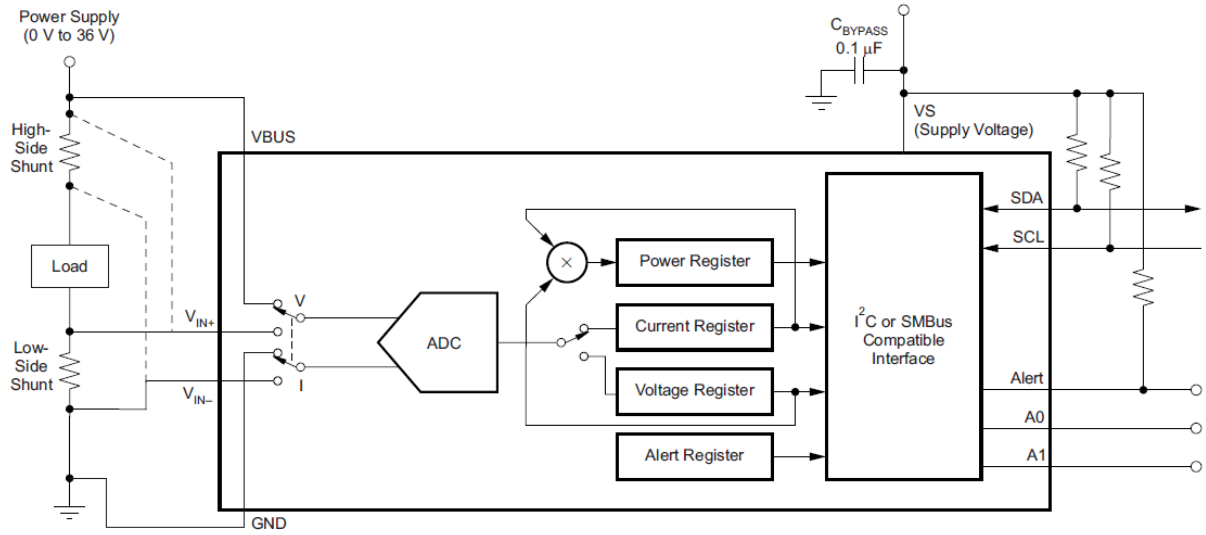


Figure 3: INA226 Block Diagram

3.1.1.2 INA226 Features

- Senses Bus Voltages From 0 V to 36 V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power supply voltage.
- High Accuracy:
  - 0.1% Gain Error (Max)
  - 10 µV Offset (Max)
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- 10-Pin, DGS (VSSOP) Package

3.1.2 OPA333

3.1.2.1 OPA333 Description

The OPA333 series of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 µV, max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V) can be used. These devices are optimized for low voltage, single-supply operation.
The OPA333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity. The OPA333 (single version) is available in the SC70-5, SOT23-5, and SO-8 packages. The OPA2333 (dual version) is offered in DFN-8 (3 mm × 3 mm), MSOP-8, and SO-8 packages. All versions are specified for operation from –40°C to +125°C.

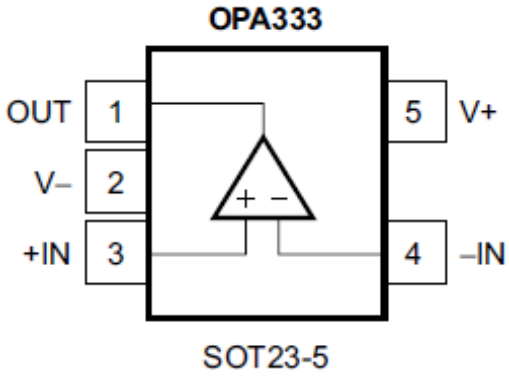


Figure 4 : OPA333 SOT23-5 Pin out

3.1.2.2 OPA333 Features

- Low Offset Voltage: 10 µV (max)
- Zero Drift: 0.05 µV/°C (max)
- 0.01-Hz to 10-Hz Noise: 1.1 µVPP
- Quiescent Current: 17 µA
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- microSize Packages: SC70 and SOT23

4 System Design Theory

Shown in Figure 2 is the precision, rail-to-rail opamp OPA333 used to mirror the sense voltage across the shunt resistor on to a precision resistor R1. OPA333 is floated up to 400 V using a 5.1 V zener diode between its supply pins. The opamp drives the gate of the 600 V P-FET in a current follower configuration. A low leakage P-FET is chosen to obtain accurate readings even at the low end of the measurement. The voltage across R1 sets the drain current of the FET and by matching the resistor R2 in the drain of the FET to be equal to R1, V_{SENSE} voltage is developed across R2 (V_{R2}). Inputs of the current monitor INA226 are connected across R2 for current sensing. Hence the current monitor does not need the high common mode capability as it will only see common mode voltages around V_{SENSE} which is usually less than 100mV. INA226 was chosen for current, voltage and power monitoring as it is a high accuracy current/voltage/power monitor with an I2C interface.

The INA226 can also sense bus voltages less than 36 V. Since the bus voltage employed here is 400 V, a divider is employed to scale down the high voltage bus to a voltage within the common mode range of INA226. In this case a ratio of 64 is chosen and hence the bus voltage LSB can be scaled accordingly to obtain the actual bus voltage reading. In this case the a modified LSB of 80 mV could be used. Precision resistors are chosen for the divider to maintain accuracy of the bus measurement.

4.1 Sizing the Zener Resistor (R_Z)

A 5.1 V Zener is used in this design to float the OPAMP OPA333 to the high voltage rail so that the transistor gate can be driven as shown in Figure 2. Zener Resistor R_Z needs to be sized correctly for proper biasing of the Zener and OPAMP.

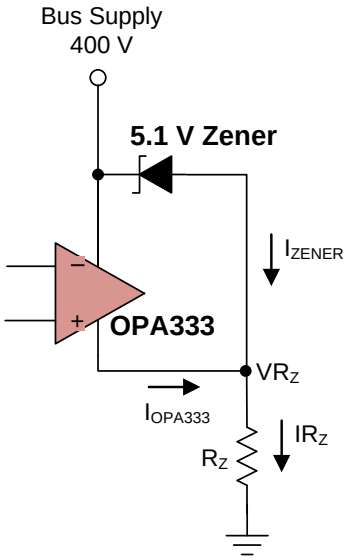


Figure 5: Zener Resistor

For this TI design MMSZ4689T1 Zener diode was used for its low nominal current of 50 µA. OPA333 has a maximum quiescent current of 25 µA. The Zener resistor needs to accommodate these currents for proper biasing of the Zener and the opamp.

$$R_Z \leq \frac{Bus\ Supply - V_Z}{I_{ZENER} + I_{OPA333}} = \frac{VR_Z}{I_{ZENER} + I_{OPA333}} = \frac{400\ V - 5.1\ V}{50\ uA + 25\ uA} = 5.26\ M\Omega \quad (1)$$

For this design we choose a R_Z of 2.4 MΩ so that the design could also work at lower common mode voltages. The R_Z resistor was split into 2 series resistors of 1.2 MΩ to split the 400 V drop between 2 resistors and to ease the power dissipation requirement for each of this resistor. Wattage requirement of each resistor is calculated as below:

$$PowerRating \geq \frac{V^2}{R} = \frac{(400\ V - 5.1\ V\ )/2)^2}{1.2\ M\Omega} = 32.48\ mW \quad (2)$$

Choosing a low power Zener and OPAMP helps with requiring low wattage resistors, hence reduction in space and cost.

4.2 Bus Voltage Divider Resistors

The INA226 device can monitor bus voltages upto 36 V. In this case the Bus voltage cannot be connected directly to the device VBUS pin. A divider is employed with R3 and R4 to scale the voltage down, see Figure 6 and Equation (3).

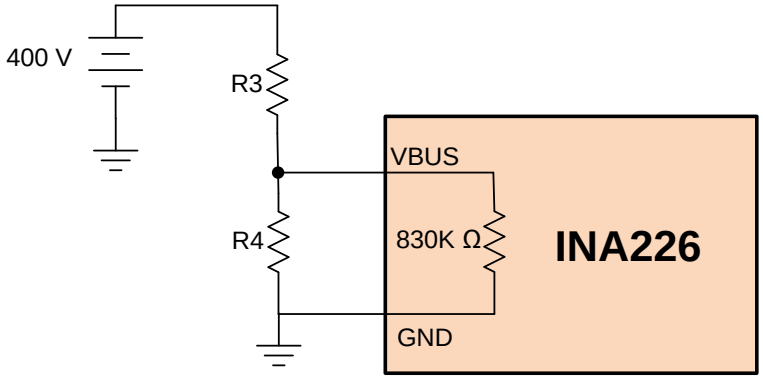


Figure 6 : Bus Voltage Divider

$$VBUS = 400 * (\frac{R4}{R3 + R4}) \quad (3)$$

A binary ratio of 64 was used for this TI design, see Equation (4)

$$\frac{R4}{R3 + R4} = \frac{1}{64} \quad (4)$$

which simplifies to

$$\frac{R3}{R4} = 63 \quad (5)$$

$$Lets\ choose\ R3 = 300K\ \Omega$$

Then $R4 = 4.76K\ \Omega$ (closest resistor available = 4.75K Ω)

Therefore,

$$VBUS = \frac{400}{64} = 6.25\ V \quad (6)$$

Another important consideration here is that INA226 has an input impedance of about 830K Ω between VBUS pin and it's ground pin. Therefore R4 should be significantly smaller than this impedance to be able to divide the voltage down accurately.
The 300K Ω resistor was split into two 150K Ω resistors to reduce the voltage dropped across each of the resistor to be less than 200 Volts each. Please see schematic in Section 9.1.

The wattage requirement of the 150K ohm R3 resistors can be calculated as:

$$Power\ Rating \geq \frac{V^2}{R} = \frac{(400\ V - 6.25\ V\ )/2)^2}{150\ K\Omega} = 0.258\ W \quad (7)$$

4.3 Transistor Selection

The P-FET type transistor (IXTT16P60P) chosen for this design was for its high voltage capability and low source-to-gate specification to support using a precision, low voltage OPAMP for the drive. Another transistor that meets the bus requirements of the application may be used in its place given that it satisfies the system requirements. The transistor drain-to-source voltage needs to be rated greater-than or equal-to the high voltage rail.

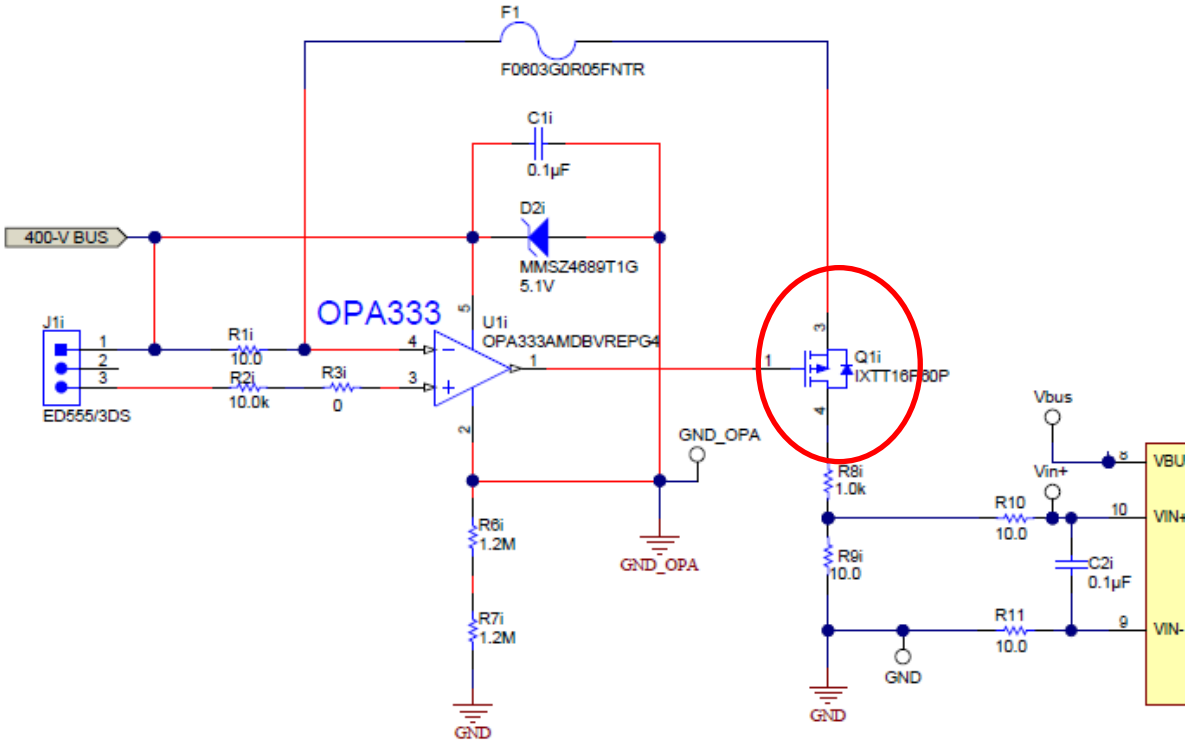


Figure 7: P-FET Transistor for isolating the high voltage bus

4.4 Transistor Power dissipation

At high voltages, even with low currents there can be significant power dissipation. The P-FET transistor in the design is one of the components with the largest power dissipation. Heat/power dissipation methods need to be employed if operating at high power for a long duration of time. Calculation of power dissipation across the transistor at a bus voltage of 400 V yields:

$$Power\ Dissipation = VBUS * I = 400 * I_{\mathrm{PFET}} = 400\ V * 8\ mA = 3.2\ W \quad (8)$$

where (see Figure 2)

$$I_{\mathrm{PFET}} = \frac{V_{\mathrm{SENSE}}}{R1} = \frac{80\ mV}{10\ \Omega} = 8\ mA \quad (9)$$

If operating at these power levels, it is recommended to refer to the transistor power rating curve and employ proper heat dissipation/cooling techniques to avoid damage to the transistor.
A 50mA fuse (F1) is placed in the feedback path of the OPA333 and a 1K (R8) resistor in series with the transistor drain terminal in order to avoid damage to rest of the board and the INA226 in the event that the transistor is damaged and a short occurs between the source and the drain of the transistor.

4.5 Error Sources

The INA226 is a high accuracy Current and Power Monitor. Its contribution to error in this design is minimal. The OPA333 used in this reference design is a precision operational amplifier whose contribution to the total error also remains minimal. The tolerance of resistors R1, R9 and the shunt resistor can contribute significantly if not chosen according to the system accuracy requirements. Transistor leakage at higher voltage can also contribute to the accuracy of the overall design.

4.6 Optional INA226 Input Filter

Place holder for an optional filter consisting of resistors R10, R11 and capacitor C2 is also available with this reference design. Please see Figure 8. Refer to the INA226 datasheet for details on choosing an input filter.

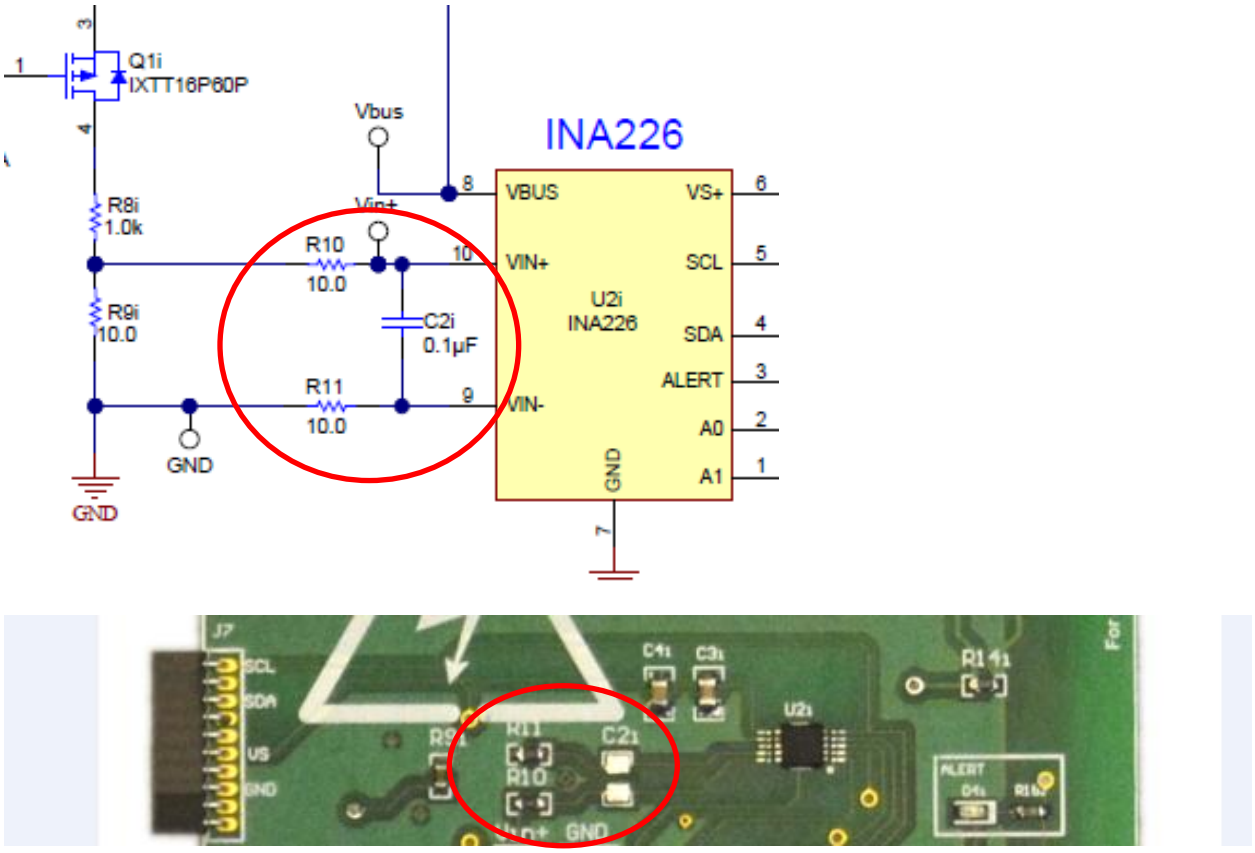


Figure 8: 400 V Current Sense Monitor PCB

5 Getting Started Hardware

5.1 Hardware Overview

The 400 V Current Shunt Monitor PCB is as shown in Figure 9. This PCB is 67.8 mm X 93 mm and is just a 2 layer board. All components are located on the top side of the PCB. The board is divided into high voltage side (upper half, circled in red), where all the high voltage traces and components are routed, and a low voltage side (lower half, circled in blue), where all the 3.3-V to 5-V supply, ground traces and components are routed.

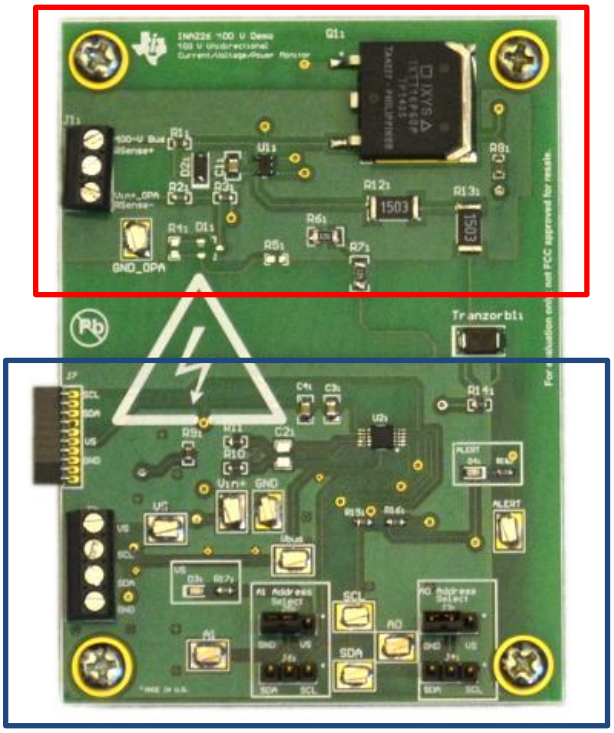


Figure 9: 400 V Current Sense Monitor PCB

5.2 Powering the Board

The PCB includes a terminal block connector J1 for the bus and the shunt connections on the upper left side of the board (see PCB board in Figure 9). Connect the high voltage source (less than 400 V) to R_{SENSE+} pin and the shunt resistor across R_{SENSE+} and R_{SENSE-}. R_{SENSE-} pin is then connected to the load. Please follow all high voltage safety precautions during testing.

Before powering up the INA226 device, make sure that the A0 and A1 adress pins are tied either to GND, VS, SCL or SDA using the jumpers as seen in Figure 9. The INA226 device on the board could be powered up using an external 3.3-V or 5-V supply using terminal block connector J2. Clock and data line connections are also brought out on to the connector J2. Alternatively for evaluation purposes, SM-USB-DIG platform along with INA226EVM software could be used to power the device and to communicate with the device. Figure 10 shows the SM-USB-DIG and the USB extender cable that comes with the INA226EVM. Figure 11 shows the INA226EVM software interface screen. Please refer to INA226EVM tools folder for details on the SM-USB-DIG platform and the EVM software.

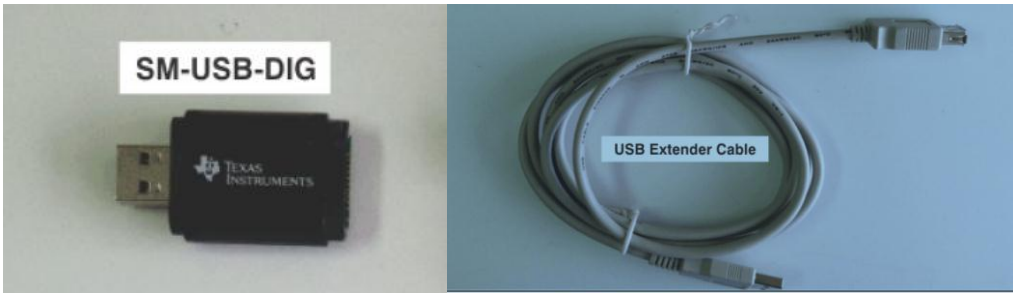


Figure 10: INA226EVM Accessories used for this TI Design

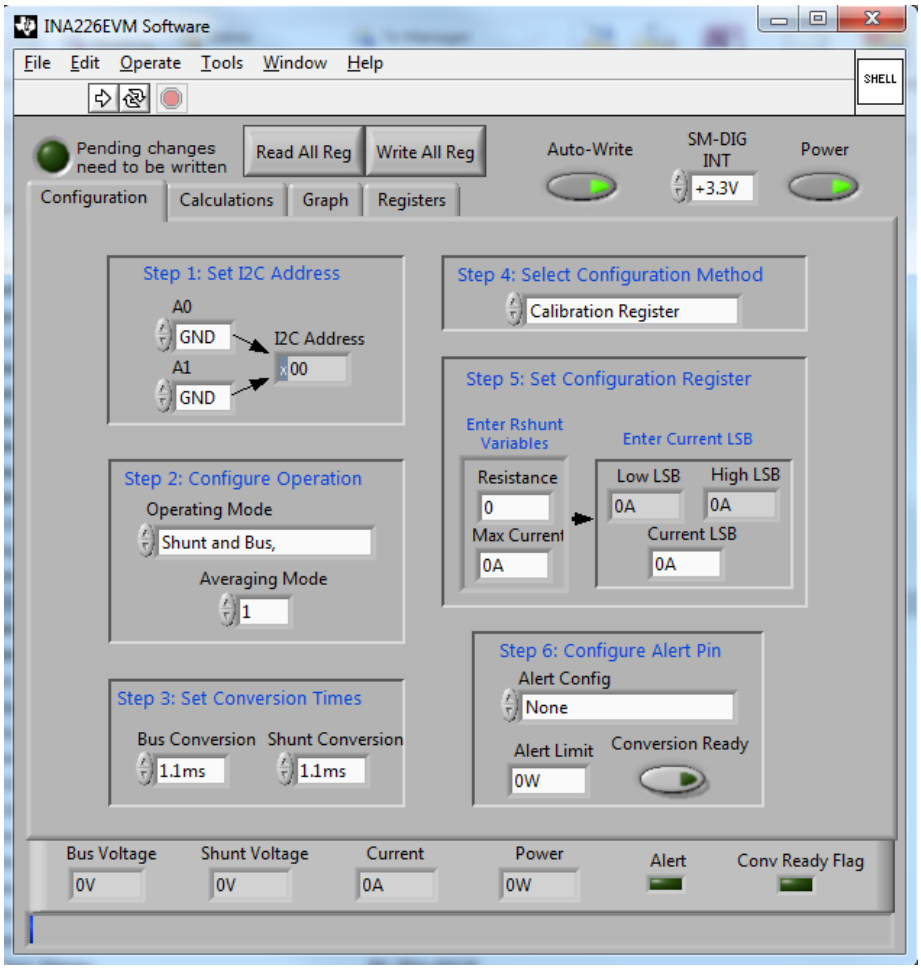


Figure 11: INA226EVM software interface

5.3 Cautions and Warnings

WARNING:
Voltages of 400V can be deadly. Proceed with maximum caution and never handle the device alone.

6 Getting Started Firmware

6.1 TI Design Evaluation Software

INA226 EVM software was used to power and communicate with the INA226 device on the TI design PCB using the SM-USB-DIG interface. Please refer to INA226EVM tools folder for details.

7 Test Setup

Figure 12 shows the test setup for this TI reference design to communicate with the on board INA226.

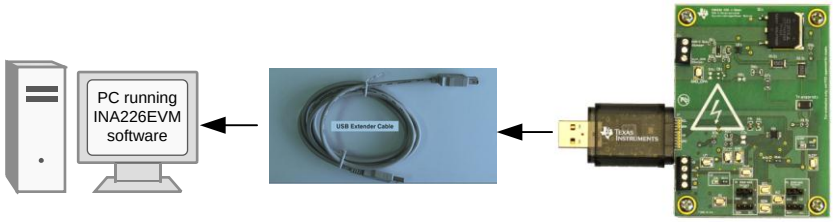


Figure 12: 400 V Current Sense reference design test setup

400 V was generated using the Glassman LVP 600-1.7 as shown in Figure 13. The differential voltage was generated using a battery setup with potentiometer to simulate different load current conditions.

Figure 13: High voltage power supply used for the testing TI design

8 Test Data

8.1 Calculating the accuracy of the load current measurement

Using the test setup described in Section 7, input differential voltage was swept from 1 mV to 80 mV and the output of the INA226 device was recorded at 400 V bus (or common mode (CM)) voltage. Relative output error was calculated using Equation (10). The results are plotted in Figure 14 and the data is tabulated in Table 1. We can see that it maintains good accuracy throughout the range of the INA226 input. (Note that INA226 maximum positive input voltage is +82.92 mV).

$$Relative\ Output\ Error(\%) = \frac{V_{\text{SENSE}} - INA226\ Shunt\ Voltage\ register\ reading}{V_{\text{SENSE}}} * 100 \quad \textbf{(10)}$$

Table 1: Relative Output Error for a range of Input sense voltage

V_{SENSE} (mV)	Equivalent load current for 10 mohm shunt resistor (A)	INA226 Shunt Voltage register reading (mV)	Relative Output Error (%)
1.2500	0.1250	1.2080	3.3600
5.0450	0.5045	4.9780	1.3280
9.9240	0.9924	9.8280	0.9674
14.9920	1.4992	14.8500	0.9472
19.9470	1.9947	19.7800	0.8372
25.5640	2.5564	25.5000	0.2504
30.0316	3.0032	30.0000	0.1054
35.0000	3.5000	34.9000	0.2857
40.0150	4.0015	39.8600	0.3874
45.1110	4.5111	44.9500	0.3569
49.9660	4.9966	49.9000	0.1321
55.6620	5.5662	55.6500	0.0216
60.0220	6.0022	60.0000	0.0367
64.9650	6.4965	64.9500	0.0231
70.0229	7.0023	70.0600	0.0530
75.5940	7.5594	75.5600	0.0450
80.6500	8.0650	80.7100	0.0744

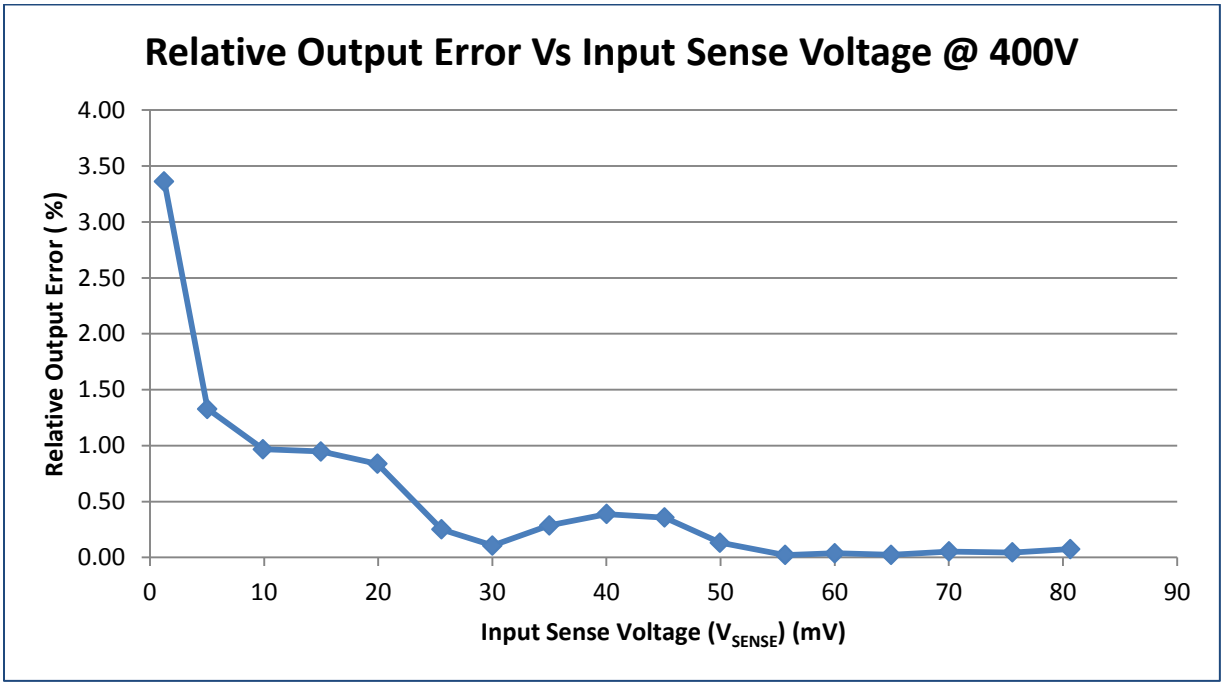


Figure 14: Relative Output Error vs Input sense voltage

8.2 Sweeping the Common Mode/Bus Voltage

Using a load condition generating 45 mV differential voltage at the input, the common mode/bus voltage was swept and the INA226 shunt voltage register reading was recorded. Table 2 and Figure 15 show the relative output error percentage calculation for each of the common mode voltage step. Please note that the zener resistor (R_Z) used on the board may not be optimal to operate the device at lower voltages. Please refer to the Section 4.1 for sizing information.

Table 2: Relative Output Error for a range of Bus Supply Voltage

Bus Supply (V)	VSENSE (mV)	INA226 Shunt Voltage register reading (mV)	Relative Output Error (%)
400	45.1110	44.9500	0.3569
350	45.1070	44.8500	0.5698
300	45.1030	44.3400	1.6917
250	45.1000	44.0200	2.3947
200	45.0980	43.4400	3.6764
150	45.0980	43.0800	4.4747
100	45.0980	43.2800	4.0312
50	45.0980	44.1100	2.1908

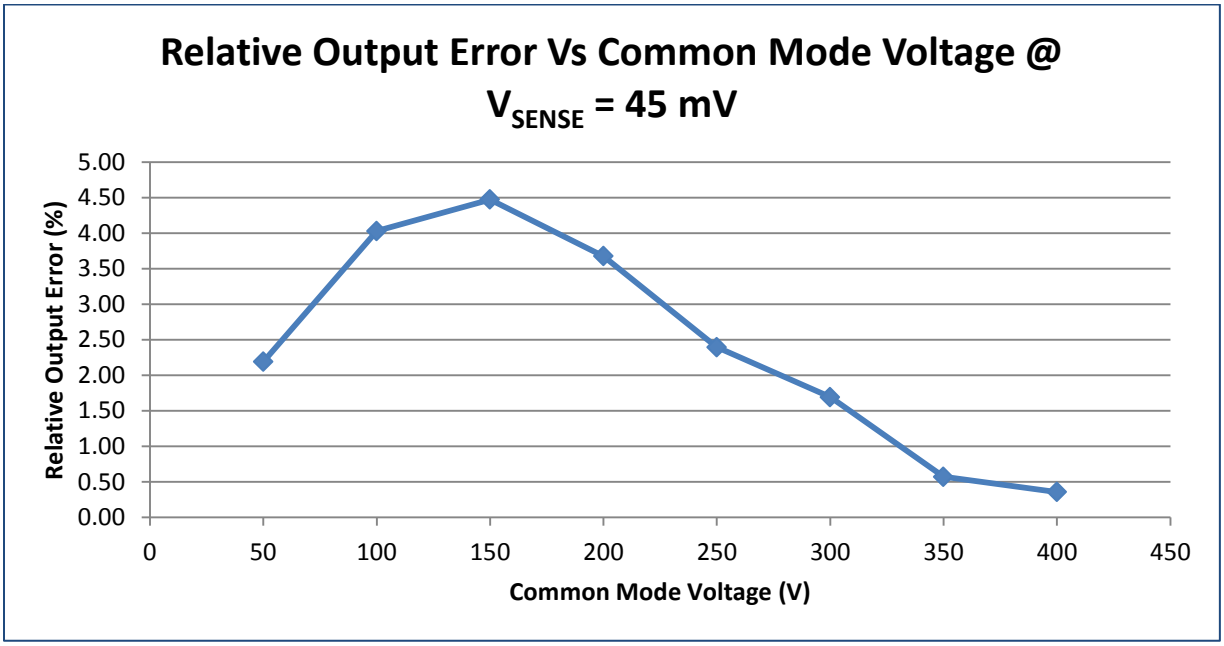


Figure 15: Relative Output Error vs Bus Supply/Common mode voltage

8.3 Bus Voltage measurements

In this reference design a binary ratio of 64 is used to scale the high voltage bus down to an acceptable common mode range of INA226. Table 3 and Figure 16 for the measurement results for a sweep of the bus supply voltage. Use INA226 bus voltage LSB times the ratio of the resistor divider chosen as the Bus Voltage LSB for this reference design.

Table 3: Bus Supply vs INA226 Bus Voltage Register Reading

Bus Supply (V)	INA226 Bus Voltage register reading (V)
400	6.2400
350	5.4500
300	4.6730
250	3.8970
200	3.1150
150	2.3310
100	1.5620
50	0.7750

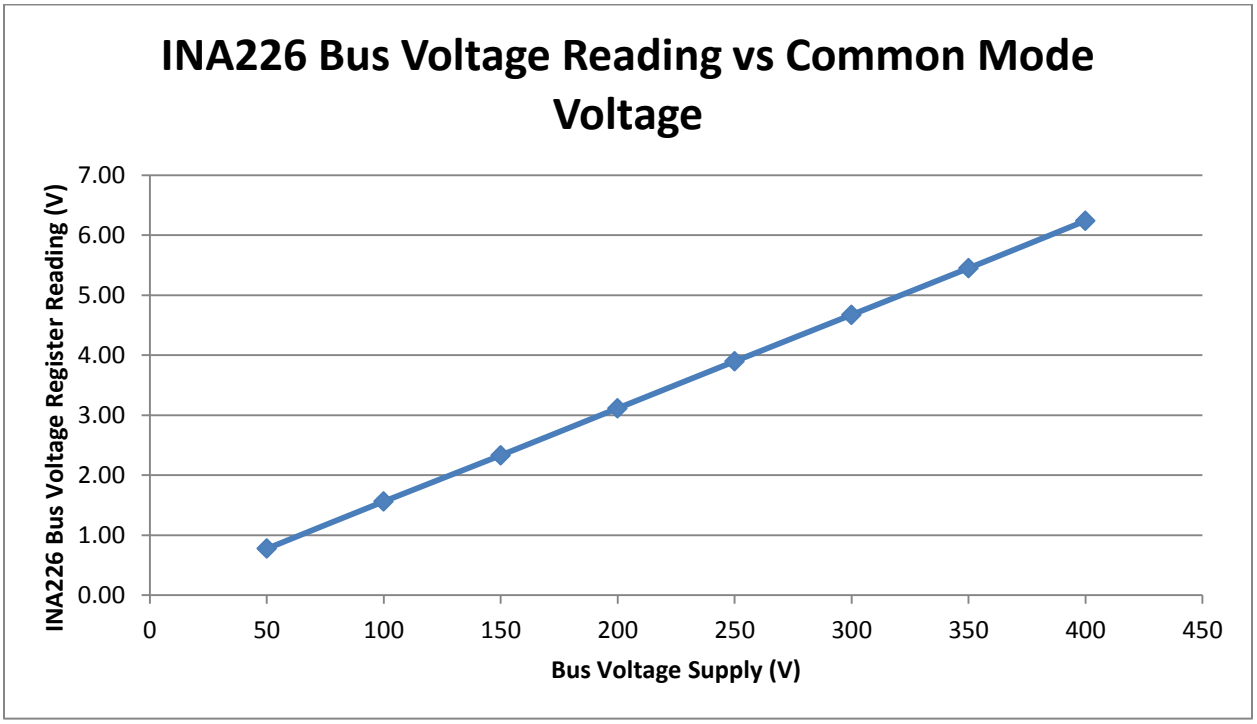


Figure 16: INA226 Bus voltage register reading vs Bus voltage supply

8.4 Power measurements

The INA226 can calculate power when the Calibration register is programmed based on the system details. Please refer to the INA226 datasheet for details on power measurement calibration. For this reference design the Bus Voltage LSB and the Power LSB will be multiplied by the ratio of the Bus voltage divider. For example, the Bus Voltage LSB value will be 1.25 mV times 64 which is 80 mV for this reference design. Similarly, after calculating the Power LSB, it will be multiplied by 64 in this case.

9 Design Files

9.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00528

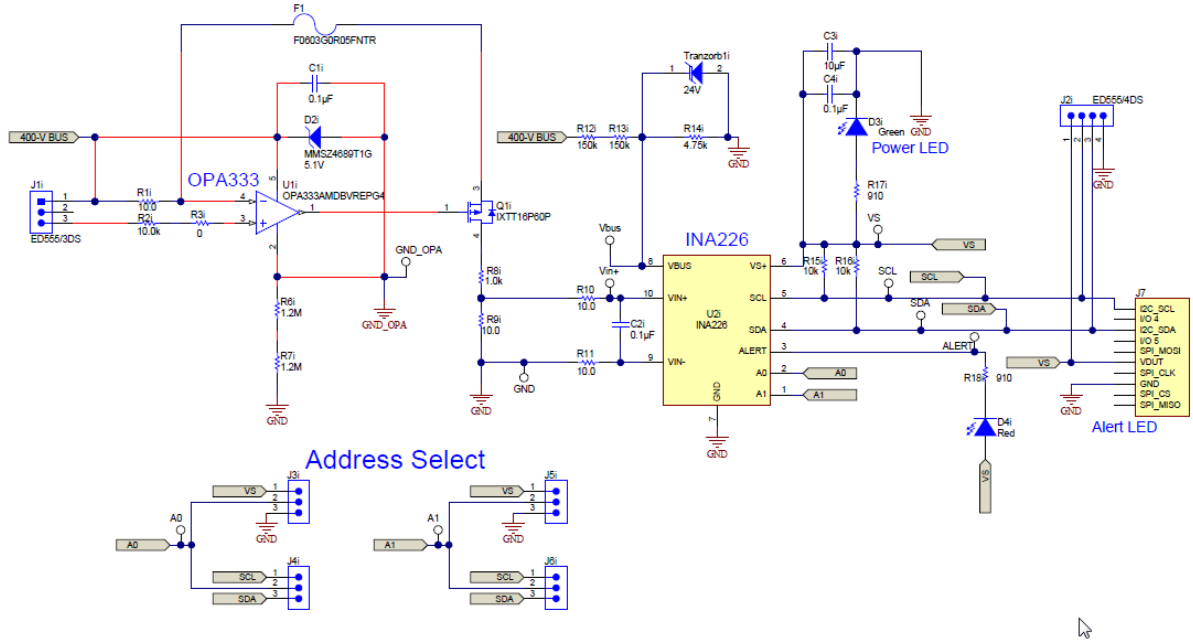


Figure 17: 40 to 400 V Current Sense Monitor Schematic

9.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/TIDA-00528

9.3 PCB Layout Recommendations

High Voltage PCB layout needs special consideration. Care must be taken to add space between the traces that are several volts apart. The PCB trace spacing used in this design meet the requirements specified in table 6-1 of the IPC-2221 standard for external conductors with conformal coating over assembly. The IPC-2221 “Generic Standard on Printed Board Design” specifies spacing requirements for various types of PCB construction, coating and applications.

Placing bypass capacitors close to OPA333 and INA226 is also critical. This helps with stability and providing noise immunity to the design.

The layout of the current-sensing resistor is also important. See Figure 18. Connect the input pins (R_{SENSE+} and R_{SENSE-}) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors.

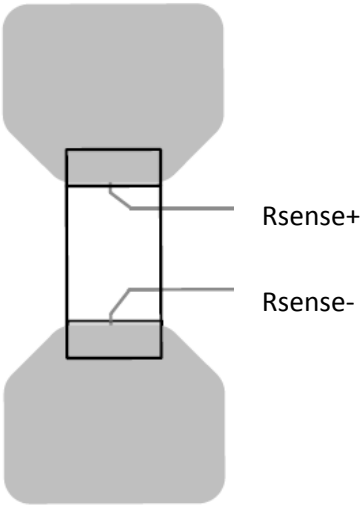


Figure 18: Shunt Resistor Layout

9.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/TIDA-00528

9.4 Altium Project

To download the Altium project files for each board, see the design files at http://www.ti.com/tool/TIDA-00528

9.5 Layout Guidelines

Please see Section 9.3.

9.6 Gerber files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/TIDA-00528

9.7 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at http://www.ti.com/tool/TIDA-00528

10 Software Files

To download the software files for this reference design, please see the link at http://www.ti.com/tool/INA226EVM

11 References

1. Texas Instruments Application circuit, INA220 datasheet, INA220
2. Texas Instruments EVM Users Guide, INA226EVM http://www.ti.com/tool/INA226EVM

12 About the Author

Rabab Itarsiwala is an Applications Engineer at Texas Instruments Inc., where she is responsible for supporting customers for current shunt monitors. This involves answering technical queries on the TI E2E forum, developing EVMs and reference design solutions, writing application notes and developing technical materials . Rabab brings to this role her experience in testing precision analog and mixed signal devices. Rabab earned her Master of Science in Electrical Engineering (MSEE) from Arizona State University, AZ.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265