High-Vin Synchronous Buck Converter

- Input: 46..50V DC
- Output: 31.0V @ 1.3A
- Controller: TPS40170
- Free-Running switching frequency of 400 kHz
- Working in continuous conduction mode
- Built on PCB PMP8665 Rev.A
1 Startup & Shutdown

The startup waveform is shown in Figure 1. The input voltage is set at 48.0V, with no load on the 31.0V output.

Channel C1: **48.0V Input voltage**  
10V/div, 10ms/div  

Channel C2: **31.0V Output voltage**  
10V/div, 10ms/div  

![Figure 1](image1)

The shutdown waveform is shown in Figure 2. The input voltage is set at 48.0V with a 1.3A load on the 48.0V output.

Channel C1: **48.0V Input voltage**  
10V/div, 5ms/div  

Channel C2: **31.0V Output voltage**  
10V/div, 5ms/div  

![Figure 2](image2)
2 Efficiency

The efficiency and load regulation are shown in Figure 3 and Figure 4.

Figure 3
PMP8665RevB is modified to Vout 31V / Fsw 600kHz, PMP10135RevB chops at 400kHz

Figure 4
3 Load step

The response to a load step and a load dump for the 31.0V output at an input voltage of 48.0V is shown in Figure 5.

Channel C2: **Output voltage**, -210mV undershoot (0.7%), 206mV overshoot (0.7%)  
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.65A to 1.30A and vice versa  
500mA/div, 1ms/div

![Figure 5](image-url)
4 Frequency response

Figure 6 shows the loop response at 48.0V input voltage and 1.3A load.

**48.0V input**
- 71 deg phase margin @ crossover frequency 29.6 kHz
- -16 dB gain margin

![Figure 6](image-url)
5 High-side FET

The drain-source voltage of the high-side FET is shown in Figure 7. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**, -1.7V minimum voltage, 50.2V maximum voltage

10V/div, 1us/div

![Figure 7](image)

The rising and falling edge are shown in Figure 8 and Figure 9. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**

10V/div, 20ns/div

![Figure 8](image) ![Figure 9](image)
The gate-source voltage of the high-side FET is shown in Figure 10. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**, -0.4V minimum voltage, 7.8V maximum voltage
2V/div, 1us/div

![Figure 10](image)

The rising and falling edge are shown in Figure 11 and Figure 12. The image was captured with 48.0V input and 1.3A load. Gate resistor mandatory!

Channel C2: **Gate-source voltage**
2V/div, 20ns/div

![Figure 11](image)  ![Figure 12](image)
6 Low-side FET

The drain-source voltage of the low-side FET is shown in Figure 13. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**, -2.0V minimum voltage, 52.4V maximum voltage 10V/div, 1us/div

![Figure 13](image)

The rising and falling edge are shown in Figure 14 and Figure 15. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**
10V/div, 20ns/div

![Figure 14](image)  ![Figure 15](image)
The gate-source voltage of the low-side FET is shown in Figure 16. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**, -2.0V minimum voltage, 8.8V maximum voltage
2V/div, 1us/div

![Figure 16](image)

The rising and falling edge are shown in Figure 17 and Figure 12. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**
2V/div, 20ns/div

![Figure 17](image)  ![Figure 18](image)
7 Output and input ripple voltage

The output ripple voltage at 1.3A load and 48.0V input voltage is shown in Figure 19.

Channel M3: **Output voltage @ 48.0 input**, 18mV peak-peak
20mV/div, 2us/div, AC coupled

![Figure 19](image1.png)

The input ripple voltage at 1.3A load and 48.0V input voltage is shown in Figure 20.

Channel M3: **Output voltage @ 48.0 input**, 227mV peak-peak
50mV/div, 2us/div, AC coupled

![Figure 20](image2.png)
8 Thermal measurement

The thermal image (Figure 21) shows the circuit at an ambient temperature of 21 °C with an input voltage of 48.0V and a load of 1.3A.

![Thermal Image](image)

**Figure 21**

<table>
<thead>
<tr>
<th>Markers</th>
<th>Label</th>
<th>Temperature</th>
<th>Emissivity</th>
<th>Background</th>
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<td>0.95</td>
<td>21.0 °C</td>
<td></td>
</tr>
<tr>
<td>Q1</td>
<td>55.5 °C</td>
<td>0.95</td>
<td>21.0 °C</td>
<td></td>
</tr>
<tr>
<td>Q2</td>
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<td>21.0 °C</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>49.7 °C</td>
<td>0.95</td>
<td>21.0 °C</td>
<td></td>
</tr>
</tbody>
</table>

Due to Vin 48V max. stress are the switching losses at HS FET; at Fsw 400kHz temperature rise $dT$ is around 33K. PMP8665B set to Fsw 600kHz to use smaller inductor 47uH.
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