TI Designs

Low Noise Power Solution Reference Design for Clock Generators

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Design Resources

TIDA-00597 Design Folder
LP3878-ADJ Product Folder
LMK03806BEVAL Product Folder

Ask The Analog Experts
WEBENCH® Design Center

Design Features

- Low Noise for Clock Generator
- Up to 800-mA output current
- Output Voltage Enable and Disable

Featured Applications

- Clock Generator
- ASIC power supplies
- DSP and FPGA power supplies

Board Image

Power Rail

TIDA-00597

LP3878-ADJ

Clock Generator LMK03806
1 System Description

Clock generator is widely used in many applications like Ethernet, Fiber Channel, PCIE and Network processors, among the characteristics, phase noise is a key parameter, which is required to meet strict requirement. If the clock phase noise is degraded, then both down-converted and up-converted signals are corrupted. Many factors degrade clock phase noise performance, and one among them is supply noise. In order to improve phase noise performance, LDO, linear regulator with low noise, is used for powering clock generator.

This design illustrates the clock phase noise degradation due to supply noise, and implements a low noise LDO to power clock generator. This design provides design files such as schematic, Gerber files, and test data.

1.1 Device Selection Considerations

In this design, the case of designing supply for the LMK03806 is depicted. LMK03806 is a high performance, multi-rate clock generator capable of synthesizing 8 different frequencies on 14 outputs. In the design, a low noise LDO with large output current like LP3878-ADJ is implemented as power supply for LMK03806.

Table 1 Design parameters

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>3.9V to 5V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>3.3V</td>
</tr>
<tr>
<td>$I_{LOAD}$</td>
<td>800mA</td>
</tr>
</tbody>
</table>
2 Block Diagram

Figure 1 gives a block diagram of the system. The red block represents the focus component of this document. The grey components are mentioned in this document and its power requirements is defined and taken into consideration to specify the system requirements and test parameters; however this component was not design into the TIDA-00597 and some of their application specific requirements are not mentioned, it is recommended to review its datasheet for additional application implementation requirements.

2.1 Component Selection

This design selects the following parts:

- **LP3878-ADJ**: 800-mA Linear Regulators with Adjustable Output Stable with Ceramic Output Cap.
- **LMK03806**: Ultra-low jitter clock generator with 14 outputs

2.1.1 LP3878-ADJ

The LP3878-ADJ is an 800 mA adjustable output voltage regulator designed to provide high performance and low noise in applications requiring output voltage as low as 1.0-V.

The LP3878-ADJ delivers superior performance:

- **Ground Pin Current**: Typically 5.5-mA @ 800-mA load and 180-μA @ 100-μA load.
- **Low Power Shutdown**: the LP3878-ADJ draws less than 10-μA quiescent current when shutdown pin is pulled low.
- **Precision Output**: Ensured output voltage accuracy is 1% at room temperature.
- **Low Noise**: broadband output noise is only 18-μV (typical) with 10-nF bypass capacitor.
The output noise spectral density of LP3878 is shown as below:

![LP3878-ADJ Output Noise Spectral Density](image)

Figure 3 LP3878-ADJ Output Noise Spectral Density

### 2.1.2 LMK03806

The LMK03806 is a high performance, ultra-low jitter, multi-rate clock generator capable of synthesizing 8 different frequencies on 14 outputs at frequencies of up to 2.6-GHz. Each output clock is programmable in LVDS, LVPECL or LVCMOS format. The LMK03806 integrates a high performance integer-N PLL, low noise VCO, and programmable output dividers to generate multiple reference clocks for SONET, Ethernet, Fiber Channel, XAUI, Backplane, PCIe, SATA and Network processors from a low cost crystal.

![LMK03806 Block Diagram](image)

Figure 4 LMK03806 Block Diagram
3 Design Considerations

This design provides the description of clock phase noise degradation due to supply noise, and provides test results. The clock generator of LMK03806 is not designed in this design. The test results are conducted on LMK03806BEVAL.

3.1 Supply Noise Impact on Phase Noise

Phase noise at the clock generator output is affected by supply noise mostly due to the following two significant reasons.

3.1.1 Ringing at Vcc Due to Change in Current Drawn by Clock Generator

Figure 5 shows a simple block diagram with the clock generator, the device under test, (DUT) supplied by the $V_{cc}$ and $I_{cc}$. The supply is considered to have source voltage, $V_S$, and source impedance, $Z_S$. This supply can either be considered as a laboratory supply or laboratory supplies + LDO. In an ideal case, $Z_S = 0$; however, in a non-ideal world, $Z_S = 0$.

With the activity of clock generator, the supply current $I_{cc}$ changes, and this changes the drop across $Z_S$, i.e., $\Delta V$, this translates to change in the supply $V_{cc}$ and is added as noise to clock generator phase noise. This noise can be minimized by using supplies with minimum $Z_S$, or the LDOs used must be robust against the changes in $I_{cc}$. Essentially, it is desirable that the ac output impedance be as low as possible. Most of the TI LDOs has low output impedance (and usually decoupling capacitors are added to minimize the ac output impedance), and thus the phase noise affected due to $V_{cc}$ ringing is less.

3.1.2 Noise Generated by LDO

Figure 6 shows the simplified LDO block diagram. The LDO output is regulated with respect to the LDO band gap reference. Any noise on the LDO band-gap reference is translated at the LDO output. Considering the noise power generated at the band gap reference $V_{NBG}$, the noise power at the output from the band gap reference $V_{NOUT}$ is as is given in Equation 1:

$$V_{NOUT} = V_{NBG} \times (1 + \frac{R_1}{R_2})$$

(1)

Along with the LDO band-gap reference, total output noise at the LDO output is the sum of noise generated by the error amplifier, noise from the pass transistor, and thermal or 4KTR noise from the
R₁ and R₂ resistor divider network. Noise from LDO band-gap reference is usually the dominant source. This design illustrates the importance of this noise, which effects phase noise. It is important to select low noise LDO to improve clock generator phase noise.
4 Design Implementation Guidelines

4.1 Input and Output Capacitor
Input and output capacitors eliminate high frequency noise and are necessary for loop stability. Consider the following recommendations:
- Utilize X7R or X5R ceramic capacitors to minimize tolerance and variation with temperature
- Capacitance ESR in the 50- to 200-kHz range must not exceed 25mΩ
- Input and output caps must be located less than 1 inch from the input and output pins
- Input minimum capacitance of 4.7-μF
- Output minimum capacitance of 10-μF
- Minimum of ±20% capacitance tolerance

4.2 Noise Bypass Capacitor
As mentioned in section 3.1.2, noise from LDO band-gap reference is usually the dominant source. A 100-nF bypass capacitor on the BYPASS pin significantly reduces band-gap noise. The following recommendation must be taken into account:
- The bypass capacitor leakage must never exceed 100-nA.
- High-quality ceramic capacitors with either an NP0 or C0G dielectric typically have very low leakage.

4.3 Setting the Output Voltage
The output voltage is set by using an external resistor divider \( R_1 \) (upper-side resistor) and \( R_2 \) (lower-side resistor). The formula for output voltage is:

\[
V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_2}{R_1}\right)
\]

(2)

\( R_2 \) must be less than 5 kΩ to ensure loop stability. To be compliant with the 5-kΩ rule, 866-Ω was chosen for \( R_2 \), then 2-kΩ was chosen for \( R_1 \) to yield the expected voltage of 3.3-V.

4.4 Feedforward Capacitor
The feedforward capacitor \( C_{FF} \) is required to increase phase margin, ensure loop stability. The \( C_{FF} \) forms both a pole and zero in the loop gain. The zero provides a beneficial phase lead (which increases phase margin), and the pole adds an undesirable phase lag that must be minimized.

The zero frequency is determined by the values of \( C_{FF} \) and \( R_1 \):

\[
F_Z = \frac{1}{2\pi C_{FF} \times R_1}
\]

(3)

The pole frequency is determined by the value of \( C_{FF} \) and the parallel combination of \( R_1 \) and \( R_2 \):

\[
F_P = \frac{1}{2\pi C_{FF} \times \frac{R_1 \times R_2}{R_1 + R_2}}
\]

(4)

For \( V_{OUT} \geq 2.5\text{-V} \), \( C_{FF} \) should be selected to set the zero frequency in the range of about 20-kHz to 100-kHz. The zero frequency is set to 36-kHz.

\[
C_{FF} = \frac{1}{2\pi F_Z \times R_1} = \frac{1}{2\pi \times 36 \times 2k\Omega \times 2k\Omega} = 2200 \text{ pF}
\]

(5)

The feedforward capacitor \( C_{FF} \) can also help to reduce output noise. This capacitor forwards (bypasses) output noise around \( R_1 \). This bypass or shorting action prevents the bandgap noise from being increased by the gain of error amplifier at frequencies higher than the resonant frequency, \( f_{\text{Resonant}} \) of \( R_1 \) and \( C_{FF} \), where,
\[ F_{\text{Resonant}} = f_Z = \frac{1}{2\pi C_{FP} \times R_1} \]  

(6)

The equation (1) becomes:

\[ V_{\text{NOUT}} = V_{\text{NBG}} \times \left(1 + \frac{R_1 \parallel \frac{1}{2\pi f \times C_{FP}}}{R_2}\right) \]  

(7)
5 Test Setup and Results
In order to show the advantage of selecting low noise LP3878-ADJ, below setups were made to quantify the benefits.

5.1 LP3878-ADJ vs DCDC Switching Supply
This setup used LP3878-ADJ and DCDC switching supply, and measure the clock phase noise.

<table>
<thead>
<tr>
<th>Equipment</th>
<th>device number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lab linear supply</td>
<td>Agilent E3631A</td>
<td>Constant voltage supply</td>
</tr>
<tr>
<td>DCDC switching supply</td>
<td>TPS62203EVM</td>
<td>3.3V output for LMK03806BEVAL</td>
</tr>
<tr>
<td>Clock generation</td>
<td>LMK03806BEVAL</td>
<td>Clock generation</td>
</tr>
<tr>
<td>Signal source analyzer</td>
<td>N9020A</td>
<td>Used to measure phase noise</td>
</tr>
</tbody>
</table>

Figure 7 represents the test setup.

Figure 8 shows the output noise of DCDC switching supply is higher than that of LP3878-ADJ. When using DCDC switching supply and LP3878-ADJ to power LMK03806, the clock phase noise is shown in Figure 9.

It can be seen that noise of DCDC switching supply is translated at the clock output and degrades the clock phase noise response.
5.2 LP3878-ADJ vs Lab Linear Power

This setup used LP3878-ADJ and lab linear power, and measures the clock phase noise.

<table>
<thead>
<tr>
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Figure 10 represents the test setup.
Figure 11 Output Noise Comparison between LP3878-ADJ and Noisy LDO

Figure 11 shows the output noise of lab linear power at lower frequency is much higher than that of LP3878-ADJ, at higher frequency, the output noise of lab linear power and LP3878-ADJ are almost the same.

When using lab linear power and LP3878-ADJ to power LMK03806, the clock phase noise is shown in Figure 12. It can be seen the phase noise response has difference at lower offset frequency and almost the same at higher offset frequency.
5.3 Noise Impact on Different Supply Rail of Clock Generation

The clock generation of LMK03806 has many supply rails, these rails can be divided into two groups of $V_{CC\_Core}$ and $V_{CC\_CLK}$. In order to check which rail with noise supply will affect clock phase noise, below setup is made. In this setup, each rail is supplied by noisy power while the remaining one continues to use LP3878-ADJ.

Figure 13 represents the test setup.

Figure 12 Clock Phase Noise Supplied by LP3878-ADJ and Lab Linear Power

Figure 13 Test Setup of Powering Different Supply Rail
Figure 14 Clock Phase Noise of LP3878-ADJ Power CLK and DCDC Supply Power Core

Figure 15 Clock Phase Noise of LP3878-ADJ Power Core and DCDC Supply Power CLK
From Figure 14 and 15, it can be seen that noise on $V_{CC,\text{core}}$ is translated at the clock output and degrades the clock phase noise response. If different rail needs different supplies, it is important to select quiet supply for core rail.
6 Design Files

6.1 Schematics

To download the Schematics for each board, see the design files at [http://www.ti.com/tool/TIDA-00597](http://www.ti.com/tool/TIDA-00597)

![Figure 16 TIDA-00597 Schematic](image)

6.2 PCB Layout Recommendations

6.2.1 Layout Guidelines

The CIN and COUT caps are placed close to the input and output pins to minimize current loops

Solid ground plane to guarantee good heat dissipation

Short and wide trace for output
6.2.2 Altium Project

To download the Altium project files for each board, see the design files at.
http://www.ti.com/tool/TIDA-00597
  • Gerber and NC-drills
  • Bill of Materials (BOM)
  • Assembly Drawings

7 Terminology

*TI Glossary: SLYZ022* This glossary lists and explains terms, acronyms, and definitions.

8 About the Author

Hank Cao
Is a System Engineer at Texas Instruments on the mobile power devices RF power group at Texas Instruments. Hank earned his Masters of Power Electronics from Nanjing University of Aeronautics and Astronautics.
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