TI Designs

Three-Phase Brushless DC (BLDC) Power Tool Motor Driver

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DRV91680	Product Folder

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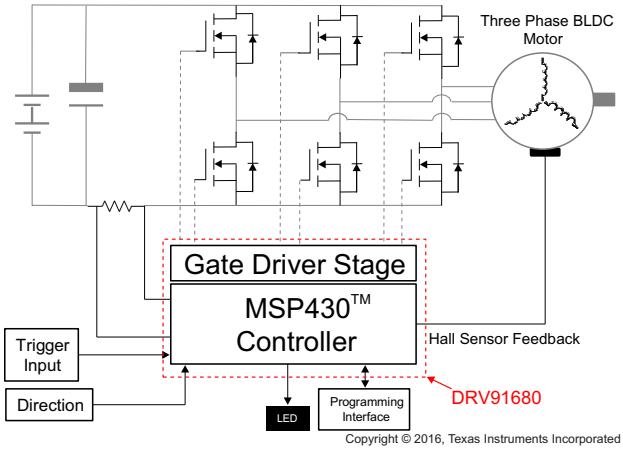
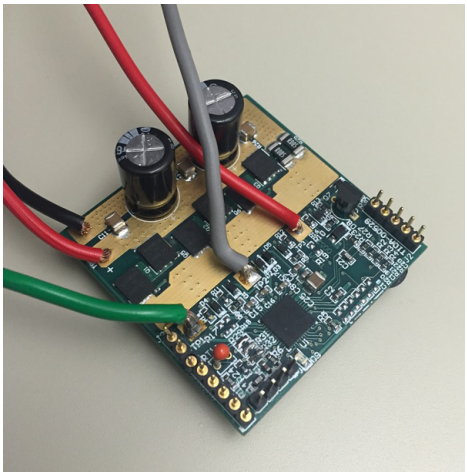
Design Features

- Compact Design
- 50 A of Peak Current
- Trigger Input
- Hall Sensor Interface
- Code Development Interface

Featured Applications

- BLDC Power Drills
- BLDC Impact Drivers





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1 Introduction

Power tools are commonly used in woodworking, metalworking, construction, and DIY projects in and around the household. Electric battery-powered power tools are popular because they are compact, lightweight, maneuverable in tight areas, clean, and easy to use. Over the past few years, these cordless power tools kept improving in terms of size, weight, torque capability, cost, efficiency, battery life, and features. Improvement in energy density in batteries and advancements in rechargeable battery technology is enabling more and more power tools to be cordless. Higher torque density, improved efficiency, and extended life of brushless DC motors are attractive when compared with existing brushed DC and cord-powered induction-motor-based power-tool designs.

This document describes a reference design built for cordless power tool applications. This design is based around Texas Instruments DRV9x family of brushless motor drives along with Texas Instruments NexFET™ discrete MOSFETs. DRV9x is a highly integrated device that includes pre-drivers, a processing core, and user interfaces needed for a single-chip brushless three-phase sensed or sensorless motor driver solution. Some of the safety features include hardware overcurrent protection, over temperature protection, and under voltage protection. The DRV9x processing core incorporates a 16-bit RISC MSP430™ CPU core. In-system programmable flash (32kB), RAM, and ROM are available to meet the needs of a variety of applications.DRV9x has rich set of peripherals for a brushless three-phase motor driver application (sensed and sensorless). The 16-bit microcontroller instruction set is compatible with TI's MSP430F5438 family.

Device Features:

- 8.0-V to 26-V single-supply controller
- Analog peripherals
  - Six independent integrated pre-drivers
  - 16-channel, 10-bit ADC
  - External regulators
    - V3P3D—20 mA maximum
    - VDD—15 mA maximum
  - 2.4-V ADC reference for external use
  - 28 GPIO ports
  - Three charge pumps to support 100% duty cycle
- RGZ package with PowerPAD™
- Programmable differential sense amp (DSA)
- Programmable overcurrent (OC) protection
- Overtemperature (OT) protection
- POR / BOR / UVLO monitors

Microcontroller features:

- 16-bit RISC architecture
  - Up to 25 MIPS
  - High endurance 32kB flash
    - 25-MHz single-cycle access
    - 2kB SRAM
- Dead time generator
- Code protection lockout
- Spi-Bi-Wire for device programming

2 Key System Specifications

Table 1. Key System Specifications of Power Tool Reference Design

PARAMETER	SPECIFICATION
DC input voltage	8 V to 22 V
Rated output power	500 W
Inverter switching frequency	25 kHz
Operating temperature range	50°C ambient (without heat sink)
Feedback	Hall sensors Single shunt current measurement
Safety features	Overcurrent protection DC bus voltage monitoring Overtemperature monitor capability

3 System Description

A cordless power tool based on DRV9x family consists of the following main blocks:

- BLDC motor (load)
- Three-phase bridge consisting of six MOSFETs
- Microcontroller with integrated pre-driver
- Rechargeable battery
- User inputs and indicators

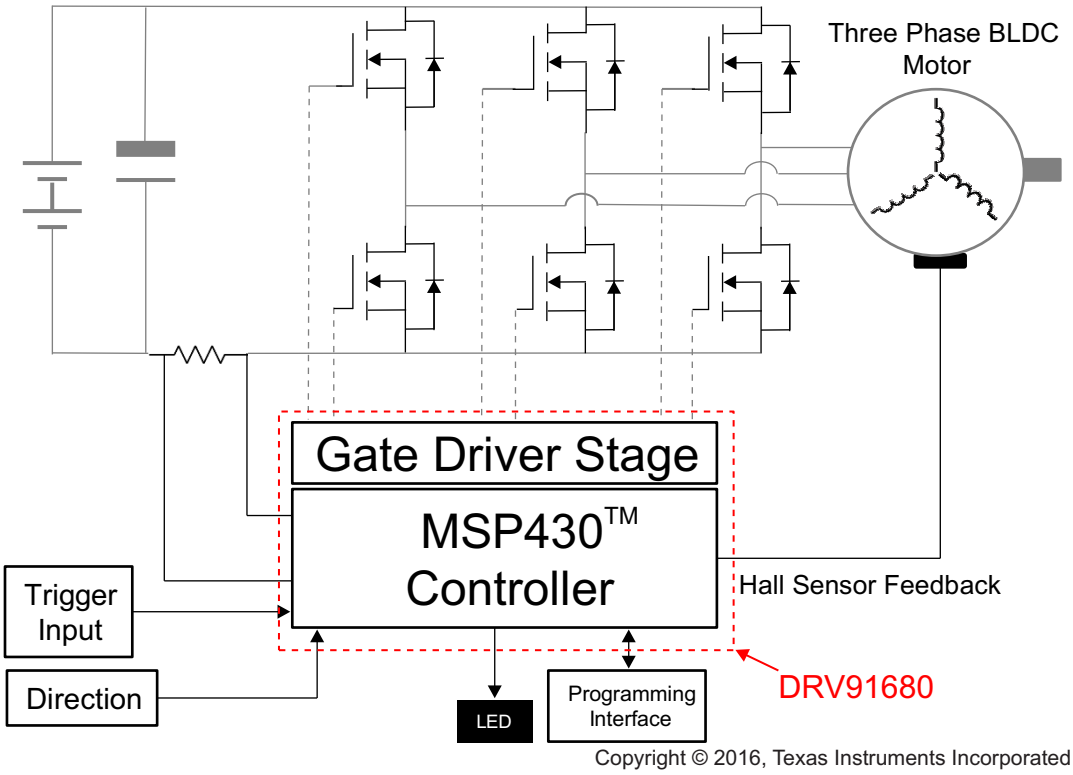

Figure 1. Power Tool Reference Design System

The trigger command directly controls the speed of the motor by controlling the average voltage applied to the motor. The average voltage applied to the motor is controlled by controlling the pulse width of the PWM. The hall-sensor feedback is continuously monitored to guarantee proper commutation of the motor.

3.1 Control Algorithm

This section outlines the motor control algorithm developed for the reference design to control a power-tool motor based on hall-sensor feedback. The interrupt routine is executed every PWM frequency or during an overcurrent event. The amount of voltage applied to the motor is controlled by interpreting the trigger level.

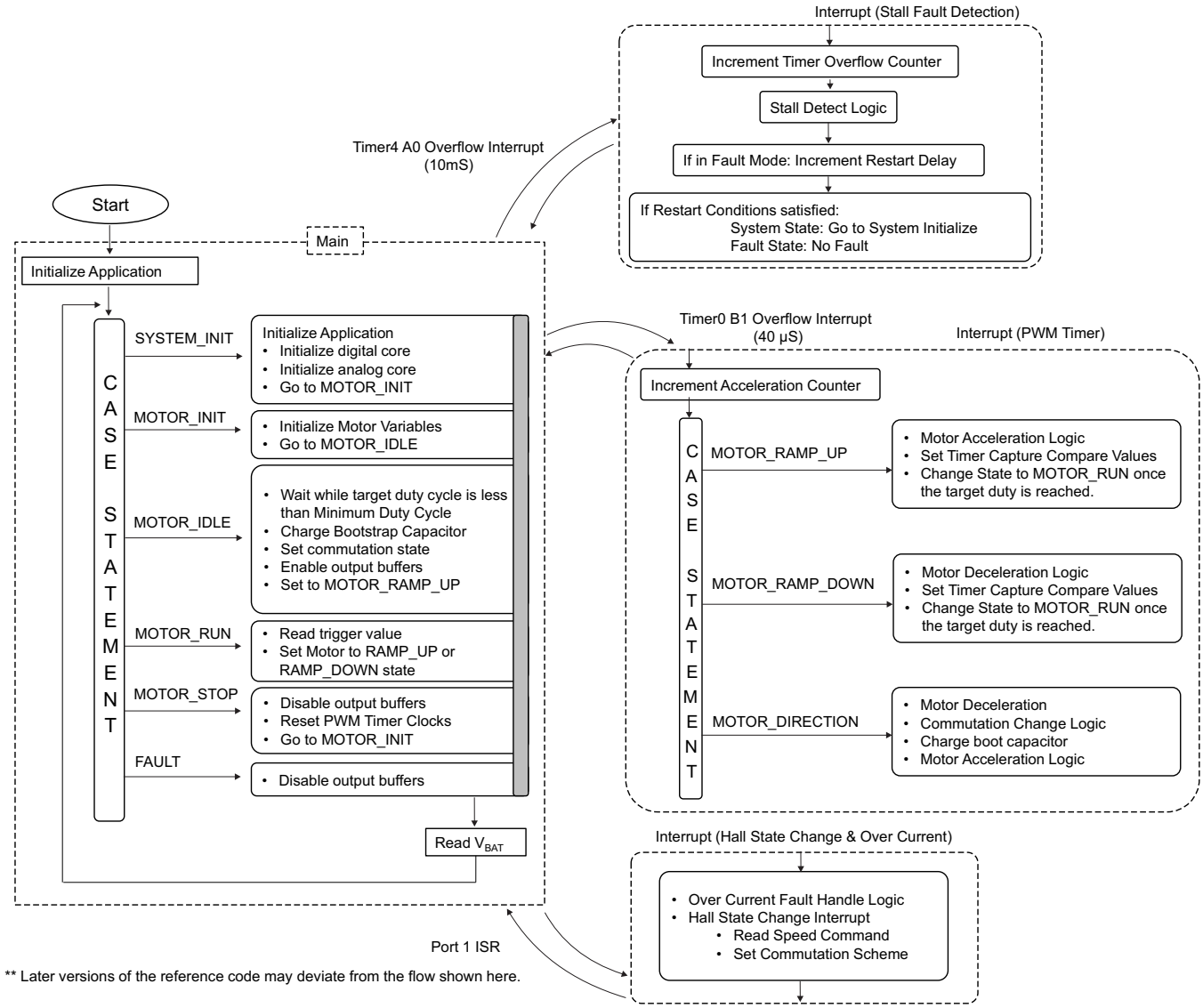

Figure 2. Motor Control Algorithm Flowchart

4 Highlighted Products

4.1 DRV91680

TI's DRV91680 integrated motor controller and pre-driver is a 26-V single supply with six internal regulators, three 47-V high-side floating pre-drivers, three 7-V low-side pre-drivers, and three internal charge pumps. Suitable applications for this device are Brushed (BDC) or Brushless (BLDC) motor systems. This product also allows an external fail-safe protection scheme to prevent accidental runoff of the motor. The built-in protection functions include overvoltage, overcurrent, and undervoltage detection capability.

4.2 CSD18509Q5B N-Channel NexFET™ Power MOSFET

CSD18509Q5B is an N-channel NexFET™ power MOSFET with ultra-low on resistance, low thermal resistance and with avalanche rating. This MOSFET is RoHS compliant, halogen free, and available in a Pb-free terminal-plated SON 5-mm × 6-mm plastic package.

5 System Design Theory

The power-tool reference design is a compact design focused on delivering bursts of energy that the tool requires. The compact design utilizes minimal space, reducing the overall system size. Electrical and thermal stresses in the design were considered in selecting the components for the design.

5.1 PWM Frequency Selection

Specification of the PWM frequency is one of the major steps in the system design process. Higher PWM frequency contributes to increase switching losses as well as leaving fewer CPU cycles per PWM period. Lowered PWM frequency contributes to audible noise if in the audible range, and it decreases the highest electrical frequency that can be synthesized. This reference design is based on a PWM frequency of 25 kHz, which is outside the audible frequency range. A PWM period of 40 µS is sufficient to implement sensed trapezoidal control as well as supervisory algorithms. PWM frequency could be reduced if the losses are higher in this design and do not meet the intended efficiency criterion.

5.2 MOSFET Selection

MOSFETs in the drive stage deliver the energy from the battery to the motor by turning on and off at the PWM frequency. The PWM frequency, turn-on time, drain current, and R_{DS_ON} of each MOSFET contribute towards the losses that occur in the system during operation. These requirements were followed in selecting the MOSFET in this reference design:

- Requirement 1: Continuous drain current of 100 A
- Requirement 2: Small footprint for the compact layout
- Requirement 3: Smaller Q_G to assist reaching the miller region faster
- Requirement 4: Smaller Q_{GD} to assist faster turn on/turn off
- Requirement 5: Smaller $R_{DS\ ON}$ to minimize switching losses
- Requirement 6: Minimum V_{GS} (<4 V)
- Requirement 7: At least 40 of V_{DS} to withstand transients (V_{BAT} = 18.0 V)

The Texas Instruments CSD18509Q5B device met the entire list of criterion in comparison with a competitor part. This device is capable of delivering 100 A if the package temperature is maintained at the recommended temperature. The MOSFET's dimensions are 5 mm × 6 mm (SON package), which is ideal for compact designs. Typically, a tradeoff exists when selecting MOSFETs with lower Q_G, lower Q_{GD}, and lower R_{DS_ON}. Q_G and Q_{GD} contribute to turn-on time, turn-off time, and switching losses. R_{DS_ON} contributes to losses during "On State" and tends to increase in MOSFETs with lower Q_G / Q_{GD}. However, TI's advanced process technology has enabled the NexFET™ devices (CSD18509Q5B) with lower QG, QGD and RDS_ON. Further, the CSD18509Q5B has a threshold voltage of 1.8V and a drain to source voltage capability of 40V. The VDS limit is critical in maintaining the device in safe operating region and prevents it from reaching an avalanche state during higher slew rates.

5.3 Gate Drive Stage Considerations

The recommended gate drive stage is shown in Figure 3. Another critical design parameter is the voltage limit on the VBOOT pin voltage limit, which is 47.7 V for DRV91680. Boot capacitor CBOOT is charged to 7 V above the UPHASE voltage by the boot strap circuit. Higher device turn-on and turn-off slew rates could cause the UPHASE voltage to exceed 40.7 V, resulting in UBOOT to reach voltages beyond 47.7 V. Therefore, voltage fluctuations on the UPHASE voltage must be limited to at least 40 V to guarantee safe operation of the DRV91680. The optional Schottky clamp will maintain the voltage across the low-side MOSFET, preventing the boot pin from reaching values beyond the recommended limit.

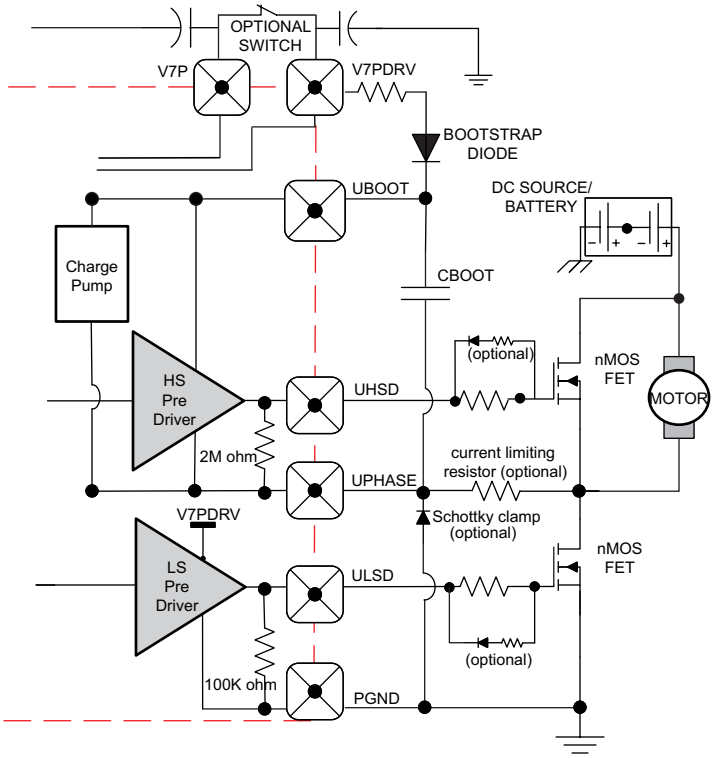

Figure 3. DRV91680 Gate Drive Boot Strap Circuit Configuration

Bootstrap capacitor CBOOT as shown in Figure 3 was sized based on the gate-charge specification and the acceptable voltage ripple across the bootstrap capacitor. The required gate charge is 100 nC, and the acceptable voltage ripple was selected as 25 mV. The calculation of bootstrap capacitor is as follows:

$$
\begin{aligned}
\text{VBOOT} &= V7P - V_{D\_Bootstrap} - V_{D\_Internal} \\
&= 7.0V - 0.720 - 0.600 \\
&= 5.680V
\end{aligned}
$$

$$
\begin{aligned}
\text{MOSFET Gate Charge } (Q_{G@6.28V}) &= 100nC \\
\Delta V_{BOOT} &= 25mV \text{ (no more than } \mathbf{10\%} \text{ voltage drop is recommended)}
\end{aligned}
$$

$$
\begin{aligned}
\Delta Q &= C\,\Delta V \\
C &= \Delta Q / \Delta V \\
&= 100nC / 25mV \\
&= 4.0\ \mu F \\
\textbf{Capacitor was selected as } C &= \mathbf{4.7\ \mu F}
\end{aligned}
\tag{1}
$$

When a 100% duty cycle is commanded to the MOSFET, the boot capacitor leakage current must be considered to estimate the voltage drop that would occur during operation . The tolerable number of PWM cycles with a 100% duty cycle, assuming the capacitor has a leakage current of 20 µA, is calculated as follows.

$$\begin{aligned}
\text{Maximum tolerable voltage drop} &= 10\% \times 5.68\ \text{V} \\
&= 0.568\ \text{V} \\
\Delta Q &= C\,\Delta V \\
&= 4.7\ \mu\text{F} \times 0.568\text{V} \\
&= 2.67\ \mu\text{C} \\
\Delta T &= \Delta Q / I \\
&= 2.67\ \mu\text{C} / 20\ \mu\text{A} \\
\Delta T &= 133.5\ \text{mili Seconds} \\
\text{Number of PWM Cycles (at 25kHz)} &= 131.5\ \text{mS} / 40\ \mu\text{S} \\
&= \mathbf{3287\ PWM\ cycles\ at\ 25kHz}
\end{aligned} \tag{2}$$

5.4 Gate Drive Resistance (R_g) Design Guidelines

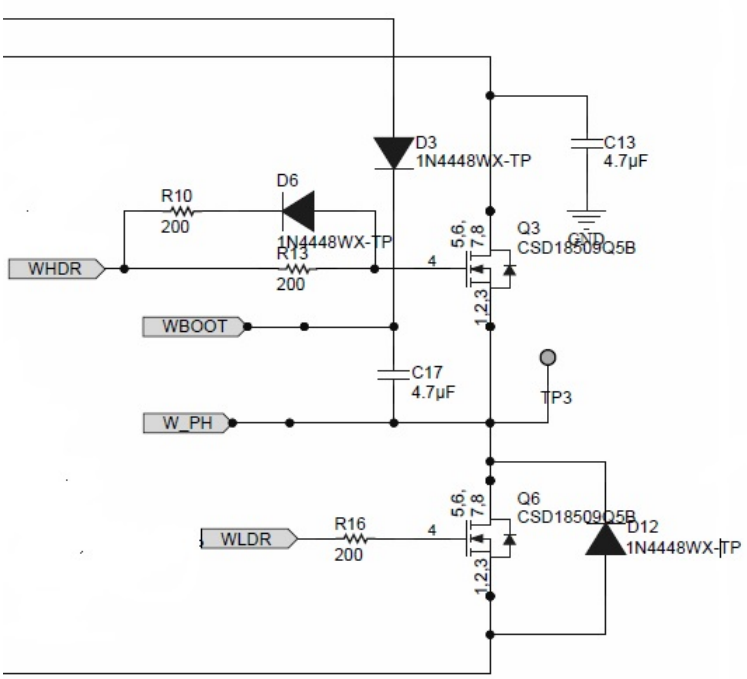

Figure 4. DRV91680 Gate Drive Circuit Configuration

Sizing of the gate-drive resistor is a major step that follows MOSFET selection. Gate-drive output-current capability and the slew rate that the MOSFET turns on are considered in sizing the gate drive resistor. The typical gate-drive current for DRV91680 is 450 mA per switch. Slew rate selection varies based on stray inductance in the design, di / dt limitations, dv / dt limitations switching losses, switching frequency, and layout. This design is based on a slew rate of 40 V / µS. The recommended range of slew rate is between 10 V / µS to 50 V / µS, based on the typical parasitic behavior of this PCB layout.

Slew rate specification	= 40 V/uS
Maximum battery voltage	= 18V
10% to 90% Voltage Difference	≈ 15V
Turn On Time	≈ 15 V / 40 (V/uS)
	= 375 nS
Gate to Drain Charge of the Capacitor	= 17 nC
Gate charge current	= 17 nC / 300 nS

(3)

R_g was selected to be 200 Ohms. The experimental data is as follows.

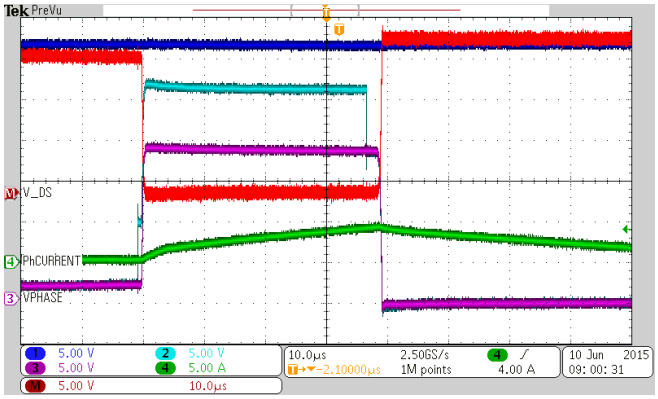

Figure 5. MOSFET Turn-on and Turn-off Characteristics with R_g = 200 Ohms

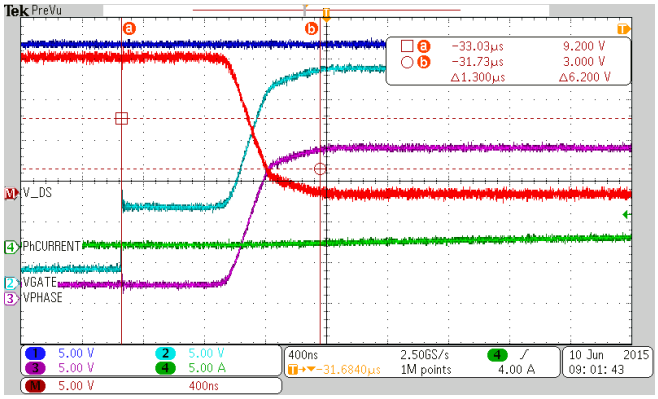

Figure 6. MOSFET Turn-on Characteristics with R_g = 200 Ohms (Slew Rate = 33.33 V / µS)

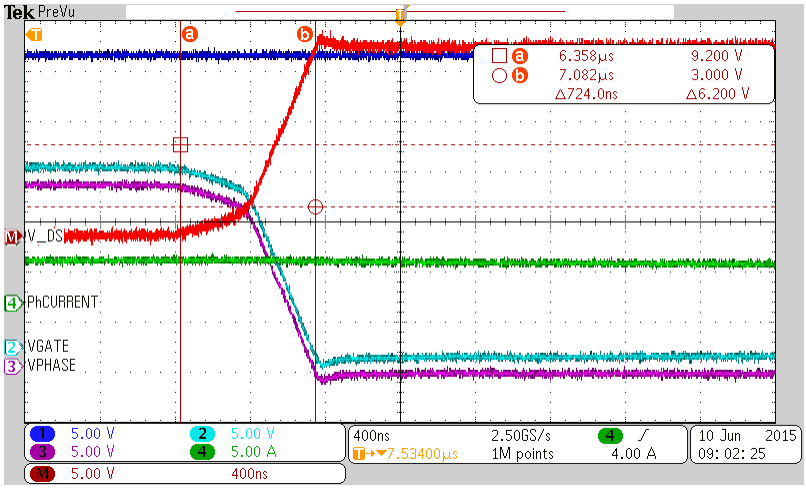

Figure 7. MOSFET Turn-off Characteristics with R_g = 200 Ohms

5.5 Thermal Performance of the Reference Design

A power tool delivers a significant amount of power within a short period of time. The delivered current as well as the resistance in the current-carrying path contributes to losses in the system that causes the system temperature to rise. Proper heat removal and heat sinking is required in an actual application to maintain the MOSFETs as well as the DRV91680 device to prevent premature failure. Thermal performance of the system is shown below at different operating points as a means of reference to the user.

Figure 8 provides a baseline thermal image without supply voltage applied to the system. There is no heat sink mounted in this reference design. Thermal images were captured at no load, 10-A peak current draw, and 50-A peak current draw. The low-side MOSFETs are higher in temperature because the PWM is applied on the low-side MOSFETs. DRV91680 is always below 32°C, even while the MOSFET temperatures are above 100°C.

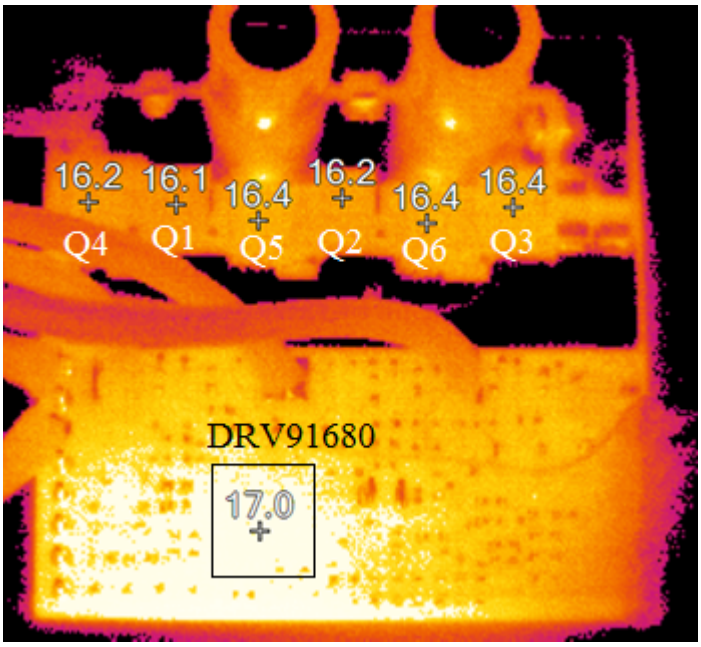

Figure 8. Temperature Profile of the Reference Design Before Power Up

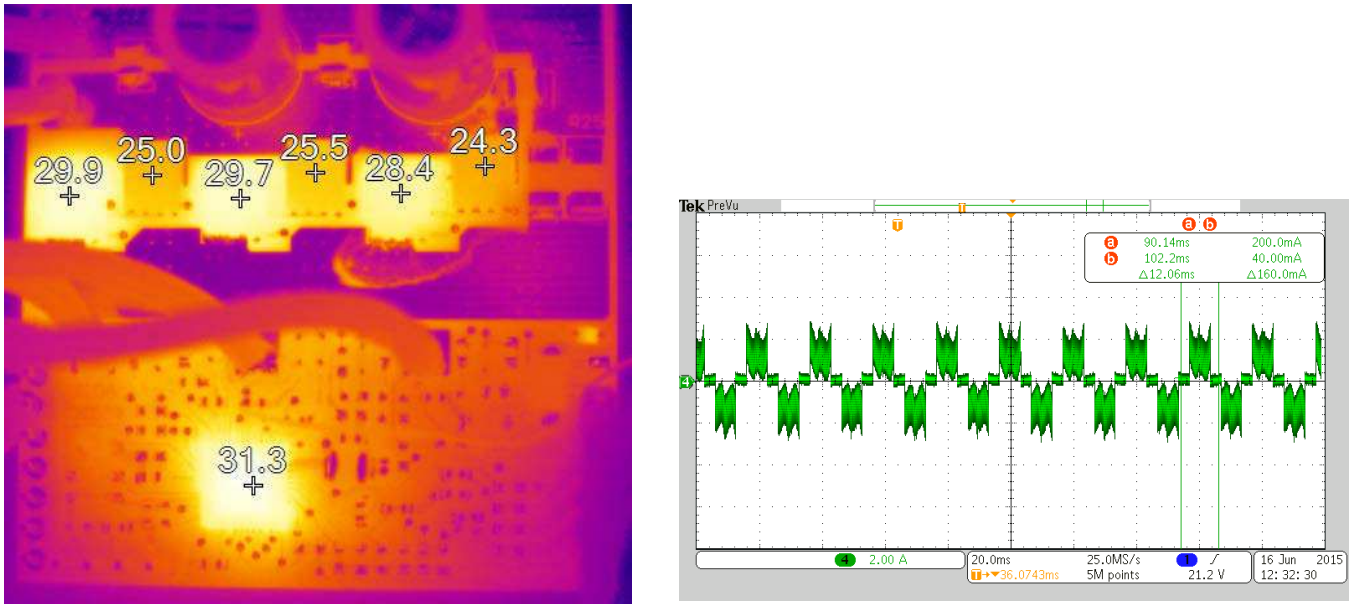

Figure 9. Temperature Profile of the Reference Design After Operating for One Minute at 2000 RPM and No Load
(Left: Thermal Image; Right: Phase Current Waveform)

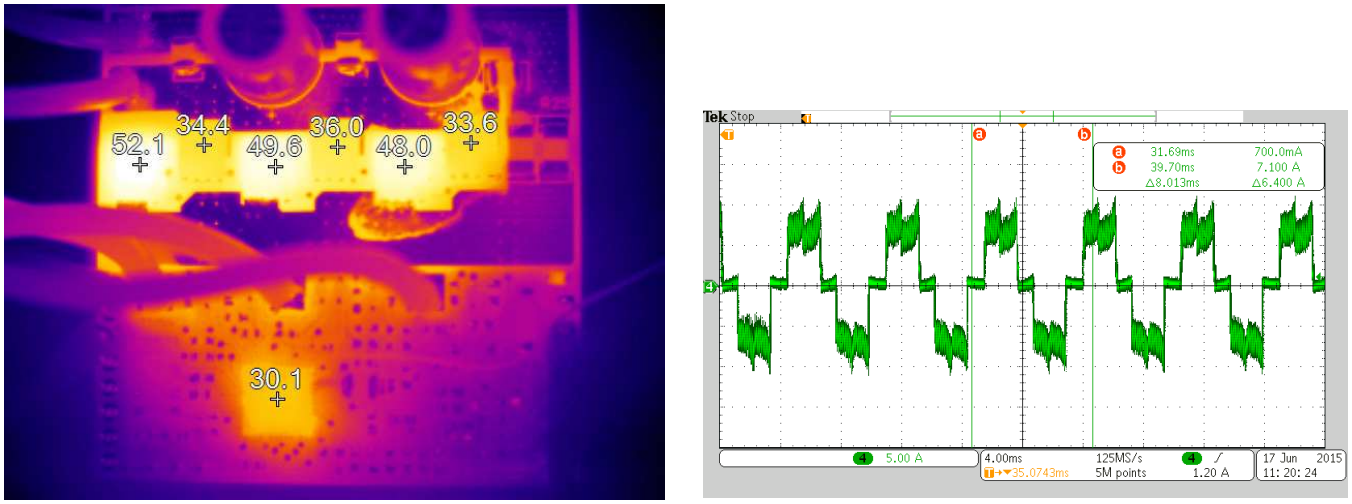

Figure 10. Temperature Profile of the Reference Design After Operating for 30 Seconds at 3300 RPM and Peak Current of 10 Amps (Left: Thermal Image; Right: Phase Current Waveform)

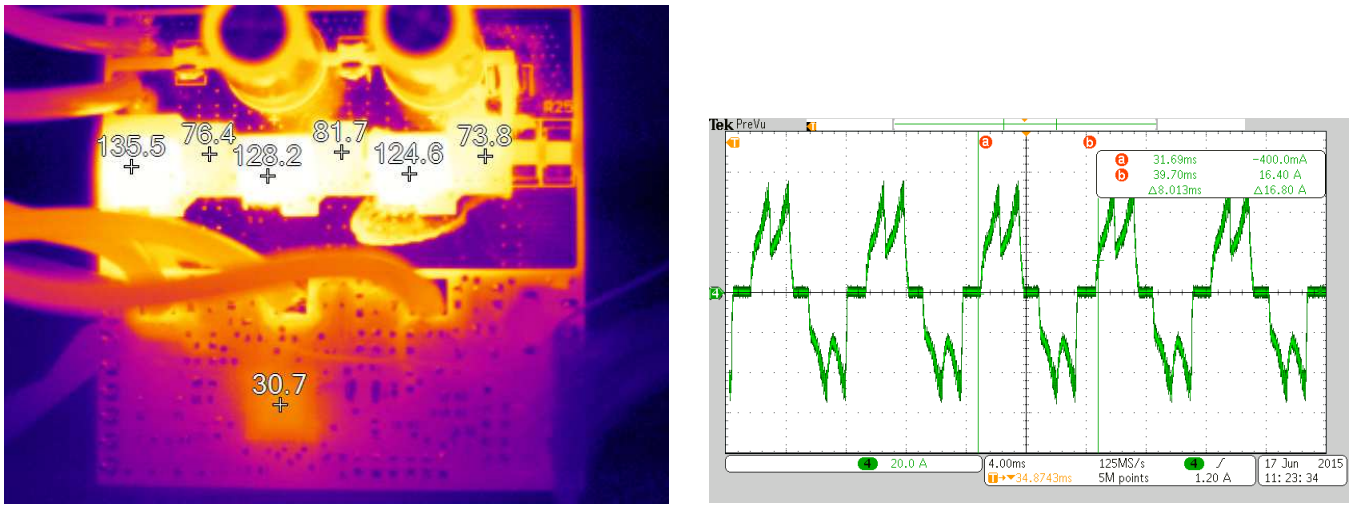

Figure 11. Temperature Profile of the Reference Design after Operating for 30 Seconds at 2800 RPM & Peak Current of 50 Amps (Left: Thermal Image; Right: Phase Current Waveform)

Table 2. Temperature Variation of the System Components with Different Load

TEMPERATURE/°C				
DEVICE	**No V_{BAT}**	**NO LOAD**	**10-A PEAK**	**50-A PEAK**
DRV91680	17.00	31.30	30.10	30.70
MOSFET (Q1)	16.10	25.00	34.40	76.40
MOSFET (Q2)	16.20	25.50	36.00	81.70
MOSFET (Q3)	16.40	24.30	33.60	73.80
MOSFET (Q4)	16.20	29.90	52.10	135.50
MOSFET (Q5)	16.40	29.70	49.60	128.20
MOSFET (Q6)	16.40	28.40	48.00	124.60

6 Advanced Features

Version 1.2 of the new firmware supports two new features for this design. The following sections explain the features and test results for those features.

6.1 Current Control Features

The power tool has certain requirements; in addition to requiring load dynamics, the tool also requires a fully-controlled torque at zero speed. Consider the following analogy: If a drill running at full speed and with no load condition hits the point in the wall where a sudden load has been applied (and if the wall is hard enough), then this action reduces the drill to zero speed; meanwhile the drive is expected to continue to complete the intended task by attempting full torque for some amount of time before the drive is shut off for protection reasons. The current control feature addresses this concern by using PWM skip mode in the DRV91680 device.

The drive operation operates in peak current mode control, which enables the specified amount of current and torque to flow through the motor for a specified amount of time. The amount of current and time are variables that may be tuned.

One important fact to remember is that allowing too much current for longer time may adversely affect heat dissipation from the bridge; hence, the balance must be stroked for choosing an appropriate amount of time. The following block diagram in Figure 12 explains the blocks used for implementing the feature. The OC limit is set through the DAC available inside the device. The OC comparator is fed with the DAC input as reference and the DSA output, which takes the current sample from the current sense resistor. Whenever the OC output has been triggered, instead of shutting the drive down, the drive continues with pulse width modulation (PWM) while in pulse skip mode.

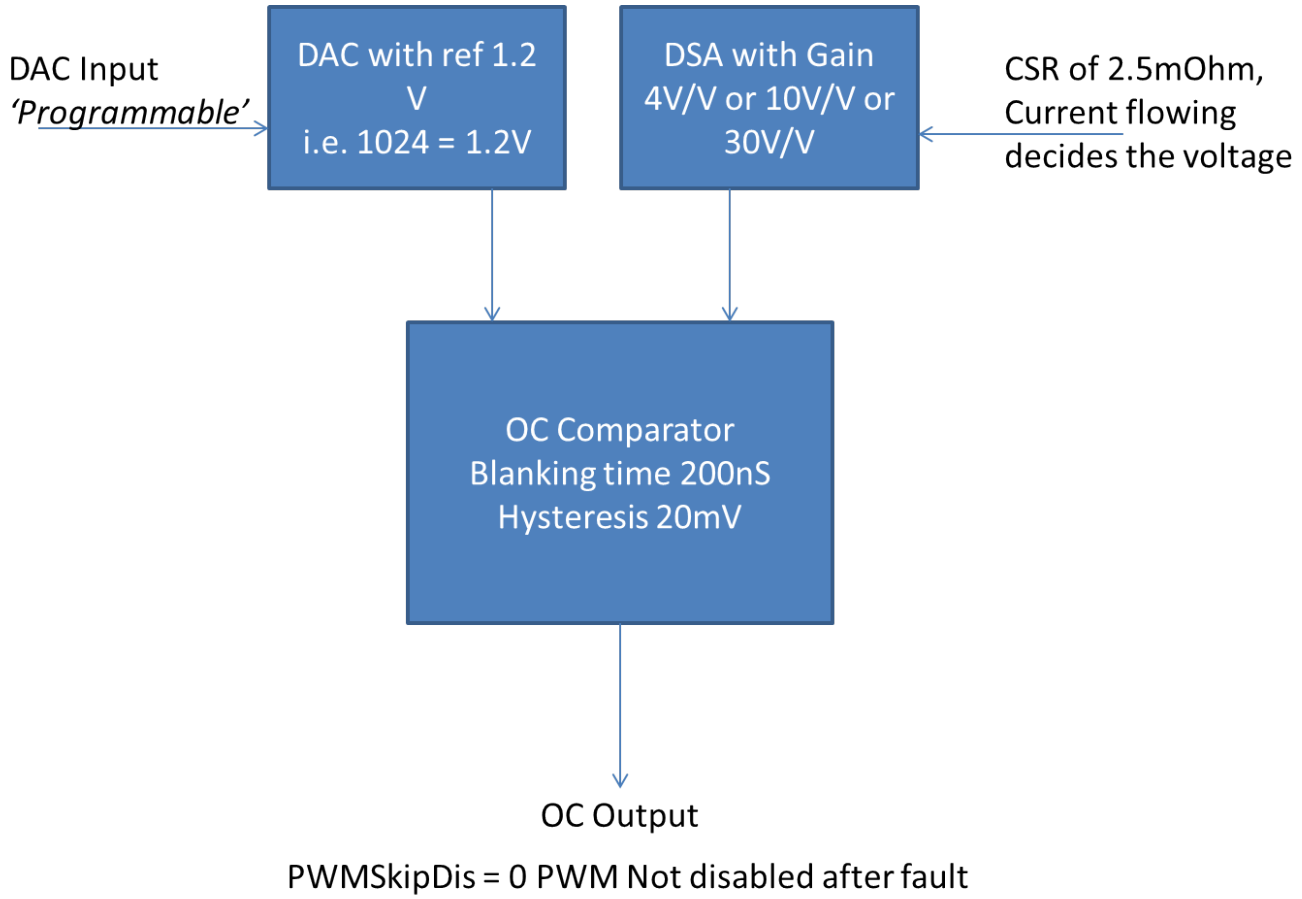

Figure 12. Block Diagram of Current Control Scheme

The following waveforms in Figure 13, Figure 14, and Figure 15 explain the current control feature. The current setting is to remain at a 15-A peak through the variable, which is part of the initial configuration as the following figures show. In normal operation without current control, the current is not allowed to go beyond the specified limit, which is a 15-A peak in this case.

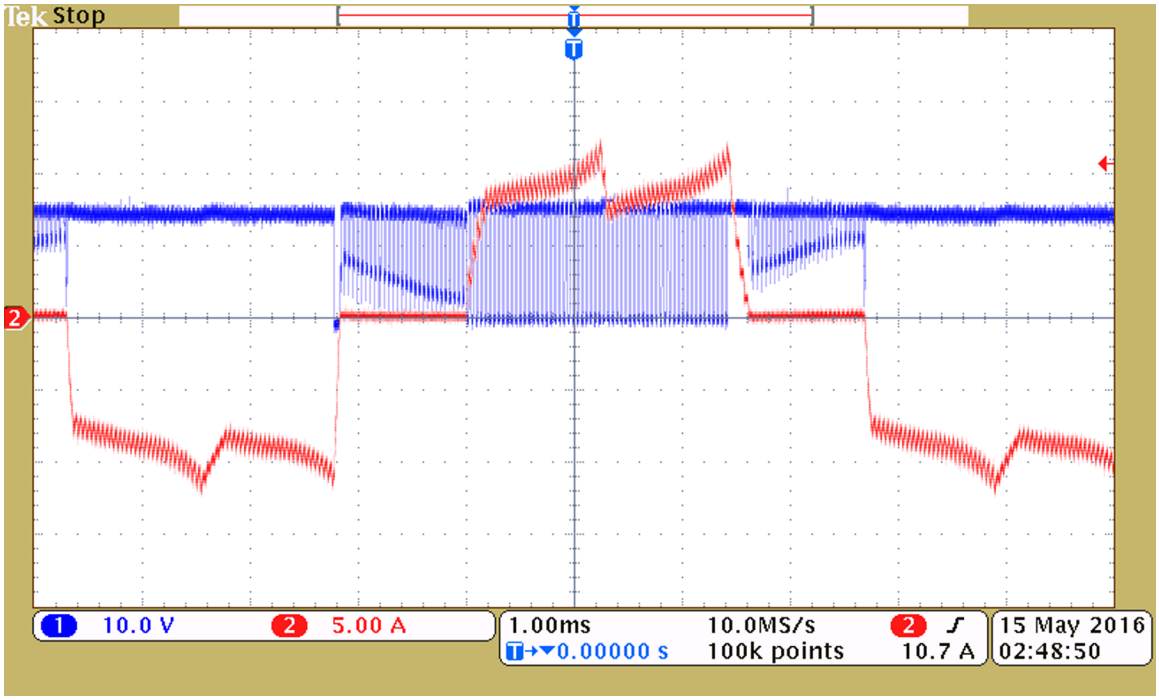

Figure 13. No Current Limit Hit

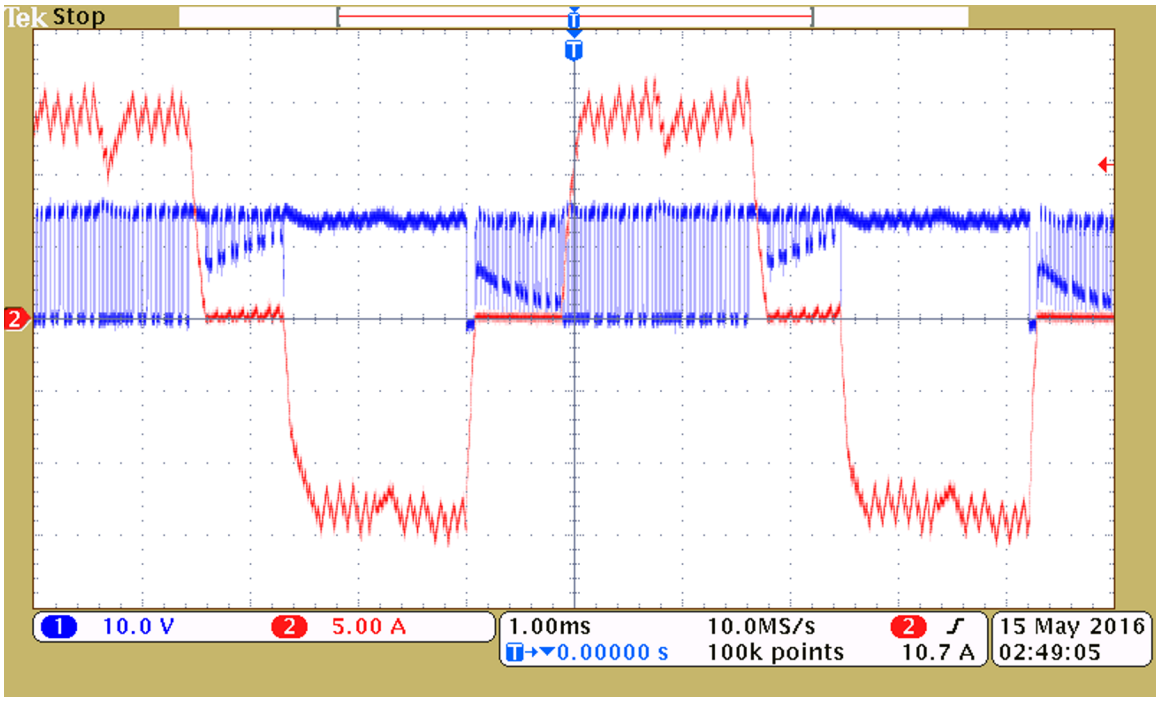

Figure 14. Current Control Feature Limiting Current to 15 A Peak

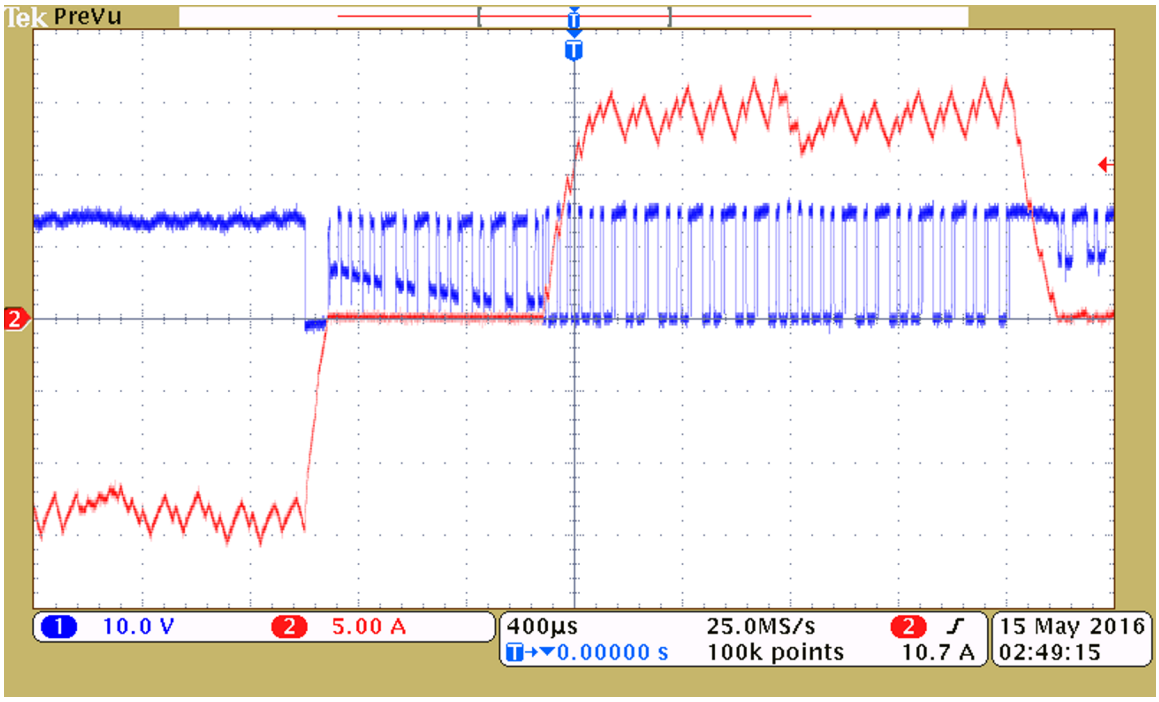

Figure 15. PWM Skip Mode After Reaching Current Limit

6.2 Phase Advance Algorithm

Sensored control is a method of driving a BLDC motor, considering the complexity and reliability of a drive. There are applications that do not use Hall sensors because of cost and feasibility options. In this case, sensor-less control is used, which estimates the rotor position through BEMF.

Adjusting the lead angle while driving a motor at different loads helps improve the overall drive efficiency. In trapezoidal control of motors, the commutation occurs every 60 electrical degrees. The zero cross occurs at 30 degrees. The user can commutate at any point after this 30 degrees of the actual commutation instance. The lead angle may be adjusted up to 30 electrical degrees effectively.

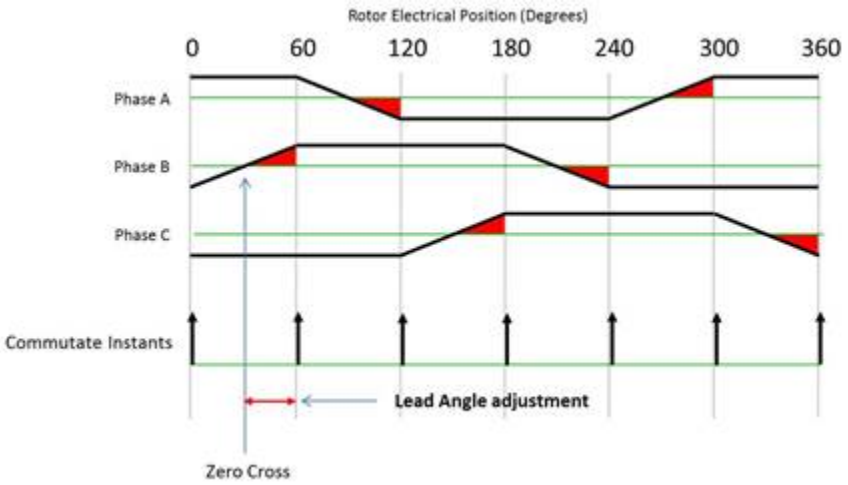

Figure 16. Lead Angle Adjustment

Trapezoidal algorithms have commutation instances occurring every 60 electrical degrees. There is a zero-crossing at 30 electrical degrees after the commutation occurs. The previous diagram shows the complete electrical cycle. The lead angle may be programmable within the limits of 0-to-30 electrical degrees where 0 indicates no lead angle adjustment.

The readings and graph below show the results of lead angle compensation at different load conditions.

- Dyno Controller: Magtrol DSP6001
- Brake: HD-705-6N
- Power Supply: 15 V, 23 A

Table 3. Observation Table for Lead Angle Test

LOAD CONDITION	INPUT VOLTAGE (V)	DIRECTION	SPEED	LEAD ANGLE	DC CURRENT
5 oz-in.	15	CW	~5600	0	—
5 oz-in.	15	CW	~5600	5	—
5 oz-in.	15	CW	~5600	10	4.7
5 oz-in.	15	CW	~5600	20	3.81
5 oz-in.	15	CW	~5600	30	3.48
10 oz-in	15	CW	~5600	0	5.4
10 oz-in	15	CW	~5600	5	5.18
10 oz-in	15	CW	~5600	10	4.96
10 oz-in	15	CW	~5600	20	4.64
10 oz-in	15	CW	~5600	30	4.25
15 oz-in	15	CW	~5600	0	8.5
15 oz-in	15	CW	~5600	5	8.1
15 oz-in	15	CW	~5600	10	7.9
15 oz-in	15	CW	~5600	20	7.7
15 oz-in	15	CW	~5600	30	7.2
20 oz-in	15	CW	~5600	0	13.5
20 oz-in	15	CW	~5600	5	13
20 oz-in	15	CW	~5600	10	12.8
20 oz-in	15	CW	~5600	20	12.4
20 oz-in	15	CW	~5600	30	11.12
25 oz-in	15	CW	~4500	0	22.9
25 oz-in	15	CW	~4900	5	22.9
25 oz-in	15	CW	~5000	10	19.8
25 oz-in	15	CW	~5600	20	16.88
25 oz-in	15	CW	~5600	30	16.2

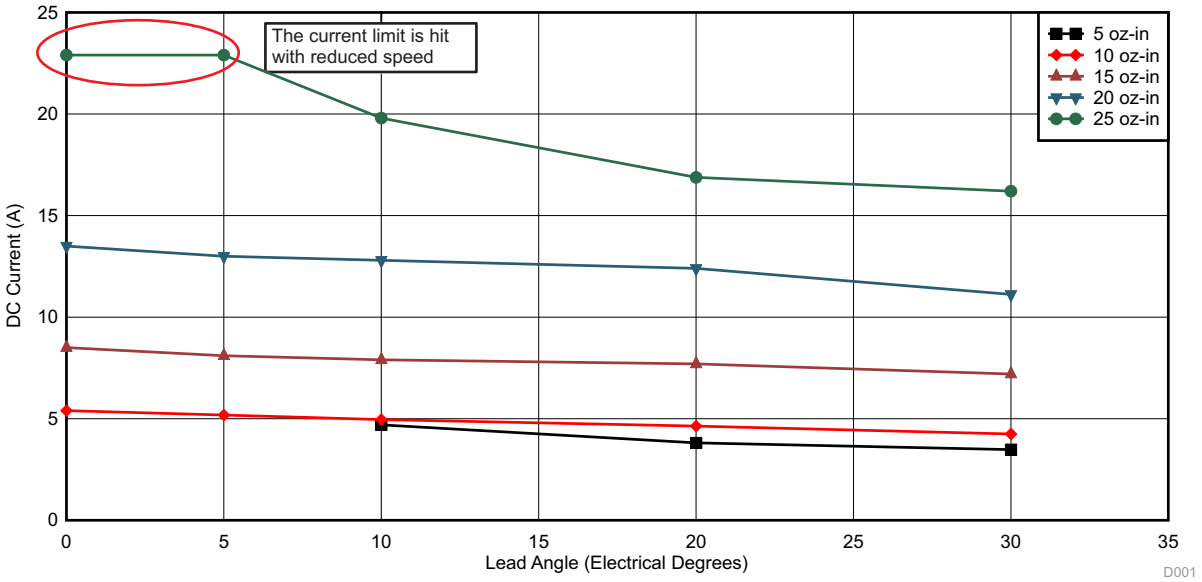

Figure 17. DC Current improvement with Lead Angle Adjustment

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00529.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00529.

7.3 Component Selection Guidelines

Current Shunt Resistor
The current shunt resistor must be placed in a return path, and overall power path must be maintained to be as short as possible to avoid adding resistance. It is desirable to have equal distance from the MOSFET source pin of the bottom switches to the current sense resistor. The resistor value and rated power of the resistor is based on individual application.

$$\begin{aligned} \text{Voltage across Current Shunt} &= R_{Shunt} \times I_{Max} \\ &= 0.0010\Omega \times 50A \\ &= 0.500\ V \\ \text{Measurement after Gain Amplifier (Gain = 4)} &= 0.500 \times 4 \\ &= 2.000\ V \end{aligned} \quad (4)$$

Current Shunt Low-Pass Filter The power stage delivering the power to the motor usually is switching at higher frequencies, which introduces noise on the sensing paths. If not filtered properly, switching noise on the current measurements could trigger false overcurrent conditions. To avoid the noise, a low pass filter is preferred, which passes on relatively cleaner signals to the amplifier where internal gain settings are used to amplify the small signals.

DC Link Clamping Circuitry Design
The DC-link-clamping circuitry in the schematic is intended to prevent DC bus voltage from reaching undesirable voltages. This circuitry may changed based on specific application requirements.

7.4 PCB Layout Recommendations

PCB layout is one of the critical factors in a power tool application as the systems are expected to deliver a significant amount of power with a compact design. The dense PCB is due to space limitations in hand-held power tool applications. The layout of the PCB design needs to be planned carefully to avoid coupling due to large voltage and current transients that occur during the motor operation. The following layout recommendations are not comprehensive, but based on standard practice. Individual designers will need to optimize the design based on each application.

Electrolytic Capacitor Selection and Placement—The electrolytic capacitor in an inverter is subjected to transients every PWM cycle to deliver the current needed. The capacitor should be sized to be able to deliver the required current at full load. Selecting a capacitor with a low-series resistance contributes to lower loss and less heat dissipation in the capacitor, extending the lifetime of the capacitor and the power tool. Selecting a capacitor with higher charge-discharge cycling contributes to improving system life. The electrolytic capacitor should be placed closer to the energy source, minimizing the distance between the capacitor and the MOSFET power stage. Capacitor sizing should be based on the maximum allowable voltage drop at the rated power. The DC link voltage must not go below the minimum voltage operation of the DRV91680 at the rated load (8 V).

Ground Routing—Power ground (PGND) and signal ground must be kept separate and tied together at the ground connection to the power source. This action minimizes possible signal-path ground bouncing due to PWM switching in the power stage. High-current-carrying paths must be properly sized to be able to deliver the required amount of current.

7.5 Layout Prints

To download the layout prints, refer to the design files at TIDA-00529.

7.6 Altium Project

To download the Altium project files, refer to the design files at TIDA-00529.

7.7 Layout Guidelines

To download the layout guidelines, refer to the design files at TIDA-00529.

7.8 Gerber Files

To download the Gerber files, refer to the design files at TIDA-00529.

7.9 Assembly Drawings

To download the assembly drawings, refer to the design files at TIDA-00529.

7.10 Software Files

To download the software files, refer to the design files at TIDA-00529.

8 Terminology

BLDC— Brushless DC

BDC— Brushed DC

9 References

1. Texas Instruments, *Trapezoidal Control of BLDC Motors using Hall Effect Sensors*, Application Report (SPRABQ6)

10 About the Authors

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Revision History B

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2016) to B Revision	Page
• Changed board image to an updated version	1
• Changed Figure 4 schematic to updated schematic	8

Revision History A

Changes from Original (July 2015) to A Revision	Page
• Added new Section 6 *New Features Supported*	12

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