TI Designs

100-V/200-V AC Input 30-W Flyback Isolated Power Supply Reference Design for Servo Drives

TI Designs

This reference design provides isolated 24-V DC, 16-V DC (×3), and 6-V outputs to power the control electronics, IGBT gate drivers, communication interface, and fan for 100-V and 200-V AC input servo drives. The power supply can be either powered directly from three-phase AC mains or can be powered from a DC link voltage. This reference design uses primary-side regulation, quasi-resonant flyback topology, and is rated for a 30-W output. The line and load regulation of the power supply is designed to be within 5%. The power supply is designed to meet the clearance, creepage, and isolation test voltages as per IEC61800-5 requirements.

Design Resources

TIDA-00315	Design Folder
UCC28711	Product Folder
LMS33460	Product Folder
TPS54332	Product Folder

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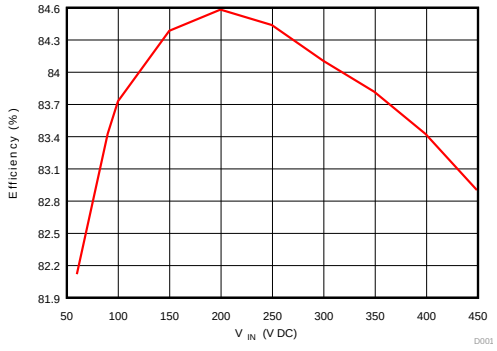
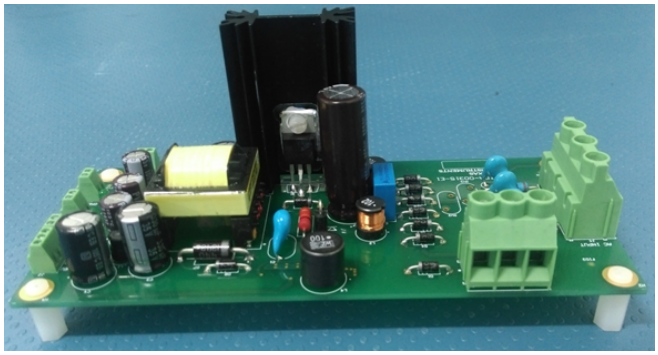
Design Features

- 30-W Main Power Supply for Servo Drives
- Can Operate With DC (60-V DC to 450-V DC Max)
- Load and Line Regulation: 5%
- Peak Efficiency of 85%
- Input UV/OV, Output Overload, and SC Protection
- Protection Against Loss of Feedback
- Lower Cost Solution Using UCC28711 Through Primary Side Regulation, Eliminating Feedback Loop
- Option of Measuring DC Link Voltage Through Transformer Winding
- Quasi Resonant Mode Controller Improves EMI
- Operating Temperature Range: –10ºC to 65ºC Max

Featured Applications

- Servo Drives
- Industrial Inverters and Solar Inverters
- UPS Systems
- Variable Speed AC/DC Drives





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1 System Description

Any motor drive does motor control function but beyond controlling the motor, other system functions also exist, such as applications management, communication, safety, HMI, and so on. Depending on the drive architecture, the main processor can manage multiple functions. Single-chip compact servo drives use a microcontroller (or microprocessor) for control, application and communication. Two-chip compact servo drives use one microcontroller as well as one microprocessor to perform different functions; for example, the microcontroller manages control loop and PWM generation whereas the microprocessor manages motion and position feedback from the motor. The power section for all servo drives contain a rectifier, DC link, inrush current limiting, and IGBT-based inverter (either discrete or using an intelligent power module [IPM]).

The main power supply, either powered directly from the AC mains or DC link is used to generate multiple voltage rails, which are required for the operation of all the control electronics in the drive. Traditional way of implementing the main power supply is to use fly back converter with PWM controller IC's such as the UCC3842/UCC3843/UCC3844. Optocouplers are used for isolated feedback to regulate the output voltage. In case the components used in the feedback path fail, the output may reach a dangerously high level, damaging all the electronic components. Controllers like the UCC3842 also possess other challenges in limiting the power during short circuit across wide input voltage range and power dissipation in the resistors used in the startup circuit.

Most of the servo drives use IPMs for IGBT inverter stage. An IPM is a kind of modularized device, integrated by the IGBT and circuits that have the functions of signal processing, self-protection, and diagnosis. IPMs have the advantages of small volume, light weight, simple design, and high reliability. As IPMs have short wiring between gate drive and the IGBT, and the power levels being small, making driving without reverse bias possible. Many low-power IPMs operate on single 15-V (or 16-V) power supply and use bootstrap-based gate drivers. In such a case, it is sufficient to generate a single 15 V (or 16 V) with the power capability to drive all six gate drivers. Figure 1 shows an example of an IPM.

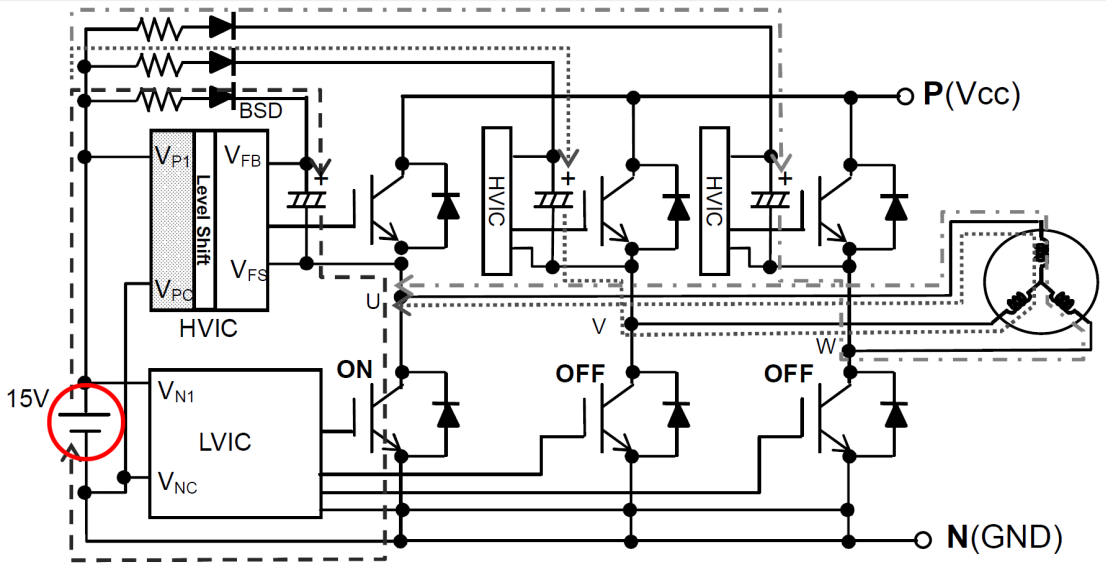

Figure 1. IPM Requiring Single 15-V Supply

Figure 2 shows an IPM with an individual pre-driver. This configuration necessitates four control power supplies: one supply for all the lower IGBTs and three individual supplies for the upper IGBTs with a proper isolation circuit. The supply voltage of each pre-driver is usually in the range of 13.5 to 16.5 V.

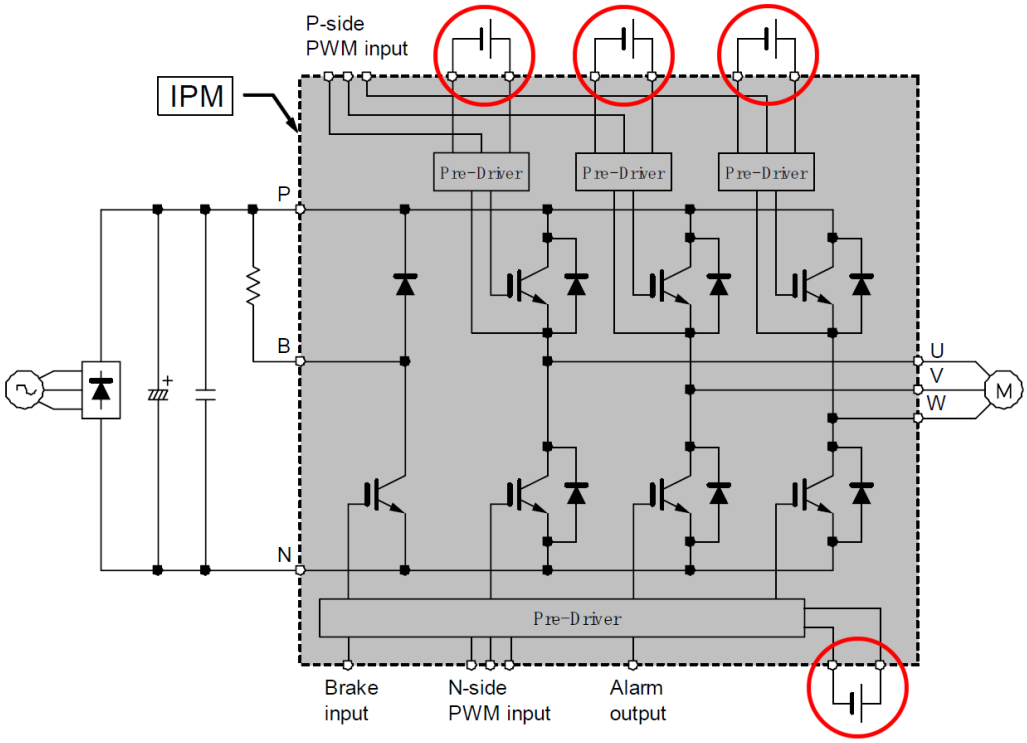

Figure 2. IPM Requiring Individual Power Supplies

The primary objective of this design is to design a power supply with a reduced BOM cost and a reusable design for drives operating at both 100-V and 200-V inputs. Other benefits include:

- Constant uniform power limit throughout the input range
- Reduced BOM cost using UCC28711 through primary side regulation, eliminating isolated secondary feedback
- Protection against component failure in feedback path

This reference design provides isolated 24-V DC, 16-V DC (×3), and 6-V outputs to power the control electronics in servo drives. The power supply can be either powered directly from three-phase AC mains or from DC-link voltage. This reference design uses quasi resonant flyback topology and is rated for a 30-W output. The line and load regulation of the power supply is designed to be within 5%. The power supply is designed to meet the clearance, creepage, and isolation test voltages as per IEC61800-5 requirements.

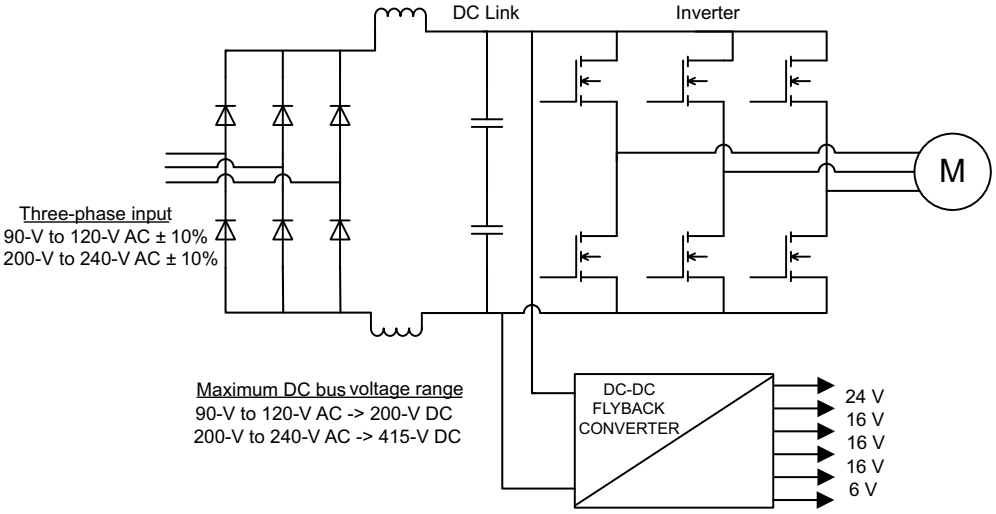

Figure 3. Servo Drive Topology

1.1 Power Supply Requirements

The main power supply requires the following to be used in servo drives applications:

- Input range from 60-V DC to 450-V DC
- Output power: 30 W
- Switching frequency: > 40 kHz
- Quasi resonant mode controller
- Expected efficiency: 80%
- Ripple voltage on secondaries: 500 mV
- Load and line regulation: 5%
- Input UV/OV shutdown
- Output overload shutdown with power limit
- Can be powered from AC mains or from DC link
- Isolated measurement of DC-link voltage (input) through indirect technique
- Detection of single-phase scenario through DC-link measurement
- EMC filter and surge protection required
- Ambient temperature: 65°C max
- Clearance and creepage as per IEC 61800-5-2

2 Design Features

This power supply design is intended for a low-cost implementation with omission of feedback components. The power supply is designed to operate across a wide input range, which suits drives operating from 100-V and 200-V AC inputs. The power supply includes the following protection features:

- Output overvoltage fault
- Input undervoltage fault
- Internal over-temperature fault
- Primary overcurrent fault

2.1 Topology Selection

Flyback topology is the most widely used SMPS topology in most of the variable speed drives; the power rating is below 150 W and it requires only a single magnetic element. This criterion serves isolation and step-up/step-down conversions as well as stores energy. Flyback topology does not require any output inductors other topologies demand. Other advantages include easy-to-create multiple output voltages, a very low component count and is affordable.

2.2 Design Requirements

To translate the aforementioned requirements to the sub-system level, the PWM controller, MOSFETs, and transformer require the following:

- PWM controller
  - Accurate voltage and constant current regulation primary-side feedback
  - Primary-side feedback, eliminating the need for optocoupler feedback circuits
  - Discontinuous conduction mode with valley switching to minimize switching losses
  - Protection functions including
    - Input/output overvoltage fault
    - Input undervoltage fault
    - Internal overtemperature fault
    - Primary overcurrent fault
    - Loss of feedback signal
- Power MOSFETs
  - Should have a rated V_{DS} ≥ 650 V to support a 450-V DC input
  - Should support a 1.5-A (min) drain current

- Transformer specifications (as per IEC61800-5-1)
  - Four isolated secondary outputs and one isolated auxiliary winding (see Figure 4):
    - Vout1 = 24 V/24 W
    - Vout2 = 16 V/1 W
    - Vout3 = 16 V/1 W
    - Vout4 = 16 V/1 W
    - Vaux = 15 V/6 W
  - Switching frequency = 67 kHz
  - Primary to secondary isolation = 7.4 kV for 1.2/50-µs impulse voltage
  - Type test voltage:
    - Primary to Secondary = 3.6 kV_{RMS}
    - Secondary1 to Secondary2 = 1.8 kV_{RMS}
    - Secondary2 to Secondary3 = 1.8 kV_{RMS}
    - Secondary3 to Secondary4 = 1.8 kV_{RMS}
    - Secondary1 to Secondary4 = 1.8 kV_{RMS}
  - Spacings:
    - Primary to Secondary clearance = 8 mm
    - Secondary1 to Secondary2 clearance = 5.5 mm
    - Secondary2 to Secondary3 clearance = 5.5 mm
    - Secondary3 to Secondary4 clearance = 5.5 mm
    - Creepage distance = 9.2 mm
  - Functional isolation primary and secondary's = 2-kV DC
  - DC isolation between secondary's = 2-kV DC

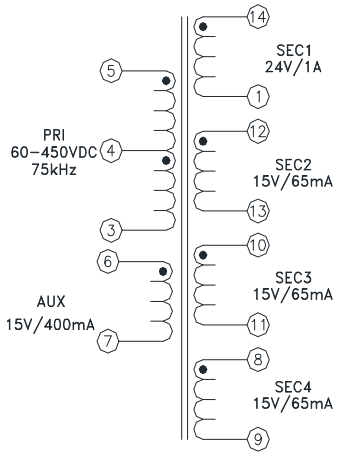

Figure 4. Transformer Configuration

3 Block Diagram

Figure 5 shows the simplified implementation diagram for the TIDA-00315. The transformer has five secondary windings (four isolated and one non-isolated). The power device is a 750-V MOSFET. In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary.

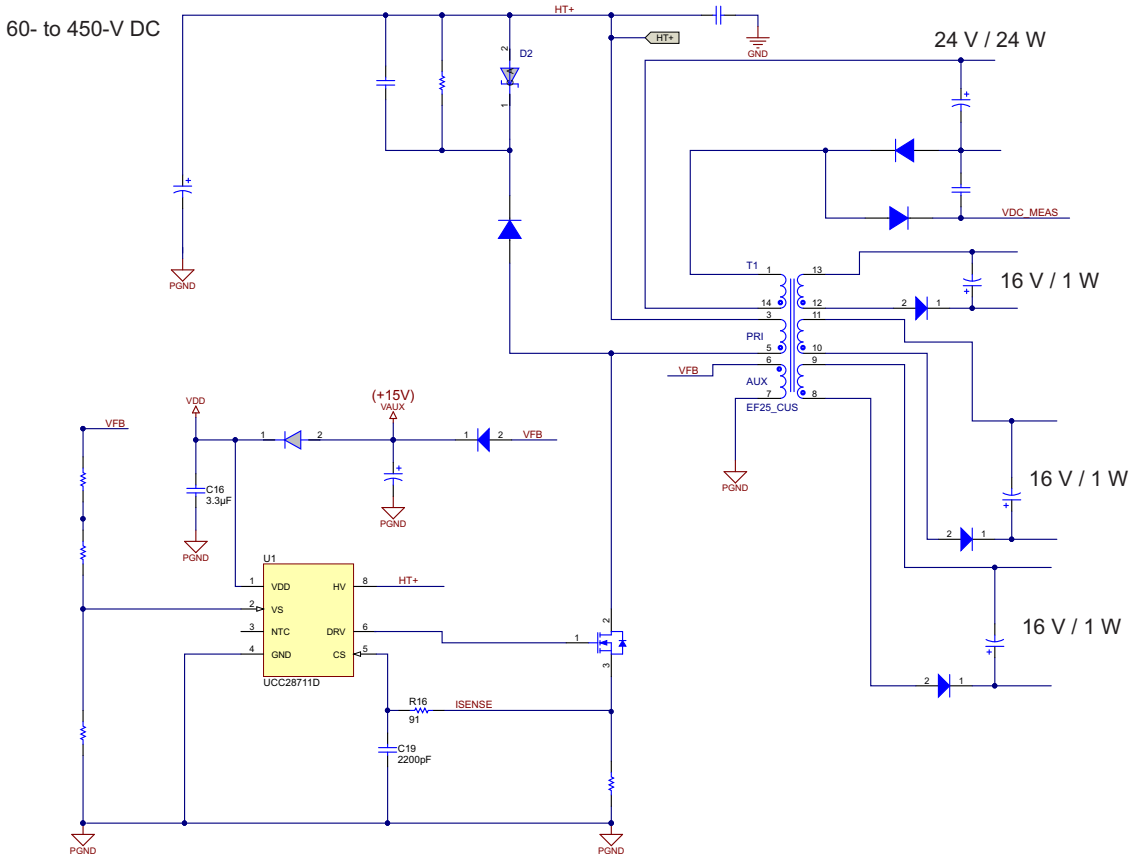

Figure 5. Simplified Diagram of Solution

To represent the secondary output voltage on the auxiliary winding accurately, the discriminator inside the input capacitor (IC) reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V. Temperature compensation on the VS reference voltage of –0.8 mV/°C offsets the change in the output rectifier forward voltage with temperature. The feedback resistor divider is selected as outlined in the VS pin description.

3.1 Primary-Side Current Regulation

When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the undervoltage lockout (UVLO) turn-off threshold.

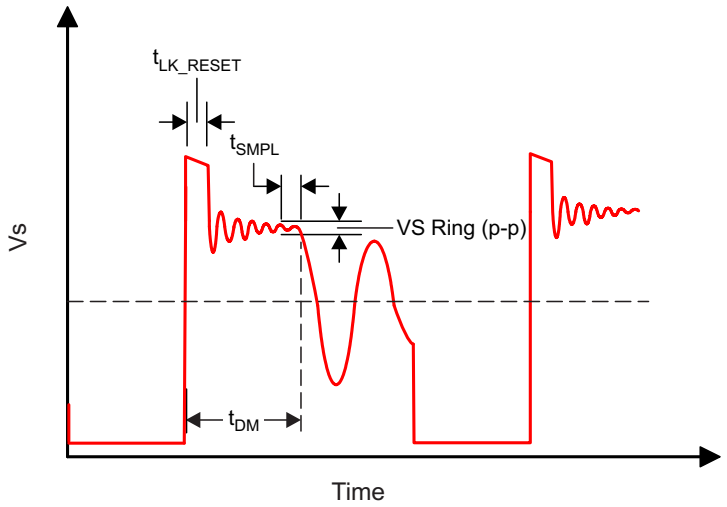

Figure 6. Aux Waveform Sampling

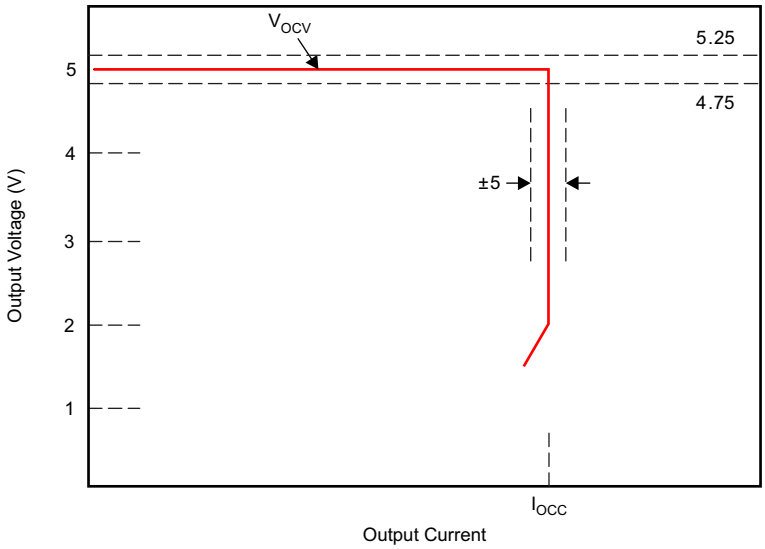

Figure 7. Power Limit

4 Highlighted Products

This reference design features the following devices, which were selected based on their specifications:

- UCC28711: Constant-voltage, constant-current PWM controller with primary-side regulation
- LMS33460: 3-V undervoltage detector
- TPS54332: 3.5 to 28-V input, 3.5-A, 1-MHz step-down converter with Eco-mode

For more information on these devices, see their respective product folders at TI.com or click on the links under Design Resources.

5 Component Selection and Circuit Design

5.1 Component Selection

The following components are selected based on their specifications.

5.1.1 UCC28711

The UCC28700 is a flyback power supply controller that provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for optocoupler feedback circuits. The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The controller has a maximum switching frequency of 130 kHz and it allows for a shut-down operation using NTC pin.

5.1.2 LMS33460

The LMS33460 is an undervoltage detector with a 3.0-V threshold and extremely low power consumption. The LMS33460 is specifically designed to monitor power supplies accurately. This IC generates an active output whenever the input voltage drops below 3.0 V. This part uses a precision on-chip voltage reference and a comparator to measure the input voltage. Built-in hysteresis helps prevent erratic operation in the presence of noise.

5.1.3 TPS54332

The TPS54332 is a 28-V, 3.5-A non-synchronous buck converter that integrates a low $R_{DS(on)}$ high-side MOSFET. To increase efficiency at light load, a pulse-skipping Eco-mode feature is automatically activated. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input UVLO. An overvoltage transient protection circuit limits voltage overshoots during start-up and transient conditions. A cycle-by-cycle current limit scheme, frequency fold back and thermal shutdown protect the device and the load in the event of an overload condition.

5.2 Circuit Design

5.2.1 Input Section

The AC input is full-wave rectified by diodes D4 through D6 and D14 through D16. Fusible resistors RF1 through RF3 provide in-rush current limiting and protection against catastrophic circuit failure. Capacitor C7 is used to filter the rectified AC supply. There is a provision to filter the DC input using two inductors L2 and L3.

5.2.1.1 Input Diode Bridge

The input bridge is selected by using the following equations:

$$P_{INMAX} = \frac{P_{OUT}}{\eta} = \frac{30}{0.8} = 37.5 \text{ W} \quad (1)$$

$$I_{INRMS} = \frac{P_{INMAX}}{\sqrt{3} \times V_{ACMIN} \times \cos\varnothing} = \frac{37.5}{1.732 \times 65 \times 0.6} = 0.555 \text{ A} \quad (2)$$

where

- cosø is the power factor, which is assumed to be 0.6

The minimum voltage rating of the rectifier is given by Equation 3:

$$V_{DCMIN} = (V_{ACMAX} \times 1.414) + (0.15 \times V_{ACMAX} \times 1.4141) = (320 \times 1.414) + (0.15 \times 320 \times 1.414) = 520.352 \text{ V} \quad (3)$$

Considering a raise in DC bus voltage due to regenerative action, diodes with 1000-V, 1-A ratings are used for the three-phase bridge rectifier.

5.2.1.2 Input Capacitors (CIN)

The DC input bulk capacitor C7 provides a smooth DC voltage by filtering low frequency AC ripple voltage.

A single 22-µF/500-V capacitor (UCY2H220MHD) is connected as DC bulk capacitor. Based on the requirement on input side, this capacitor value can be changed.

5.2.1.3 Input Filter Inductors

The required corner frequency of the filter is given by Equation 4:

$$f_C = f_{SW} \times 10^{\frac{Att}{40}} \quad (4)$$

where

- f_C is the desired corner frequency of the filter
- f_{SW} is the operating frequency of the power supply (67 kHz)

Assuming a 60-dB attenuation at the switching frequency of the power supply, the cut-off frequency of the filter is given by

$$f_C = 67\text{ k} \times 10^{\frac{-60}{40}} = 2.1\text{ kHz} \quad (5)$$

The cut-off frequency can also be calculated using Equation 6:

$$f_C = \frac{1}{2\pi\sqrt{LC}} \quad (6)$$

Back-calculating the value of inductor required using Equation 6 leads to an inductance of 60 µH, which can be split into two to be placed on both the lines of the DC bus.

NOTE: For this design, none of the inductors are used. L1 and L2 are just replaced by a short.

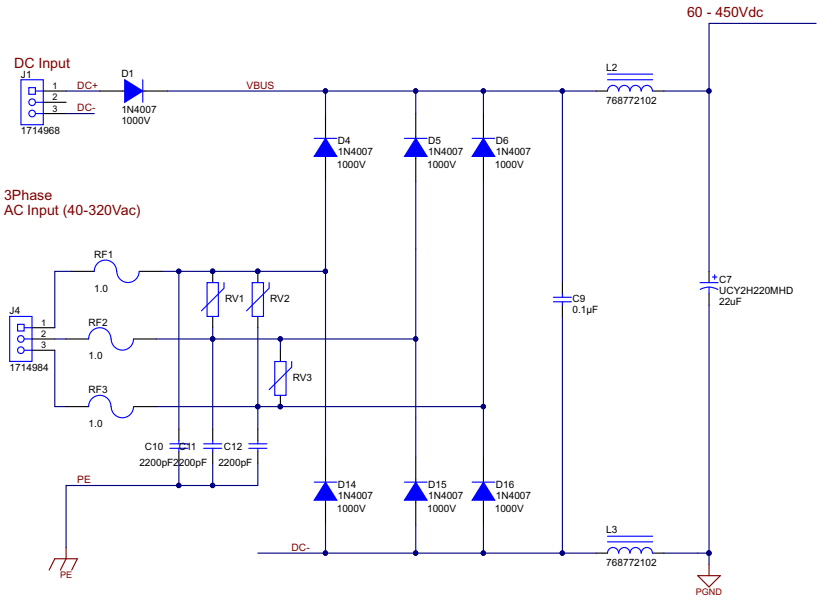

Figure 8. Input Section

5.2.1.4 Surge Protection

Considering 320-V AC input with a 10% variation, MOV of 390-V AC with a peak current rating of 2500 A specified for 8/20-µs waveform has been used to suppress surge at the input. For 100-V rated drives, the voltage rating of the MOV needs to be lowered.

5.2.2 Controller Section

5.2.2.1 VDD Capacitor Selection (C_{DD})

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the UCC28711 family. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The C_{VDD} is selected using Equation 7 based on the desired startup time (dt_{CDDS}) of the UCC28700 controller and knowing the start current (I_{START}), as well as, the UCC28711 device startup threshold ($V_{VDD(on)}$). Assuming startup time for the device (dt_{CDDS}) is 1 second, the value of VDD capacitor can be calculated as in Equation 7. The start current for the UCC28711 is 1.5 µA, the start-up threshold $V_{VDD(on)}$ is 21 V, and I_{HV} is 250 µA (typ).

$$C_{VDD} = \frac{\left(I_{HV} - I_{START}\right) \times dt_{CDDS}}{V_{VDD(ON)}} = \frac{\left(250\ \mu - 1.5\ \mu\right) \times 1}{21} = 11.83\ \mu F \quad (7)$$

In this design, a 10-µF capacitor is used on VDD pin.

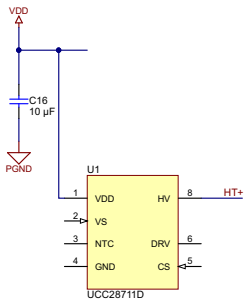

Figure 9. VDD Capacitor

Note that after C_{VDD} has been charged up to the device turn-on threshold ($V_{VDD(on)}$), the UCC28711 initiates three small gate drive pulses (DRV) and start sensing current and voltage (see Figure 10). If a fault is detected, such as an input undervoltage, the UCC28711 terminates the gate drive pulses and discharges CDD to initiate an undervoltage lockout. This capacitor will be discharged with the run current of the UCC28711 (I_{RUN}) until the VDD turnoff ($V_{VDD(off)}$) threshold is reached. Note the CDD discharge time (t_{CDD}) from this forced soft start can be calculated knowing the controller run current (IRUN) without out gate driver switching, the controller's VDD turnoff threshold ($V_{VDD(off)}$), and the following equations. If no fault is detected, the UCC28711 continues to drive the MOSFET and control the input and output currents, and a soft start will not be initiated.

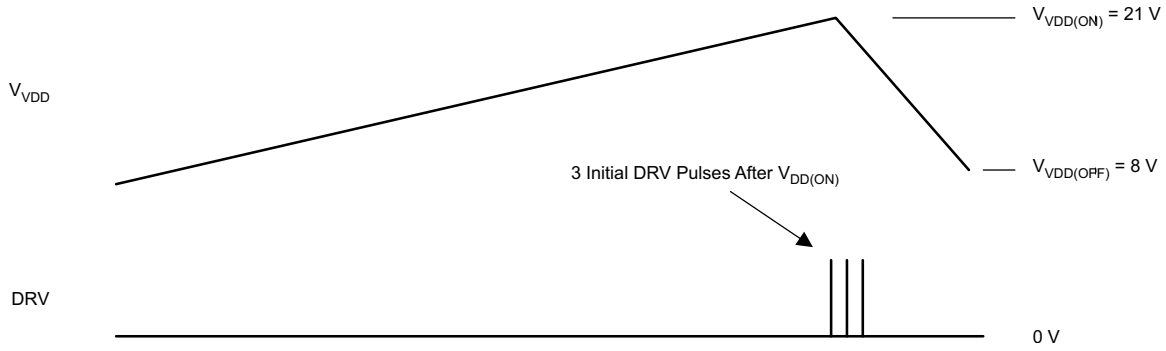

Figure 10. Power-On Sequence

5.2.2.2 Calculation of Duty Cycle

The transformer demagnetizing duty cycle (D_{MAG}) is fixed to 42.5% based on the UCC28711 control law methodology.
$D_{MAG} = 0.425$

T_R is the estimated period of the LC resonant frequency at the switch node.
$T_R = 2\ \mu s$

Calculate maximum duty cycle (D_{MAX}):

$$D_{MAX} = 1 - D_{MAG} - f_{MAX}\frac{T_R}{2} = 1 - 0.425 - 70\ k\frac{2\ \mu}{2} = 0.505 \quad (8)$$

5.2.2.3 Calculation of Transformer Peak Current

Calculate the transformer primary peak current (I_{PPK}) based on a minimum flyback input voltage. This calculation includes the reduction in flyback input voltage caused by the ripple voltage across the input capacitor.

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times V_{INMIN} \times D_{MAX}} = \frac{2 \times 30}{0.8 \times 60 \times 0.505} = 2.475\ A \quad (9)$$

5.2.2.4 Transformer Calculations

5.2.2.4.1 Calculation of Primary Inductance (L_{PM})

The primary magnetizing inductance (L_{PM}) is selected based on minimum flyback input voltage, transformer, primary peak current, efficiency, and maximum switching frequency (f_{MAX}).

$$L_{PM} = \frac{\frac{2 \times P_{OUT}}{\eta}}{I_{PPK}^2 \times f_{MAX}} = \frac{\frac{2 \times 30\ W}{0.8}}{2.69^2 \times 67\ kHz} = 154.7\ \mu H \quad (10)$$

The design uses a transformer with L_{PM} equal to 150 µH.

5.2.2.4.2 Calculation of Turns Ratio

Assuming:

- V_{QAON} = 2 V, estimated voltage drop across FET during conduction
- V_{RCS} = 0.75 V, voltage drop across current sense resistor
- V_{DG} = 0.8 V, estimated forward voltage drop across output diode

The transformer turns ratio primary to secondary (N_{PS}) is calculated in Equation 11 based on volt-second balance. Note in the Equation 11, L_{SM} is the secondary magnetizing inductance.

$$N_{PS} = \frac{N_P}{N_S} = \sqrt{\frac{L_{PM}}{L_{SM}}} = \frac{D_{MAX} \times \left(V_{INMIN}\sqrt{2} \times 0.6 - V_{QAON} - V_{RCS}\right)}{D_{MAG} \times \left(V_{OUT} + V_{DG}\right)} \approx 2.5 \tag{11}$$

Assuming:

- V_{DDMIN} = 8 V, UCC28711 minimum VDD voltage before UVLO turnoff
- V_{DE} = 0.8 V, estimated auxiliary diode forward voltage drop
- V_{OUT_INIT} = 13 V, minimum voltage on the output at initial turn on.

The transformer auxiliary to secondary turns ratio (NAS) is calculated in Equation 12.

$$N_{AS} = \frac{N_A}{N_S} = \frac{V_{DDMIN} + V_{DE}}{V_{OUT\_INIT} + V_{DG}} = \frac{8 + 0.8}{13.8} = 0.64 \tag{12}$$

5.2.2.4.3 Calculation of Transformer Primary RMS Current (I_{PRMS})

$$I_{PRMS} = I_{PPK}\sqrt{\frac{D_{MAX}}{3}} = 2.475 \times \sqrt{\frac{0.505}{3}} = 1.0151 \text{ A} \tag{13}$$

5.2.2.4.4 Calculation of Transformer Secondary RMS Current (I_{SRMS})

Transformer secondary peak currents (I_{SPK}) are calculated and RMS currents for each secondary are calculated using the following equations:

$$I_{SRMS} = I_{SPK}\sqrt{\frac{D_{MAG}}{3}} \tag{14}$$

$$I_{S1PK}(24\text{ V Output}) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{48}{24.8 \times 0.425} = 4.55 \text{ A } (1.714 \text{ A}_{RMS}) \tag{15}$$

$$I_{S2PK}(16\text{ V Output}) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{2}{16.8 \times 0.425} = 0.28 \text{ A } (0.105 \text{ A}_{RMS}) \tag{16}$$

$$I_{S3PK}(16\text{ V Output}) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{2}{16.8 \times 0.425} = 0.28 \text{ A } (0.105 \text{ A}_{RMS}) \tag{17}$$

$$I_{S4PK}(16\text{ V Output}) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{2}{16.8 \times 0.425} = 0.28 \text{ A } (0.105 \text{ A}_{RMS}) \tag{18}$$

$$I_{AUX\_PK}(15\text{ V Output}) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{12}{15.8 \times 0.425} = 1.788 \text{ A } (0.672 \text{ A}_{RMS}) \tag{19}$$

5.2.2.5 Primary Side Regulation

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. To represent the secondary output voltage on the auxiliary winding accurately, the discriminator (inside the UCC28711) reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V; it is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Do not place a filter capacitor on this input, which would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC input run, stop thresholds, and compensate the current-sense threshold across the AC input range. This information is sensed during the MOSFET on-time. For the AC-input run/stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage.

The values for the auxiliary voltage divider upper-resistor RS1 and lower-resistor RS2 can be determined by the following equations. Note RS1 so the converter will go into UVLO when the input is below 80% of the minimum specified input voltage.

$$R_{S1} = \frac{\frac{N_{AS}}{N_{PS}} V_{INMIN} \sqrt{2} \times 0.8}{I_{VSL(RUN)}} = \frac{\frac{N_{AS}}{N_{PS}} V_{INMIN} \times 0.8}{I_{VSL(RUN)}} = \frac{\frac{0.64}{2.5} 100 \times 0.8}{225\ \mu} = 91\,k\Omega \text{ (Rounded off to 86.8 k}\Omega\text{)} \quad (20)$$

where

- N_{AS} and N_{PS}: transformer turns ratios
- $I_{VSL(run)}$: the run-threshold for the current pulled out of the VS pin during the MOSFET on-time (equal to 220 µA max from the UCC28711 datasheet)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} = \frac{86.8K \times 4.05}{(0.64 \times 24.6) - 4.05} = 30.061\,k\Omega \text{ (Rounded off to 28 k}\Omega\text{)} \quad (21)$$

where

- V_{OCV}: regulated output voltage of the converter
- V_F: secondary rectifier forward voltage drop at near-zero current
- N_{AS}: transformer auxiliary-to-secondary turns ratio
- R_{S1}: the VS divider high-side resistance
- V_{VSR}: CV regulating level at the VS input (equal to 4.05 V typical from the UCC28711 datasheet)

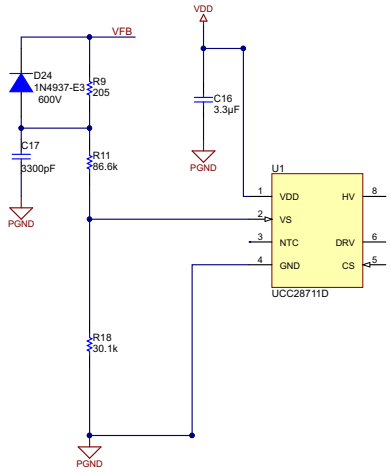

Figure 11. Primary Feedback

The output overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal VOUT, the device stops switching and the internal current consumption is I_{FAULT}, which discharges the VDD capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

Protection is included in the event of component failures on the VS pin. If a complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

5.2.2.6 MOSFET Selection

To meet the required voltage and current specifications, 650-V/7-A rated MOSFET (AOT7S65) with the following characteristics has been chosen:

- $R_{DS(on)}$ = 0.65 Ω
- C_{OSS} = 23 pF

The maximum FET gate drive turn ON current (limited by the UCC28711) is I_{DRIVE} = 0.025 A (maximum gate sink current is internally limited and is approximately 0.2 A).

Q_g = 9.2 nC, gate charge just above the miller plateau.

$$\text{Estimated } V_{DS} \text{ rise and fall time} = t_r = \frac{Q_g \times 2}{I_{drive}} = \frac{9.2\ \text{nC} \times 2}{0.2\ \text{A}} = 92\ \text{ns} \tag{22}$$

Power loss by driving the FET's gate (P_g):

- $P_g = 14\ V \times Q_g \times f_{MAX} = 14\ V \times 13\ nC \times 67k = 12.2\ mW$
- Qg1, Gate charge at 14 V drive (see Figure 12)
- Vg = 14 V (from UCC28711 datasheet)

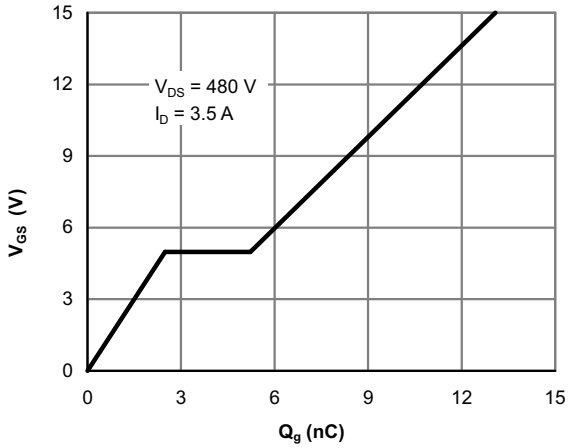

Figure 12. Gate-Charge Characteristics for MOSFET

Calculating the average input voltage to the flyback at the maximum input voltage (V_{INMAX}):

$$V_{FLY} = V_{INMAX} \times \sqrt{2} - \frac{V_{INRIPPLE}}{2} - 2 \times V_{FDA} = 320 \times \sqrt{2} - \frac{36.76}{2} - 2 \times 0.8 = 432.57\ V \tag{23}$$

FET average switching loss (P_{SW}):

$$P_{SW} = \left(V_{FLY} - \left(V_{OUT} + V_{VDG}\right) \times N_{PS}\right) \frac{I_{PPK} \times t_r \times f_{MAX}}{2} = \left(432.57 - \left(24 + 0.8\right) \times 2.5\right) \frac{2.69 \times 52.5\ n \times 67\ k}{2} = 1.75\ W \tag{24}$$

FET C_{OSS} power dissipation (P_{COSS}):

Average FET drain to source capacitance = 23 pF

$$P_{COSS} = \frac{C_{OSS}}{2} \times V_{FLY}^2 \times f_{MAX} = \frac{23\ p}{2} \times 432.57^2 \times 67\ k = 0.144\ W \tag{25}$$

Power loss from $R_{DS(on)}$ (P_{RDSON})

$$P_{RDSON} = I_{PRMS}^2 \times R_{DSON} = 1.1^2 \times 0.65 = 0.786 \text{ W} \quad (26)$$

Total power loss per MOSFET = 1.75 + 0.0122 + 0.786 + 0.144 = 2.6922 W

5.2.2.7 MOSFET Thermal Calculations

Thermal resistance of MOSFET, junction to case, max = 1.2°C/W

Thermal resistance of heat sink, max = 9°C/W (for heat sink 513201B02500G)

MOSFET temperature rise = (1.2 + 9) × 2.7362 = 28°

With an ambient temperature varying from −20°C/W to 65°C/W, the FET temperature would be in the range from 8°C to 93°C (less than 150°C as specified in datasheet).

A MOSFET with voltage rating of ≥650 V can be used if a higher de-rating is required to enhance reliability.

5.2.2.8 Current Sensing

Based on a nominal maximum current sense signal of 0.75 V, the sense resistor is calculated as given in Equation 27.

$$R_{CS} = \frac{0.75}{I_{PPK}} = \frac{0.75}{2.69} = 0.278\ \Omega \quad (27)$$

The actual value of sense resistor needs to be tuned based on the allowable power limit during fault conditions. In this design, a 0.27-Ω resistor is used as R_{CS}.

Nominal current sense resistor power dissipation is calculated in Equation 28.

$$P_{RCS} = I_{PRMS}^2 \times R_{CS} = 1.1^2 \times 0.27 = 0.3267 \text{ W} \quad (28)$$

The UCC28711 always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.78 to 0.195 V. There is additional protection if the CS pin reaches 1.5 V, which results in a UVLO reset and restarts sequence.

5.2.2.9 Line Compensation

The current-sense (CS) pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The current-sense threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. The series resistor RLC provides the function of feed-forward line compensation to eliminate change in IPP due to change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. The value of R_{CS} is determined by the target output current in constant-current (CC) regulation. The value of RLC can be determined by Equation 29:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} = \frac{25 \times 86.8\text{ K} \times 0.27 \times 300\text{ n} \times 2.5}{150\ \mu} = 2.93\ \text{k}\Omega \quad (29)$$

where

- R_{LC}: Line compensation resistor
- R_{S1}: VS pin high-side resistor value
- R_{CS}: current-sense resistor value
- T_D: current-sense delay including MOSFET turn-off delay; add 50 ns to MOSFET delay
- N_{PA}: transformer primary-to-auxiliary turns ratio
- L_P: transformer primary inductance
- K_{LC}: current-scaling constant (equal to 25 A/A from datasheet of UCC28711)

NOTE: The value of R_{LC} may require adjustments based on the noise or ringing on the current sense which is dependent on routing of the signals. A 91-Ω resistor is used in the design.

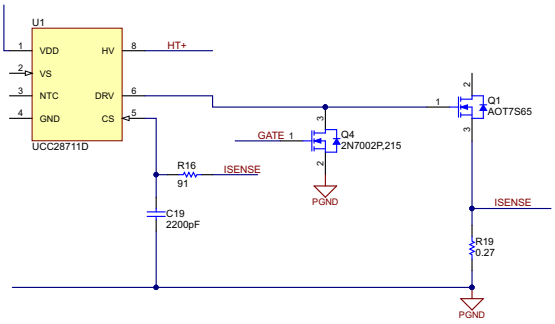

Figure 13. Current Sense

5.2.2.10 MOSFET Gate-Drive

The DRV pin of the UCC28711 is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turn-on characteristic of the driver is a 25-mA current source, which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the low-side driver $R_{DS(on)}$ and any external gate-drive resistance. To improve the efficiency and reduce switching loss in the power device, an external BJT based current buffer may be used to drive MOSFET's with higher voltage rating having high Qg.

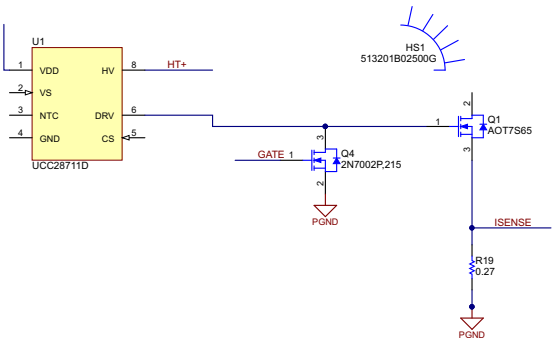

Figure 14. MOSFET Gate Drive

The turning off the MOSFET Q1 (in case of undervoltage and overvoltage condition) is taken care by the LMS33460 (as explained in Section 5.2.4.1). However, the output of the LMS33460 is also connected to the gate of MOSFET Q1 through another smaller switch Q4. This will take care of any kind of turn-off of the device (the three pulses that comes from the device while starting the switching are also prevented).

5.2.3 Output Diodes

5.2.3.1 24-V Output Diode

Calculate diode reverse voltage (V_{RDG})

$$V_{RDG1} = V_{OUT1} + \frac{V_{INMAX}\sqrt{2}}{N_{PS}} = 24 + \frac{320\sqrt{2}}{2.5} = 205 \text{ V} \quad (30)$$

Calculate peak output diode (I_{DGPK})

$$I_{DG1PK} = I_{S1PK} = 4.55 \text{ A} \quad (31)$$

This design uses a schottky diode with a 4-A/400-V rating (MUR440) with a forward voltage drop (V_{FDG}) of 1.25 V. V_{FDG} = 1.25 V; Estimated diode power loss (P_{DG}).

$$P_{DG1} = \frac{P_{OUT1} \times V_{FDG}}{V_{OUT}} = \frac{24 \times 1.25}{24} = 1.25 \text{ W} \quad (32)$$

5.2.3.2 16-V Auxiliary Output Diode

Calculate diode reverse voltage (V_{RDG})

$$V_{RDG2} = V_{OUT2} + \frac{V_{INMAX}\sqrt{2}}{N_{PS}} = 16 + \frac{320\sqrt{2}}{3.7} = 138 \text{ V} \quad (33)$$

Calculate peak output diode (I_{DG2PK})

$$I_{DG2PK} = I_{AUX\_PK} = \frac{0.28 \text{ A}}{0.105 \text{ Arms}} \quad (34)$$

This design has a 3-A, 200-V super-fast rectifier (MURS320-13-F) with a forward voltage drop (V_{FDG}) of 875 mV at 3 A.

Estimated diode power loss (P_{DG2})

$$P_{DG2} = \frac{P_{OUT2} \times V_{FDG2}}{V_{OUT2}} = \frac{1 \times 0.875}{16} = 0.054 \text{ W} \quad (35)$$

NOTE: The same diode has been used for all 16-V outputs.

5.2.3.3 15-V Auxiliary Output Diode

Calculate diode reverse voltage (V_{RDG})

$$V_{RDG\_AUX} = V_{OUT\_AUX} + \frac{V_{INMAX}\sqrt{2}}{N_{PS}} = 15 + \frac{320\sqrt{2}}{3.7} = 137 \text{ V} \quad (36)$$

Calculate peak output diode (I_{DG2PK})

I_{AUX_PK} = 1.788 A (0.672 A_{RMS})

This design uses a 3-A, 200-V Super-fast rectifier (MURS320-13-F) with a forward voltage drop (V_{FDG}) of 875 mV at 3 A.

Estimated diode power loss (PDG_AUX)

$$P_{DG\_AUX} = \frac{P_{OUT\_AUX} \times V_{FDG\_AUX}}{V_{OUT\_AUX}} = \frac{6 \times 0.875}{15} = 0.35 \text{ W} \quad (37)$$

5.2.4 Output Capacitors

Select an output ESR based on 90% of the allowable output ripple voltage:

$$ESR_{COUT\_24V} = \frac{V_{RIPPLE} \times 0.9}{I_{SPK}} = \frac{25\ m \times 0.9}{4.55\ A} \approx 4.95\ m\Omega \quad (38)$$

The output capacitor (C_{OUT}) was selected to have a ripple of less than 25 mV on V_{OUT}.

$$C_{OUT\_24V} \geq \frac{20\ \mu \times \frac{P_{OUT}}{V_{OUT} \times 2}}{V_{RIPPLE}} = \frac{20\ \mu \times \frac{24}{24 \times 2}}{0.025} \approx 400\ \mu F \quad (39)$$

Two numbers of 330-µF/35-V aluminum electrolytic capacitor with a ripple current rating of 1000 mA are connected in parallel at the output diode to support the ripple current.

$$C_{OUT\_16V} \geq \frac{20\mu \times \frac{1}{16 \times 2}}{0.025} = 25\ \mu F \quad (40)$$

A 100-µF/35-V capacitor with a ripple current ratings of 460 mA are connected at each of the 16-V outputs.

$$C_{OUT\_AUX} \geq \frac{20\mu \times \frac{6}{15 \times 2}}{0.025} = 160\ \mu F \quad (41)$$

This design uses a 220-µF/35-V capacitor with a ripple current rating of 490 mA.

Estimate the total output capacitor RMS current (I_{COUT_RMS})

$$I_{COUT\_RMS\_24V} = \sqrt{\left(\frac{I_{SPK} \times \sqrt{D_{MAG}}}{\sqrt{3}}\right)^2 - \left(\frac{P_{OUT}}{V_{OUT}}\right)^2} = \sqrt{\left(\frac{4.55 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{24}{24}\right)^2} = 1.39\ A \quad (42)$$

$$I_{COUT\_RMS\_16V} = \sqrt{\left(\frac{0.28 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{1}{16}\right)^2} = 85\ mA \quad (43)$$

$$I_{COUT\_RMS\_AUX} = \sqrt{\left(\frac{1.788 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{6}{15}\right)^2} = 0.716\ A \quad (44)$$

5.2.4.1 Overvoltage Detection

The LMS33460 is a micro-power under voltage sensing circuit with an open drain output configuration, which requires a pull resistor. The LMS33460 features a voltage reference, a comparator with precise thresholds, and built-in hysteresis to prevent erratic reset operation. This IC generates an active output whenever the input voltage drops below 3.0 V. The resistor divider in Figure 15 is derived with 450-V DC as an overvoltage trip point. A Zener diode (D28) clamps the input voltage at the LMS33460 to less than 8 V (absolute max of the device) when the DC bus voltage is at its max of 450-V DC.

The device has a minimum hysteresis voltage of 100 mV, which translates to approximately 11 V on the DC bus. Hysteresis can also be adjusted with R14.

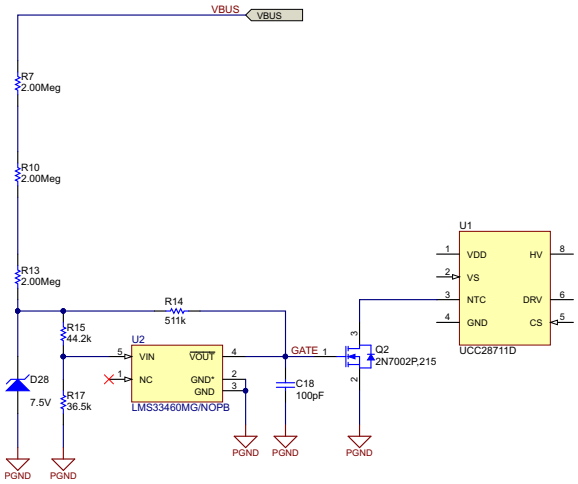

Figure 15. Undervoltage Protection

The UCC28711 has NTC input, which can be used to interface an external negative temperature coefficient resistor for remote temperature sensing to allow user-programmable external thermal shutdown. The shutdown threshold is 0.95 V with an internal 105-µA current source, which results in a 9.05-kΩ thermistor shutdown threshold. Pulling this pin low shuts down PWM action. The signal from the LMS33460 is interfaced to this pin to shut down the controller during overvoltage.

5.2.4.2 HV Startup

The UCC28711 has an internal 700-V start-up switch. Since the DC bus can be as high as 450-V DC, an external Zener voltage regulator limits the voltage at the HV pin to about 550-V DC. The typical startup current is approximately 300 µA, which provides fast charging of the VDD capacitor. The internal HV start-up device is active until VDD exceeds the turn-on UVLO threshold of 21 V, at which time the HV start-up device is turned off. In the off state, the leakage current is very low to minimize standby losses of the controller. When VDD falls below the 8.1-V UVLO turn-off threshold, the HV start-up device is turned on.

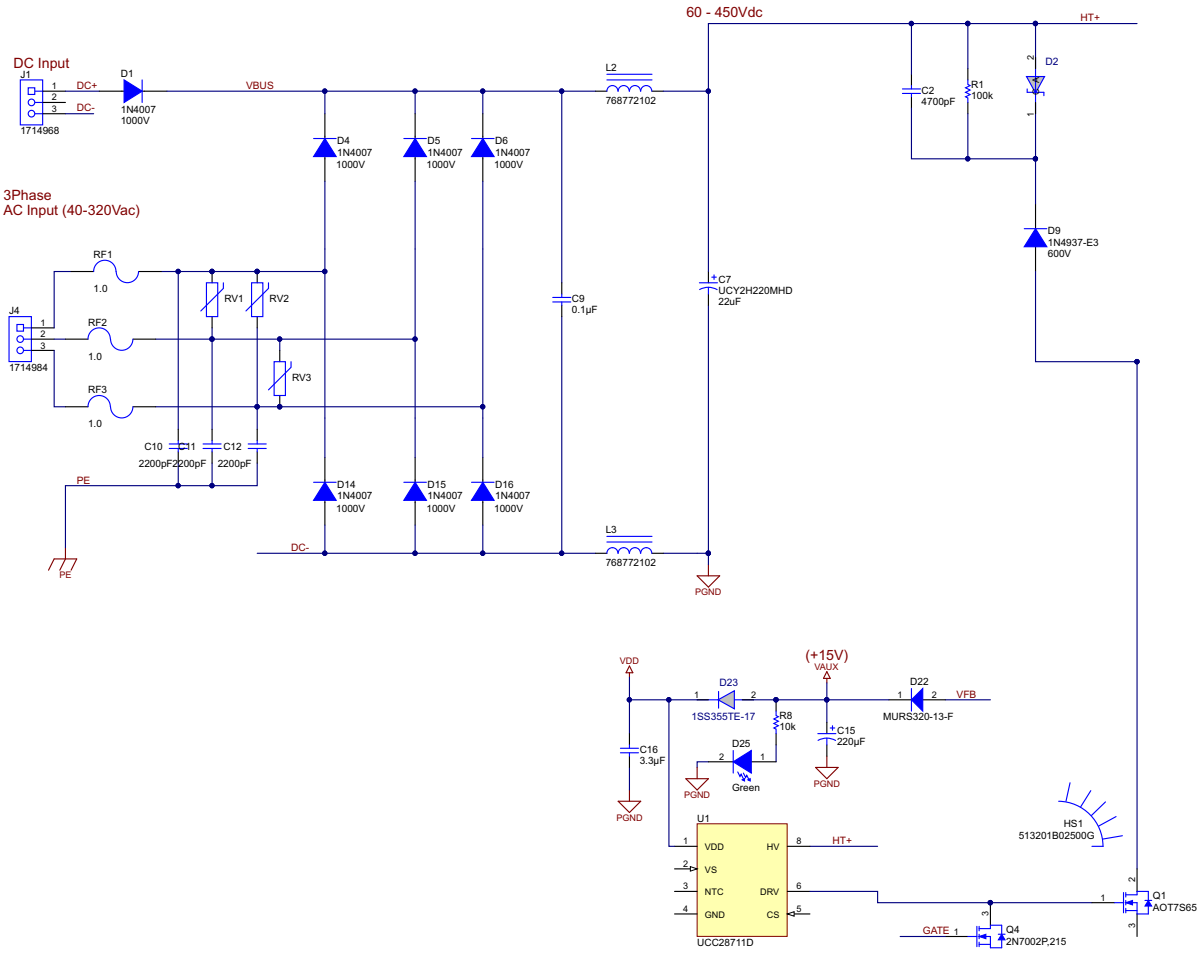

Figure 16. Start-up Circuit

The DC link voltage is directly connected to the HV pin of the UCC28711 because the maximum voltage on DC link is 450 V, which is within the limit of 700 V start-up switch of the UCC28711.

5.2.5 Input Voltage Sensing

AC input voltage and DC link voltage are measured in the drives for various reasons:

1. To detect single phase failure
2. DC Link undervoltage and overvoltage condition
3. To control the inverter output voltage

When a drive application does not mandate high accuracy measurements, the flyback converter itself can measure the AC input as well as DC link voltage. When the primary switch is ON, the induced voltage at the secondary (D8 in Figure 17) will be the DC link voltage times the turn ratio, which will also be proportional to the AC mains input voltage. This voltage is rectified and filtered with RC network. Voltage scaling can be performed based on the ADC input voltage range.

At 450-V DC input with a turns ratio of 3.75, the forward induced voltage is given by

$$V_{DC\_MEAS(max)} = \frac{450}{3.75} = 120 \text{ V} \quad (45)$$

$$V_{DC\_MEAS(min)} = \frac{65}{3.75} = 16 \quad (46)$$

This voltage is stepped down through a resistive divider 0.01587 to scale it to 1.9044 V and 0.25 V. This step-down ratio can be adjusted based on the application requirements.

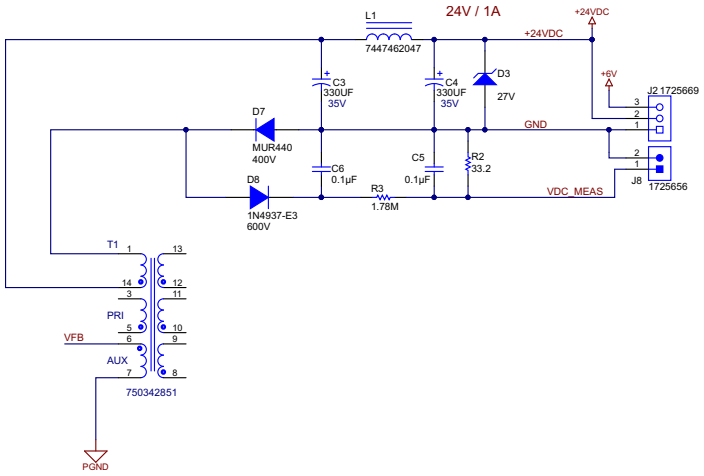

Figure 17. DC Link Voltage Measurement

5.2.6 Transformer Construction

Table 1. Magnetic Details

CORE TYPE	BOBBIN
EE25	14-pin (vertical)

Table 2. Electrical Details of the Transformer

PARAMETER	TEST CONDITIONS	VALUE
Inductance	50 kHz, 100 mV, L_S	150.0 µH ±10%
Saturation current	20% rolloff fromn initial	2.78 A
Leakage inductance	tie (6+7+8+9+10+11+12+13+14), 100 kHz, 100 mV, L_S	5 µH max
Dielectric	1250-V AC, 1 second	
Dielectric	Tie (5+6, 9+10+11+12+13+14), 3125-V AC, 1 second	
Dielectric	2500-V AC, 1 second	
Dielectric	2500-V AC, 1 second	
Dielectric	2500-V AC, 1 second	
Turns ratio	(5-3):(6-7)	3.75:1, ±2%
Turns ratio	(5-3):(8-9)	3.75:1, ±2%
Turns ratio	(5-3):(10-11)	3.75:1, ±2%
Turns ratio	(5-3):(12-13)	3.75:1, ±2%
Turns ratio	(5-3):(14-1)	2.5:1, ±2%

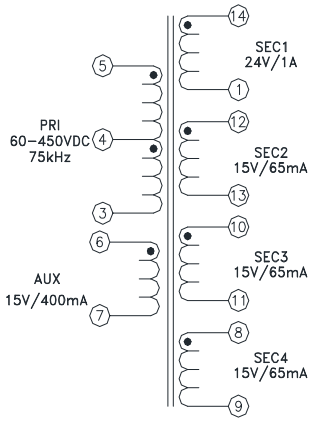

Figure 18. Transformer Pin Out

5.2.7 24-V to 6-V Switcher

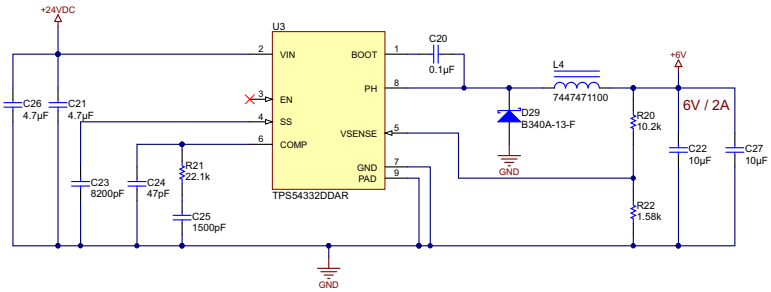

Figure 19. 24-V to 6-V Switcher

A DC/DC converter TPS54332 converts 24-V DC to 6-V DC at 2 A. Note that when a 12-W output is available at the 6-V rail, the corresponding output power should be derated from the 24-W output.

The TPS54332 can accept input voltage from 3-V to 28-V DC on VIN pin. In this case, 24-V is directly connected to the VIN pin and two 4.7-µF capacitors (C26 and C21) are connected on VIN pin. The device can be enabled and disabled by using the EN pin. Capacitor C23 is used to decide the output rise time. With a value of 8200 pF, the slow start time is 3.28 ms.

The switching frequency of the TPS54332 is fixed at 1 MHz.

With an internal reference voltage V_{REF} = 0.8 V, the output of the TPS54332 is set using Equation 47.

$$V_{OUT} = V_{REF} \times \left(\frac{R20}{R22} + 1 \right) \quad (47)$$

The selected values are R20 = 10.2 kΩ and R22 = 1.58 kΩ

The TPS54332 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application. The reverse voltage must be higher than the maximum voltage at the PH pin, which is Vin(max) + 0.5 V. The peak current must be greater than IOUTMAX plus half the peak-to-peak inductor current. This design uses the Diodes, Inc. B340A with a reverse voltage of 40 V, a forward current of 3 A, and a forward voltage drop of 0.5 V.

Two components need to be selected for the output filter: the output inductor L4 and the output capacitors (C22 and C27). This design uses an inductor 7447471100 (from Würth Electronics) and two capacitors of value 10 µF are used in parallel. The compensation is external so loop stability can be decided as per the requirement.

6 Test Results

6.1 Functional Test Results

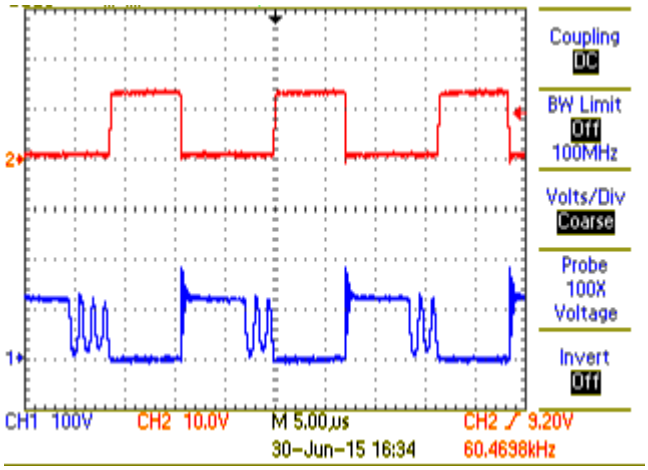

Figure 20. FET Voltage at 60-V Input / 30-W Output (CH1: V_{DS} and CH2: V_{GS})

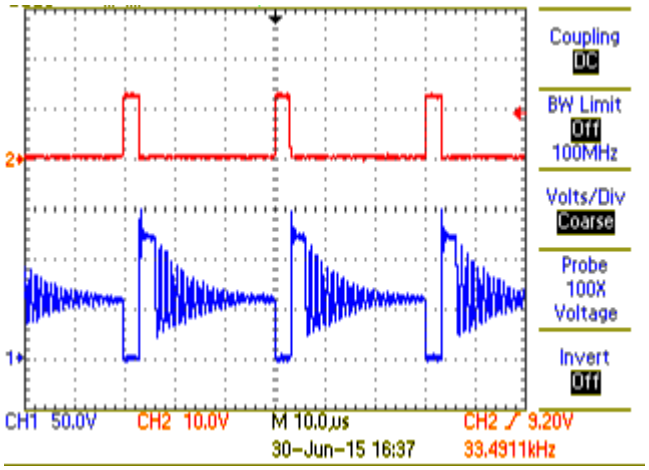

Figure 21. FET Voltage at 60-V Input / No Load Output (CH1: V_{DS} and CH2: V_{GS})

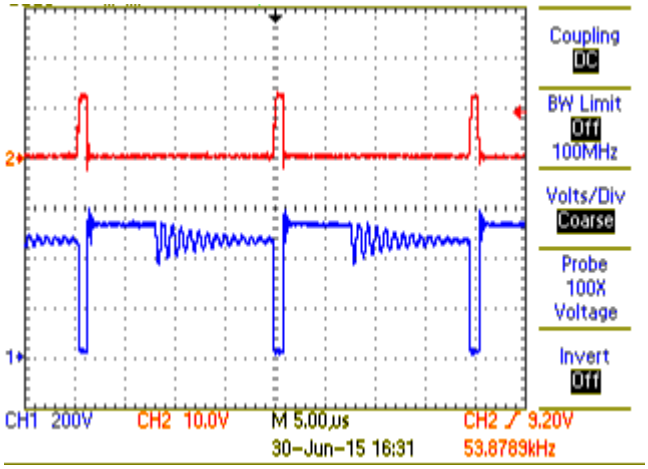

Figure 22. FET Voltage at 450-V Input / 30-W Output (CH1: V_{DS} and CH2: V_{GS})

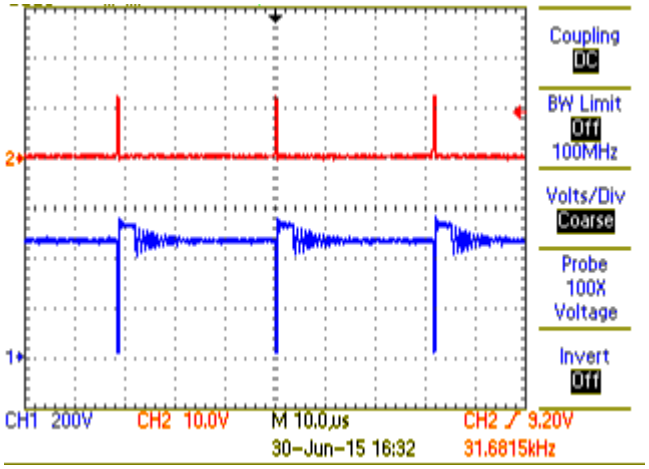

Figure 23. FET Voltage at 450-V Input / No Load Output (CH1: V_{DS} and CH2: V_{GS})

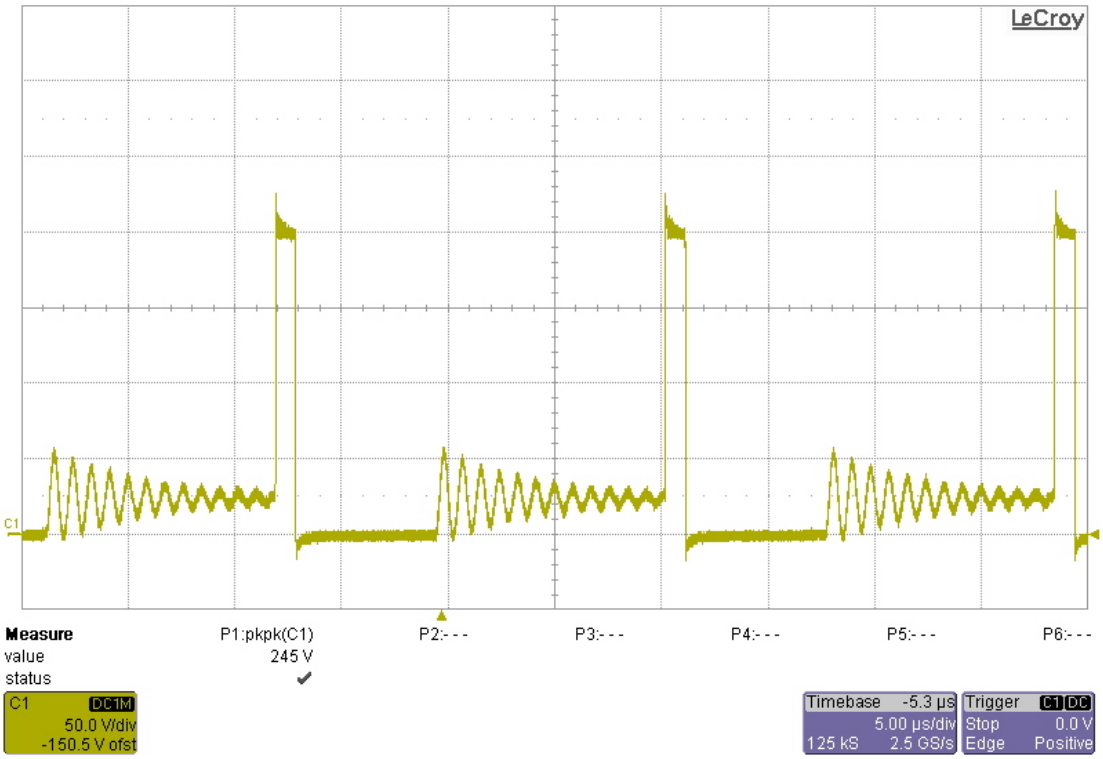

Figure 24. 24-V Output Diode (D7) Voltage Stress With V_{IN} = 450-V DC and 30-W Output

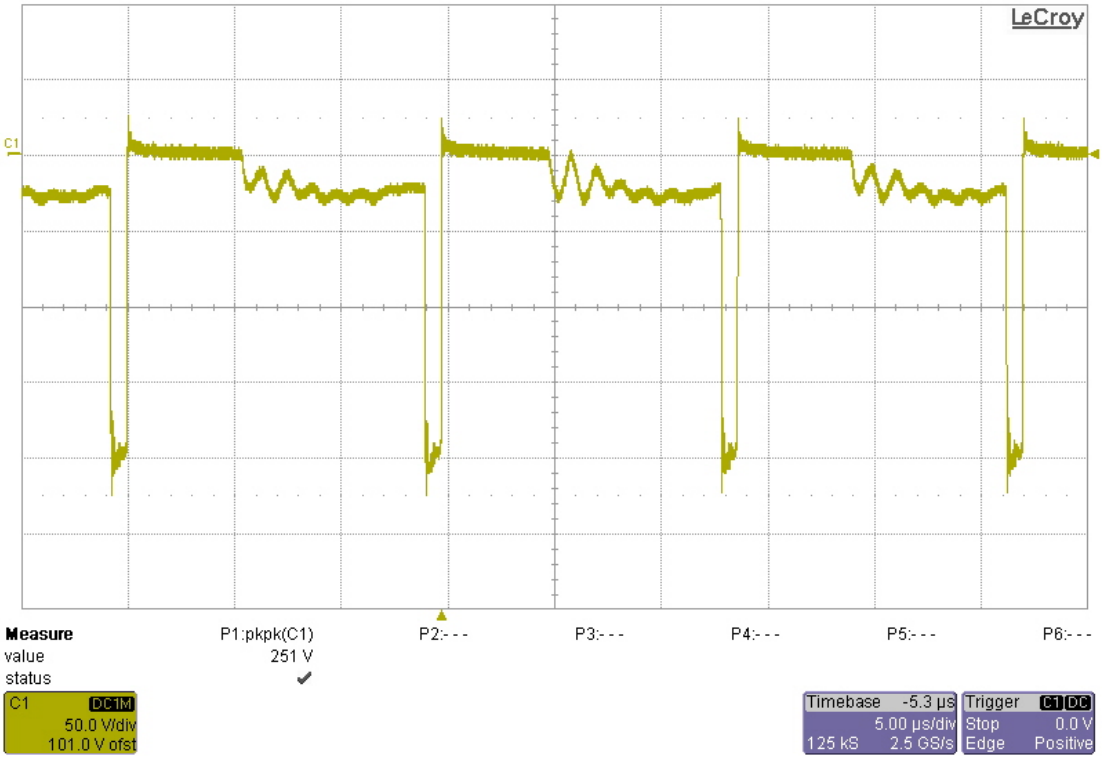

Figure 25. 24-V Output Diode (D8) Voltage Stress With V_{IN} = 450-V DC and 30-W Output

6.2 Output Ripple Under Different Test Conditions

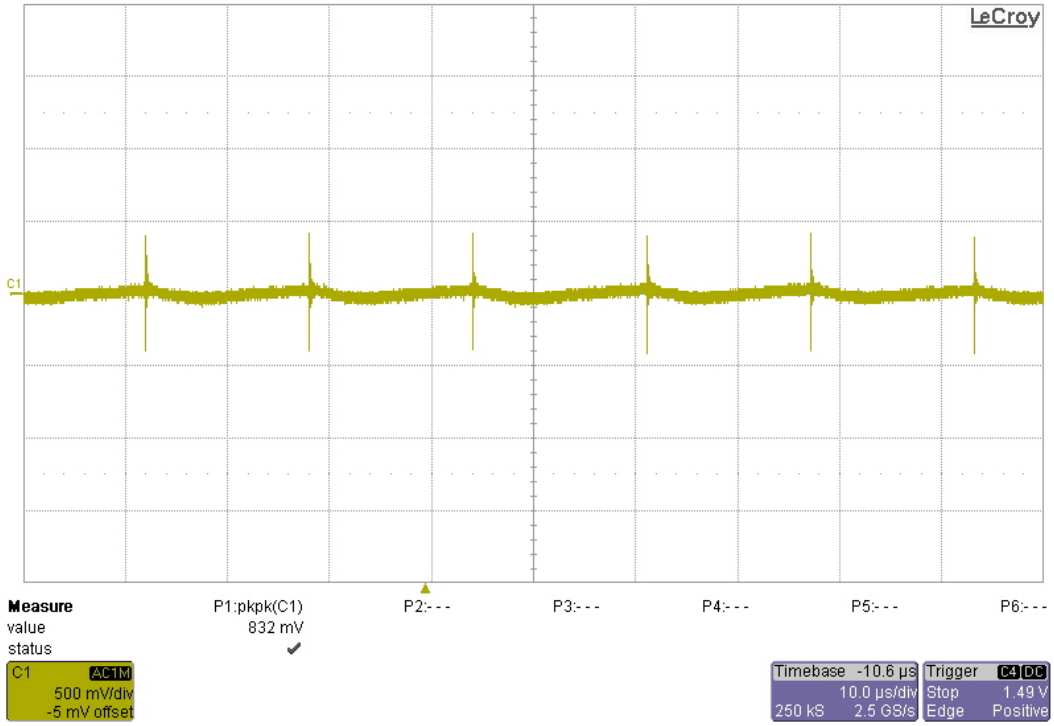

Figure 26. Ripple at 24-V Output With V_{IN} = 60-V DC and Full Load (24 V Loaded With 24 W and Other Outputs Loaded With Individual Full Load Conditions)

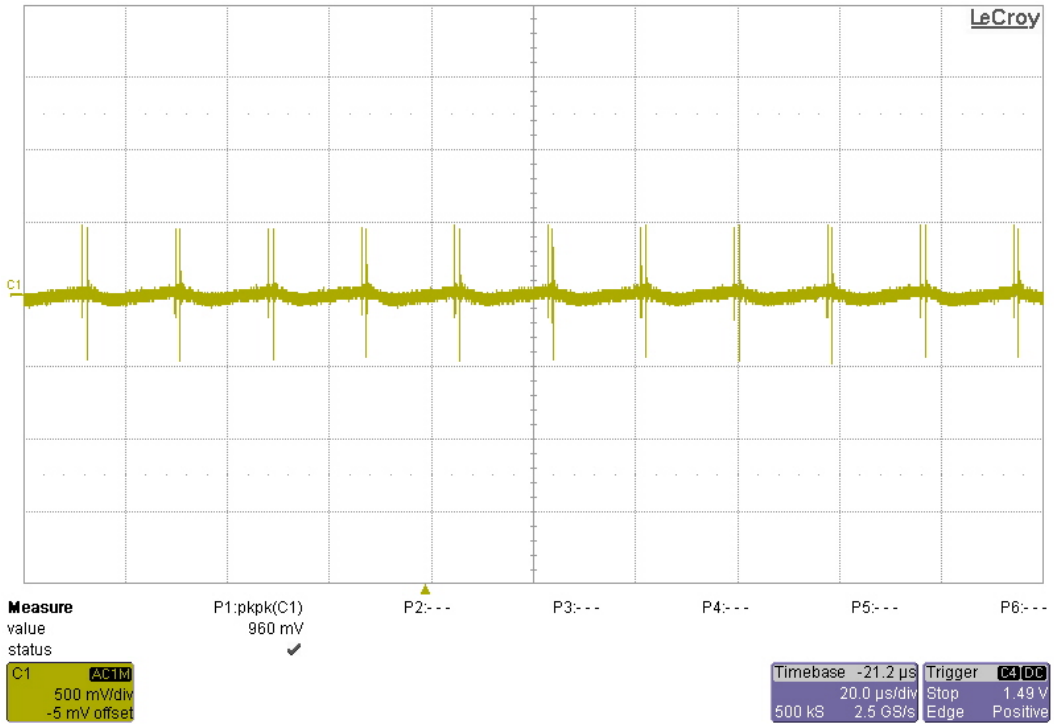

Figure 27. Ripple at 24-V Output With V_{IN} = 450-V DC and Full Load (24 V Loaded With 24 W and Other Outputs Loaded With Individual Full Load Conditions)

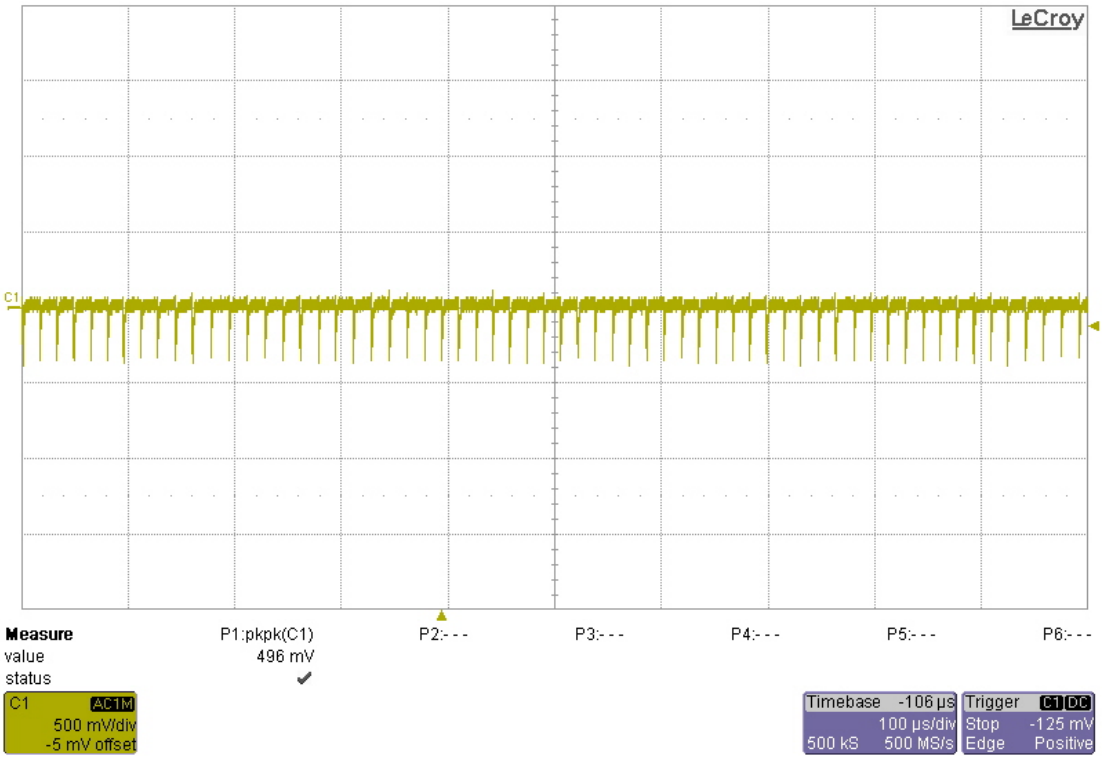

Figure 28. Ripple at 16VDC1 Output With V_{IN} = 60-V DC and Full Load

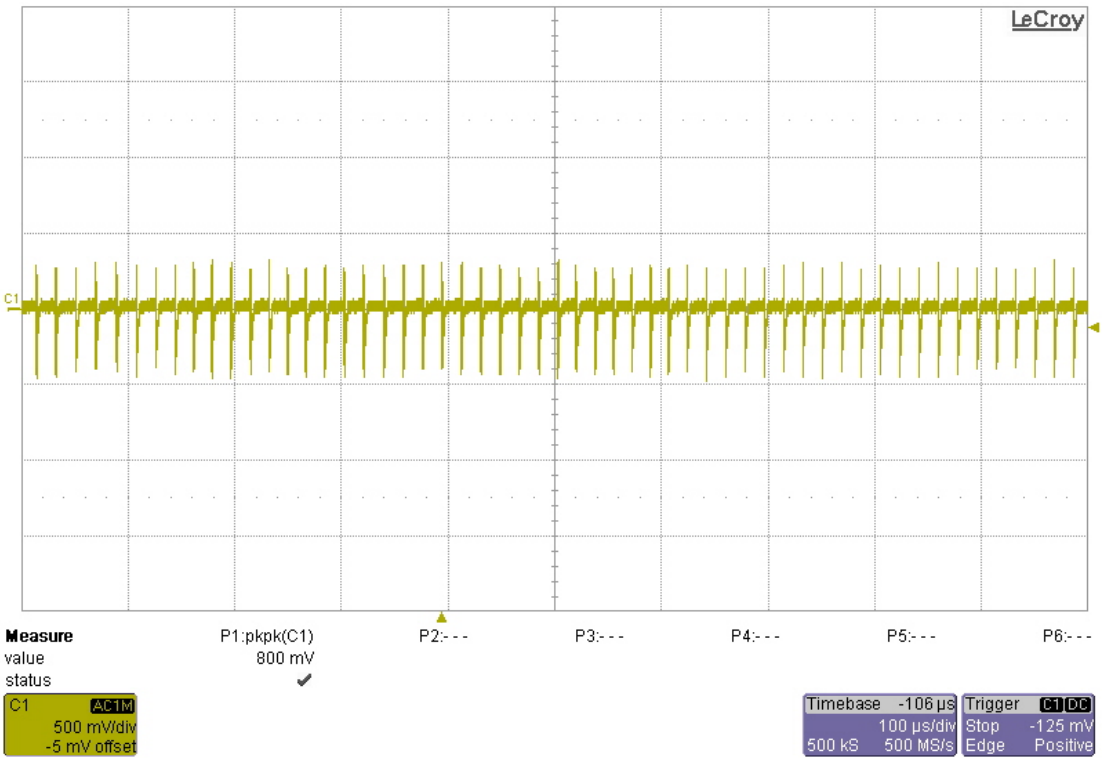

Figure 29. Ripple at 16VDC1 Output With V_{IN} = 450-V DC and Full Load

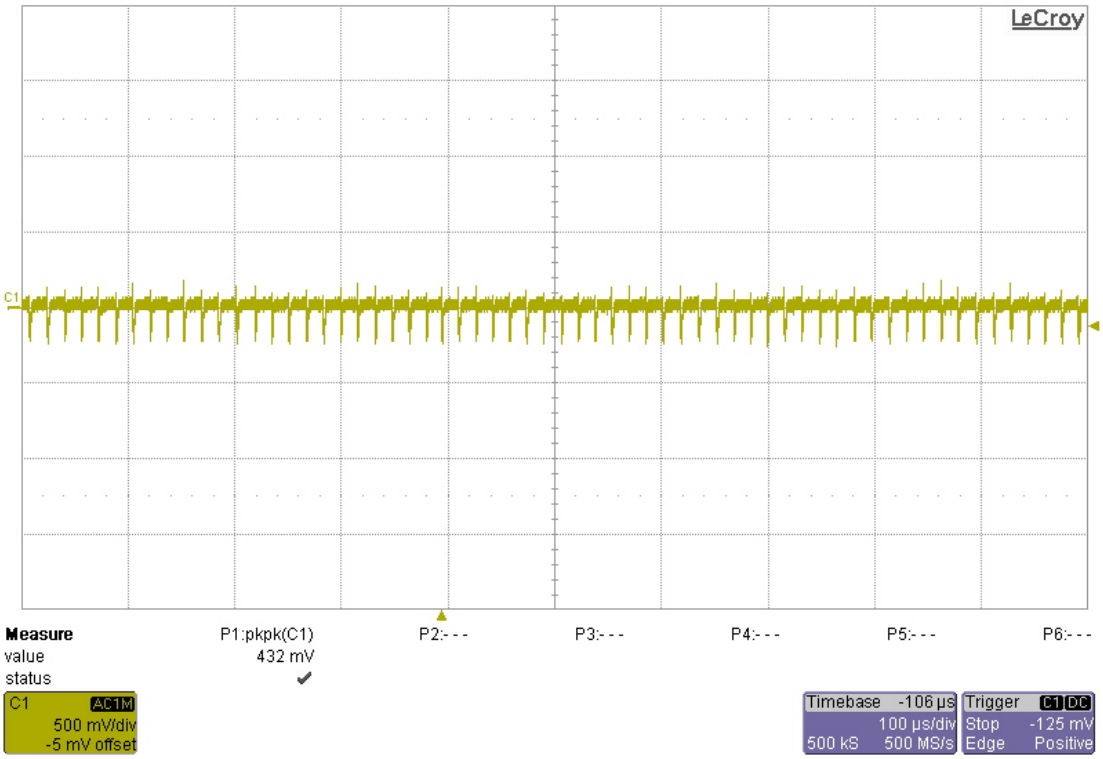

Figure 30. Ripple at 16VDC2 Output With V_{IN} = 60-V DC and Full Load

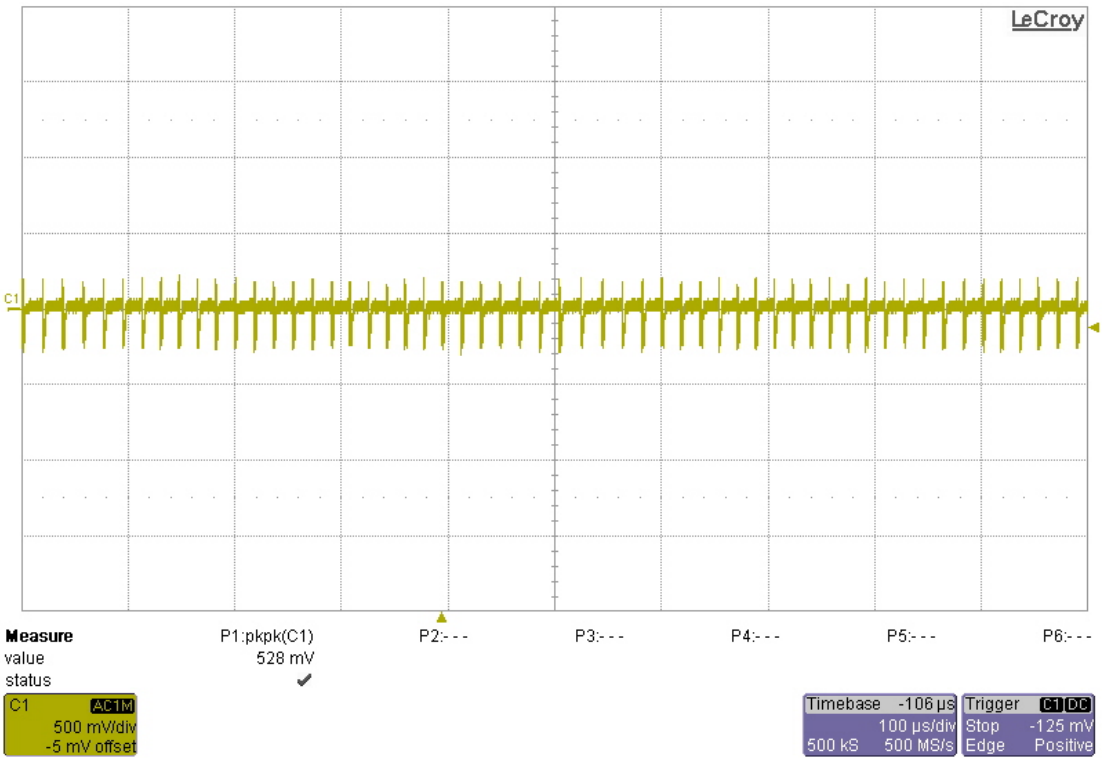

Figure 31. Ripple at 16VDC2 Output With V_{IN} = 450-V DC and Full Load

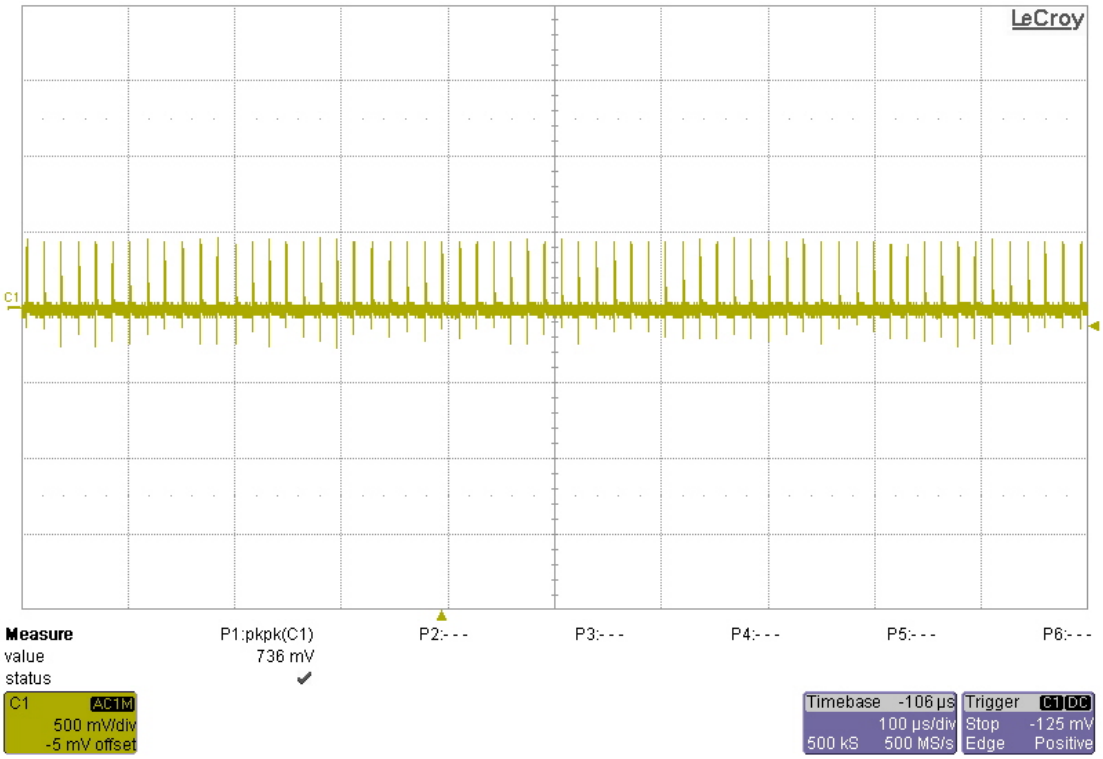

Figure 32. Ripple at 16VDC3 Output With V_{IN} = 60-V DC and Full Load

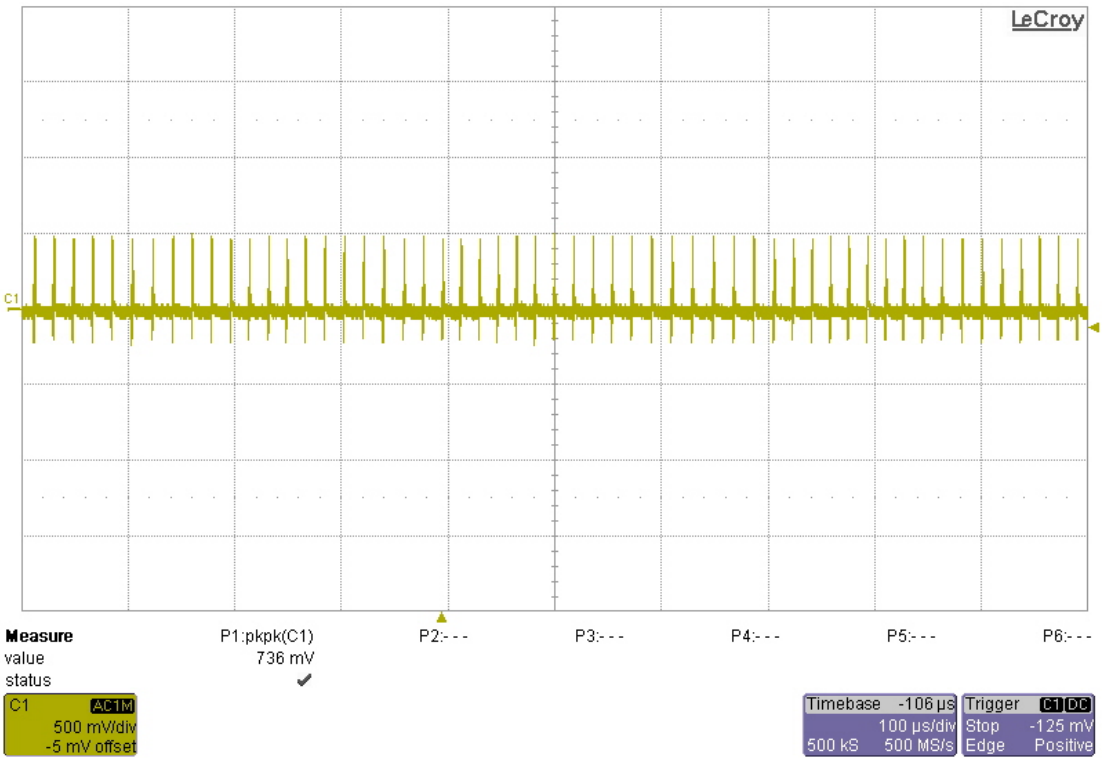

Figure 33. Ripple at 16VDC3 Output With V_{IN} = 450-V DC and Full Load

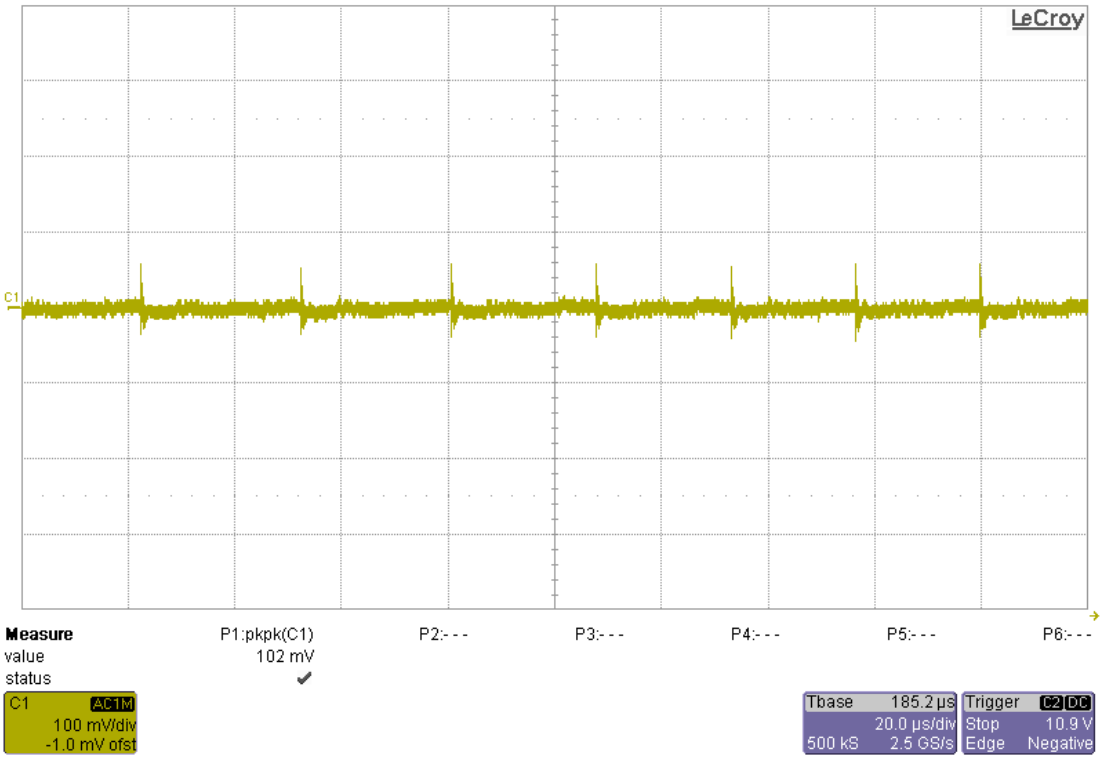

Figure 34. Ripple at 6-V Output With V_{IN} = 60-V DC and Full Load

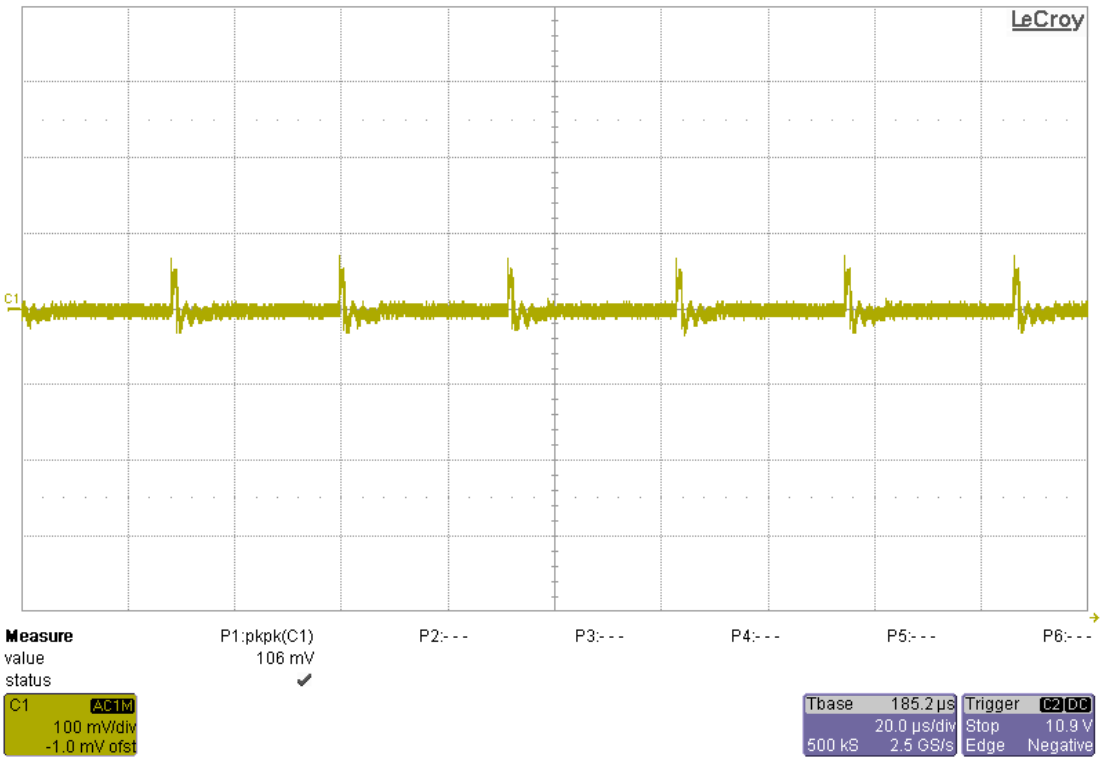

Figure 35. Ripple at 6-V Output With V_{IN} = 450-V DC and Full Load

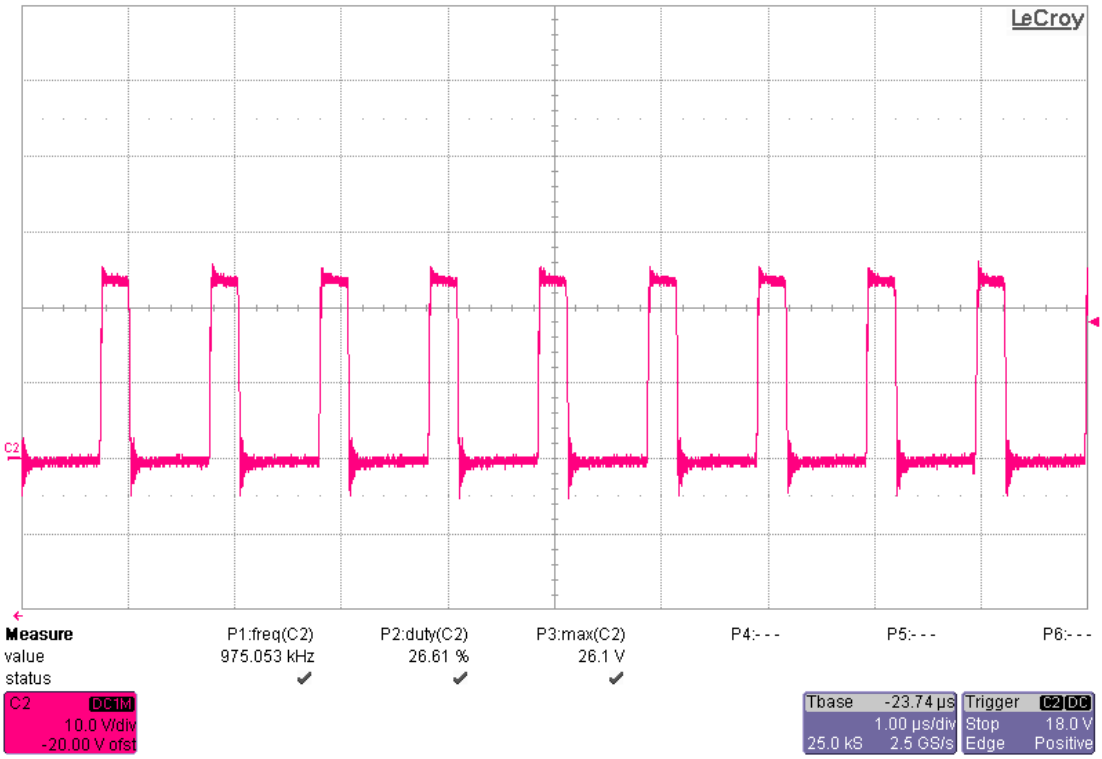

Figure 36. Switching Waveform for Switcher at V_{IN} = 60-V DC and Full Load

6.3 Efficiency

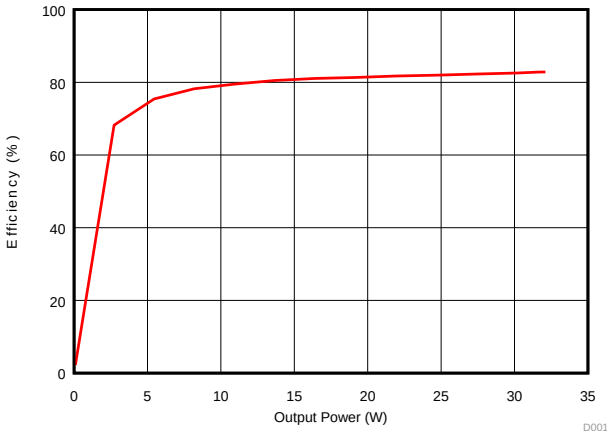

Figure 37. Efficiency Versus Output Power at V_{IN} = 450-V DC

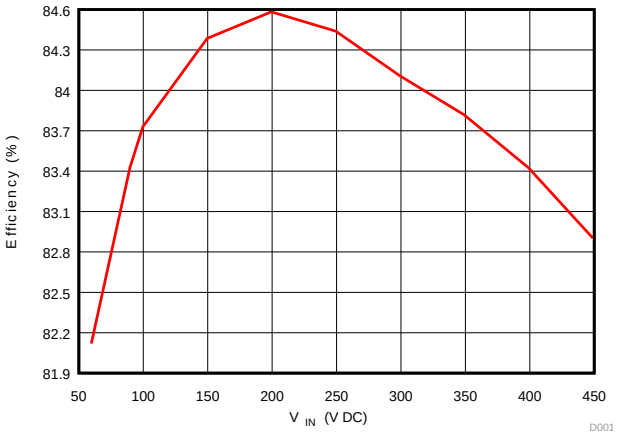

Figure 38. Efficiency Versus Input Voltage at Full Load

6.4 Line Regulation

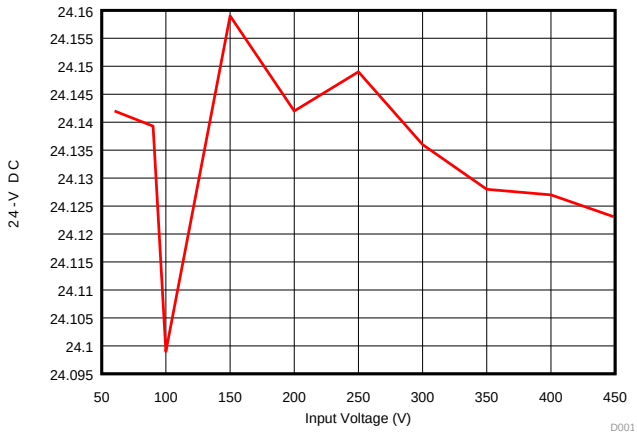

Figure 39. 24-V Output Line Regulation With Full Load

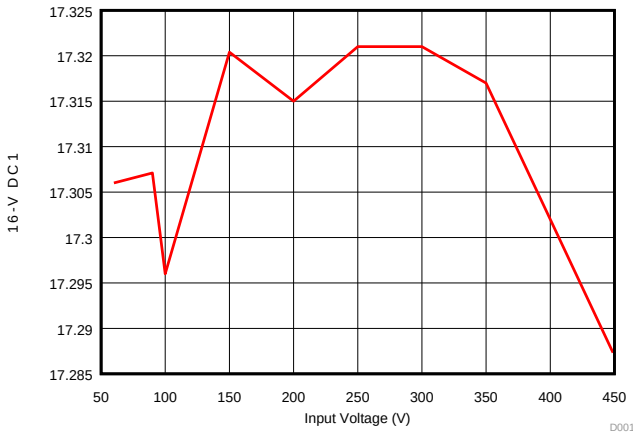

Figure 40. 16VDC1 Output Line Regulation With Full Load

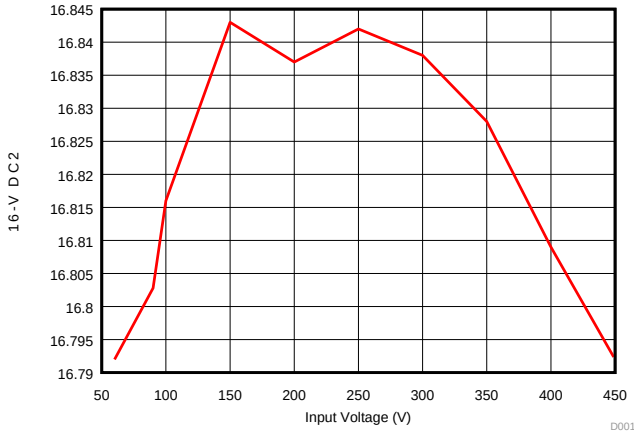

Figure 41. 16VDC2 Output Line Regulation With Full Load

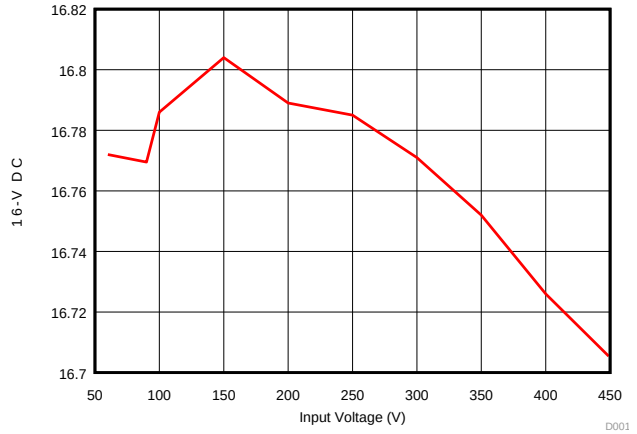

Figure 42. 16VDC3 Output Line Regulation With Full Load

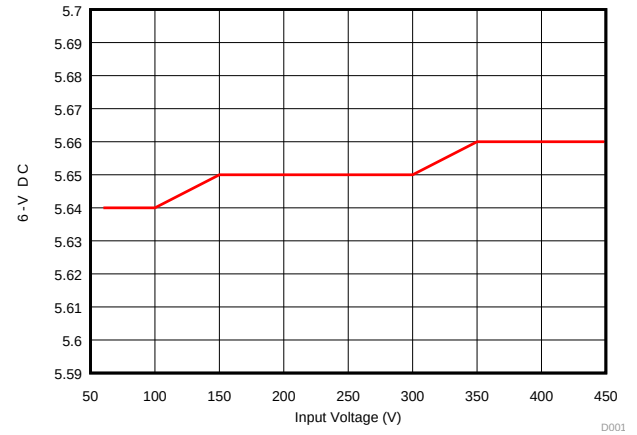

Figure 43. 6-V Output Line Regulation With Full Load

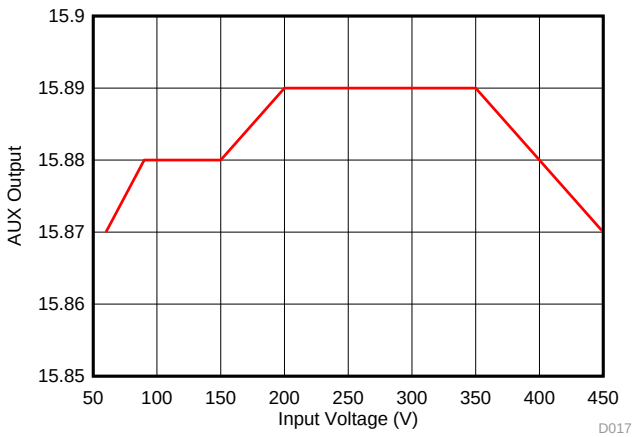

Figure 44. AUX Output Line Regulation With Full Load

6.5 Load Regulation

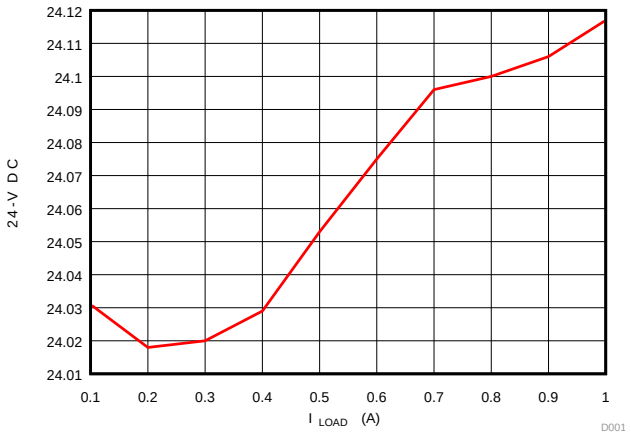

Figure 45. 24-V Output Load Regulation With V_{IN} = 450-V DC

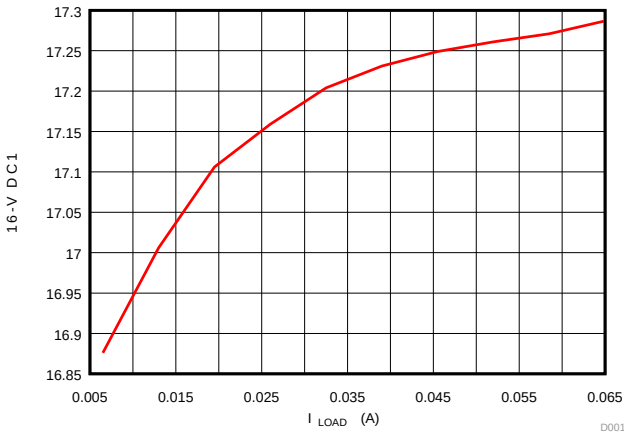

Figure 46. 16VDC1 Output Load Regulation With V_{IN} = 450-V DC

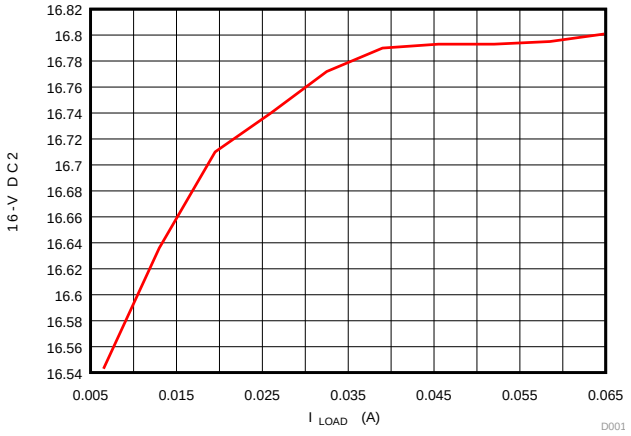

Figure 47. 16VDC2 Output Load Regulation With V_{IN} = 450-V DC

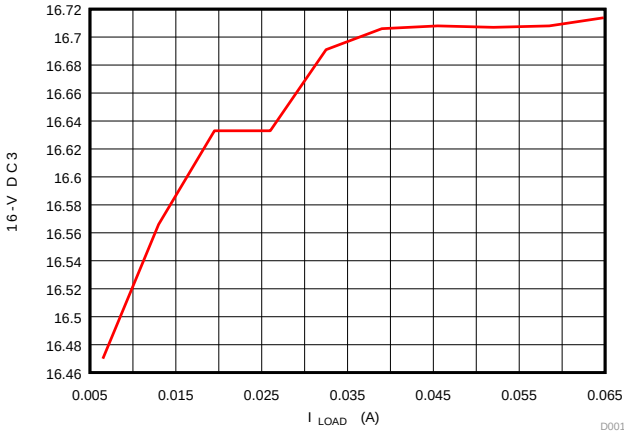

Figure 48. 16VDC3 Output Load Regulation With V_{IN} = 450-V DC

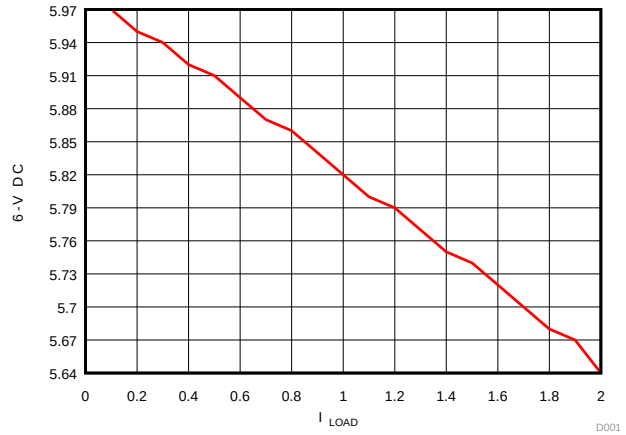

Figure 49. 6-V Output Load Regulation With V_{IN} = 450-V DC

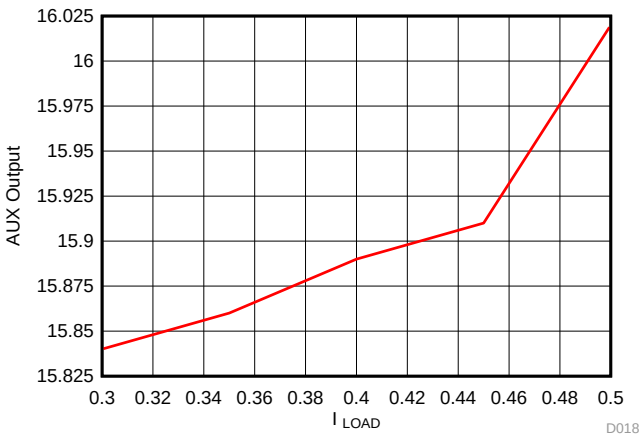

Figure 50. AUX Output Load Regulation With V_{IN} = 450-V DC

6.6 Overload Test and Output Power Limit

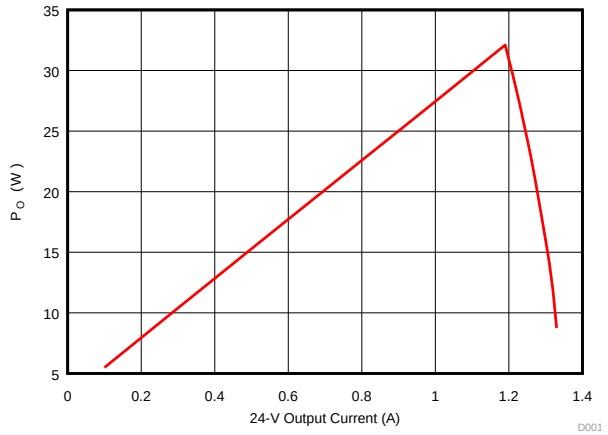

Figure 51. Overload and Current Limit at 24-V Output With V_{IN} = 450-V DC

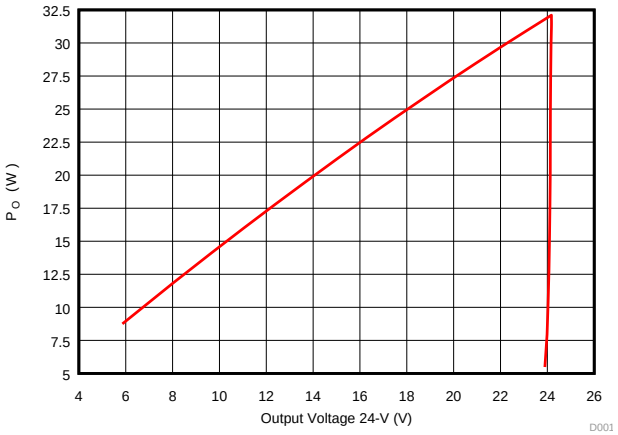

Figure 52. Overload at 24-V Output: Voltage Versus Output Power With V_{IN} = 450-V DC

6.7 DC Link Voltage Measurement

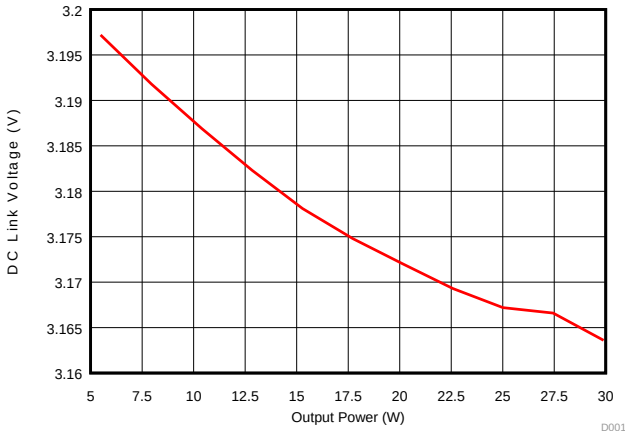

Figure 53. DC Link Voltage Measurement With Varying Output Load

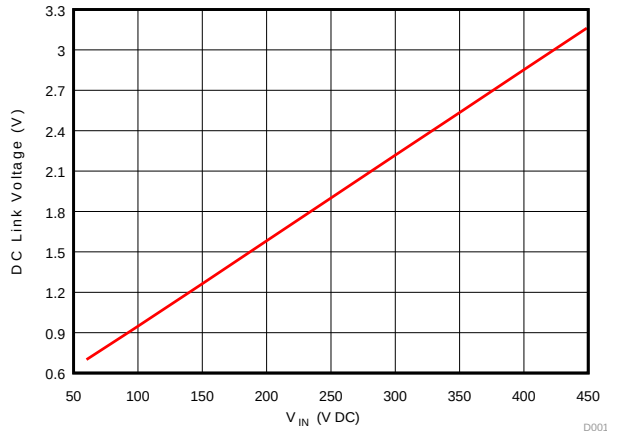

Figure 54. DC Link Voltage Measurement With Full Load

6.8 Undervoltage and Overvoltage Test

Figure 55 and Figure 56 capture the input overvoltage and undervoltage limits. When the input voltage exceeds 454-V DC, the PWM controller is shut down and it recovers when the input voltage falls back to approximately 396-V DC. The hysteresis in turn-off and turn-on voltages can be adjusted by varying R14.

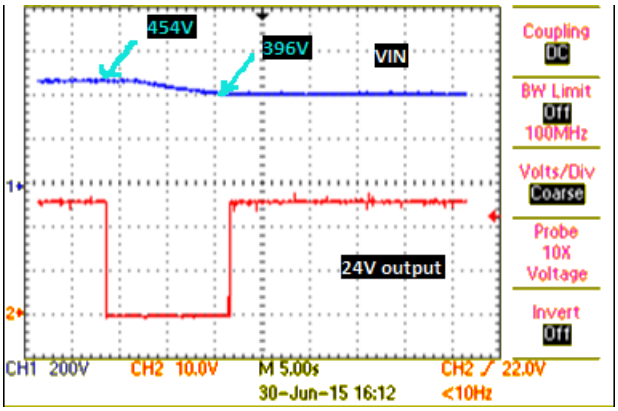

Figure 55. DC Link Voltage Measurement With Full Load (Showing Overvoltage Condition)

The power supply turns on at around 100-V DC and shuts down when the input voltage falls below 31-V DC. The ratio of turn ON to turn OFF is fixed for undervoltage shutdown operation and is controlled within the UCC28711.

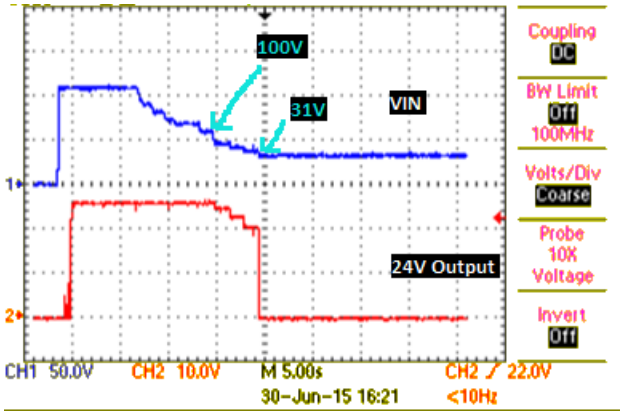

Figure 56. DC Link Voltage Measurement With Full Load (Showing Undervoltage Condition)

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00315.

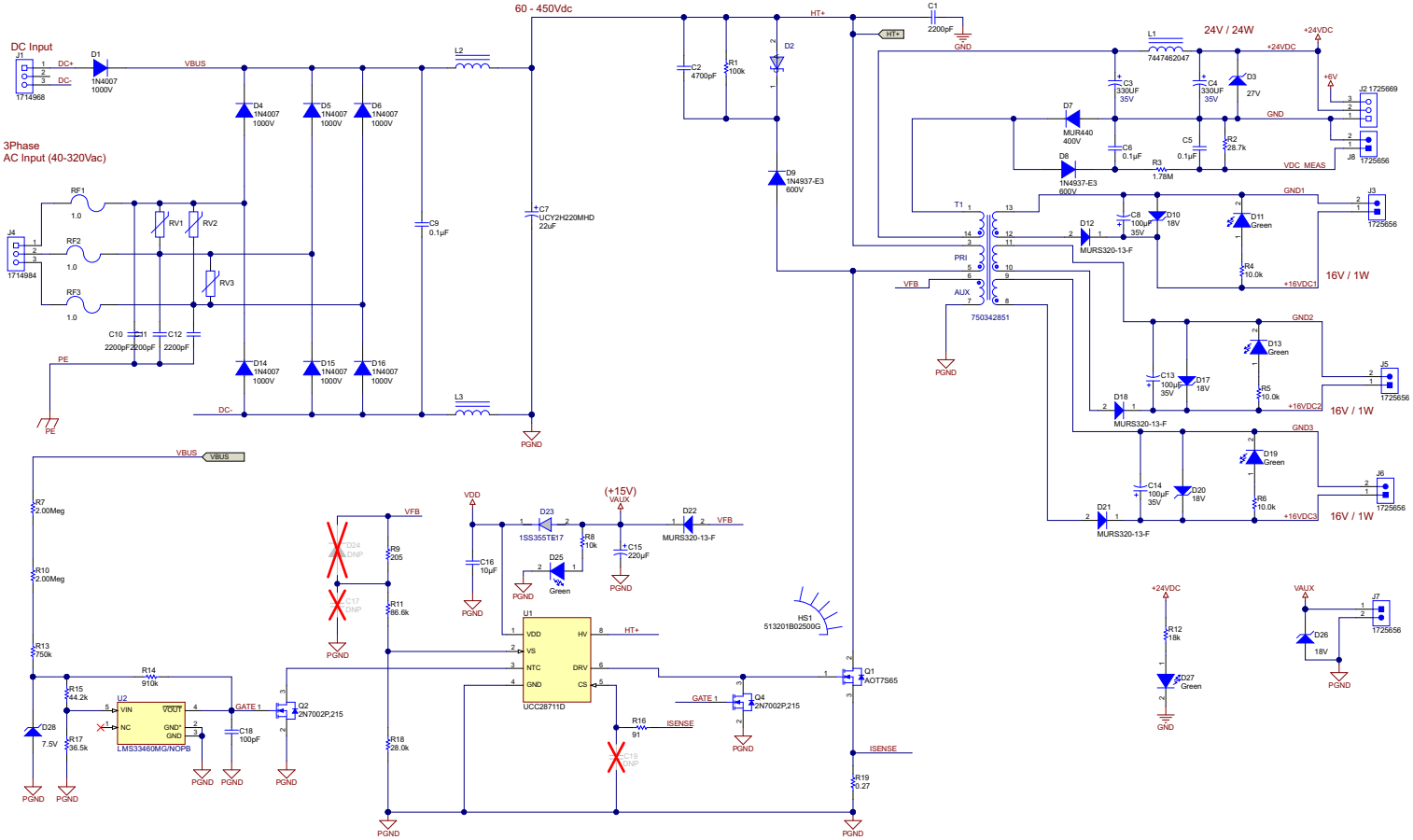

Figure 57. TIDA-00315 Schematic Page 1

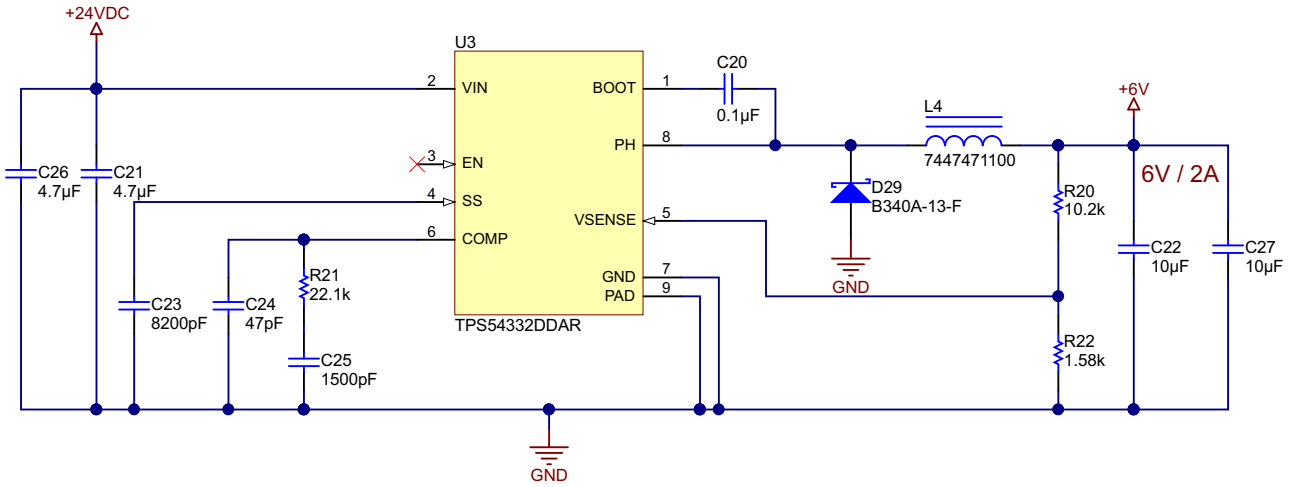

Figure 58. TIDA-00315 Schematic Page 2

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00315.

7.3 PCB Layout Guidelines (UCC28711)

A proper layout is critical for the power supply to function accurately. Major guidelines on the layout for the proper functioning of the controller are described in the following diagrams.

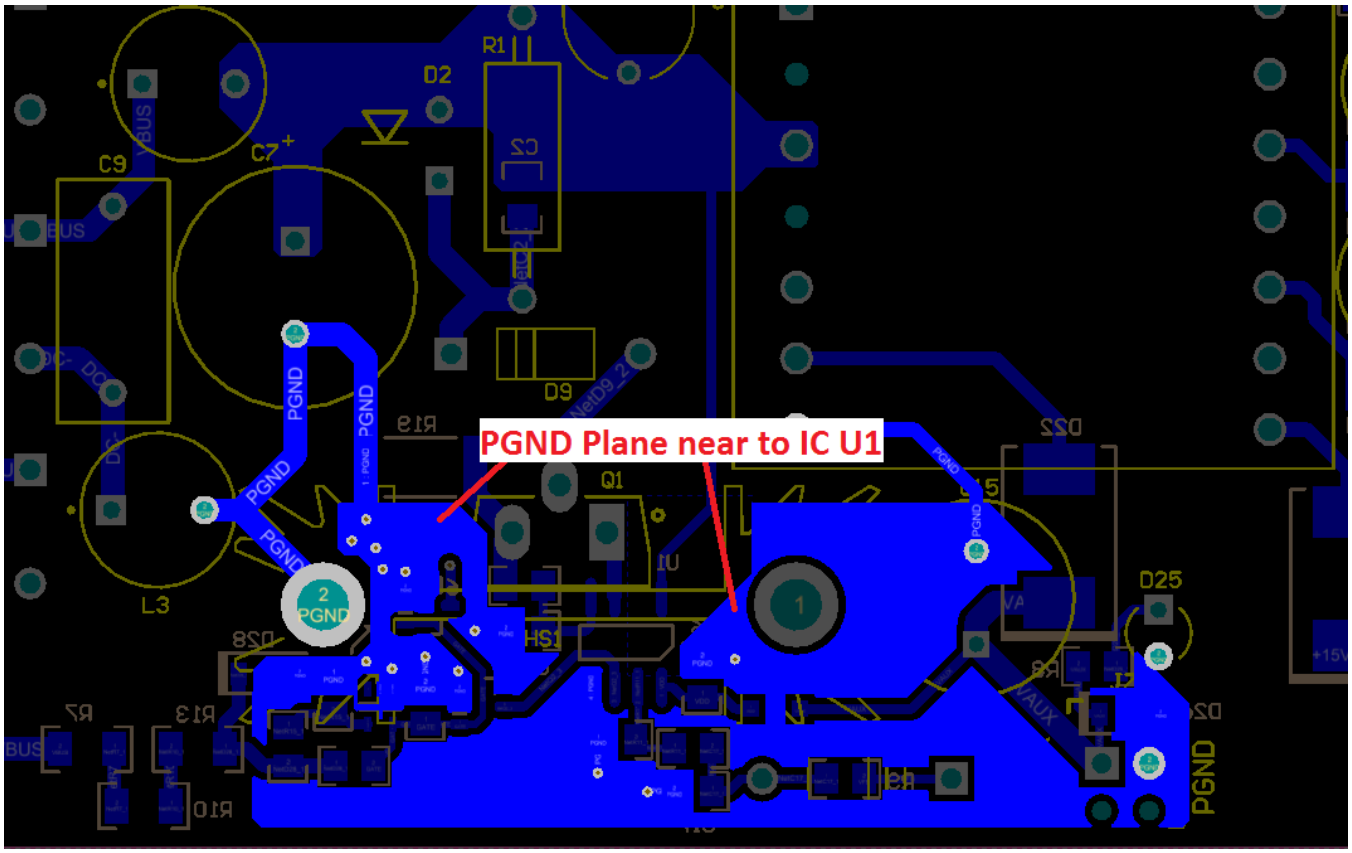

Figure 59. Layout of Ground Plane Near IC U1

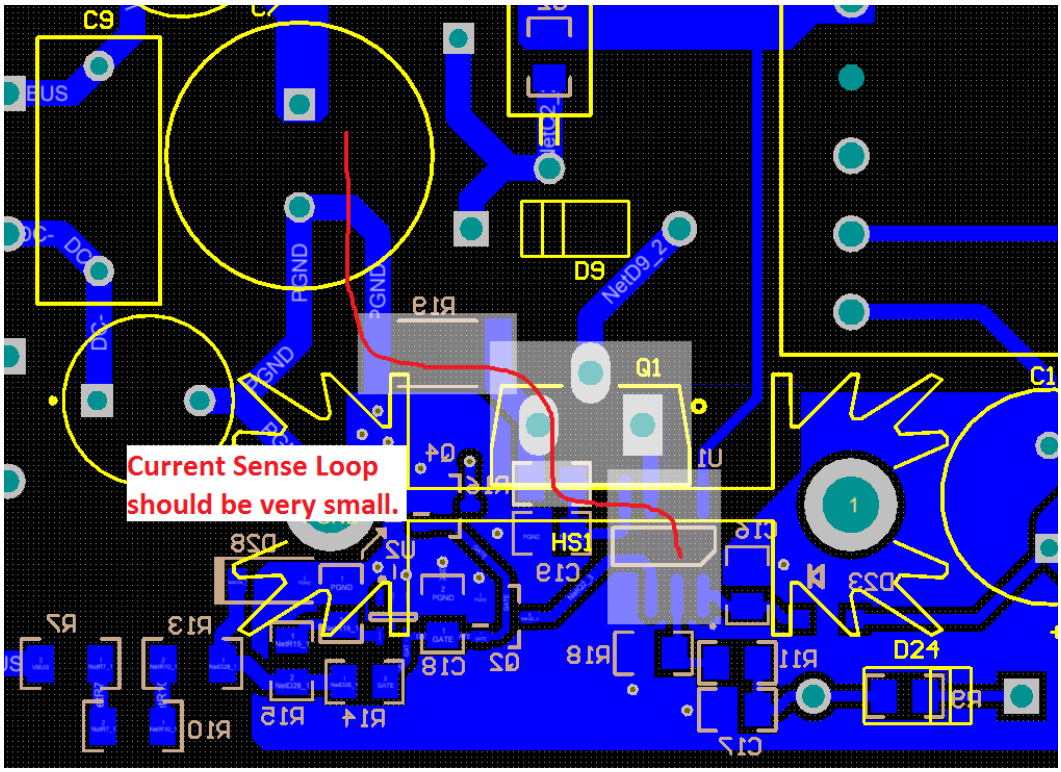

Figure 60. Layout for Placing Current Sense Loop

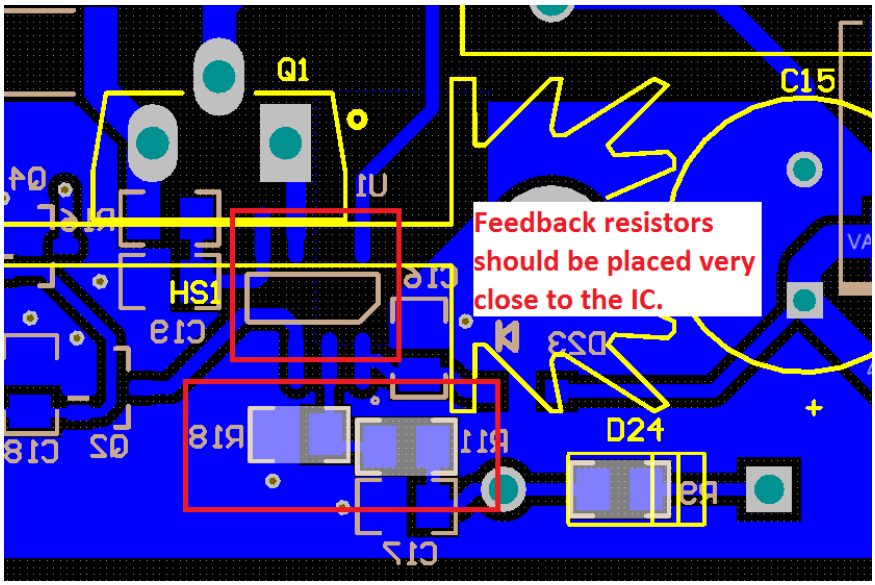

Figure 61. Layout of Feedback Resistors

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00315.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00315.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00315.

8 References

1. Texas Instruments, *5W USB Flyback Design Review/Application Report* (SLUA653)
2. Texas Instruments, *Constant-Voltage, Constant-Current Controller With Primary-Side Regulation*, UCC28711 Datasheet (SLUSB86)
3. Texas Instruments, *3V Under Voltage Detector*, LMS33460 Datasheet (SNVS158)
4. Texas Instruments, *400- to 690-V AC Input 50-W Flyback Isolated Power Supply Reference Design for Motor Drives*, TIDA-00173 Design Guide (TIDU412)
5. Mitsubishi Electric, *Bootstrap Circuit Design Manual*, DIPIPM Application Note (http://www.mitsubishielectric.com/semiconductors/files/manuals/dipipm_bootstrap_circuit_e.pdf)
6. Fuji Electric, *Fuji IGBT-IPM Application Manual* (http://www.fujielectric.com/products/semiconductor/model/igbt/application/box/doc/pdf/RH983a/REH983a.pdf)

9 About the Author

SALIL CHELLAPPAN is a Systems Manager, Member, and Group Technical Staff at Texas Instruments, where he is responsible for developing customized power solutions as part of the Power Design Services group. Salil brings to this role his extensive experience in power electronics, power conversion, EMI/EMC, power and signal integrity, and analog circuits design spanning many high-profile organizations. Salil holds a bachelor of technology degree from the University of Kerala.

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Revision History

Changes from Original (August 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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