Automotive Synchronous Buck – 9.0V @ 150mA

- Input 10..45V DC / 58V peak
- Output 9.0V @ 150mA
- Converter TPS54061
- Free-Running switching frequency of 1000 kHz
- Working in continuous conduction mode
- Modified TPS54061EVM-142
1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 20.0V, with no load on the 9.0V output.

Channel C1: **20.0V Input voltage**
5V/div, 1ms/div

Channel C2: **9.0V Output voltage**
5V/div, 1ms/div

Figure 1
2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 20.0V with a 150mA load on the 9.0V output.

Channel C1: **20.0V Input voltage**
5V/div, 1ms/div

Channel C2: **9.0V Output voltage**
5V/div, 1ms/div

Figure 2
3 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 3 and Figure 4.

![Figure 3](image1)

![Figure 4](image2)
4 Load Step – 4.7uF Output Capacitance

The response to a load step and a load dump for the 9.0V output at an input voltage of 30.0V and 4.7uF output capacitance is shown in Figure 5.

Channel C2: **Output voltage**, -140mV undershoot (1.6%), 167mV overshoot (1.9%)
200mV/div, 2ms/div, AC coupled

Channel C1: **Load current**, load step 30mA to 150mA and vice versa
50mA/div, 2ms/div

![Figure 5](image)
5 Load Step – 10uF Output Capacitance

The response to a load step and a load dump for the 9.0V output at an input voltage of 30.0V and 10uF output capacitance is shown in Figure 6. It is not necessary to modify the compensation network.

Channel C2: **Output voltage**, -127mV undershoot (1.4%), 167mV overshoot (1.9%)
200mV/div, 2ms/div, AC coupled

Channel C1: **Load current**, load step 30mA to 150mA and vice versa
50mA/div, 2ms/div

![Figure 6](image-url)

Figure 6
6 Frequency Response – 4.7uF Output Capacitance

Figure 7 shows the loop response at 10V, 30V and 40V input voltage, 150mA load and 4.7uF output capacitance.

10V input
- 150mA load 62 deg phase margin, 32.6 kHz bandwidth, -16 dB gain margin

30V input
- 150mA load 67 deg phase margin, 33.5 kHz bandwidth, -16 dB gain margin

45V input
- 150mA load 69 deg phase margin, 33.5 kHz bandwidth, -17 dB gain margin

Figure 7
7 Frequency Response – 10uF Output Capacitance

Figure 8 shows the loop response at 10V, 30V and 40V input voltage, 150mA load and 10uF output capacitance.

It is not necessary to modify the compensation network.

10V input
• 150mA load 72 deg phase margin, 21.0 kHz bandwidth, -21 dB gain margin

30V input
• 150mA load 75 deg phase margin, 21.6 kHz bandwidth, -20 dB gain margin

45V input
• 150mA load 76 deg phase margin, 21.7 kHz bandwidth, -21 dB gain margin

Figure 8
8 Switching Node

The drain-source voltage on the switching node is shown in Figure 9. The image was captured with 45V input and 150mA load.

Channel C2: **Drain-source voltage**, -2.0V minimum voltage, 47.0V maximum voltage

10V/div, 1us/div

![Figure 9](image-url)
9 Output Ripple Voltage

The output ripple voltage at 150mA load and 10V, 30V and 45V input voltage is shown in Figure 10.

Channel M1: **Output voltage @ 10V input**, 9mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M2: **Output voltage @ 30V input**, 6mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M3: **Output voltage @ 45V input**, 7mV peak-peak
20mV/div, 5us/div, AC coupled

![Figure 10](image_url)
10 Input Ripple Voltage

The input ripple voltage at 150mA load and 10V, 30V and 45V input voltage is shown in Figure 11.

Channel M1: **Input voltage @ 10V input**, 45mV peak-peak
50mV/div, 5us/div, AC coupled

Channel M2: **Input voltage @ 30V input**, 57mV peak-peak
50mV/div, 5us/div, AC coupled

Channel M3: **Input voltage @ 45V input**, 57mV peak-peak
50mV/div, 5us/div, AC coupled

![Input Ripple Voltage Chart]

**Figure 11**
11 Thermal measurement

The thermal image (Figure 12) shows the circuit at an ambient temperature of 21 °C with an input voltage of 30.0V and a load of 150mA.

![Thermal Image](image)

**Figure 12**

<table>
<thead>
<tr>
<th>Markers</th>
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<td>0.95</td>
<td>21.0 °C</td>
</tr>
<tr>
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