PMP10117RevC Test Results

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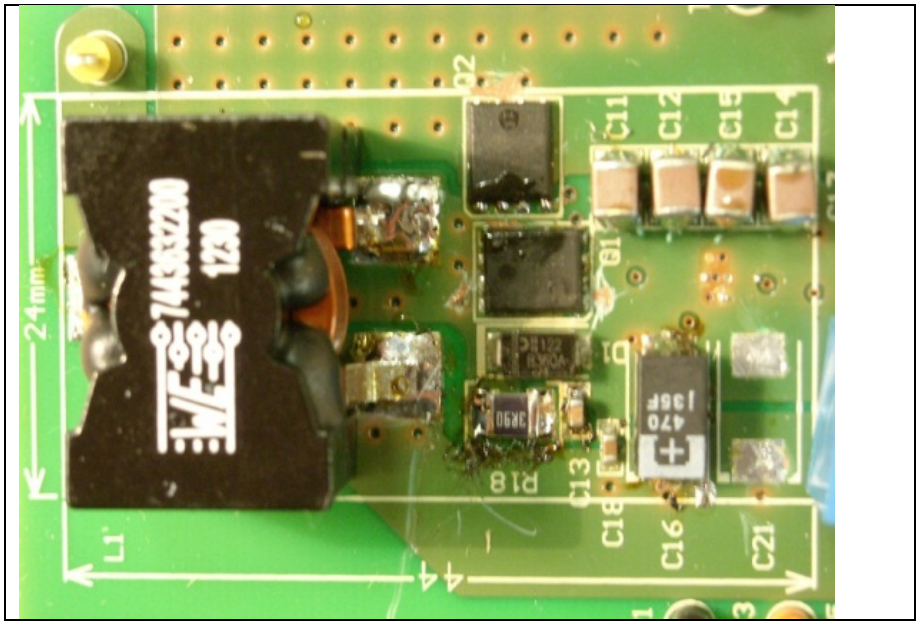
Topology: Buck
Device: TPS40170 "deep impact"

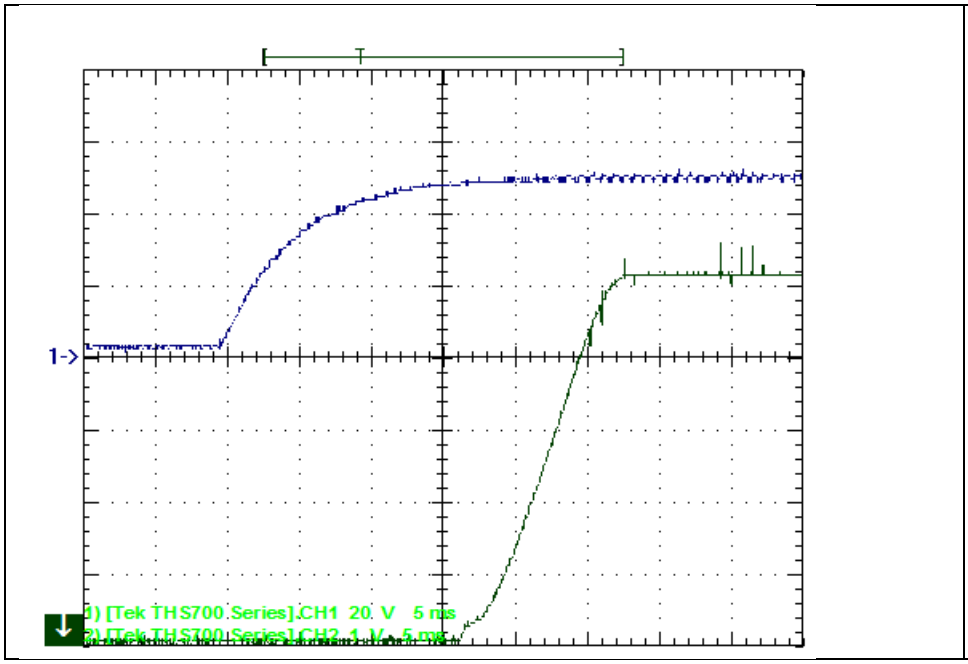
All measurements have been performed at 48V input voltage and 9A output if not otherwise mentioned;

***RevC**: added input filter w/ WE 8070 series, # 744.334.0150, 1.5uH / 4.4milliOhms, 16.5Arms / 18.5Asat, 18.4 x 7.9 x 7.2mm*



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 48V, with 9A load at the output. (Power supply 6554A was switched on)



Ch1=> input voltage 20V/div

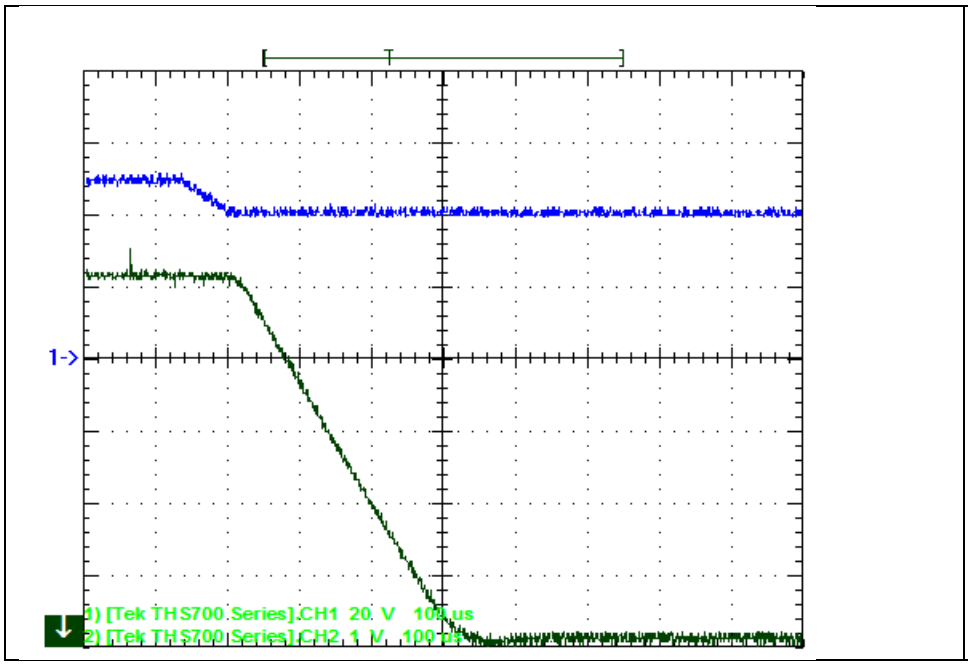
Ch2=> output voltage 2V/div

5ms/div

Figure 1

2 Shutdown

The shutdown waveform is shown in the **Error! Reference source not found.**. The input voltage was set at 48V, with 9A load on the output. (Power Supply was disconnected)



Ch1=> input voltage 20V/div

Ch2=> output voltage 10V/div

100µs/div

Figure 2

3 Efficiency

The efficiency is shown in the Figure 3 below.

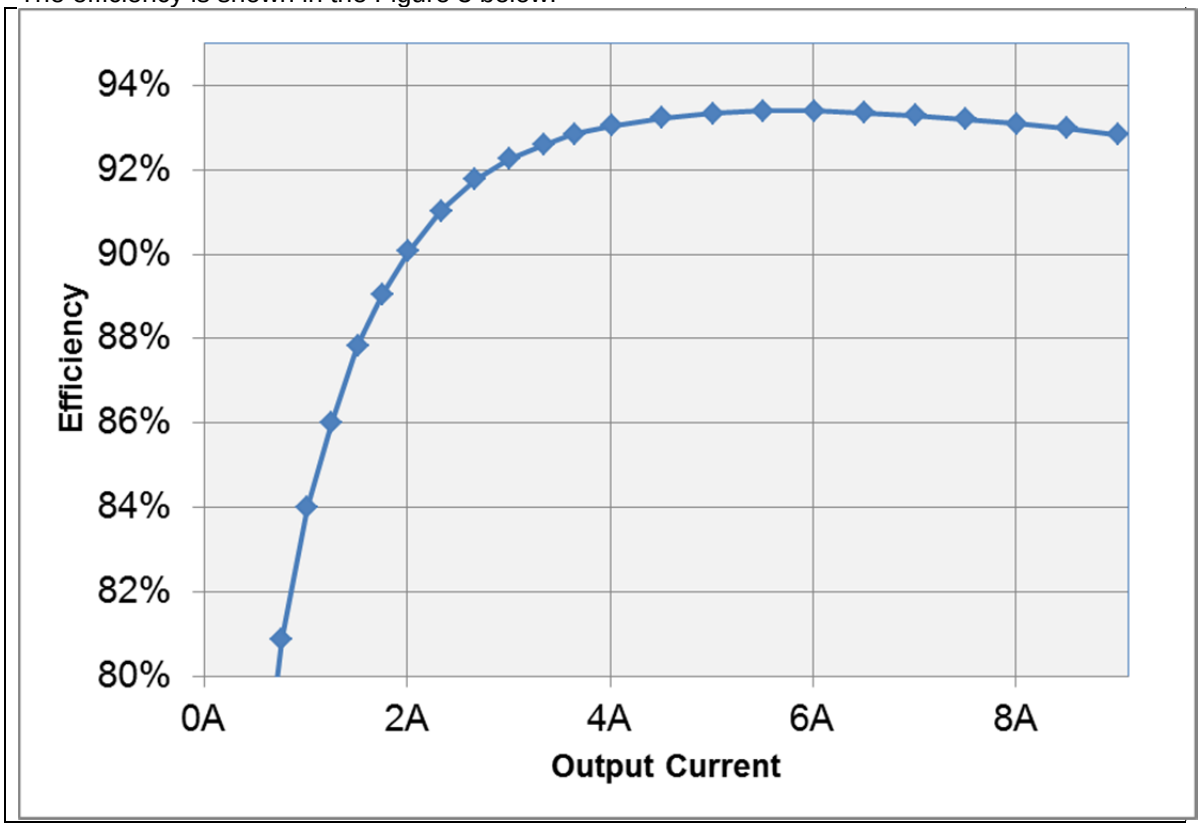


Figure 3

4 Load Regulation

The load regulation is shown in the Figure 4 below, regulation <2mV

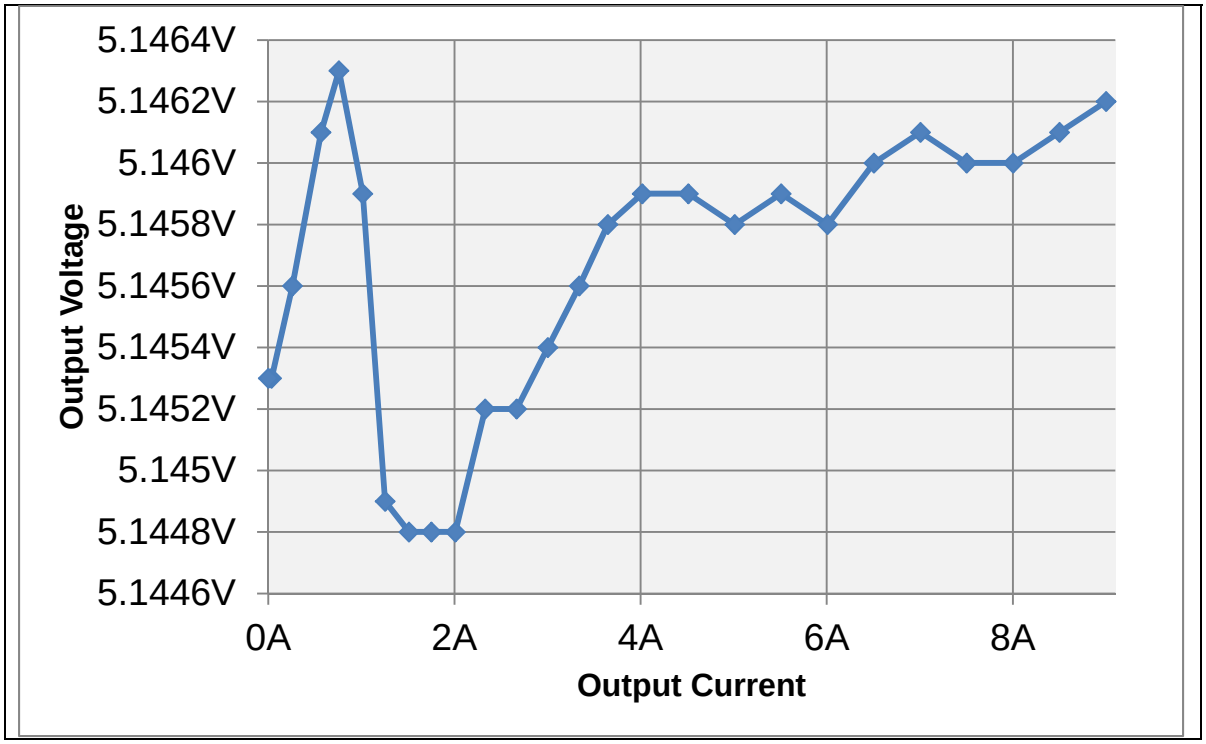
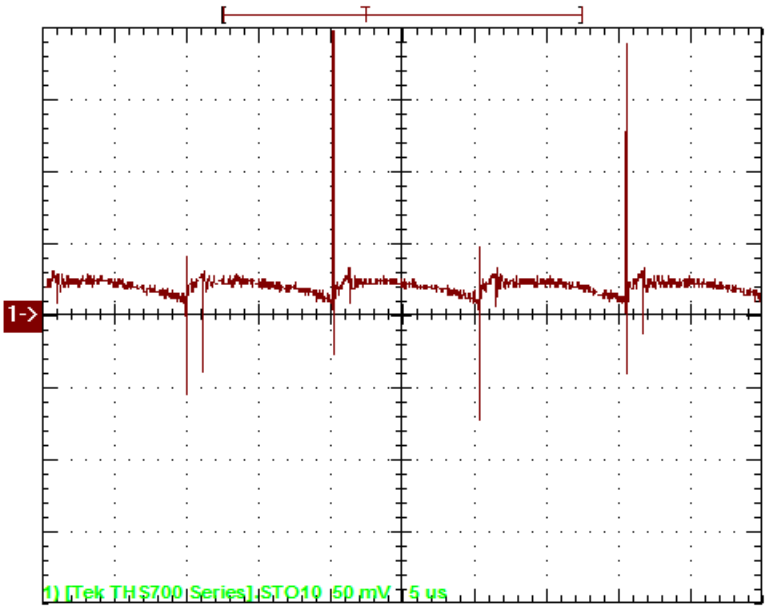


Figure 4

5 Ripple Voltage

The output ripple voltage is shown in Figure 5.



Ch1 => output voltage
50mV/div

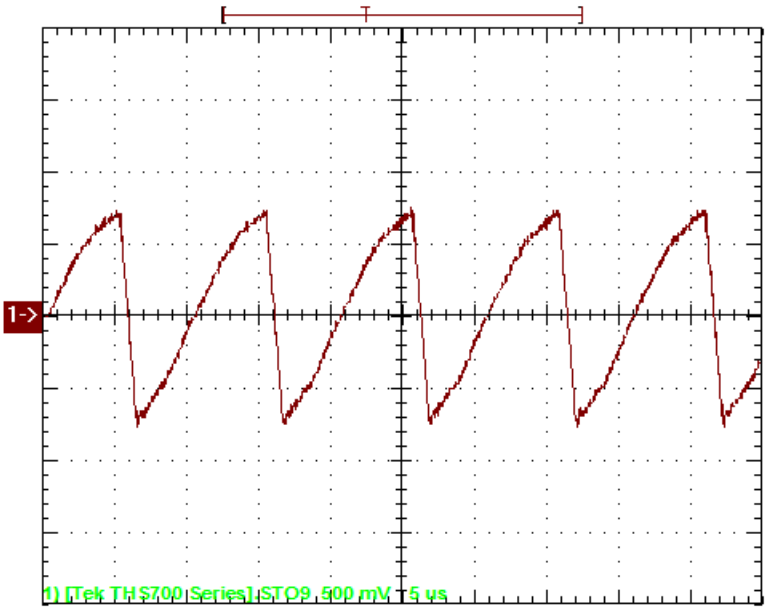
AC coupled

20MHz bandwidth setting

5µs/div

Figure 5

The input ripple voltage is shown in Figure 6.



Ch1 => voltage C17
500mV/div

AC coupled

20MHz bandwidth setting

5µs/div

Figure 6

6 Control Loop Frequency Response

Figure 7 shows the loop response with 9A load (6060B).

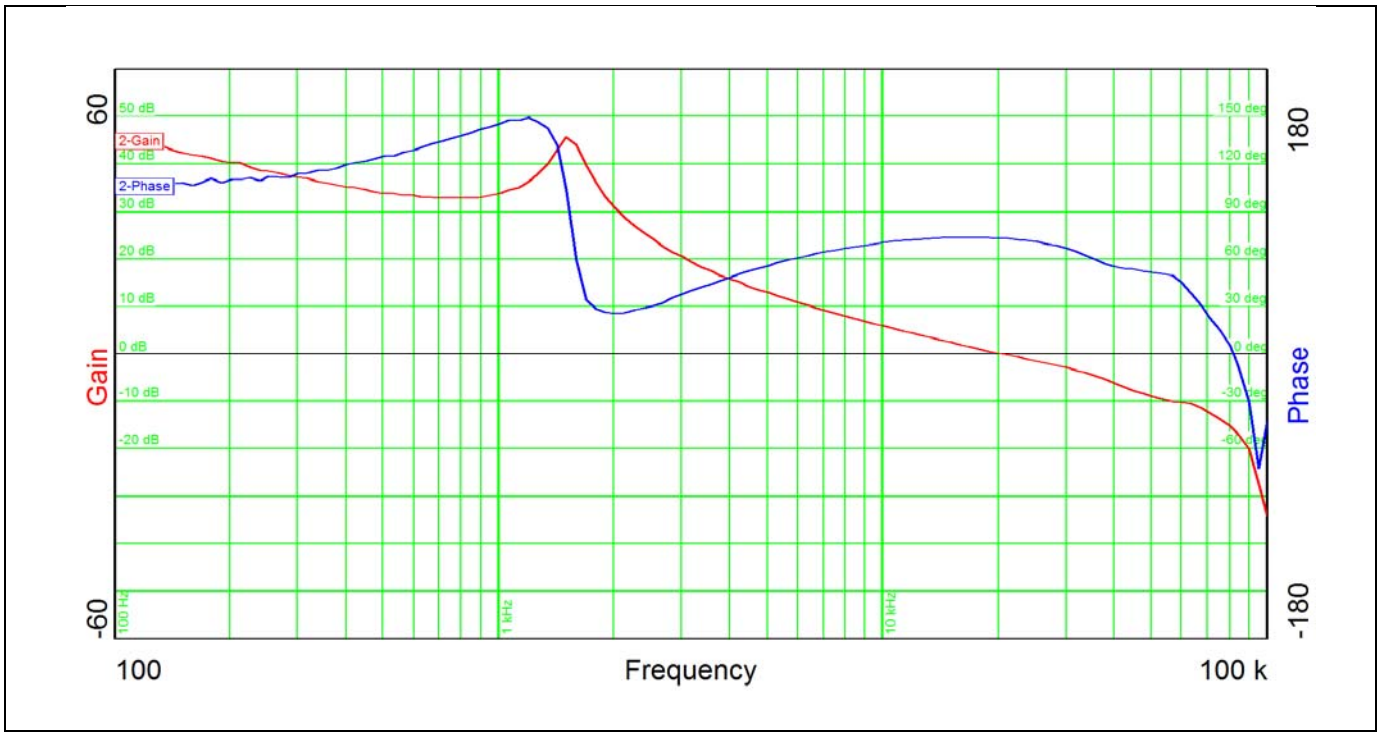


Figure 7

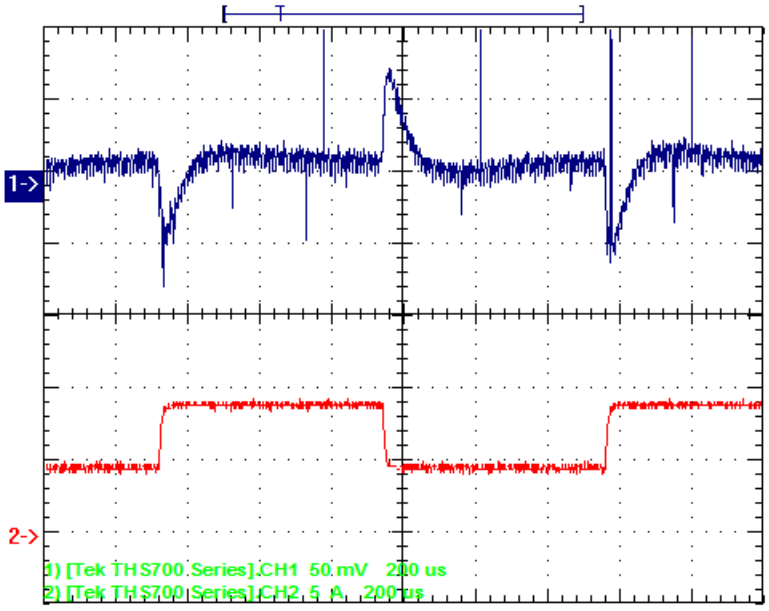
Table 1 summarizes the results from Figure 7

Bandwidth (kHz)	20.4
Phasemargin	73°
slope (20dB/decade)	-0.96
gain margin (dB)	-16
slope (20dB/decade)	-3.7
freq (kHz)	81.7

Table 1

7 Load Transients

The Figure 8 shows the response to load transients. The load is switching from 4.5A to 9A.with 800Hz frequency (6060B load).



Ch1 => output voltage 50mV/div

deviation <2%

Ch2 => output current 5A/div

20MHz bandwidth setting

200µs/div

Figure 8

8 Miscellaneous Waveforms

8.1 Switch node (LS-FET Q1)

With input voltage set to 48V and 9A Iout results in the waveform shown in Figure 9

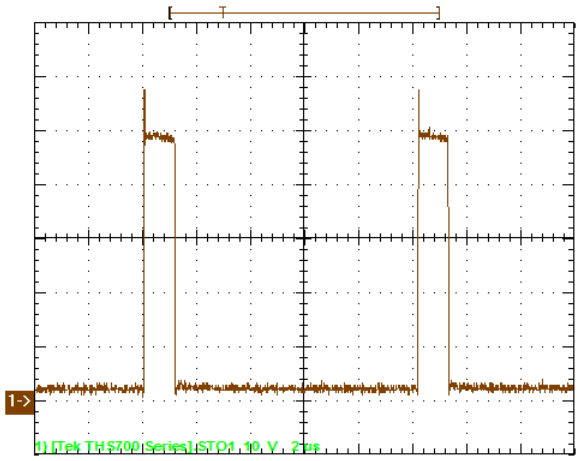
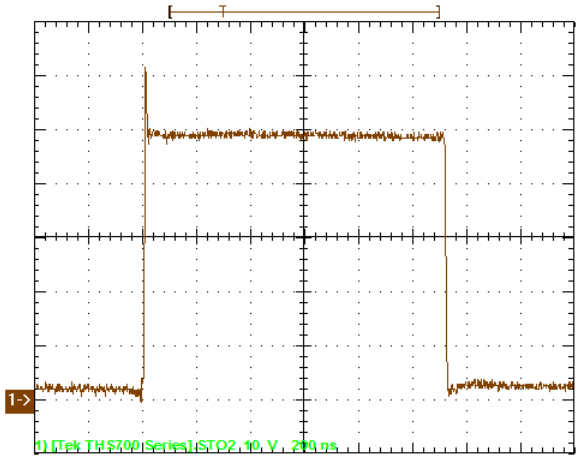
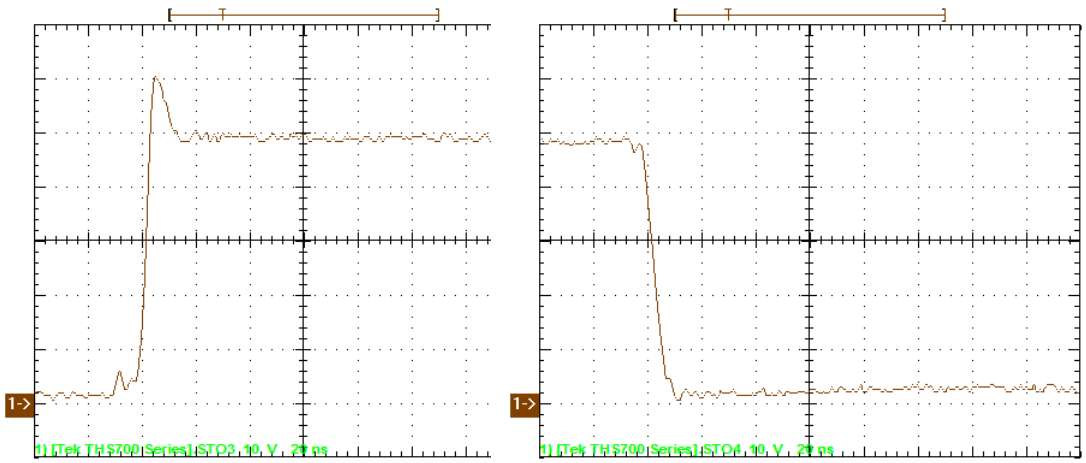
	Ch1 => 10V/div 2us/div full BW
	Ch1 => 10V/div 200ns/div
	Ch1 => 10V/div 20ns/div

Figure 9

8.2 Gate Q1 (LS-FET)

Figure 10 shows the waveform across gate Q1 to GND

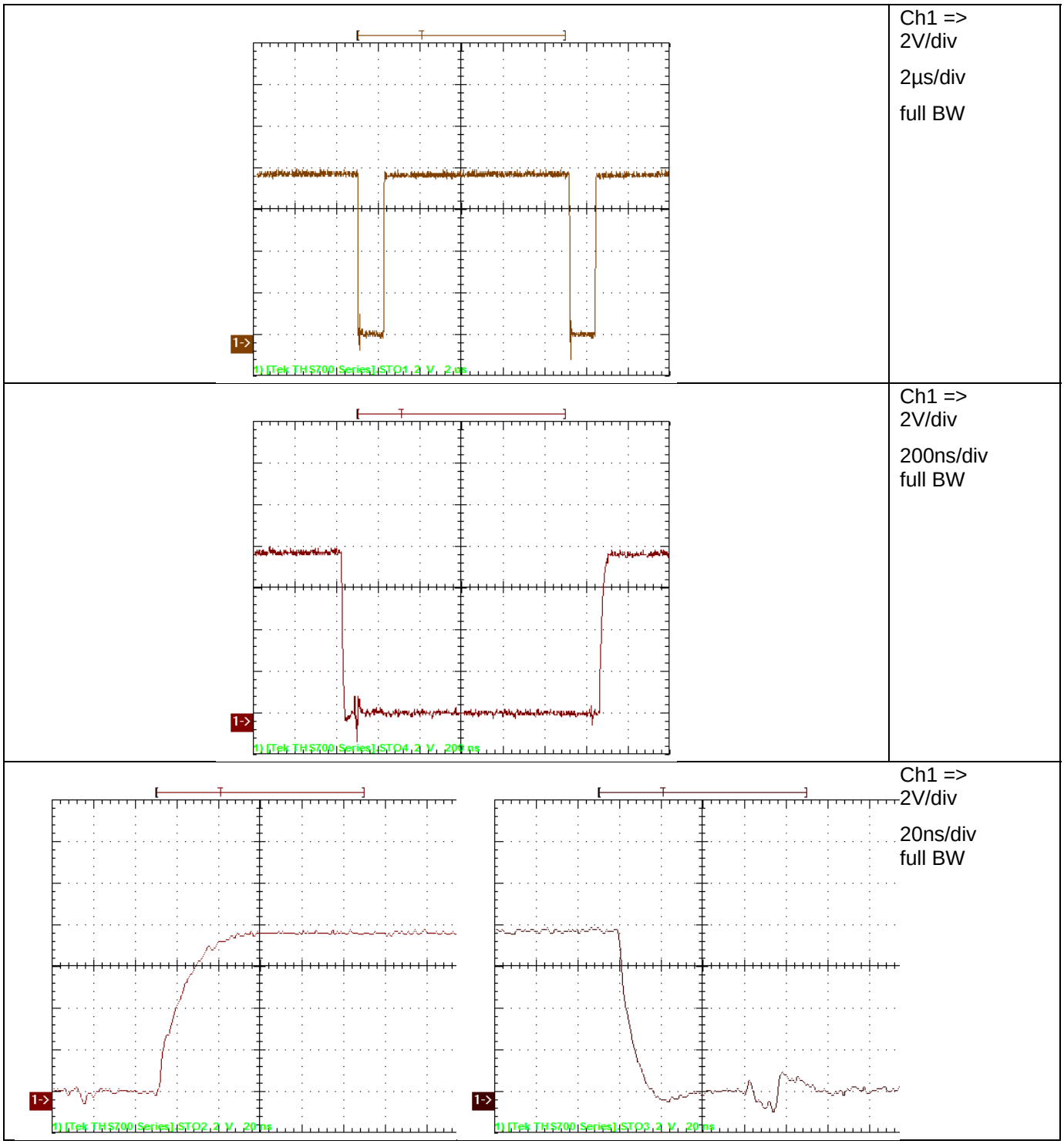


Figure 10

8.3 Drain-Source Voltage of the High Side MOSFET

Measured with reference to VIN and waveform is displayed inverted.
The waveform is shown in Figure 11, gate vs. switchnode:

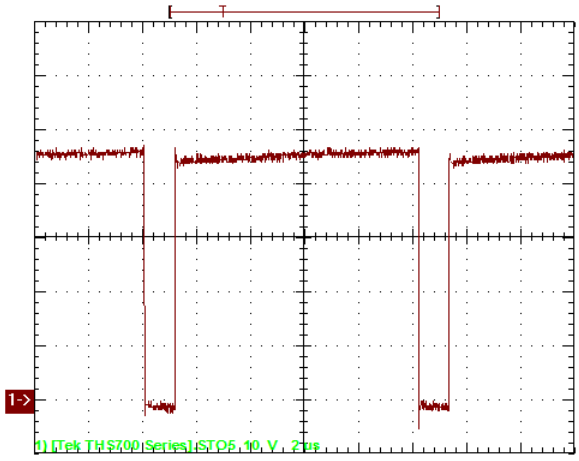
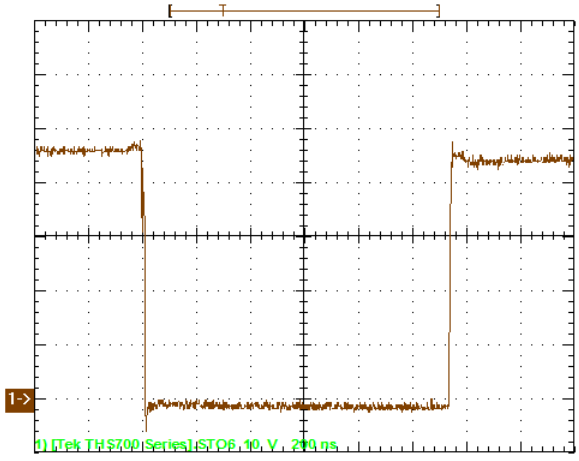
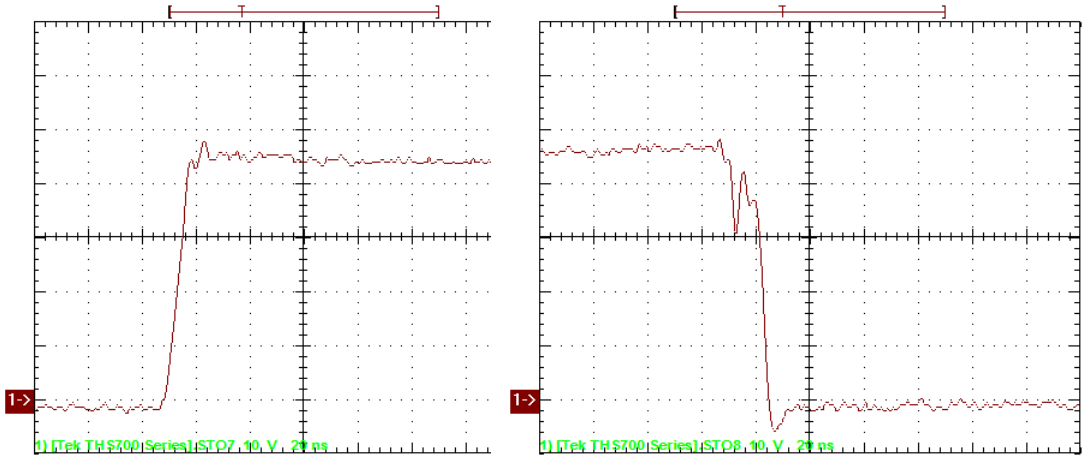
	Ch1 => 10V/div 2µs/div
	
	Ch1 => 10V/div 20ns/div

Figure 11

8.4 Gate Q2 High Side MOSFET (gate-switchnode)

With input voltage set to 48V and 9A Iout results in the waveform shown in Figure 12

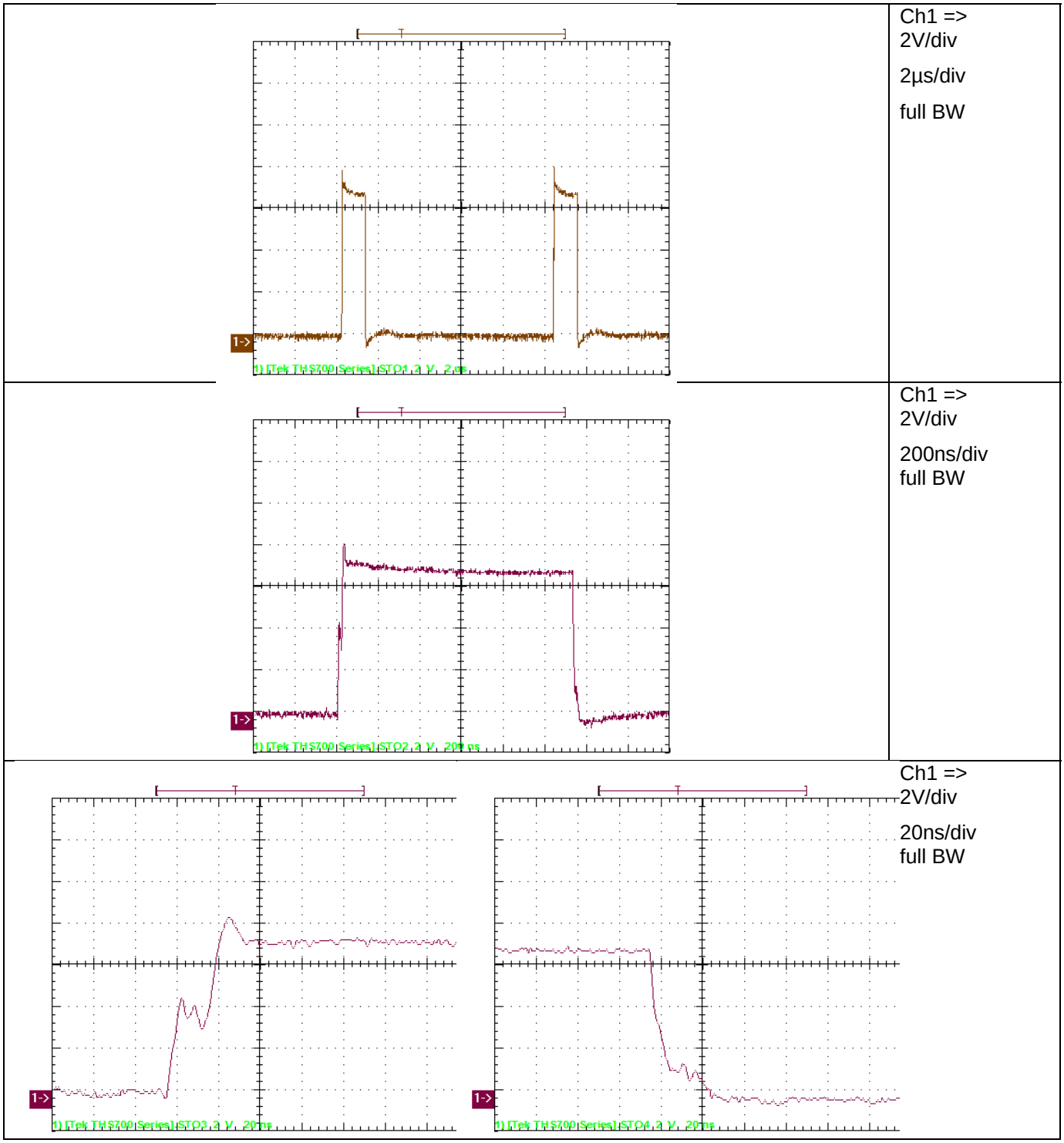


Figure 12

9 Thermal Image

Figure 13 shows the thermal image at 48V input and 9A output (30 mins full load)

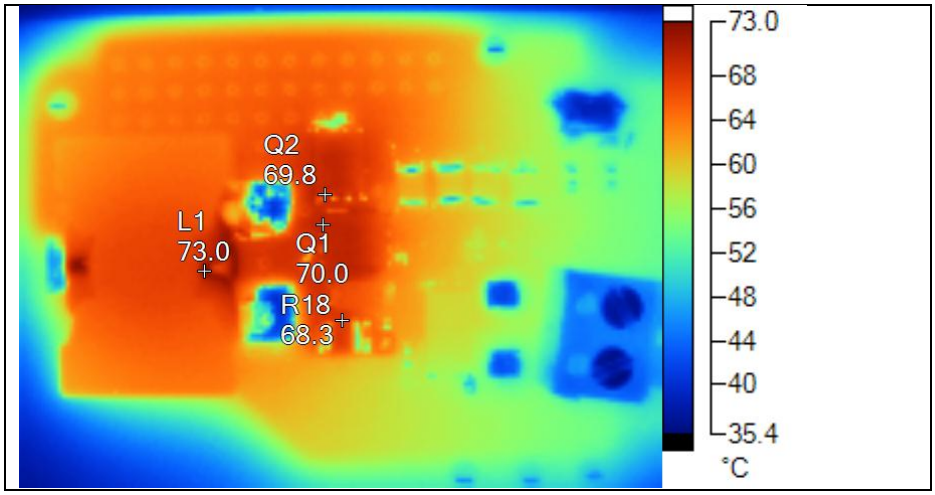


Figure 13

Name	Temperature
L1	73.0°C
Q2	69.8°C
Q1	70.0°C
R18	68.3°C

Table 2

10 Appendix, added input filter to attenuate reflected ripple

Revision C:

In Revision C inductor 74433401050 from Wuerth Electronic is chosen as input filter inductor L2. Figure 14 shows the input ripple voltage across C20 (Channel 1) and C11-C15 (Channel 2). The ripple voltage across C20 is reduced by a factor of 10.

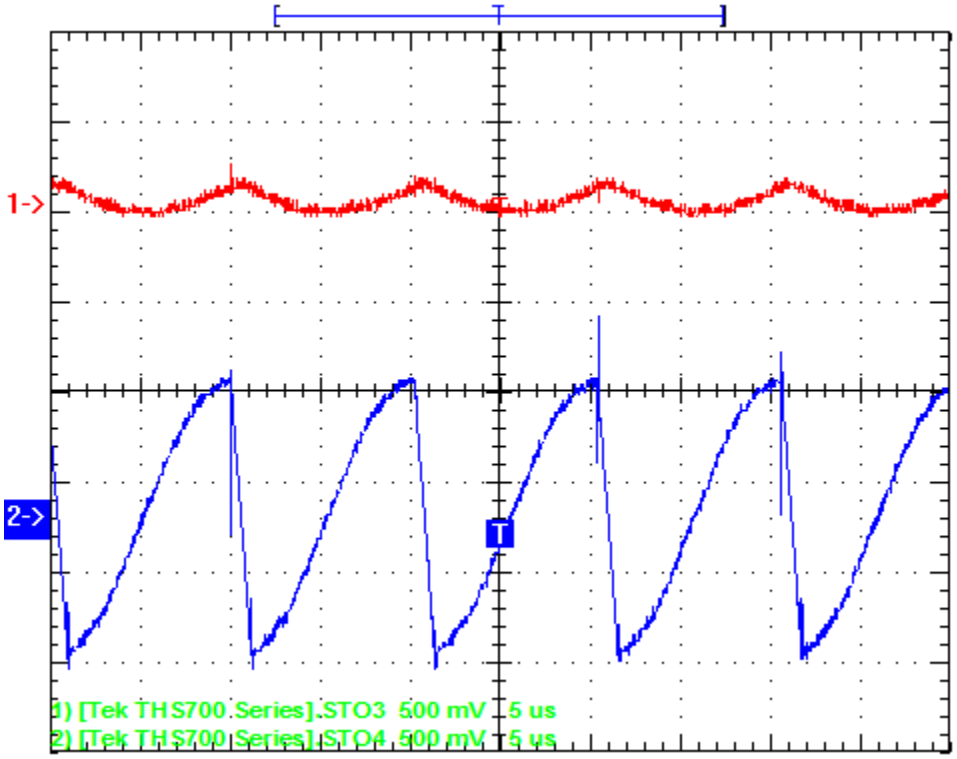


Figure 14

Attenuation roughly -20dB (1.5Vpp vs. 150mVpp) and far less RF content

Current consumption with and without L2 is as follows;
estimated power losses 3Arms^2 x 5milliOhms around 45mW, measured 86mW:

	Without L2	With L2
V_{in}	48.001 V	47.993 V
I_{in}	1.0359 A	1.0377 A
I_{out}	8.995 A	8.992 A

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