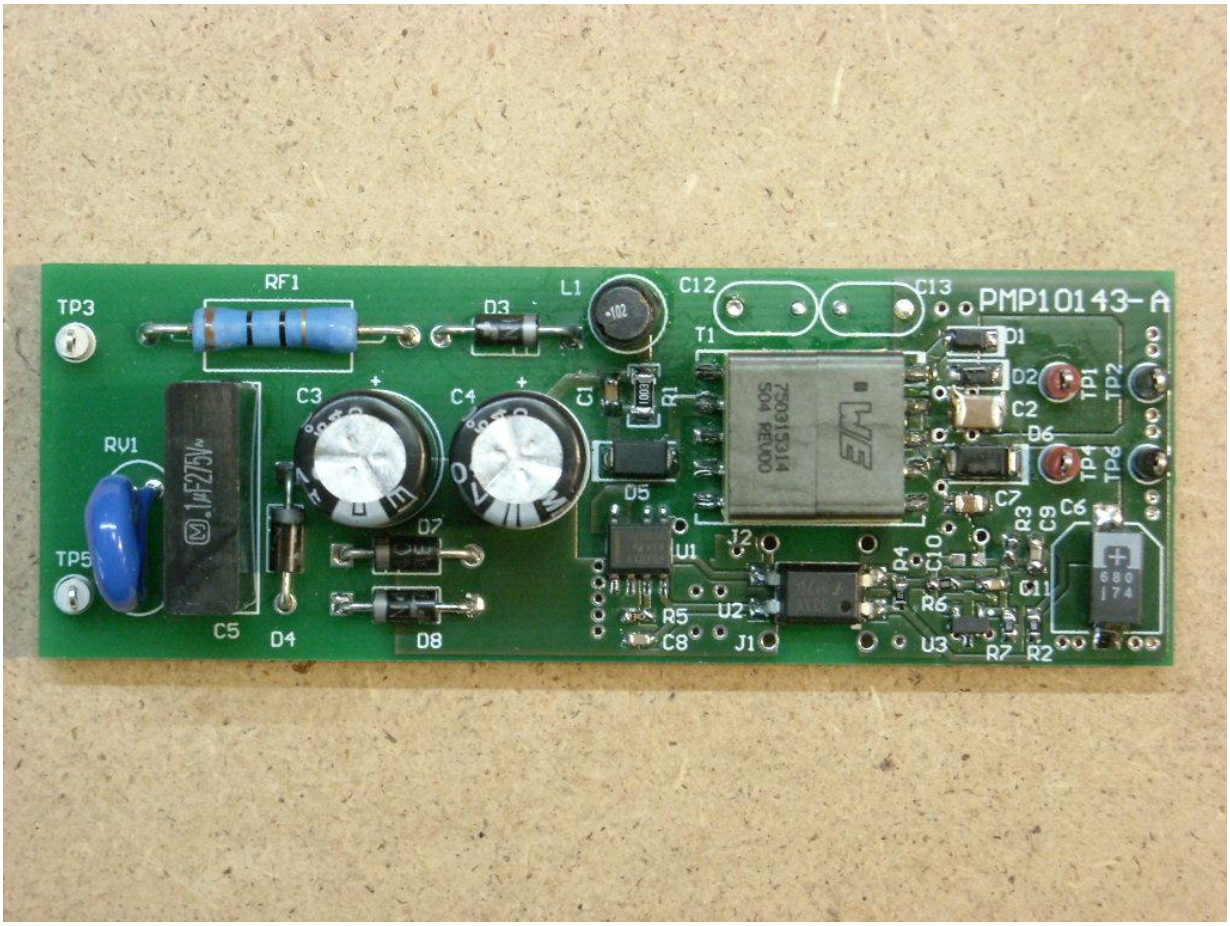
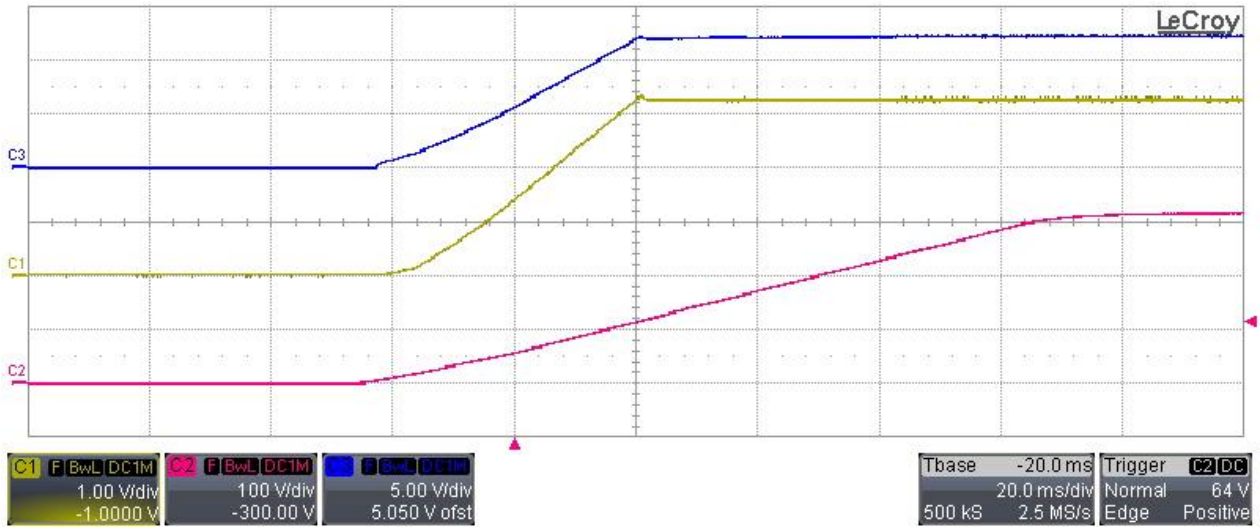
PHOTO OF THE PROTOTYPE



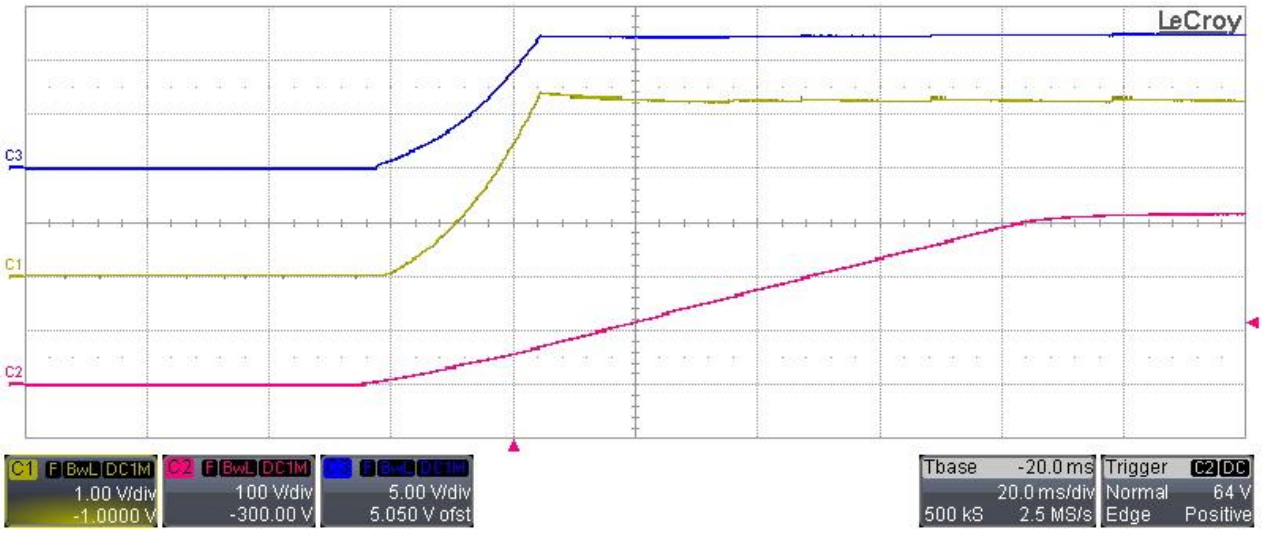
1 Output Voltage at Startup

The output voltage ramp-up behavior for both outputs is shown in the pictures below. The input voltage has been set to 322Vdc. In the upper picture both outputs have been fully loaded, while for the bottom one no load has been applied.

Ch1: 3.3Vout (1V/div, 20MHz BWL, 20msec/div)
Ch2: Input DC voltage (100V/div, 20MHz BWL)
Ch3: 12Vout (5V/div, 20MHz BWL)
Both outputs loaded at nominal value:

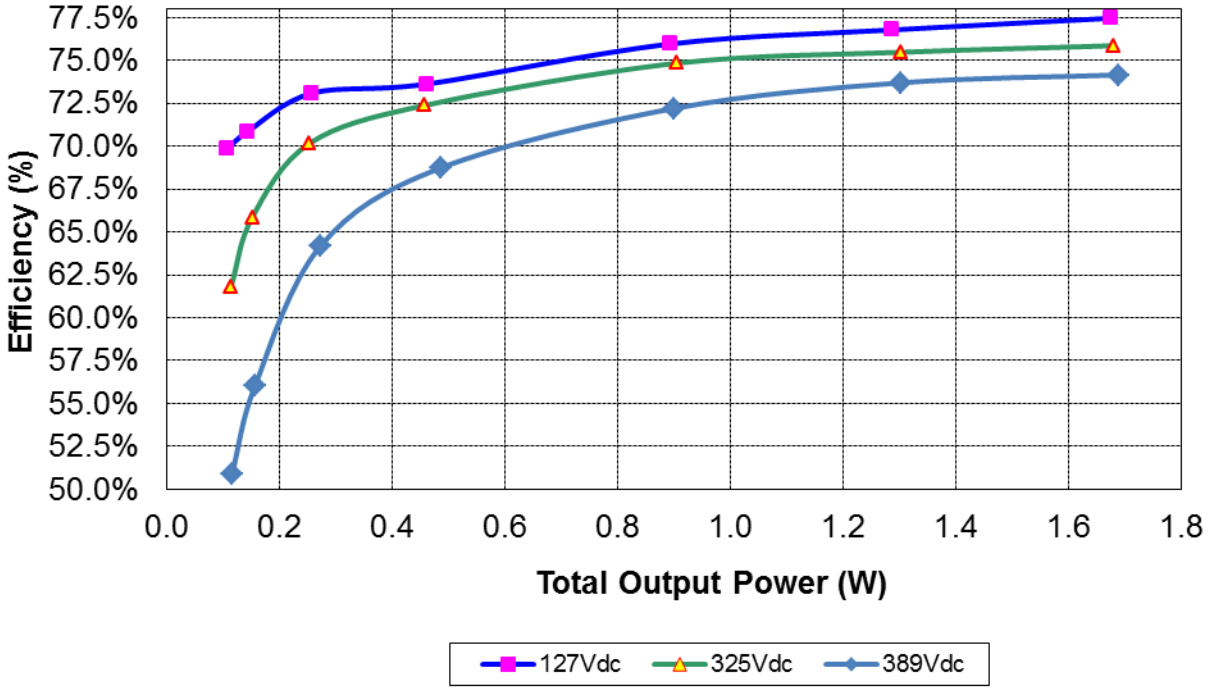


Ch1: 3.3Vout (1V/div, 20MHz BWL, 20msec/div)
Ch2: Input DC voltage (100V/div, 20MHz BWL)
Ch3: 12Vout (5V/div, 20MHz BWL)
Both outputs unloaded:


LeCroy
C3
C1
C2
C1 F BwL DC1M
1.00 V/div
-1.0000 V
C2 F BwL DC1M
100 V/div
-300.00 V
5.00 V/div
5.050 V ofst
Tbase -20.0 ms
20.0 ms/div
500 kS 2.5 MS/s
Trigger C2 DC
Normal 64 V
Edge Positive

2 Efficiency

The efficiency data are shown in the tables and graphs below. All outputs have been loaded proportionally. The input voltage has been set to 200Vdc, 325Vdc and 375V (equivalent to the rectified 141Vac, 230Vac and 265Vac).



Vin (Vdc)	Vin (Vac)	Iin (mA)	Pin (W)	V12 (V)	I12 (mA)	V3.3 (V)	I3.3 (mA)	Pout (W)	Ploss (W)	Eff (%)
127	90	0.234	0.030	12.54	0	3.268	0	0.000	0.030	0.0%
127	90	1.203	0.153	11.47	6.2	3.268	10.9	0.107	0.046	69.9%
127	90	1.590	0.202	11.64	6.2	3.268	21.7	0.143	0.059	70.9%
127	90	2.77	0.352	11.66	10.7	3.268	40.5	0.257	0.095	73.1%
127	90	4.92	0.625	11.87	10.7	3.268	101.9	0.460	0.165	73.6%
127	90	9.25	1.175	11.88	19.9	3.268	200.7	0.892	0.282	76.0%
127	90	13.18	1.674	11.90	25.0	3.267	302.3	1.285	0.389	76.8%
127	90	17.02	2.162	11.91	30.5	3.267	401.3	1.674	0.487	77.5%

Vin (Vdc)	Vin (Vac)	Iin (mA)	Pin (W)	V12 (V)	I12 (mA)	V3.3 (V)	I3.3 (mA)	Pout (W)	Ploss (W)	Eff (%)
325	230	0.288	0.094	13.14	0	3.277	0	0.000	0.094	0.0%
325	230	0.565	0.184	11.29	6.9	3.268	10.9	0.114	0.070	61.8%
325	230	0.705	0.229	11.63	6.9	3.268	21.6	0.151	0.078	65.8%
325	230	1.108	0.360	11.71	10.3	3.268	40.4	0.253	0.107	70.2%
325	230	1.945	0.632	12.09	10.3	3.268	101.9	0.458	0.175	72.4%
325	230	3.72	1.209	12.05	20.7	3.267	200.6	0.905	0.304	74.8%
325	230	5.31	1.726	12.11	26.0	3.267	302.3	1.302	0.423	75.5%
325	230	6.81	2.213	12.14	30.3	3.267	401.3	1.679	0.534	75.9%

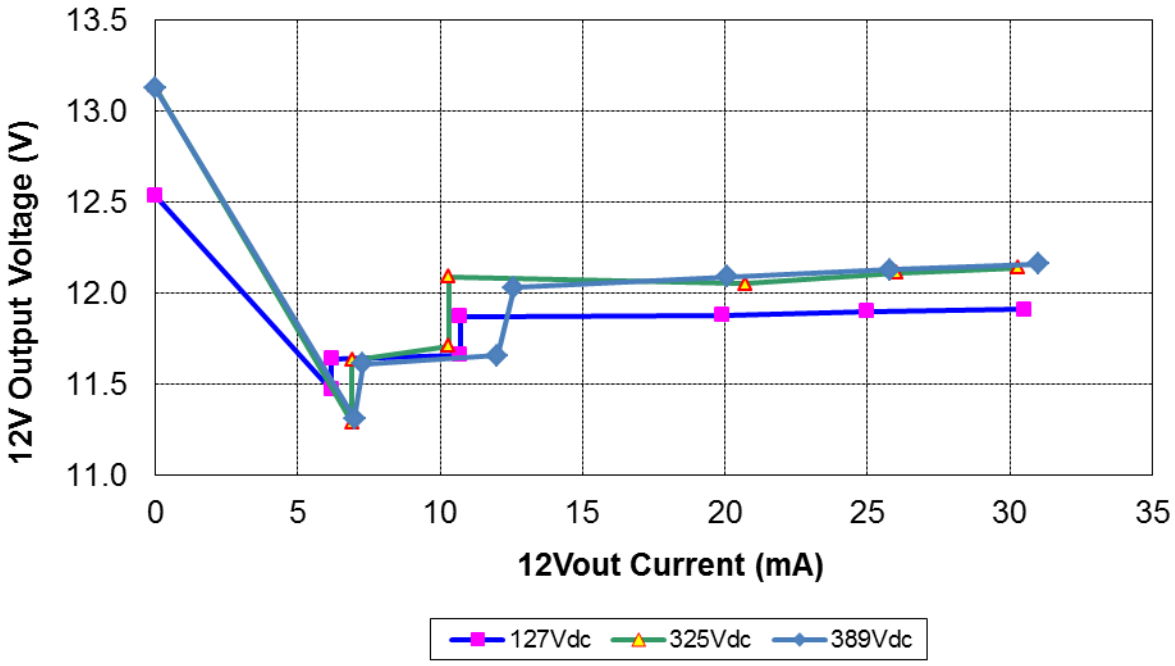
Vin	Vin	Iin	Pin	V12	I12	V3.3	I3.3	Pout	Ploss	Eff

(Vdc)	(Vac)	(mA)	(W)	(V)	(mA)	(V)	(mA)	(W)	(W)	(%)
389	275	0.374	0.145	13.13	0	3.281	0	0.000	0.145	0.0%
389	275	0.582	0.226	11.31	7.0	3.271	11.0	0.115	0.111	50.9%
389	275	0.716	0.279	11.61	7.3	3.271	21.8	0.156	0.122	56.0%
389	275	1.092	0.425	11.66	12.0	3.271	40.6	0.273	0.152	64.2%
389	275	1.815	0.706	12.03	12.6	3.271	102.0	0.485	0.221	68.7%
389	275	3.203	1.246	12.09	20.1	3.270	200.8	0.900	0.346	72.2%
389	275	4.541	1.766	12.13	25.8	3.269	302.5	1.302	0.465	73.7%
389	275	5.857	2.278	12.16	31.0	3.269	401.5	1.689	0.589	74.2%

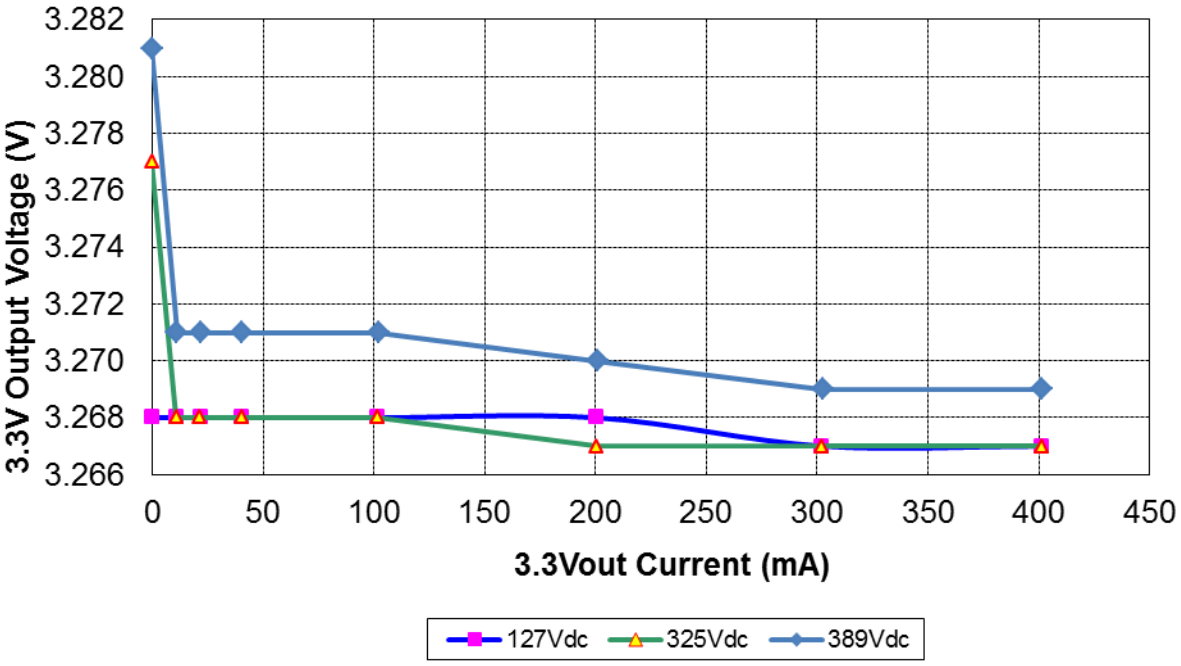
3 Output Voltage Regulation vs. Load

Both output voltages variation versus their own loads have been plotted in the graphs below.

12Vout:



3.3Vout:



4 Cross regulation

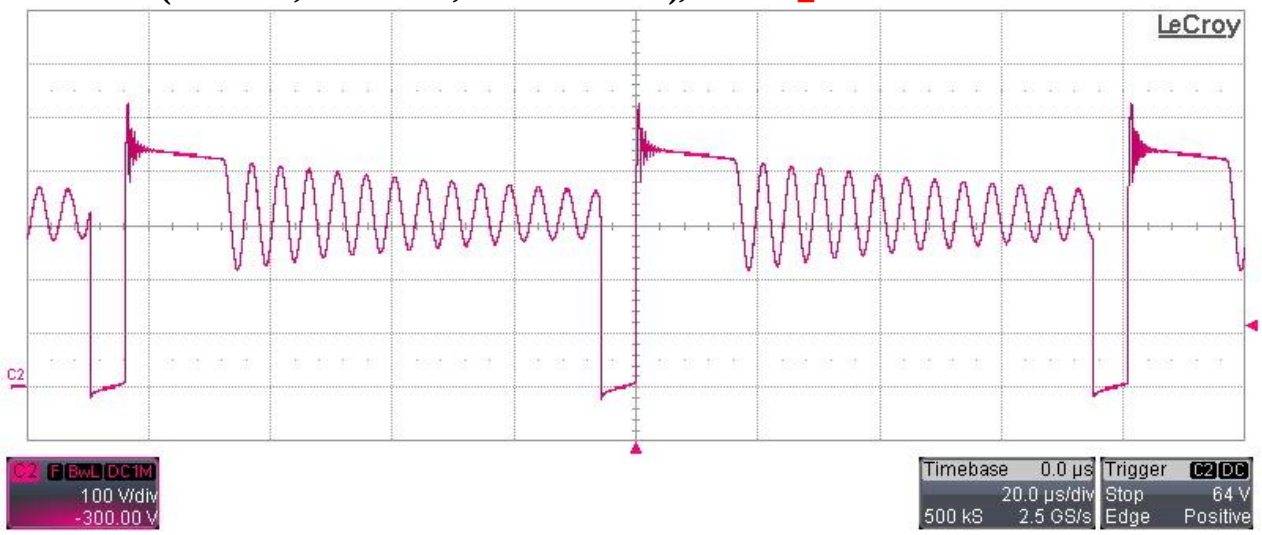
4.1 A minimum current of 30mA on 3.3Vout is needed to get V12 ≥ 11V when this outputs was loaded to 30mA

4.2 A minimum current of 13mA on 3.3Vout is needed to get V12 ≥ 11V when this outputs was loaded to 15mA

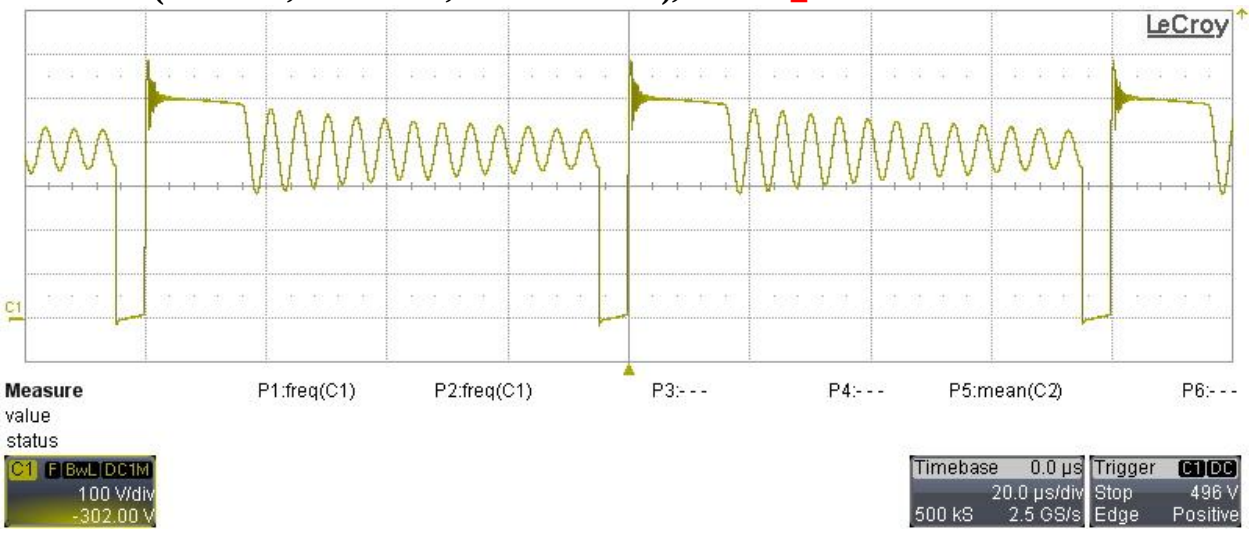
5 Switching Node Waveforms

The images below show the voltage on switch node (pin 8 of U1) at 325Vdc and 389Vdc input voltage and full load conditions.

Ch2: Pin 8 of U1 (100V/div, 20usec/div, 200MHz BWL), 325Vdc_in



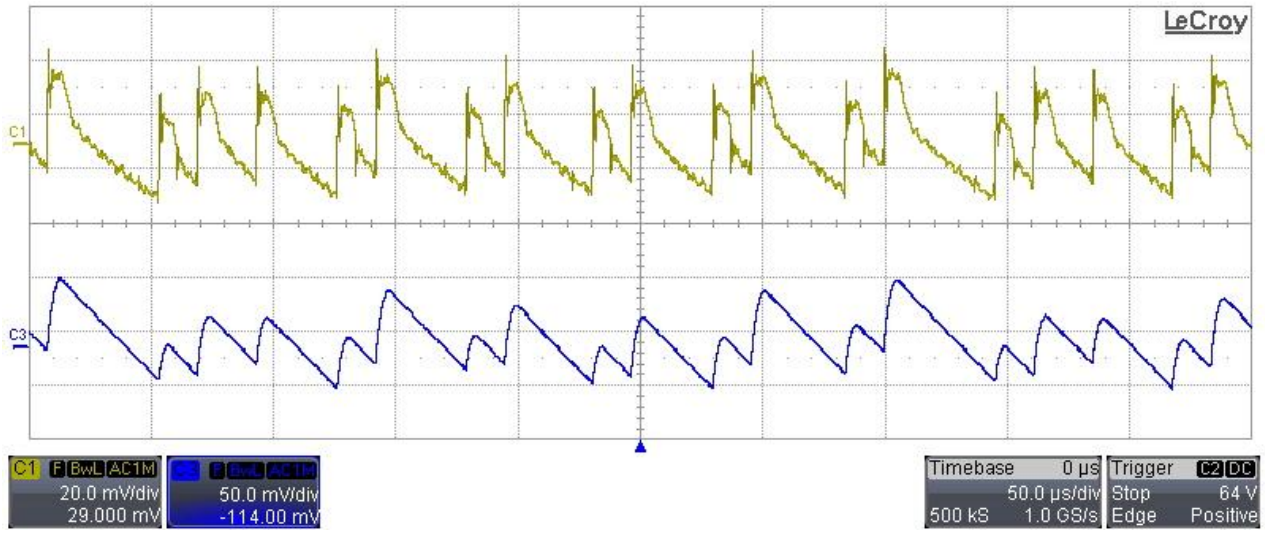
Ch1: Pin 8 of U1 (100V/div, 20usec/div, 200MHz BWL), 389Vdc_in



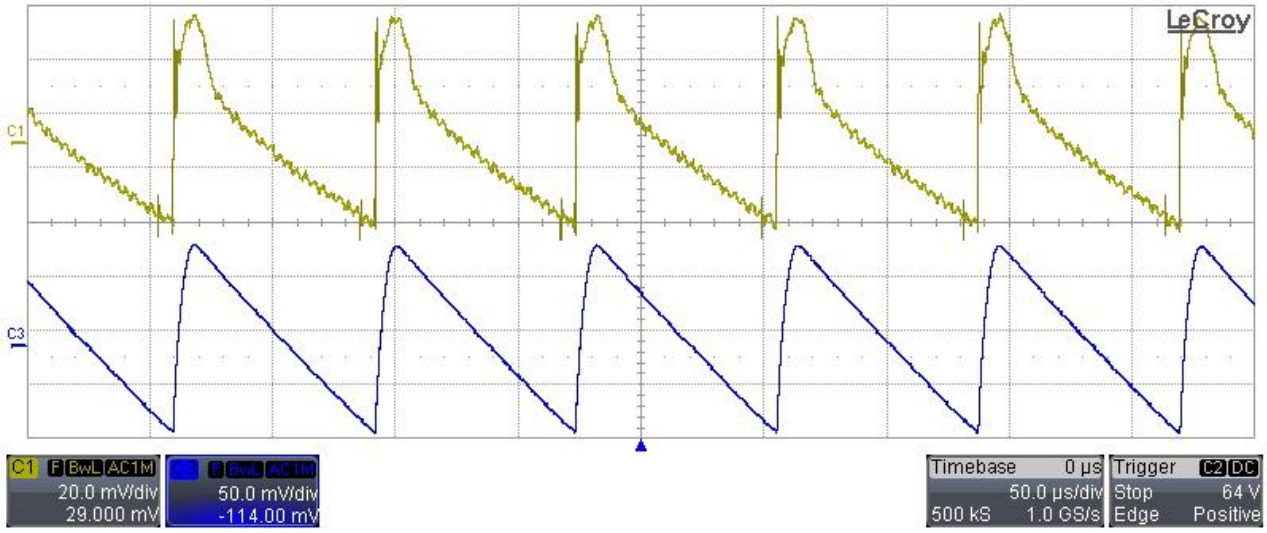
6 Output Ripple Voltages

The output ripple voltages on both outputs are shown below.
The input voltage has been set to 130Vdc and 322Vdc and the outputs fully loaded.

Ch1: 3.3Vout (20mV/div, 20MHz BWL, AC coupling, 50usec/div)
Ch2: 12Vout (50mV/div, 20MHz BWL, AC coupling)
Vin = 130Vdc



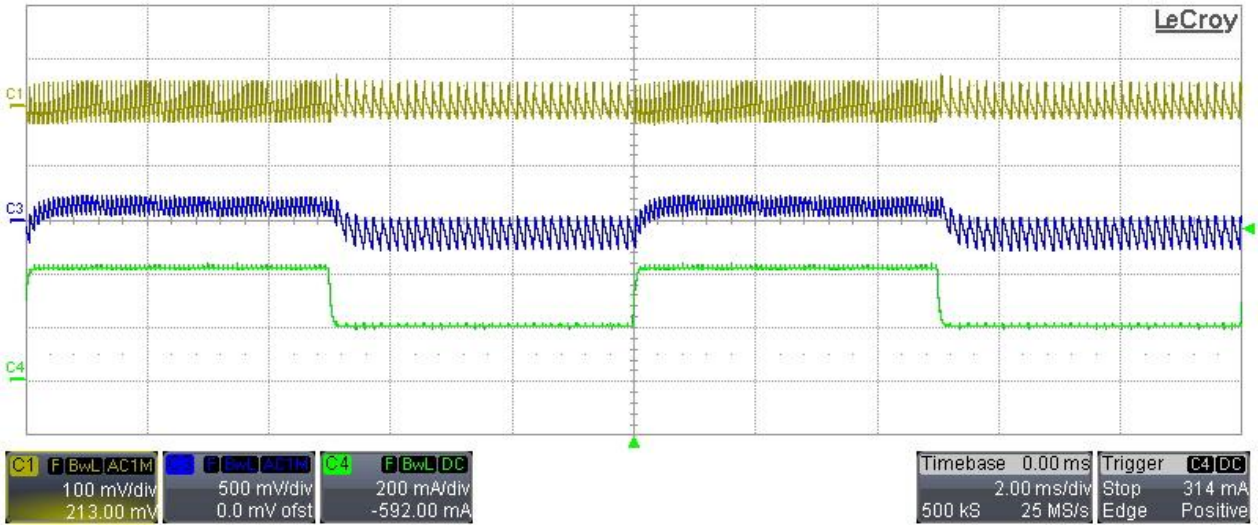
Ch1: 3.3Vout (20mV/div, 20MHz BWL, AC coupling, 50usec/div)
Ch2: 12Vout (50mV/div, 20MHz BWL, AC coupling)
Vin = 322Vdc



7 Transient Response on 3.3Vout with 12V fully loaded

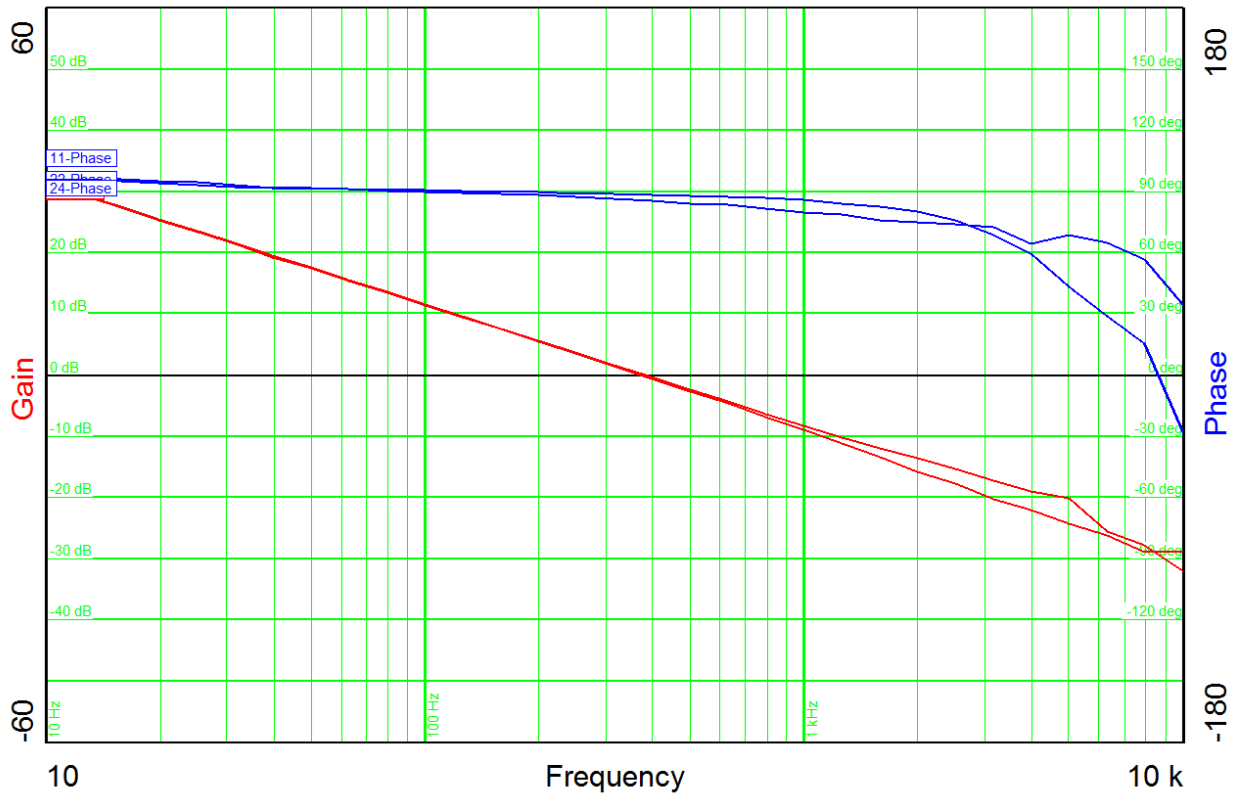
The 3.3V output voltage variation, and 12Vout, versus transient load is shown below. The input voltage has been set to 325Vdc and the load on the 3.3Vout switched between 200A and 400mA while the load on the 12Vout has been kept constant to 30mA.

Ch1: 3.3Vout (100mV/div, 20MHz BWL, AC coupling, 2msec/div)
Ch3: 12Vout (500mV/div, 20MHz BWL, AC coupling)
Ch4: 3.3 output current (200mA/div, 20MHz BWL, DC coupling)



8 Loop Analysis

The loop response vs frequency is plotted below. The converter has been tested at 130Vdc and 320Vdc input voltage in full load conditions. The crossover frequency was 372 Hz, the phase margin 85.8 degrees, and the gain margin 28.9dB.


60
50 dB
40 dB
11-Phase
24-Phase
20 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
-60
Gain
10 Hz
100 Hz
1 kHz
180
150 deg
120 deg
90 deg
60 deg
30 deg
-30 deg
-60 deg
-120 deg
-180
Phase
10
Frequency
10 k

9 Thermal Analysis

The thermal analysis of the converter shows the temperatures for each component, in the graphs below. The converter has been placed horizontally on the bench without any forced convection. The input voltage was 325Vdc with both outputs fully loaded. The ambient temperature was 23C.

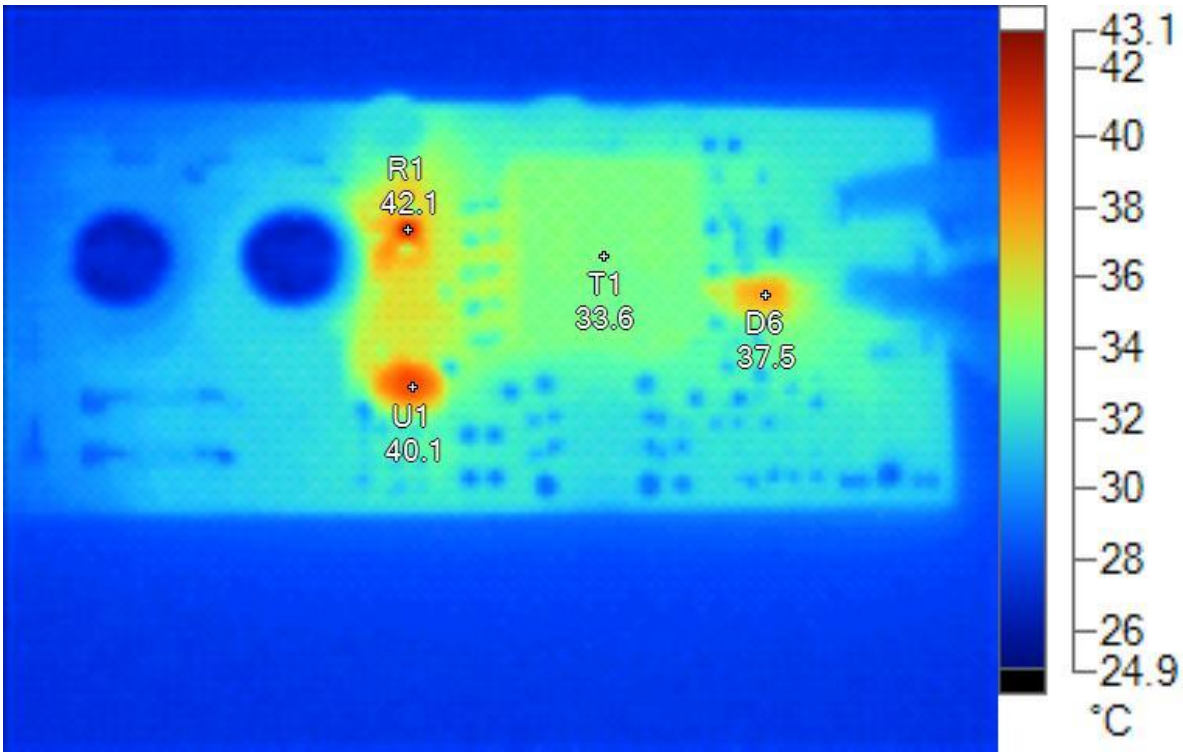


Image Info

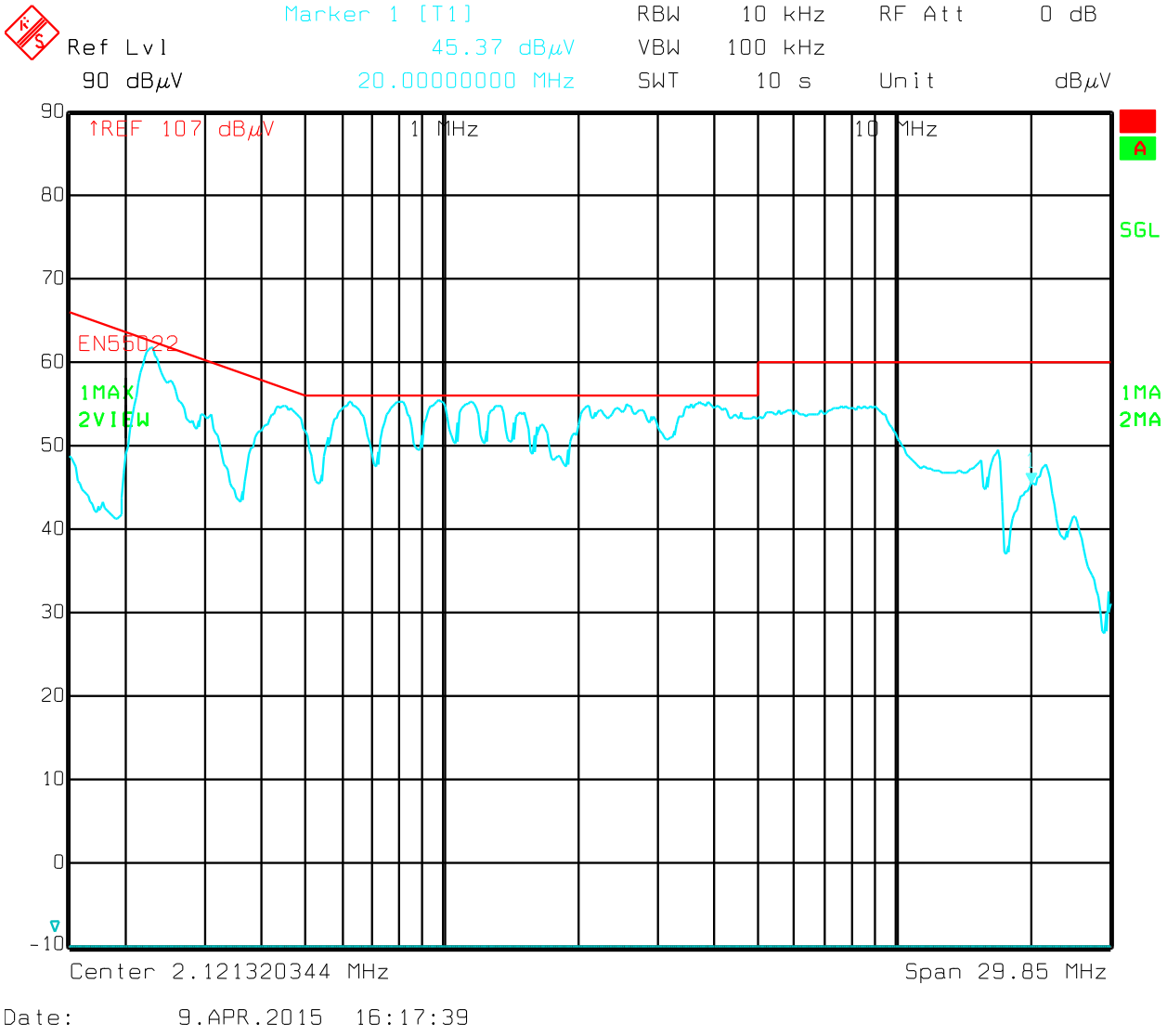
Background temperature	23.0°C
Average Temperature	29.8°C
Image Range	26.0°C to 42.1°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	3/6/2015 5:44:25 PM

Main Image Markers

Name	Temperature
U1	40.1°C
R1	42.1°C
D6	37.5°C
T1	33.6°C

10 EMI Measurement

The graph below shows the EMI conducted emission measurement. The board has been supplied @ 230Vac by means of an isolation transformer BR350, a LISN Hameg HM6050-2 and the Rohde & Schwarz receiver 9KHz…3.5GHz measured the EMI signature. The load was a passive resistor for both outputs; the ground of the 3.3V has been connected to the ground of the LISN. The limit shows the EN55022 Grade B and the receiver detector was set to "quasi peak".



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