

TIDA-00782 Test Results

About Test Results

This reference design incorporates the DLP 0.45" WXGA chipset comprising of the DLP4501 DMD and DLPC6401 controller. The TI design enables faster development cycles for this specific chipset.

If You Need Assistance

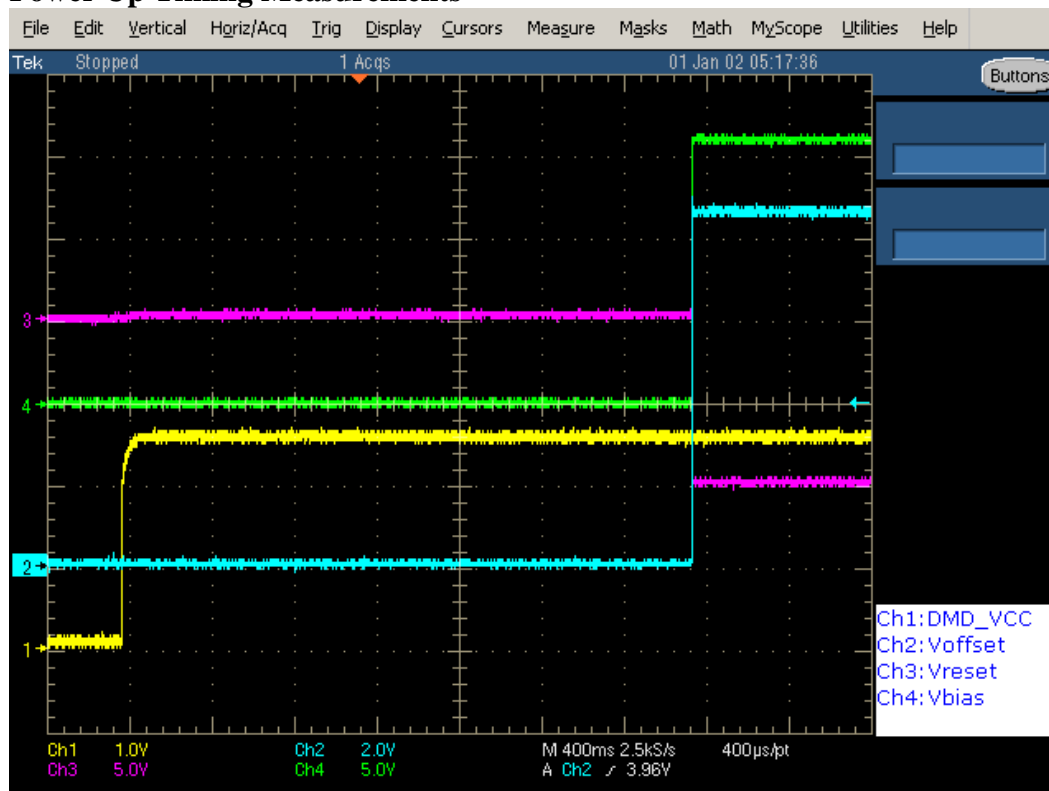
Refer to the DLP and MEMS TI E2E Community support forums:

https://e2e.ti.com/support/dlp_mems_micro-electro-mechanical_systems/f/947

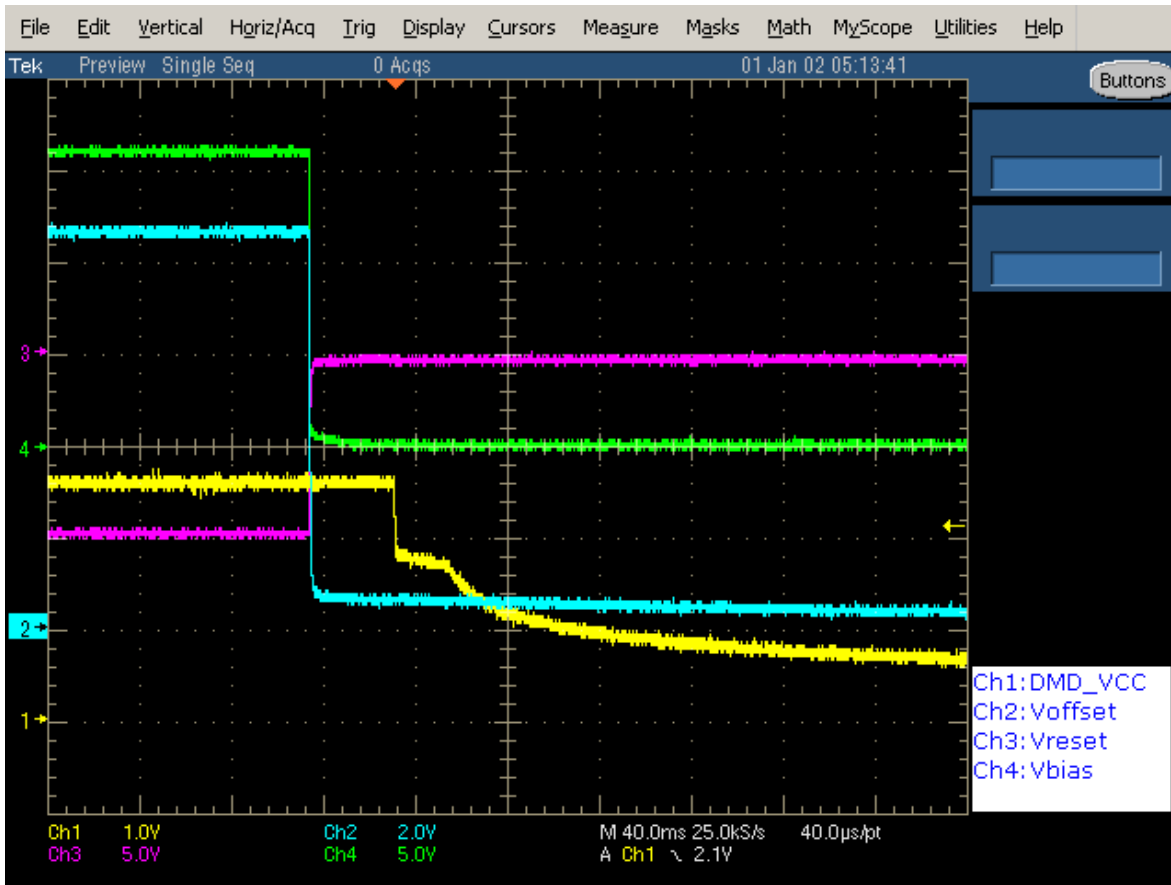
2. Power Up and Power Down Timing Measurements

Power Up and Power Down timing requirements are described in detail in the DLP4501 datasheet. Key signals measured are PROJ_ON and the power supplies to the DMD- VBIAS, VOFFSET and VRESET. For more details on the timing requirements please refer the DLP4501 device datasheet.

Power Up Timing Measurements



Power down Timing Measurements



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