PMP11328 Test Report

Xilinx application: TPS544C25 for 0.85V 25A max electrical and 22.5A max thermal for outdoor application on 16 layer PCB with max external heat sink at 70 degrees C and max 75 degrees C in PCB itself away from dissipaters:
TPS544C25 EVM was modified to meet dynamic response requirements of the application by changing output capacitors to values as shown in the PMP11328 schematic. See next page for proposed inductor and actual inductor used in testing due to availability. Voltage control loop then adjusted to target 50 kHz bandwidth with the 190 nH inductor proposed or roughly 40 kHz with 240 nH inductor used in test. Tests performed here were the “risk areas” specific to this application. See the EVM User Guide for additional tests with original EVM.

Risk areas: Thermal performance at max ambient and dynamic load response with 8A step load at 10A per usec and 17mV max over / undershoot allowed:

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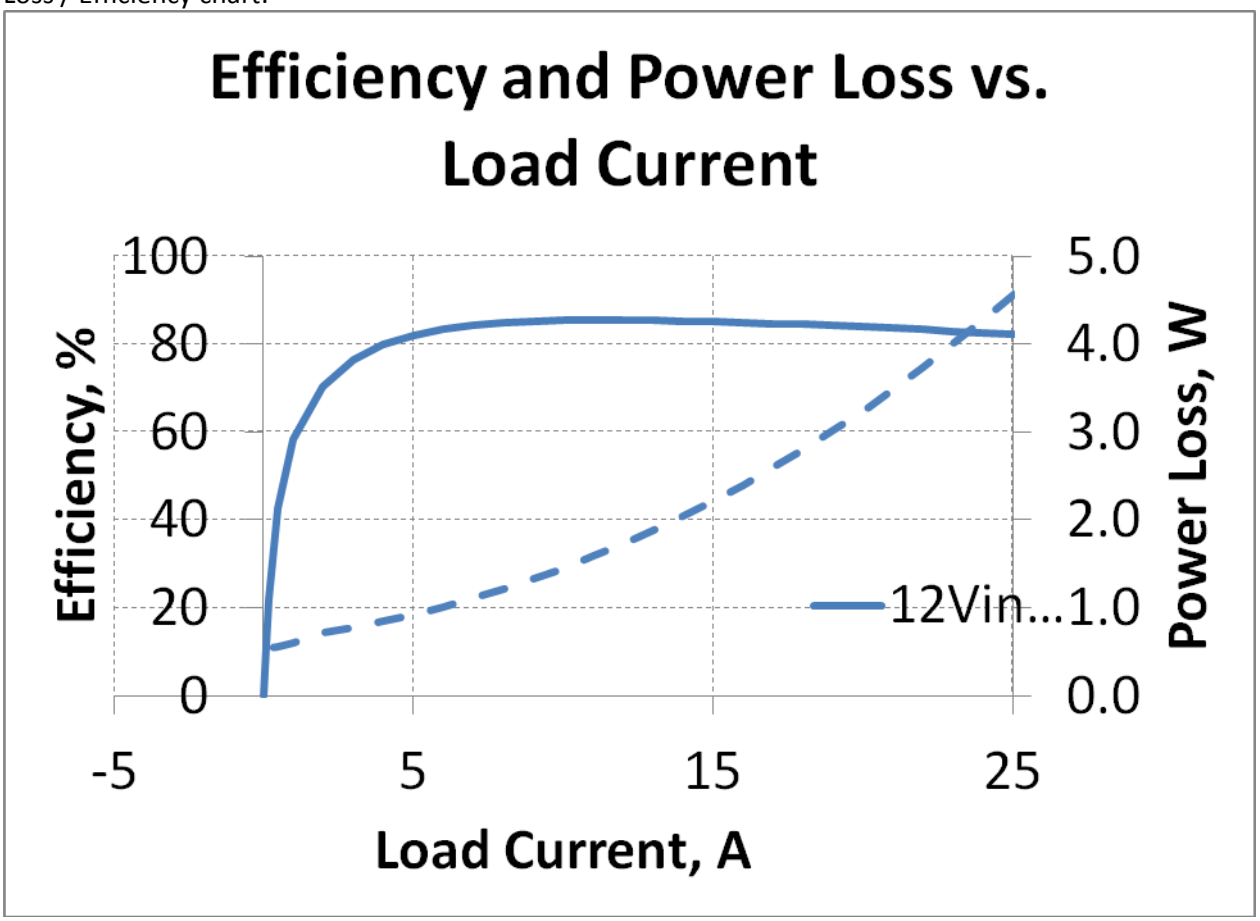
Regulation, Loss and efficiency data on EVM with IHLP4040DZ-11 240nH
Taken Friday August 14, 2015 by Ryan Manack

VIN	IVIN	ILOAD	VOUT	PIN	POUT	PLOSS	EFF
12.002	2.153	25.018	0.85025	25.840	21.271	4.569	82.318
12.002	2.058	24.018	0.85024	24.704	20.421	4.283	82.663
12.002	1.964	23.015	0.85023	23.575	19.568	4.007	83.004
12.002	1.871	22.014	0.85023	22.459	18.717	3.742	83.339
12.002	1.779	21.011	0.85023	21.352	17.864	3.488	83.663
12.002	1.688	20.011	0.85023	20.261	17.014	3.247	83.974
12.002	1.598	19.008	0.85021	19.177	16.161	3.016	84.271
12.002	1.509	18.008	0.85020	18.111	15.311	2.800	84.538
12.002	1.421	17.005	0.85020	17.050	14.458	2.592	84.796
12.002	1.333	16.003	0.85020	16.003	13.606	2.397	85.023
12.002	1.247	15.003	0.85020	14.968	12.755	2.213	85.216
12.002	1.162	14.000	0.85020	13.942	11.903	2.040	85.371
12.002	1.077	12.999	0.85019	12.930	11.052	1.878	85.475
12.002	0.994	11.997	0.85020	11.926	10.200	1.726	85.528
12.003	0.911	10.996	0.85019	10.933	9.349	1.584	85.512
12.003	0.829	9.993	0.85018	9.947	8.496	1.451	85.410
12.003	0.748	8.994	0.85017	8.975	7.646	1.328	85.200
12.003	0.667	7.989	0.85017	8.006	6.792	1.213	84.844
12.003	0.587	6.988	0.85017	7.048	5.941	1.108	84.287
12.003	0.508	5.988	0.85016	6.101	5.091	1.011	83.437
12.003	0.430	4.987	0.85018	5.164	4.240	0.924	82.102
12.003	0.353	3.986	0.85020	4.233	3.389	0.844	80.056
12.003	0.276	2.984	0.85020	3.311	2.537	0.775	76.603
12.003	0.200	1.984	0.85022	2.400	1.687	0.713	70.289
12.003	0.119	0.982	0.85018	1.429	0.835	0.594	58.431
12.003	0.080	0.481	0.85018	0.962	0.409	0.553	42.529
12.003	0.058	0.179	0.85017	0.692	0.152	0.540	21.997
12.003	0.050	0.080	0.85018	0.606	0.068	0.538	11.255
12.003	0.045	0.000	0.85017	0.538	0.000	0.538	N/A

Going forward IHLP4040DZ-01 190nH will be used, losses similar but DZ-01 more reliable in high temperature operation due to lower hot spot temperatures for similar losses:
Losses at 22.5A or 90% max electrical are 3.875W based upon average of 22A & 23A losses.

Loss / Efficiency chart:



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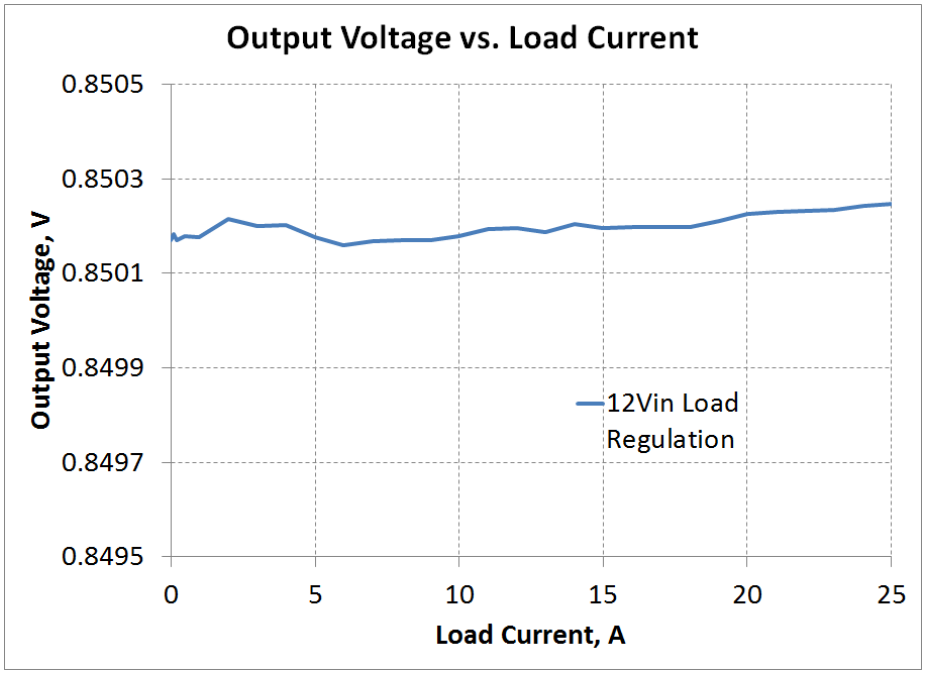
Load regulation: 80uV total variation with load


Output Voltage vs. Load Current
0.8505
0.8503
0.8501
0.8499
0.8497
0.8495
Output Voltage, V
0
5
10
15
20
25
Load Current, A
12Vin Load Regulation

PMP9008B 500kHz TPS544C20 Top side:
Thermal proxy for 0.85Vout TPS544C25 with higher Vout of 1.0V from TPS544C20 offsetting slightly lower Rdson of high side FET. Low side FETs have same Rdson and switching frequency same at 500kHz setting. (TPS544C20 is DCAP mode vs. TPS544C25 synchronizable voltage mode control)
No fan and stabilized > 20 minutes run
12.106Vin 2.191ain 1.0043Vout 22.50A or 3.93W loss
Compare with 3.87W at 22.5A on TPS544C25EVM
Top side TPS544C20 at 77 deg. C
PCB at far edge ~ 2 inches away at 47 deg. C or 30 deg. Cooler

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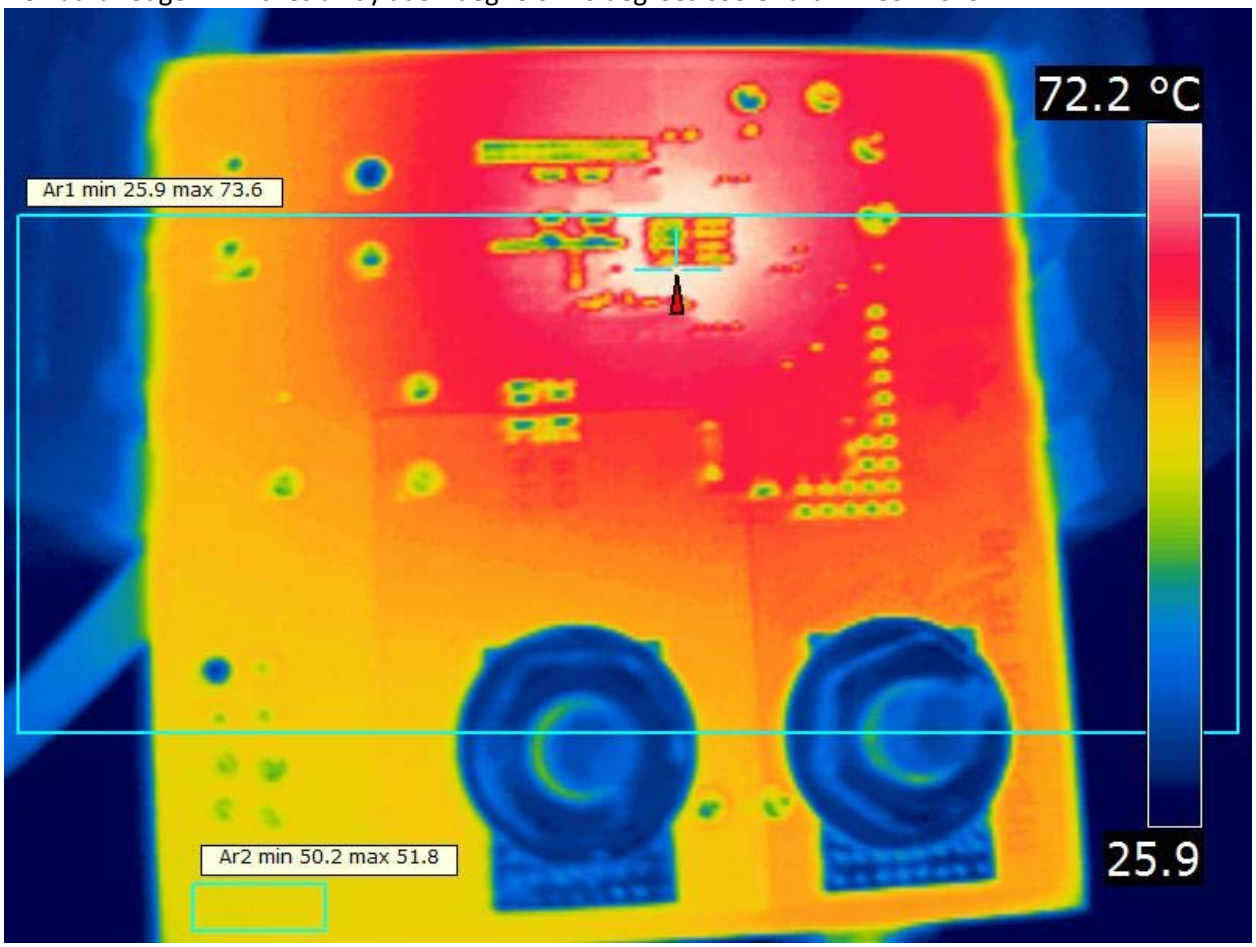
If PCB can be held to 75 degrees C or 28 degrees C hotter:
PCB Copper losses will increase from 500mWmW (estimated) to 555mW or by 55mW;
Main inductor losses will increase from 943mW to 1026mW or 83mW based upon Vishay loss calculator;
Conduction losses in TPS544C25 will increase from 1.300W to 1.362W per figures 5 & 6 on page 12 of TPS544C25 datasheet
Other losses of about 1.2W, mostly switching should not change much
Overall increase will be about 200mW or less than 5%.
Hence, the temperature rise of 30 degrees C seen above should not be more than 32 degrees C.
Hence, for a PCB at 75 degrees C about 2 inches from TPS544C25 I am estimating a max of 107 degrees C reading with actual junction temperature quite close.

PMP9008B 500kHz TPS544C20 Bottom side
12.106Vin 2.191ain 1.0043Vout 22.50A or 3.93W loss
Compare with 3.87W at 22.5A on TPS544C25EVM
Bottom side: hot spot at U1 at 74 deg. C
Top side TPS544C20 at 77 deg. C
PCB at far edge ~ 2 inches away at 51 deg. C or 26 degrees cooler than TPS544C20



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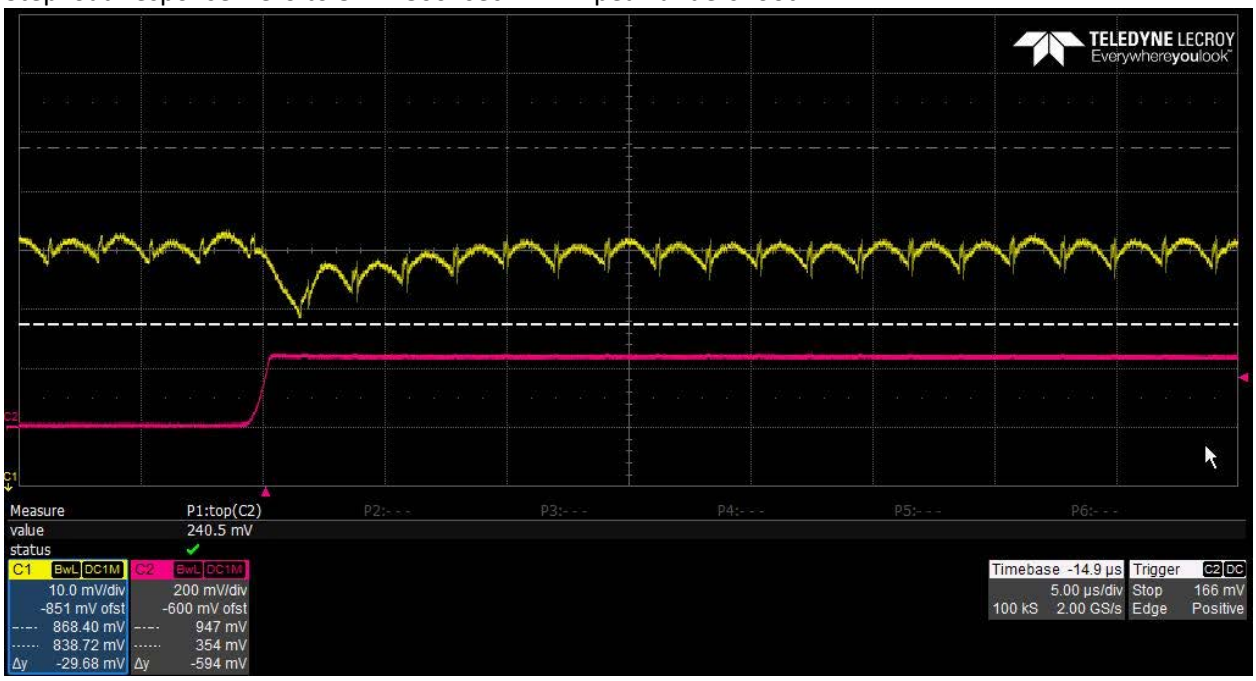
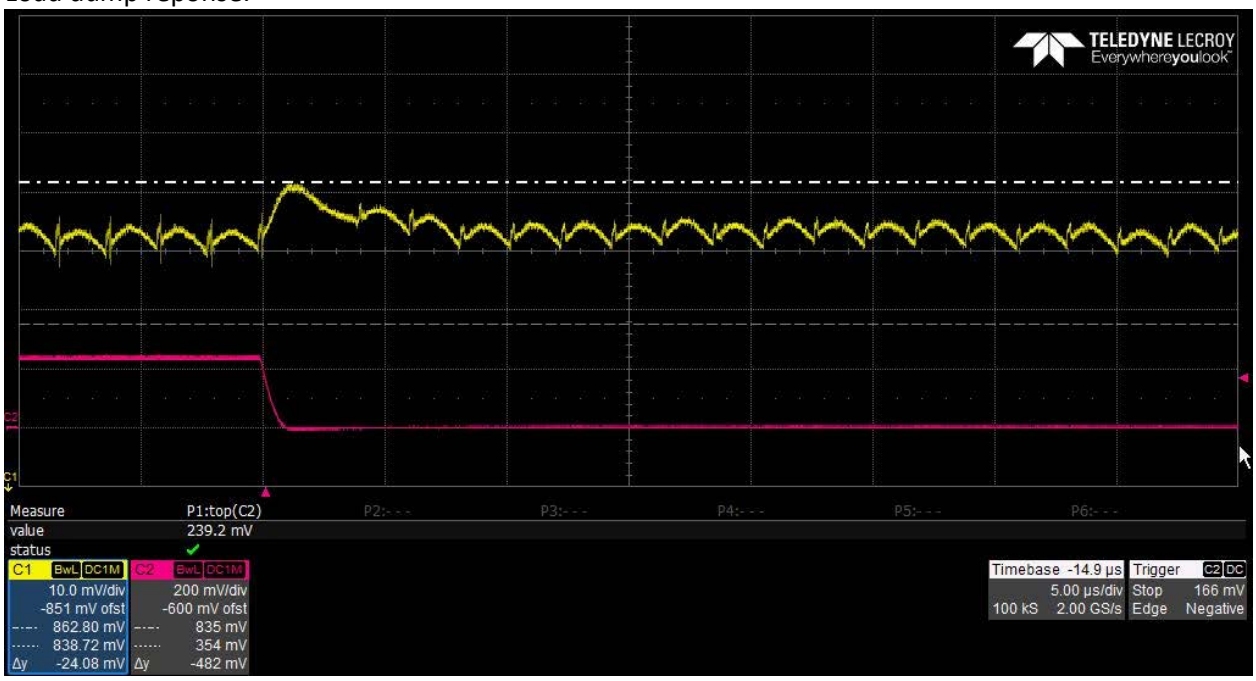
Dynamic response:
Step load response: zero to 8A in 800nsec: 12mV peak undershoot



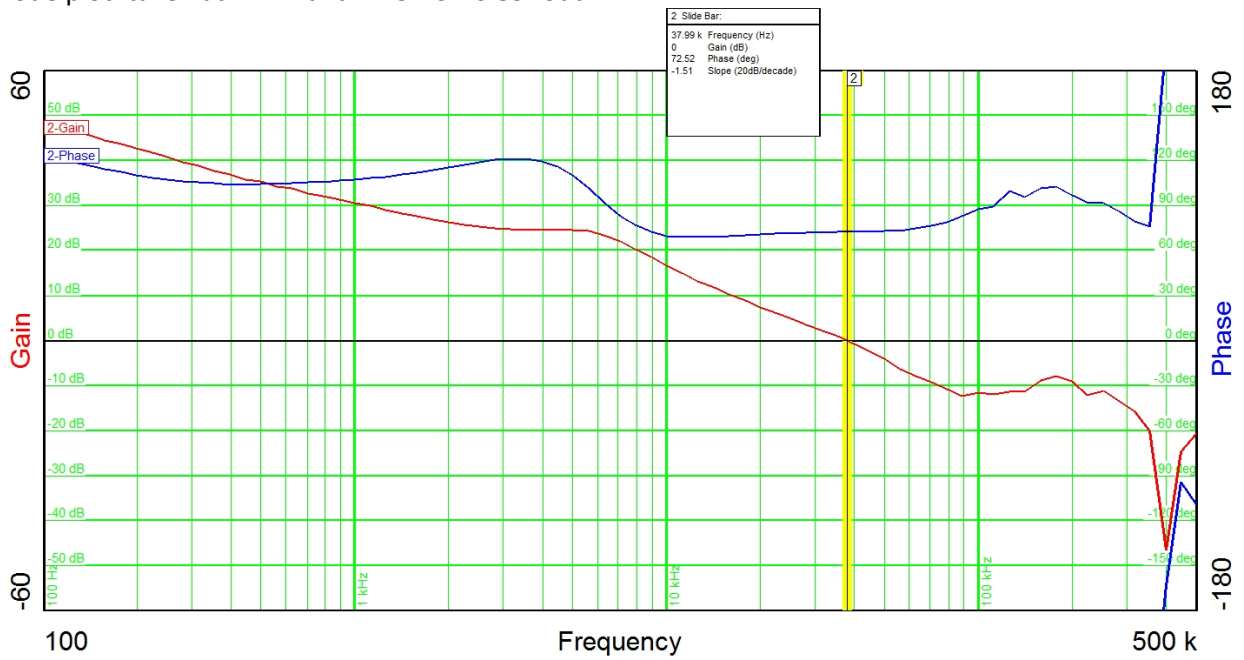
Channel 1 yellow is Vout at output caps and show peak undershoot of 12mV from DC value of Vout
Channel 2 is dynamic load current measured as voltage across 30mohms rising from zero mV to 240 mV in 0.8 usec or 0A to 8A at 10A per usec.

Load dump reponse:



Channel 1 yellow is Vout at output caps and show peak overershoot of 12mV from DC value of Vout

Channel 2 is dynamic load current measured as voltage across 30mohms falling from 240 mV to 0 mV in 0.8 usec or 8A to 0A at -10A per usec.
Total load step and dump band within +/-12mV vs. target of less than +/-17mV.
Bode plot: taken at 12Vin and 12.5A off 0.85Vout:



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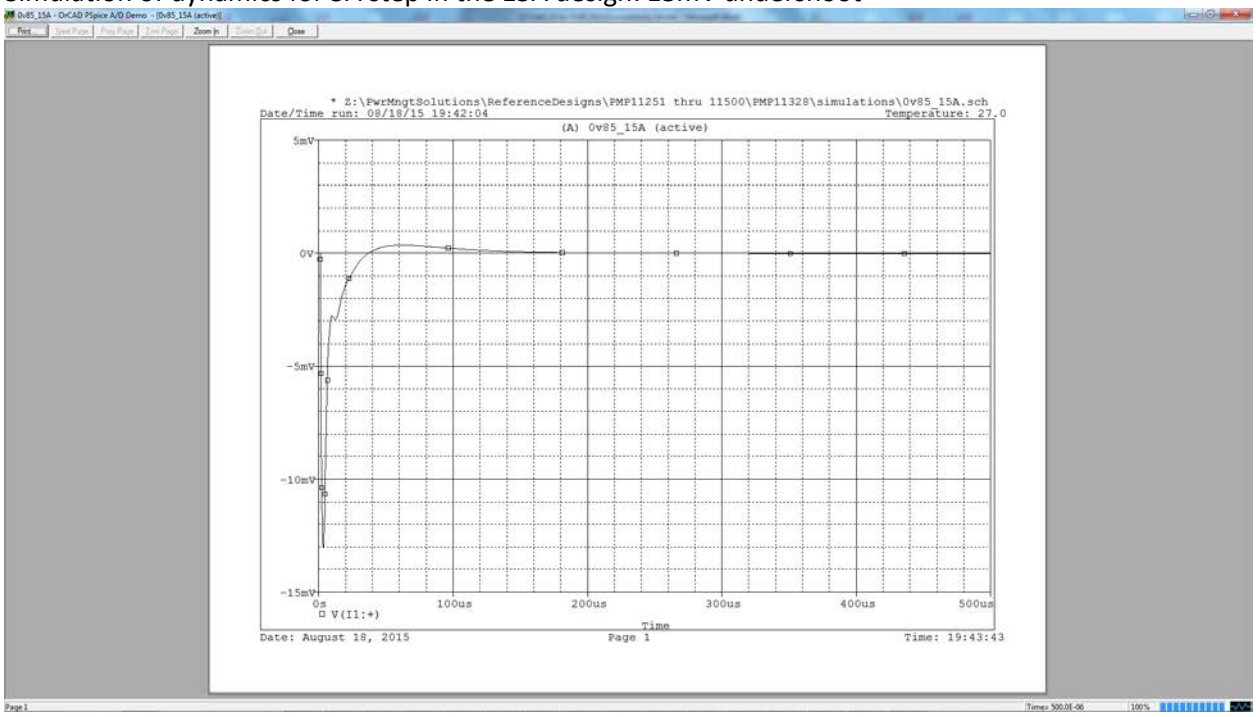
Notes: tested with 240 nH inductor vs. 190 nH inductor proposed in design:
Reducing inductor value will increase switching frequency ripple by 25% or by 1mV p-p from the 4-5mV now seen.
Bode plot will see increase of crossover from 38 kHz to 48 kHz with similar > 60 degrees phase margin.
Dynamic response should actually be improved to at least offset the added switching frequency ripple.

Simulation of dynamics for 5A step in the 15A design: 13mV undershoot



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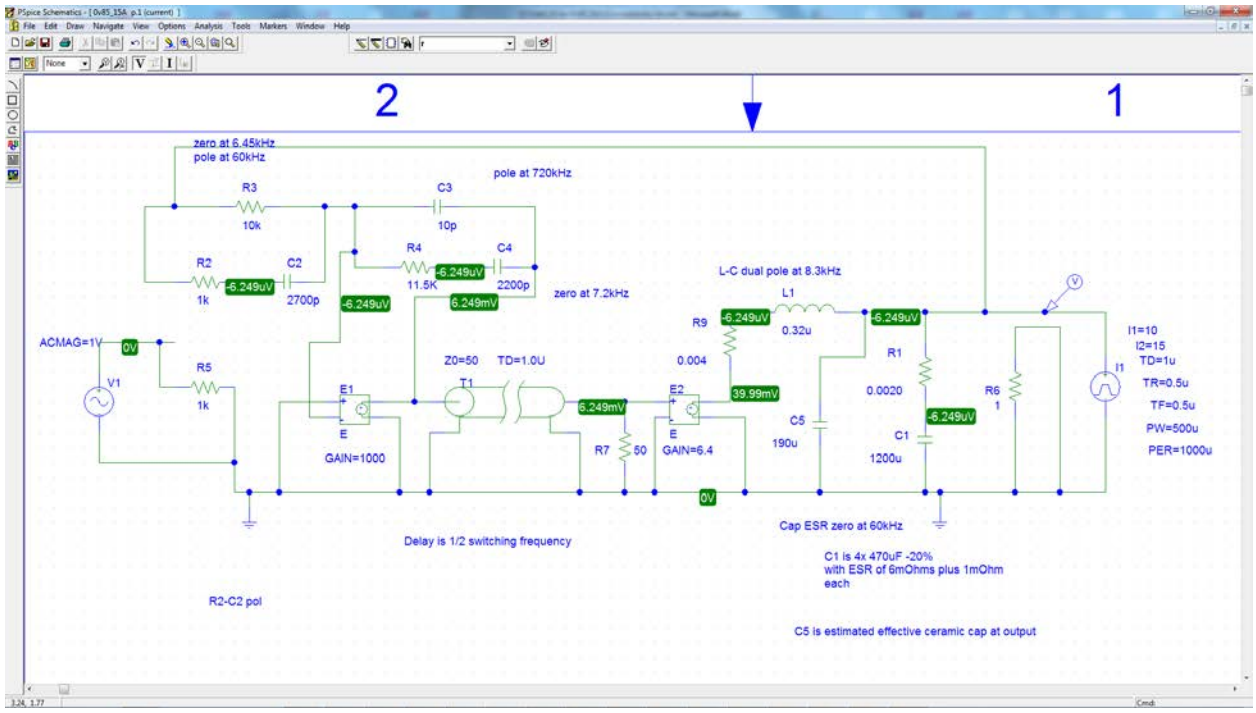
PSPICE schematic for same:



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