Topography: Boost
Device: LM5121
The measurements were done with additional airflow at 3Vin unless otherwise mentioned; The board is operational down to Vin 4.5V w/out bias power; For operation at Vin 3V..4.5V a bias supply is needed to power Vcc in a range 9V..14V; For this test purposes the design simply has been powered out of Vout, means:

- startup needs input voltage >4.5V
- maximum input voltage <14V; at higher Vin the controller will be damaged

Furthermore:
Full load operation at Vin 3V needs a source that is able to drive >25Adc
Limit continuous full load operation <60secs or use forced cooling 1m/s (200lfm)
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 4.5V, with 7A load at the output. Power supply was connected.

![Figure 1](image1.png)

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 4.5V, with 7A load at the output. Power supply output enabled.

![Figure 2](image2.png)
The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply was connected.

![Figure 3](image)

**Figure 3**

The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply output enabled.

![Figure 4](image)

**Figure 4**
2 Shutdown

The shutdown waveform is shown in the Figure 5. The input voltage was set at 3V, with 7A load on the output. Power supply was disconnected.

![Figure 5]

The shutdown waveform is shown in the Figure 6. The input voltage was set at 3V, with 7A load on the output. Power supply output disabled.

![Figure 6]
The shutdown waveform is shown in the Figure 7. The input voltage was set at 4.5V, with 7A load on the output. Power supply was disconnected.

Figure 7

The shutdown waveform is shown in the Figure 8. The input voltage was set at 4.5V, with 7A load on the output. Power supply output disabled.

Figure 8
The shutdown waveform is shown in the Figure 9. The input voltage was set at 6V, with 7A load on the output. Power supply was disconnected.

![Figure 9](image)

The shutdown waveform is shown in the Figure 10. The input voltage was set at 6V, with 7A load on the output. Power supply output disabled.

![Figure 10](image)
3 Efficiency
The efficiency is shown in the Figure 11 below.

Figure 11
4 Load Regulation

The load regulation of the output is shown in the Figure 12 below.

![Figure 12](image-url)
5 Line Regulation

Line regulation at 7A output current is shown in Figure 13

![Figure 13](image13.png)

With the same measurement the full load efficiencies across input voltage were calculated

![Figure 14](image14.png)
6 Ripple Voltage

6.1 Output

The output ripple voltage is shown in Figure 15. The image was taken with a 7A load and 3V, 4.5V and 6V at the input.

![Figure 15](image)

The output ripple voltage before filtering at L2 is shown in Figure 16. The image was taken with a 7A load 3V at the input.

![Figure 16](image)
The output ripple voltage before filtering at L2 is shown in Figure 17. The image was taken with a 7A load 4.5V at the input.

![Figure 17](image)

The output ripple voltage before filtering at L2 is shown in Figure 18. The image was taken with a 7A load 6V at the input.

![Figure 18](image)
### 6.2 Input

The input ripple voltage is shown in Figure 19. The image was taken with a 7A load 35V at the input.

![Figure 19](image-url)

<table>
<thead>
<tr>
<th>Channel</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch1</td>
<td>Output voltage @ 6Vin</td>
</tr>
<tr>
<td>Ch2</td>
<td>Output voltage @ 4.5Vin</td>
</tr>
<tr>
<td>Ch4</td>
<td>Output voltage @ 3Vin</td>
</tr>
</tbody>
</table>

- 50mV/div
- AC coupled
- 20MHz bandwidth setting
- 1µs/div

Ch1 => output voltage @ 6Vin
Ch2 => output voltage @ 4.5Vin
Ch4 => output voltage @ 3Vin
7 Control Loop Frequency Response

Figure 20 shows the loop response with 7A load and 3V input.

![Figure 20](image)

Figure 21 shows the loop response with 7A load and 4.5V input.

![Figure 21](image)
Figure 22 shows the loop response with 7A load and 6V input.

Table 1 summarizes the results:

<table>
<thead>
<tr>
<th></th>
<th>3V</th>
<th>4.5V</th>
<th>6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (kHz)</td>
<td>1.29</td>
<td>2.79</td>
<td>4.2</td>
</tr>
<tr>
<td>Phasemargin</td>
<td>71°</td>
<td>90°</td>
<td>99°</td>
</tr>
<tr>
<td>slope (20dB/decade)</td>
<td>-0.96</td>
<td>-0.87</td>
<td>-0.808</td>
</tr>
<tr>
<td>gain margin (dB)</td>
<td>-1.76</td>
<td>-5.29</td>
<td>-7.2</td>
</tr>
<tr>
<td>slope (20dB/decade)</td>
<td>+0.617</td>
<td>+0.486</td>
<td>+0.2</td>
</tr>
<tr>
<td>freq (kHz)</td>
<td>45.5</td>
<td>49.6</td>
<td>55</td>
</tr>
</tbody>
</table>

Table 1

Loop bandwidth drops by input voltage – see transient response:
8 Load Transients

The Figure 23 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to **3.2V** – the deviation is 3%

![Figure 23](image)

The Figure 24 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 4.5V – the deviation is below 3%

![Figure 24](image)
The Figure 25 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 6V.
9 Miscellaneous Waveforms

9.1 3V Input

9.1.1 Switch node (Low Side FET)

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 26.

![Figure 26](image-url)
9.1.2 Gate of Low side MOS-FET

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 27.
9.1.3 Hi Side MOS FET

The waveform is shown in Figure 28 (the same setup as above)
9.1.4 Hi Side MOS FET Gate

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 29.

Figure 29
9.2 4.5V Input

9.2.1 Switch node (Low Side FET)

With input voltage set to 4.5V and 7A iout results in the waveform shown in Figure 30

![Figure 30](image-url)
9.2.2 Gate of Low side MOS-FET

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 31.
9.2.3 Hi Side MOS FET

The waveform is shown in Figure 32 (the same setup as above).
9.2.4 Hi Side MOS FET Gate

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 33.
9.3  6V Input

9.3.1 Switch node (Low Side FET)

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 34.
9.3.2 Gate of Low side MOS-FET

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 35.

Ch1 =>
2V/div
500ns/div

Figure 35
9.3.3 Hi Side MOS FET

The waveform is shown in Figure 36 (the same setup as above)

Figure 36
9.3.4 Hi Side MOS FET Gate

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 37.
10 Thermal Image

Figure 38 shows the thermal image at 6V input and 7A output (no additional airflow)

![Figure 38](image)

<table>
<thead>
<tr>
<th>Name</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2</td>
<td>49.1°C</td>
</tr>
<tr>
<td>Q2</td>
<td>48.0°C</td>
</tr>
<tr>
<td>Q3</td>
<td>49.1°C</td>
</tr>
<tr>
<td>D4</td>
<td>48.6°C</td>
</tr>
</tbody>
</table>

Table 2

Figure 39 shows the thermal image at 4.5V input and 7A output (no additional airflow)

![Figure 39](image)

<table>
<thead>
<tr>
<th>Name</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2</td>
<td>60.1°C</td>
</tr>
<tr>
<td>Q2</td>
<td>61.3°C</td>
</tr>
<tr>
<td>Q3</td>
<td>59.5°C</td>
</tr>
<tr>
<td>D4</td>
<td>57.6°C</td>
</tr>
</tbody>
</table>

Table 3
Figure 40 shows the thermal image at 3V input and 7A output (no additional airflow)

<table>
<thead>
<tr>
<th>Name</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q2</td>
<td>120.1°C</td>
</tr>
<tr>
<td>R2</td>
<td>115.6°C</td>
</tr>
<tr>
<td>Q3</td>
<td>101.6°C</td>
</tr>
<tr>
<td>D4</td>
<td>98.1°C</td>
</tr>
</tbody>
</table>

Table 4

Figure 40 shows the thermal image at 3V input and 7A output (with additional airflow)

<table>
<thead>
<tr>
<th>Name</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2</td>
<td>67.8°C</td>
</tr>
<tr>
<td>Q2</td>
<td>64.8°C</td>
</tr>
<tr>
<td>Q3</td>
<td>54.3°C</td>
</tr>
</tbody>
</table>

Table 5
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