

# TI Designs

## bq76PL536A-Q1 Reference Design



### TI Designs

The bq76PL536A-Q1 is a stackable, three-to-six series cell lithium-ion battery pack protector and analog front end (AFE) that incorporates a precision analog-to-digital converter (ADC), independent cell voltage and temperature protection, cell balancing, and a precision 5-V low drop-out regulator (LDO) to power user circuitry. The bq76PL536A-Q1 integrates a voltage translation and precision ADC system to measure battery cell voltage with high accuracy and speed. The bq76PL536A-Q1 provides full protection (secondary protection) for overvoltage, undervoltage, and overtemperature conditions. When safety thresholds have been exceeded, the bq76PL536A-Q1 device sets the FAULT output. No external components are required to configure or enable the protection features. Cell voltage and temperature protection functions are independent of the ADC system. Programmable protection thresholds and detection delay times are stored in the error check/correct (ECC) OTP EPROM, which increases the flexibility and reliability of the battery management system.

### Design Resources

[TIDA-00821](#)

Tool Folder Containing Design Files

[bq76PL536A-Q1](#)

Product Folder

[TMS570](#)

Product Folder



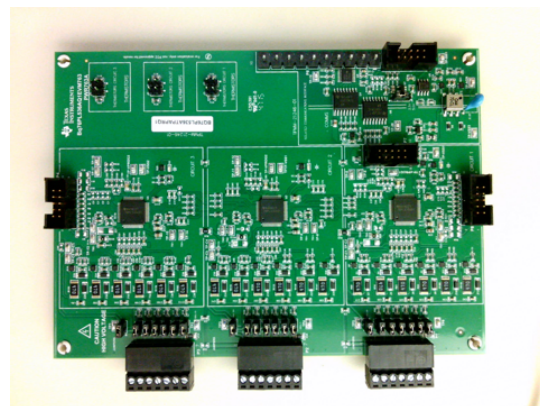
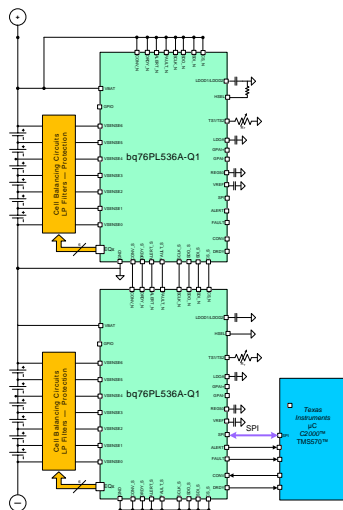
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### Design Features

- Module Transient Suppression Diode
- In-Rush Protection
- Zener Diode
- Front-End Inrush Protection and Nyquist Filter
- EMC Susceptibility Filter
- Balancing Field Effect Transistor (FET) and Resistors
- Minimizing Power Consumption When Host Loses Power
- Temperature Sensing
- Host Interface
- Internal Voltage Regulators

### Featured Applications

- Electric and Hybrid Electric Vehicles
- Uninterruptible Power Systems (UPS)
- E-Bike and E-Scooter
- Large-Format Battery Systems





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## 1 Key System Specifications

**Table 1. Key System Specifications**

PARAMETERS	SPECIFICATIONS
Shutdown current	12 $\mu$ A (typical)
Number series cells	Three to six cells
OV and UV detection delay time	0 ms to 3200 ms
OT detection delay time	0 ms to 2550 ms
Operating temperature range	-40°C to 105°C
ADC accuracy	$\pm$ 5 mV at -40°C to 105°C
ADC conversion	6 $\mu$ s
Supply voltage range $V_{MAX}$	-0.3 V to 36 V (absolute maximum)
Thermal shutdown	142°C (typical)

## 2 System Description

The bq76PL536A-Q1 is a three-to-six series lithium-ion (Li-Ion) battery monitor, secondary protector, and analog front end (AFE) that can be stacked vertically to monitor up to 192 cells without the need for additional isolation components between integrated circuits (ICs).

This device incorporates a precision analog-to-digital converter (ADC); independent cell voltage and temperature protection; cell balancing, and a precision 5-V regulator to power user circuitry. The bq76PL536A-Q1 additionally provides full (secondary) protection for overvoltage, undervoltage, and overtemperature conditions.

### 2.1 bq76PL536A-Q1

The bq76PL536A-Q1 device is a stackable battery monitor and protector for three-to-six Li-Ion cells in series. The bq76PL536A-Q1 integrates an AFE along with a precision ADC, which is used to precisely measure battery cell voltages. A separate ADC is used to measure temperature.

In addition to temperature measurement, the device monitors overvoltage and undervoltage per channel for protection. Non-volatile memory stores the user-programmable protection thresholds and delay times. A fault output signals whenever one of these thresholds has been exceeded.

A stack of bq76PL536A-Q1 devices is capable of supporting cell stacks of 192 cells. A high-speed serial peripheral interface (SPI) connects all the devices.

### 2.2 TMS570

The TMS570LS31x5/21x5 device is a high-performance automotive-grade microcontroller family for safety systems. The safety architecture includes dual CPUs in lockstep, CPU and memory built-in self-test (BIST) logic, error-correction coding (ECC) on both the flash and the data SRAM, parity on peripheral memories, and loopback capability on peripheral I/Os.

The TMS570LS31x5/21x5 device family integrates the ARM® Cortex™-R4F floating-point CPU. The CPU offers an efficient 1.66 DMIPS/MHz and has configurations that can run up to 180 MHz, providing up to 298 DMIPS. The device supports the word-invariant big-endian (BE-32) format.

The TMS570LS3135 device has 3MB of integrated flash and 256KB of data RAM. The TMS570LS2135 device has 2MB of integrated flash and 256KB of data RAM. The TMS570LS2125 device has 2MB of integrated flash and 192KB of data RAM. Both the flash and RAM have single-bit error correction and double-bit error detection. The flash memory on this device is a nonvolatile, electrically erasable, and programmable memory implemented with a 64-bit-wide data bus interface.

The flash operates on a 3.3-V supply input (same level as the I/O supply) for all read, program, and erase operations. When in pipeline mode, the flash operates with a system clock frequency of up to 180 MHz. The SRAM supports single-cycle read and write accesses in byte, halfword, word, and doubleword modes.

The TMS570LS31x5/21x5 device features peripherals for real-time control-based applications, including two next generation high-end timer (N2HET) timing coprocessors and two 12-bit ADCs supporting up to 24 inputs.

### 3 Block Diagram

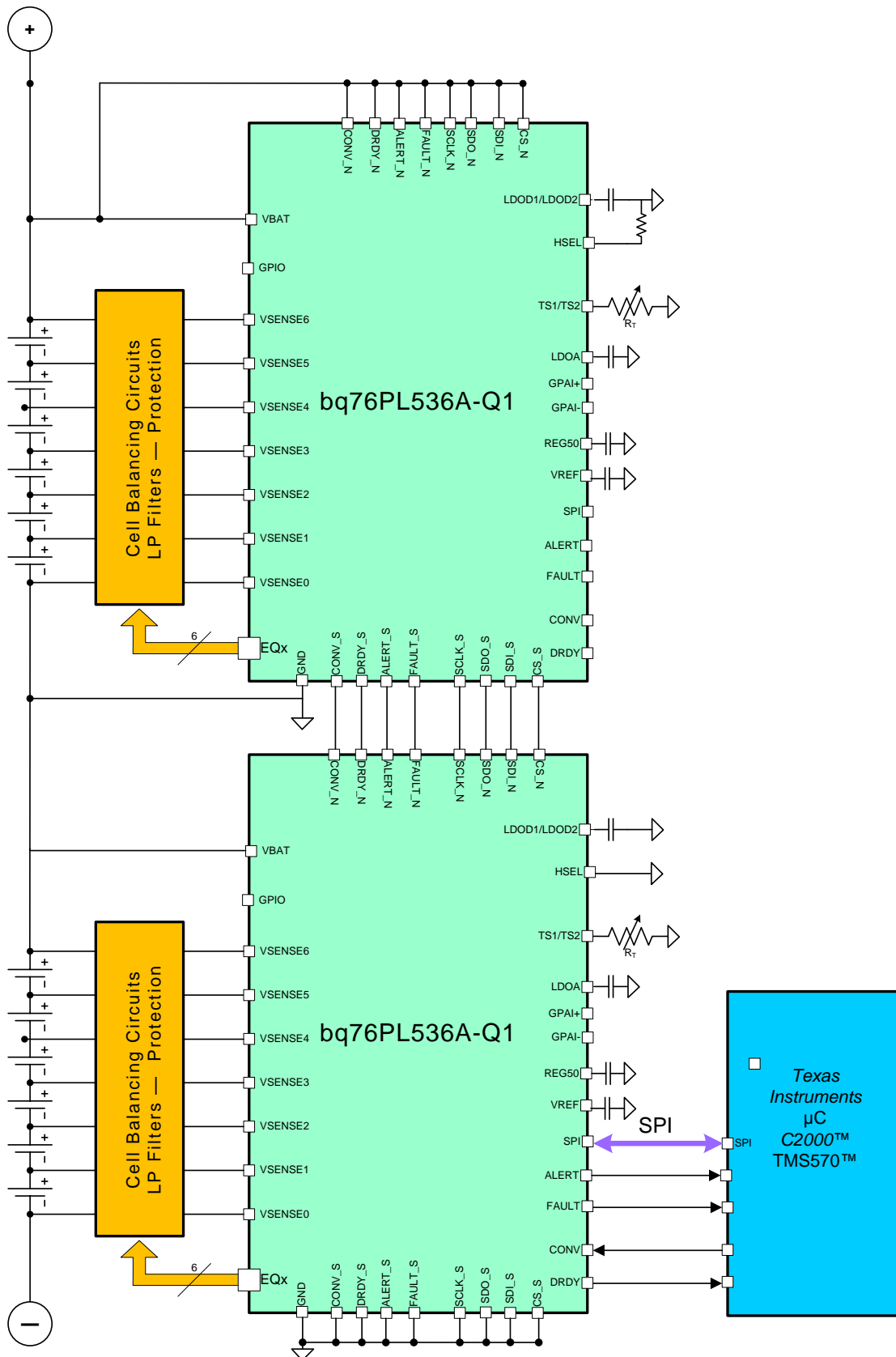


Figure 1. TIDA-00821 Block Diagram

### 3.1 Highlighted Products

#### 3.1.1 bq76PL536A-Q1

The following Figure 2 shows the functional block diagram for the bq76PL536A-Q1.

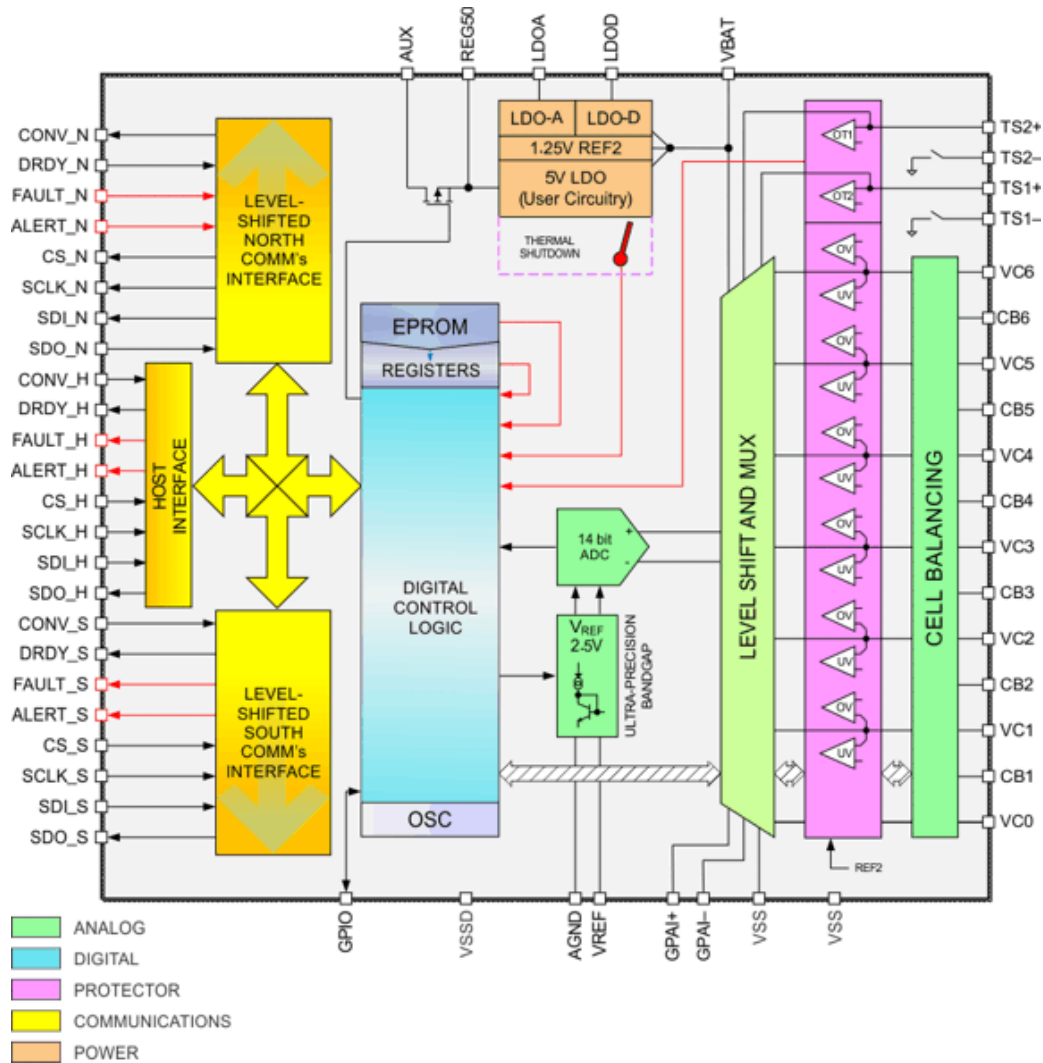


Figure 2. bq76PL536A-Q1 Functional Block Diagram

#### Features

- Three-to-six series cell support, all chemistries
- Hot-pluggable
- High-speed serial peripheral interface (SPI) for data communications
- Stackable vertical interface
- Isolation components not required between devices
- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 2: –40°C to 105°C ambient operating temperature range
  - Device HBM classification level 2
  - Device CDM classification level C4B

- High-accuracy ADC:
  - $\pm 1$ -mV typical accuracy
  - 14-bit resolution, 6- $\mu$ s conversion time
  - Nine ADC inputs
  - Dedicated pins for synchronizing measurements
- Configuration data stored in error check/correct (ECC) one-time-programmable (OTP) registers
- Built-in comparators (secondary protector) for:
  - Overvoltage and undervoltage protection
  - Overtemperature protection
  - Programmable thresholds and delay times
  - Dedicated fault signals
- Cell balancing control outputs with safety timeout
  - Balance current set by external components
- Supply voltage range from 7.2 V to 27 V continuous and 36-V peak
- Low power:
  - Typical 12- $\mu$ A sleep, 45- $\mu$ A idle
- Integrated precision 5-V, 3-mA LDO

For more information on this device, see the respective product folder at [www.ti.com](http://www.ti.com).

## 4 System Design Theory

### 4.1 Analog-to-Digital Conversion (ADC)

The integrated 14-bit (unsigned) high-speed successive approximation register (SAR) ADC uses an integrated band-gap reference voltage ( $V_{REF}$ ) for the cell and brick measurements. The ADC has a front end multiplexer for nine inputs: six cells, two temperature sensors, and one general-purpose analog input (GPAI). The GPAI can be further multiplexed to measure the brick voltage between the BATx pin and GND or the voltage between the GPAI+ and GPAI– pins.

The ADC and reference have been factory trimmed to compensate for gain, offset, and temperature-induced errors for all inputs. The measurement result is not allowed to roll over because of offset error at the top and bottom of the range. For example, a reading near zero does not underflow to 0x03ff because of offset error and vice-versa.

The converter returns 14 valid unsigned magnitude bits in the following format:

```
<00xxxxxx xxxxxxxx>
```

Each word returns in the big-endian format in a register pair consisting of two adjacent 8-bit registers. The most significant bit (MSB) of the word is located in the lower-address register of the pair, that is, data for cell 1 is returned in registers 0x03 and 0x04 as 00xxxxxx xxxxxxxxb.

### 4.2 Cell Balancing

The bq76PL536A-Q1 has six dedicated outputs (CB1 to CB6) that can be used to control external N-FETs as part of a cell balancing system. The implementation of appropriate algorithms is controlled by the system host. The CB\_CTRL[CBAL1–6] bits control the state of each of the outputs. The outputs are copied from the bit state of the CB\_CTRL register, that is, a 1 in this register activates the external balance field-effect transistor (FET) by placing a high on the associated pin.

The CBx pins switch between approximately the positive and negative voltages of the cell across which the external FET is connected. This switching allows the use of a small, low-cost N-FET in series with a power resistor to provide cell balancing.

### 4.3 Internal Voltage Regulators

The bq76PL536A-Q1 device derives power from the BAT pin using several internal low dropout (LDO) voltage regulators. The device contains separate LDOs for internal analog circuits (5 V at LDOA), digital circuits (5 V at LDOD1 and LDOD2), and external user circuits (5 V at REG50). Place filter capacitors as close to the IC as possible. The internal LDOs and internal  $V_{REF}$  must not be used to power external circuitry, with the exception that the LDODx must be used to source power to any external pullup resistors.

### 4.4 Undervoltage Lockout and Power-On Reset

The device incorporates two comparators to detect low  $V_{BAT}$  conditions. The first detects low voltage where some device digital operations are still available. The second (POR) detects a voltage below which the device operation is not ensured.

### 4.5 Thermal Shutdown (TSD)

The bq76PL536A-Q1 contains an integrated thermal shutdown circuit with the sensor located near the REG50 LDO and has a threshold of thermal shutdown (TSD). When triggered, the REG50 regulator reduces its output voltage to zero and the ADC is turned off to conserve power. The thermal shutdown circuit has a built-in hysteresis that delays recovery until the die has cooled slightly. When the thermal shutdown is active, the DEVICE\_STATUS[TSD] bit is set. The IO\_CONTROL[SLEEP] and ALERT[SLEEP] bits also become set to reduce power consumption.

**CAUTION**

The secondary protector settings are disabled in the TSD state.

Temperature measurement and monitoring do not function because of a loss of power if the thermistors are powered from the REG50 or AUX pins and TSD occurs. Protection dependent schemes implemented by the designer and depend on the REG50 voltage also may not function as a result of the loss of the REG50 output.

## 4.6 System Critical Circuits

This section describes circuits that are global in nature and required for reliable system performance, such as survival of hot-plug events including protection for inrush currents and electrostatic discharge (ESD) protection.

### 4.6.1 Module Transient Suppression Diode (TVS)

Figure 3 shows that the transient suppression diode (TVS) is visible as the  $Z_{TVS}$ . The primary purpose of the TVS diode is to enable the clamping of transient voltages to below the bq76PL536A-Q1 absolute maximum (36 V). These transients usually occur during hot-plug events. A 36-V Zener diode is not as effective as a 5.1- or 5.6-V Zener diode across each cell connection, as Figure 3 shows. TI recommends using a 5.1- or 5.6-V Zener diode.

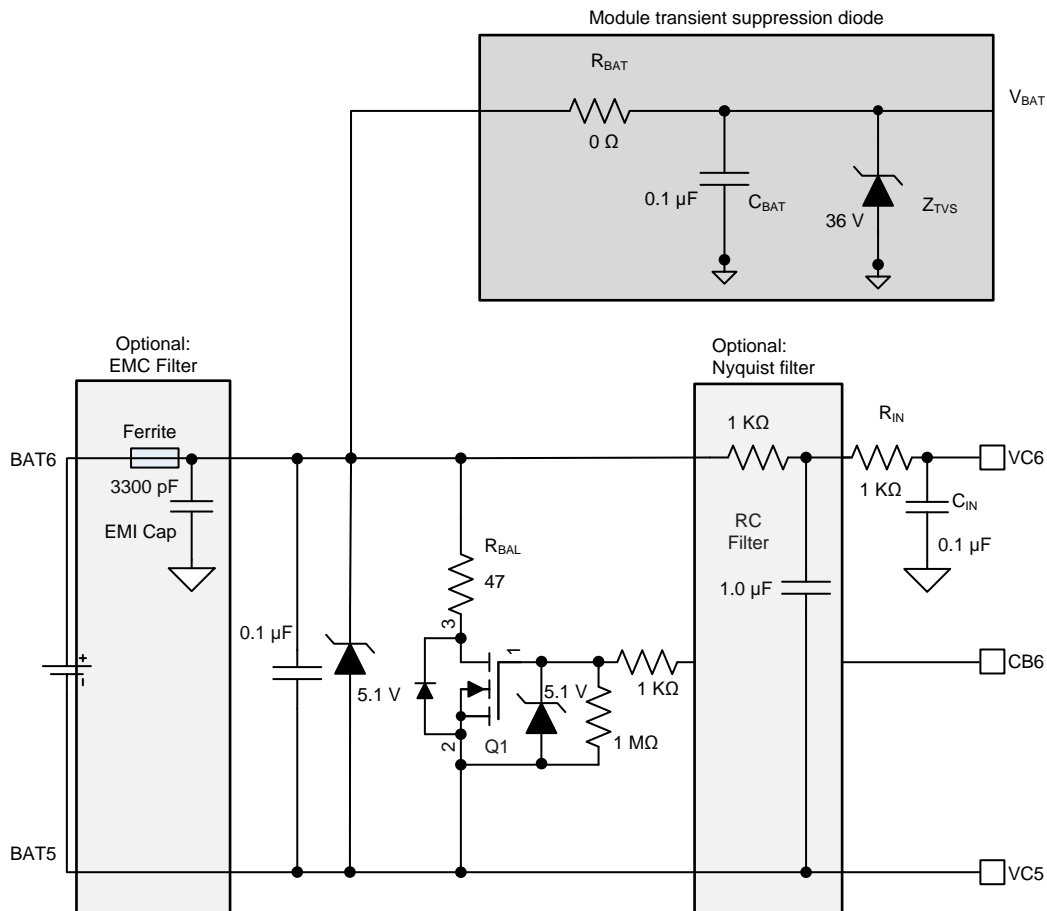


Figure 3. Module Transient Suppression Diode



### 4.6.2 Inrush Protection

The preceding Figure 3 shows the inrush current protection for the bq76PL536A-Q1 device, where  $R_{BAT}$  is in the highest cell connection to the bq76PL536A-Q1 BAT pins. The  $R_{BAT}$  in Figure 3 must be between 0  $\Omega$  to 3  $\Omega$ .

TI recommends to select  $C_{BAT}$  as a 0.1- $\mu$ F capacitor.

**NOTE:** The  $V_{MODULE}$  measurement has a small offset because of the current consumption of the device through the 0- to 3- $\Omega$  series resistor. The host must subtract this offset from the  $V_{MODULE}$  value.

### 4.6.3 Zener Diodes

Zener diodes must be placed close to the cell connection on the system PCB, with one Zener diode across each input channel. The Zener diodes are necessary to the system and serve two functions:

- Provide overvoltage protection to the ADC inputs
- Provide a path for inrush currents during hot plug-in

The schematic in Figure 4 shows the Zener diode.

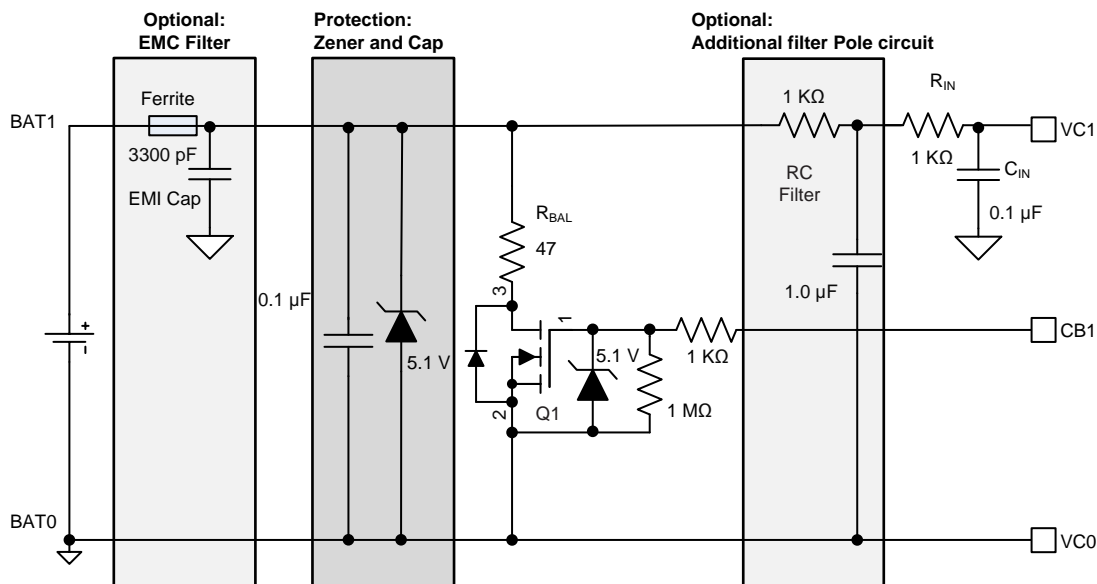


Figure 4. Protection Zener and Capacitor

The designer must ensure that the selected Zener diodes meet the following conditions:

1. The bq76PL536A-Q1 inputs are protected from input voltage transients and kept below 6 V.
2. The Zener maximum reverse current ( $I_Z$ ) at normal battery-cell voltage levels must be as low as possible to keep the quiescent-system current draw low.
3. The Zener must be capable of withstanding instantaneous or continuous currents that the bq76PL536A-Q1 may experience in a fault event. These events can include cable connect, cable disconnect, inrush, or reverse battery voltage.
4. The capacitor acts as a divider during the transient and cell connection sequence. The capacitor also helps to compensate for the inductance of the wire and reduce noise.

#### 4.6.4 Front End Inrush Protection and Nyquist Filter

The series resistors on the bq76PL536A-Q1 sense inputs ( $R_{IN}$  in Figure 5) are necessary to the system and serve two functions:

1.  $R_{IN}$  protects the ADC inputs from inrush currents during a hot plug-in. This requirement limits the input series resistance to a minimum of 100  $\Omega$ . This resistance must be kept as low as possible to minimize the input voltage offset, which is also subject to drift over temperature. For this reason,  $R_{IN}$  must be kept below 1 k $\Omega$ .
2. Together with the capacitors on each input,  $R_{IN}$  provides an RC filter for high-frequency noise on the ADC inputs.

The tuning of this filter cutoff depends on the preference of the customer and the noise, which may be present in the end application. TI recommends using a 0.1- $\mu\text{C}$  capacitor to support the ADC switch-capacitor input and connecting this to GND (BAT0). The cutoff frequency can be calculated with the following Equation 1:

$$f_c = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} \times \text{Hz} \tag{1}$$

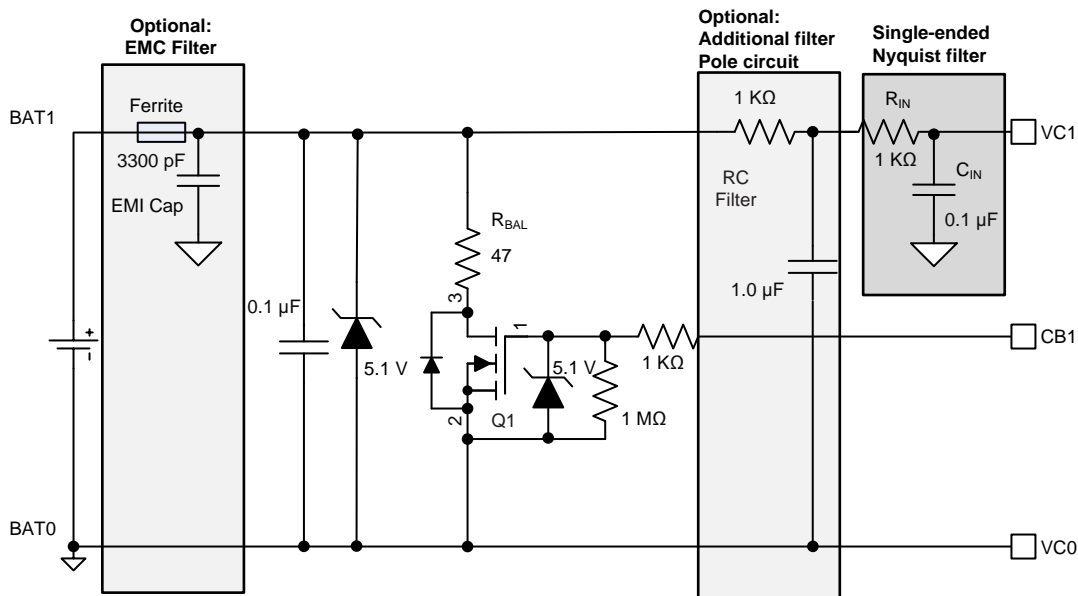


Figure 5. Cell Input Single-Ended Nyquist Filter—Minimum Circuit

- For applications that require a very low filter cutoff frequency, a differential capacitor can be used to provide the bulk of the ADC input filtering.
- Keep the low-pass RC filter components close to the IC wherever possible, especially the 0.1- $\mu\text{C}$  single-ended capacitor, which must be the closest component to the  $V_{CX}$  input.
- Connect the unused  $V_{CX}$  inputs to the next lower  $V_{CX}$  input with a 1-k $\Omega$  resistor.
- The addition of a simple two-pole filter decreases the noise bandwidth and measurement error introduced by the typical inverter noise (see Figure 6).

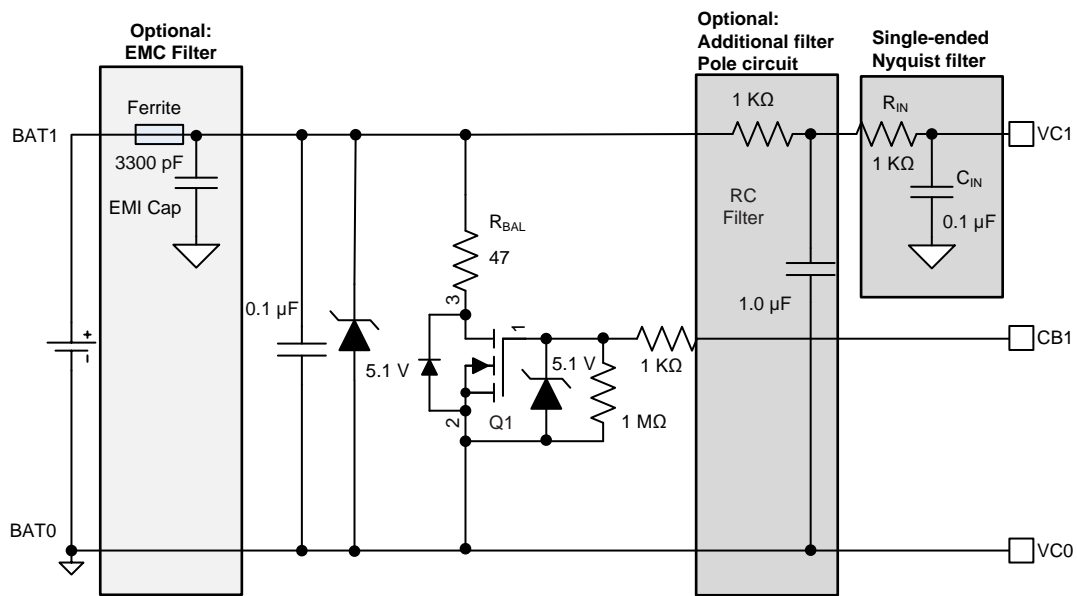


Figure 6. Cell Input Differential Nyquist Filter—Additional Filter Pole Circuit

#### 4.6.5 EMC Susceptibility on Cell Inputs

Extra components are necessary to improve the electromagnetic compatibility (EMC) performance for automotive applications in electrically noisy environments (see Figure 7).

- Use ferrite beads or small inductors in series with the cell inputs. The bead and small capacitor must be located near each other.
- Add a 3300-pF capacitor from each cell input to the GND (BAT0) of that IC. This value may require adjustment for the PCB layout and field conditions specific to the preferences of the designer.

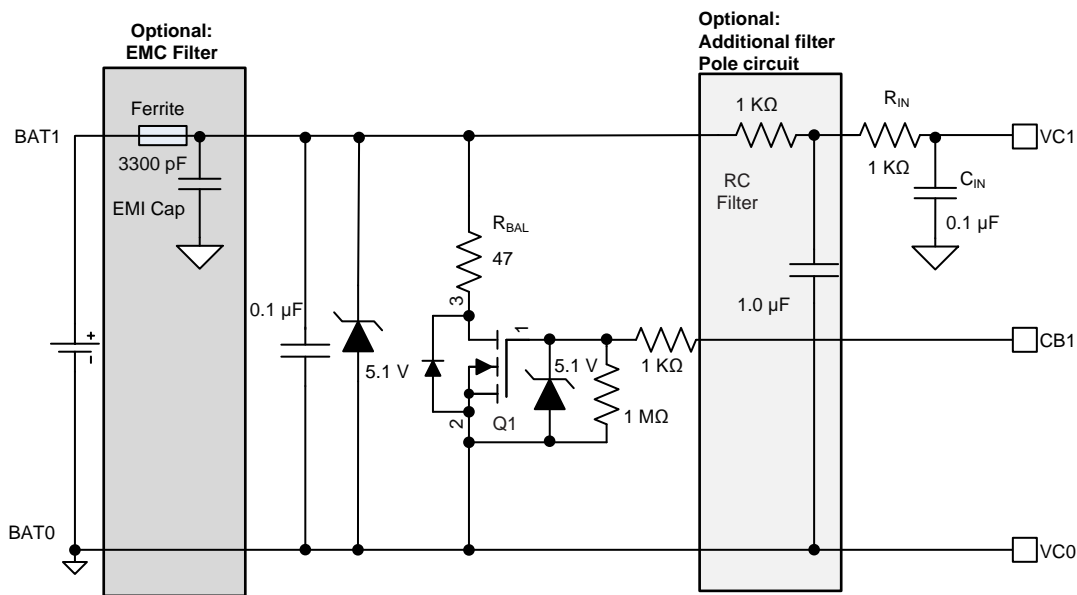


Figure 7. EMC Filter on Cell Inputs

#### 4.6.6 Voltage Reference

The bq76PL536A-Q1 derives power from the BAT pin using several internal LDO voltage regulators. Separate LDOs exist for the internal analog circuits (5 V at LDOA), digital circuits (5 V at LDOD1 and LDOD2), and external user circuits (5 V at REG50). The BAT pin must be connected to the most-positive cell input from cell 3, 4, 5, or 6 depending on the number of cells connected. Place the filter capacitors as close to the IC as possible. The internal LDOs and internal  $V_{REF}$  must not be used to power external circuitry, with the exception that LDODx must be used to source power to any external pullup resistors

Figure 8 shows the following internal voltage references:

1. LDOA internal, analog 5-V LDO bypass connection: This pin requires a 2.2- and 0.1-  $\mu\text{F}$  ceramic capacitor for stability.
2. LDOD1 and LDOD2 comprise the internal, digital 5-V LDO bypass connection 1 and 2 and require a 2.2- and 0.1- $\mu\text{F}$  ceramic capacitor for stability. They are internally tied together by default; however, they must be externally tied together.
3. REG50 5-V user LDO output: This output requires a 2.2- $\mu\text{F}$  ceramic capacitor for stability. REG50 is disabled when the device is in sleep mode. REG50 cannot be used as a pullup source to terminate the device pins.
4.  $V_{REF}$  internal analog voltage reference (positive): This reference requires a 10- $\mu\text{F}$ , low equivalent series resistance (ESR) ceramic capacitor to connect to AGND for stability. Select a large VDS.

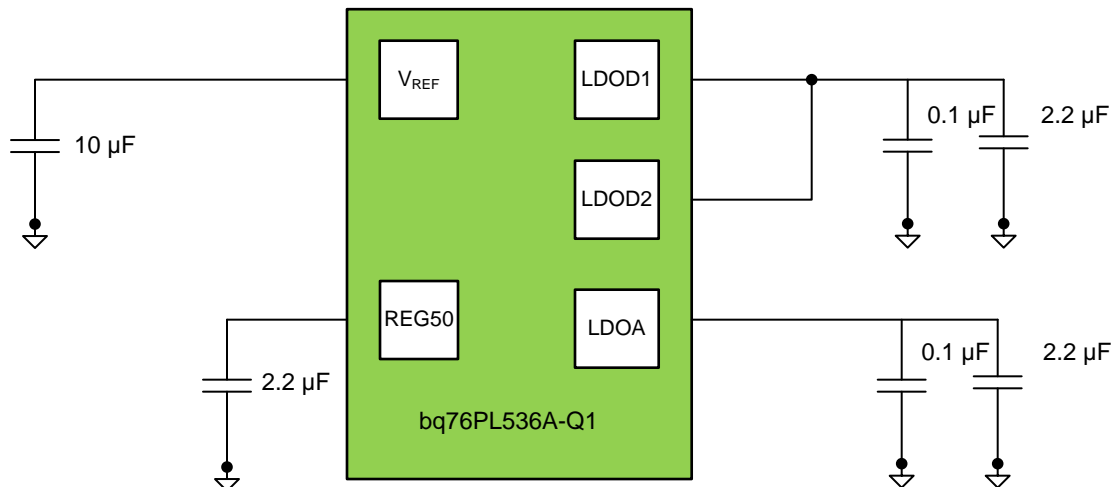


Figure 8. Internal Voltage References

#### 4.6.7 Balance FET and Resistor

Select the balance FET based on the following criteria (see Figure 9):

- Consider and select the  $V_{DS}$  while factoring in the derating requirements selected based on stack voltage.
- Select a large  $V_{GS}$  and preferably one that has ESD protection from the gate to source, which protects the part during hot plugging.
- Consider the  $V_{GS}$  threshold only if the design calls for the discharge resistors to be turned on at low battery voltages.

TI recommends using the CSD16301Q2 device because of its 25  $V_{DS}$ , 10  $V_{GS}$  to approximately  $\pm 8 V_{GS}$ , and the 5.1- or 5.6-V Zener diode between cells. The device also provides a 5.1-V Zener diode to source for additional protection.

Because of the discharge currents for this application, the  $R_{DS}$  value does not require much consideration.

Power dissipation of the FET is a function of the discharge current selected and the resistance value of the FET at that worst-case condition (usually at a hot temperature). The  $I^2R$  represents the power dissipated. Take caution when selecting the size if using very small packages.

The  $R_{V_{GS}}$  resistor is placed to make sure that the gate of the FET has been turned off and does not float into a linear or ON state, which causes excessive leakage currents on the cell in cases of FET failure or PCB open.

A series resistor must be placed between the EQ pin and the FET gate to limit the current going into the FET during a hot plug-in or other transient events.

Select the balancing resistor,  $R_{BAL}$ , to set the desired balance current. If present, the resistors in series with the cell connections (top and bottom, in front of the Zener diode) must also be included in this calculation. These resistors must be sized appropriately to handle the thermal dissipation of continuous cell balancing.

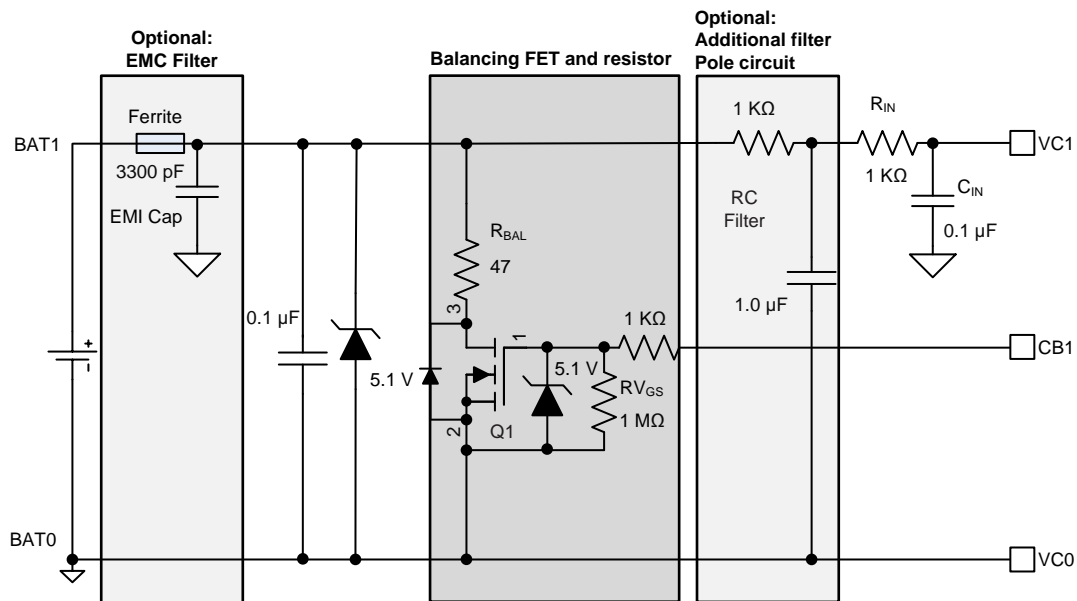


Figure 9. Balancing FET and Resistor

#### 4.6.8 Setting Host versus Slave Mode

The bq76PL536A-Q1 configures to host mode when the HSEL has been disabled. In the host mode, the bq76PL536A-Q1 device provides an SPI pin for connection to a local microcontroller (MCU). When HSEL is enabled (high), the bq76PL536A-Q1 device makes the current mode interface, which provides common-mode voltage isolation between successive bq76PL536A-Q1 devices. The base IC (host) must have the HSEL connected to the GND and the slave device must have the HSEL connected to local LDODs with a 100-kΩ pullup resistor (see Figure 10).

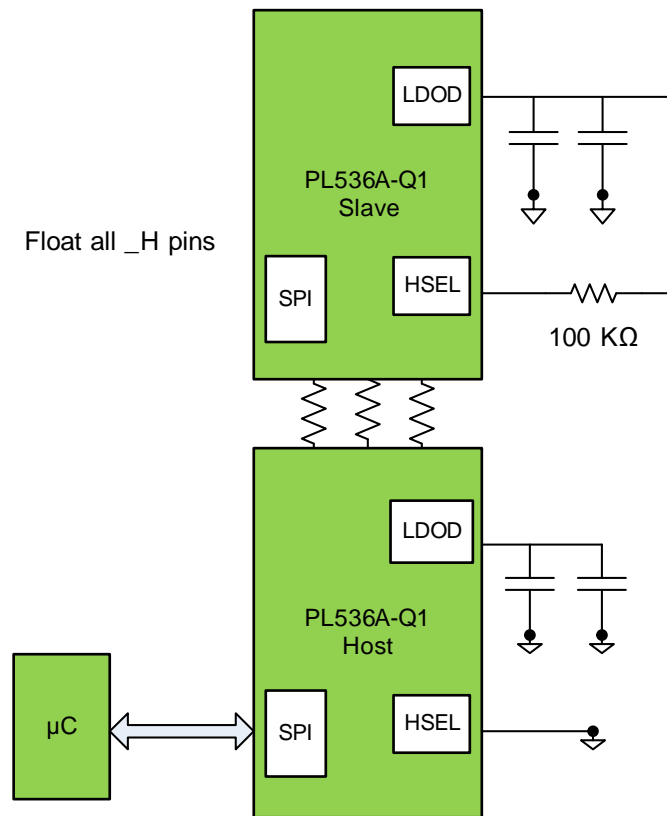


Figure 10. Setting Host and Slave Modes

#### 4.6.9 Thermistors and Temperature Measurements

The bq76PL536A-Q1 device can measure the voltage TS1+, TS−, TS2+, and TS2− differential inputs using the ADC (see Figure 11). These inputs are typically driven by an external thermistor or resistor divider network. The TSn inputs use the REG50 output divided down and internally connected as the ADC references during conversions.

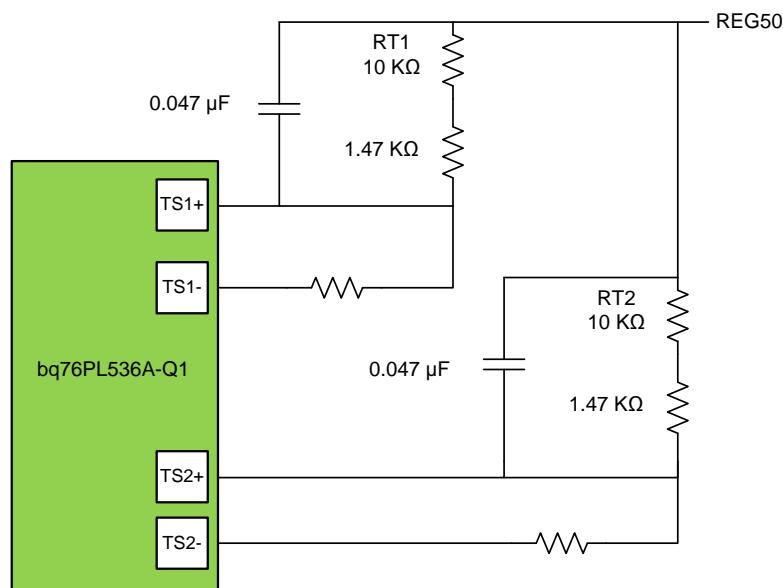


Figure 11. Thermistor Circuits

### 4.6.10 Host Communication

Connecting the bq76PL536A-Q1 device to a host controller through a single-ended communication interface (SPI) requires the following:

1. The CONV\_H, SDI\_H, and SCLK\_H pins must be connected by a 10-K $\Omega$  pulldown resistor going to GND (see Figure 12). If the design does not require use of the bq76PL536A-Q1 CONV\_H pin, the pin can be tied directly to GND or through a resistor. No external pullup resistors are required for the Alert\_H, Fault\_H, and SDO\_H pins.

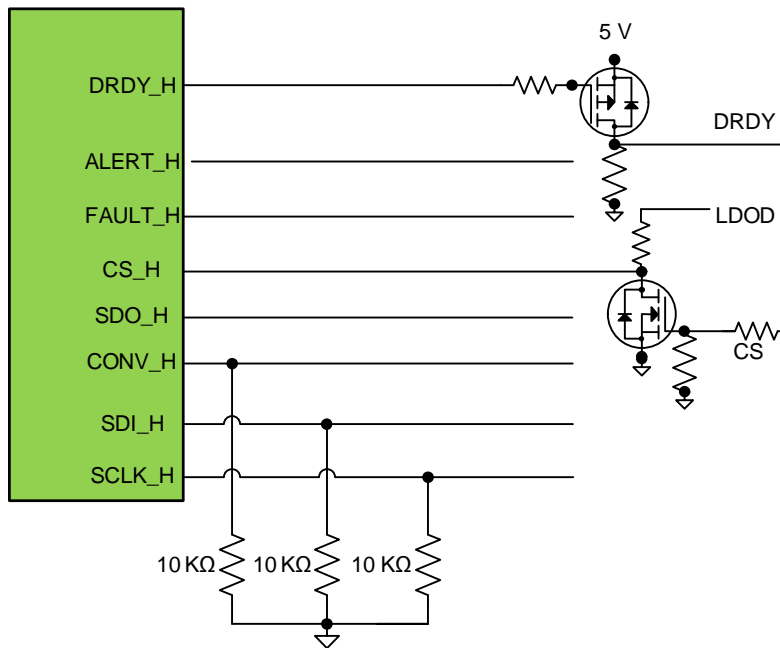


Figure 12. Host Communication

2. The CS\_H pin must be connected by a pullup resistor going to LDOD (see Figure 13). An indeterminate logic level on CS\_H allows the SDO\_H pin to source high levels of current to the unpowered external devices. The SDO\_H pin sources approximately 250 nA (nominal) to the external device when CS\_H = 1. Consider this current to be negligible and ignore it. If CS\_H is not a true logic '1', this current can be substantially higher: 1 mA to 10 mA, or more. Put a 5.6-V Zener diode from the CS\_H to GND if LDOD has applied more than 6 V with external power for EPROM programming.

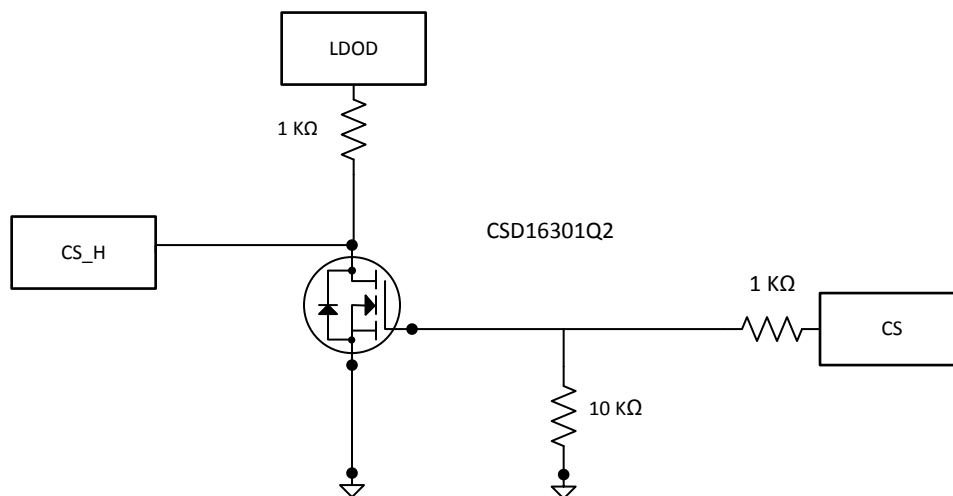
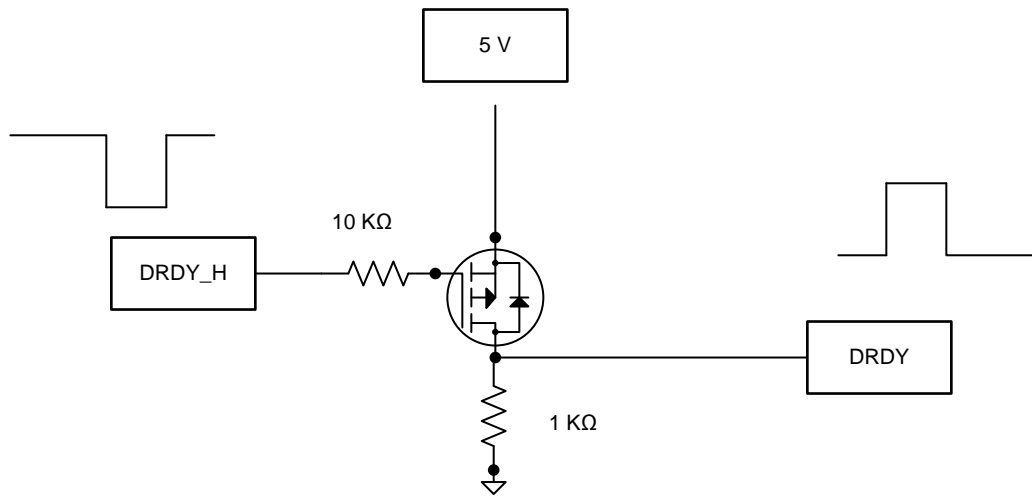


Figure 13. Inverting CS\_H Signal

3. The DRDY\_H pin has two handling methods:
  - (a) Remove the DRDY\_H connection to user circuits. Most designs do not require this pin function. The user firmware can wait approximately 100  $\mu\text{s}$  ( $\text{ADC\_ON} = 1$ ) or approximately 700  $\mu\text{s}$  ( $\text{ADC\_ON} = 0$ ) after the conversion start before reading the data as an alternative to reading this pin.
  - (b) Add an isolating circuit such as a simple, single CET inverter, as [Figure 14](#) shows. The user software senses the inverted signal. P-CET selection is not critical. Do not use the 5-V source from the bq76PL536A-Q1 device. Use a VDD source that powers down when the user circuits power down.



**Figure 14. Inverting DRDY\_H Signal**

The bq76PL536A-Q1 is capable of single-ended, multi-drop, and daisy chain configurations. [Table 2](#) provides a quick checklist for each configuration to ensure that a bq76PL536A-Q1 device is properly configured.

**Table 2. Design Requirements and Checklist for Single-Ended, Multi-Drop, and Stacked (Daisy-chain) Communication**

CHECK LIST	PINS	NAMES	SINGLE-ENDED	MULTI-DROP	DAISY CHAIN	
					HOST	SLAVE
1	1, 3, 5, 7, 9, and 11	VCX	RC filter, <a href="#">Figure 5</a> for reference circuit.	RC filter, <a href="#">Figure 5</a> for reference circuit.	RC filter, <a href="#">Figure 5</a> for reference circuit.	RC filter, <a href="#">Figure 5</a> for reference circuit.
2	13	VCO	Connect to local GND.	Connect to local GND.	Connect to local GND.	Connect to local GND.
3	2, 4, 6, 8, 10, and 12	CBx	Cell balancing, <a href="#">Figure 9</a> . Value of $R_{BAL}$ determines balancing current. Balancing current = $BAT1 / R_{BAL}$ .	Cell balancing, <a href="#">Figure 9</a> . Value of $R_{BAL}$ determines balancing current. Balancing current = $BAT1 / R_{BAL}$ .	Cell balancing, <a href="#">Figure 9</a> . Value of $R_{BAL}$ determines balancing current. Balancing current = $BAT1 / R_{BAL}$ .	Cell balancing, <a href="#">Figure 9</a> . Value of $R_{BAL}$ determines balancing current. Balancing current = $BAT1 / R_{BAL}$ .
4	16	$V_{REF}$	10- $\mu\text{F}$ low-ESR, ceramic capacitor to GND as shown in <a href="#">Figure 8</a> .	10- $\mu\text{F}$ low-ESR, ceramic capacitor to GND as shown in <a href="#">Figure 8</a> .	10- $\mu\text{F}$ low-ESR, ceramic capacitor to local GND as shown in <a href="#">Figure 8</a> .	10- $\mu\text{F}$ low-ESR, ceramic capacitor to local GND as shown in <a href="#">Figure 8</a> .
5	17	LDOA	2.2- $\mu\text{F}$ and 0.1- $\mu\text{F}$ low-ESR ceramic capacitors to GND as shown in <a href="#">Figure 8</a> .	2.2- $\mu\text{F}$ and 0.1- $\mu\text{F}$ low-ESR ceramic capacitors to GND as shown in <a href="#">Figure 8</a> .	2.2- $\mu\text{F}$ and 0.1- $\mu\text{F}$ low-ESR ceramic capacitors to GND as shown in <a href="#">Figure 8</a> .	2.2- $\mu\text{F}$ and 0.1- $\mu\text{F}$ low-ESR ceramic capacitors to GND as shown in <a href="#">Figure 8</a> .
6	18 and 46	LDOD1, LDOD2	LDOD1 and LDOD2 should be tied externally. 2.2- $\mu\text{F}$ and 0.1 $\mu\text{F}$ ceramic capacitors are required as shown in <a href="#">Figure 8</a> .	LDOD1 and LDOD2 should be tied externally. 2.2- $\mu\text{F}$ and 0.1 $\mu\text{F}$ ceramic capacitors are required as shown in <a href="#">Figure 8</a> .	LDOD1 and LDOD2 should be tied externally. 2.2- $\mu\text{F}$ and 0.1 $\mu\text{F}$ ceramic capacitors are required as shown in <a href="#">Figure 8</a> .	LDOD1 and LDOD2 should be tied externally. 2.2- $\mu\text{F}$ and 0.1 $\mu\text{F}$ ceramic capacitors are required as shown in <a href="#">Figure 8</a> .
7	19 and 20	TS1+, TS1-	Float, if not used. See <a href="#">Figure 11</a> for reference.	Float, if not used. See <a href="#">Figure 11</a> for reference.	Float, if not used. See <a href="#">Figure 11</a> for reference.	Float, if not used. See <a href="#">Figure 11</a> for reference.
8	21	CONV_S	Terminate by connecting to GND as shown in <a href="#">Figure 15</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 16</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 17</a> .	Connect to CONV_N (Host IC) as shown in <a href="#">Figure 17</a> .
9	22	DRDY_S	Terminate by connecting to GND as shown in <a href="#">Figure 15</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 16</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 17</a> .	Connect to DRDY_N (Host IC) as shown in <a href="#">Figure 17</a> .
10	23	ALERT_S	Terminate by connecting to GND as shown in <a href="#">Figure 15</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 16</a> .	Terminate by connecting to GND as shown in <a href="#">Figure 17</a> .	Connect to ALERT_N (Host IC) as shown in <a href="#">Figure 17</a> .



**Table 2. Design Requirements and Checklist for Single-Ended, Multi-Drop, and Stacked (Daisy-chain) Communication (continued)**

CHECK LIST	PINS	NAMES	SINGLE-ENDED	MULTI-DROP	DAISY CHAIN	
					HOST	SLAVE
11	24	FAULT_S	Terminate by connecting to GND as shown in Figure 15.	Terminate by connecting to GND as shown in Figure 16.	Terminate by connecting to GND as shown in Figure 17.	Connect to FAULT_N (Host IC) as shown in Figure 17.
12	26	SCLK_S	Terminate by connecting to GND as shown in Figure 15.	Terminate by connecting to GND as shown in Figure 16.	Terminate by connecting to GND as shown in Figure 17.	Connect to SCLK_N (Host IC) as shown in Figure 17.
13	27	SDO_S	Terminate by connecting to GND as shown in Figure 15.	Terminate by connecting to GND as shown in Figure 16.	Terminate by connecting to GND as shown in Figure 17.	Connect to CONV_N (Host IC) as shown in Figure 17.
14	28	SDI_S	Terminate by connecting to GND as shown in Figure 15.	Terminate by connecting to GND as shown in Figure 16.	Terminate by connecting to GND as shown in Figure 17.	Connect to CONV_N (Host IC) as shown in Figure 17.
15	29	CS_S	Terminate by connecting to GND as shown in Figure 15.	Terminate by connecting to GND as shown in Figure 16.	Terminate by connecting to GND as shown in Figure 17.	Connect to CONV_N (Host IC) as shown in Figure 17.
16	31	AUX	Float, if not used.	Float, if not used.	Float, if not used.	Float, if not used.
17	32	REG50	2.2- $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 8.	2.2- $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 8.	2.2- $\mu$ F low-ESR, ceramic capacitor to local GND as shown in Figure 8.	2.2- $\mu$ F low-ESR, ceramic capacitor to local GND as shown in Figure 8.
18	36	CONV_H	Add a 10-k $\Omega$ pull-down resistor to GND. If the CONV_H is not used, it can be connected to GND directly or through a 10-k $\Omega$ resistor as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND. If the CONV_H is not used, it can be connected to GND directly or through a 10-k $\Omega$ resistor as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND. If the CONV_H is not used, it can be connected to GND directly or through a 10-k $\Omega$ resistor as shown in Figure 12.	Float
19	37	DRDY_H	Float, if not used. User F/W must wait $\approx$ 100 $\mu$ S (ADC_ON = 1) or $\approx$ 700 $\mu$ S after conversion starts and reads the data. If used, then add an inverter circuit as shown in Figure 14.	Float, if not used. User F/W must wait $\approx$ 100 $\mu$ S (ADC_ON = 1) or $\approx$ 700 $\mu$ S after conversion starts and reads the data. If used, then add an inverter circuit as shown in Figure 14.	Float, if not used. User F/W must wait $\approx$ 100 $\mu$ S (ADC_ON = 1) or $\approx$ 700 $\mu$ S after conversion starts and reads the data. If used, then add an inverter circuit as shown in Figure 14.	Float
20	38	ALERT_H	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Float
21	39	FAULT_H	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Float
22	40	SCLK_H	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Float
23	41	SDO_H	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Connect to microcontroller as shown in Figure 12.	Float
24	42	SDI_H	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Add a 10-k $\Omega$ pull-down resistor to GND as shown in Figure 12.	Float
25	43	CS_H	Add a simple inverter to isolate from user circuit as shown in Figure 13.	Add a simple inverter to isolate from user circuit as shown in Figure 13.	Add a simple inverter to isolate from user circuit as shown in Figure 13.	Float
26	44	HSEL	Short to GND to communicate to Host as shown in Figure 10.	Short to GND to communicate to Host as shown in Figure 10.	Short to GND to communicate to Host as shown in Figure 10.	A 100K full-up to LDOD1,2 to configure as slave as shown in Figure 10.
27	45	GPIO	Open drain, put (110-k $\Omega$ to 1 M $\Omega$ ) pullup resistor to REG50. If pullup resistor is not included in hardware design, system F/W must program a 0 in IO_CONTROL[GPIO_OUT] to prevent excess current.	Open drain, Put (10K -1M) pullup resistor to REG50. If pullup resistor is not included in hardware design, system F/W must program a 0 in IO_CONTROL[GPIO_OUT] to prevent excess current.	Open drain, Put (10K -1M) pullup resistor to REG50. If pullup resistor is not included in hardware design, system F/W must program a 0 in IO_CONTROL[GPIO_OUT] to prevent excess current.	Open drain, Put (10K -1M) pullup resistor to REG50. If pullup resistor is not included in hardware design, system F/W must program a 0 in IO_CONTROL[GPIO_OUT] to prevent excess current.
28	47	GPAI-	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.
29	48	GPAI+	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.	Connect to GND, if not used. Differential analog input absolute maximum input range is 2.5 V. Short to GND, if not used.
30	50	TEST	Connect to GND	Connect to GND	Connect to local GND	Connect to local GND
31	52	CS_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to CS_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
32	53	SDI_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to SDI_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
33	54	SDO_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to SDO_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
34	55	SCLK_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to SCLK_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.

**Table 2. Design Requirements and Checklist for Single-Ended, Multi-Drop, and Stacked (Daisy-chain) Communication (continued)**

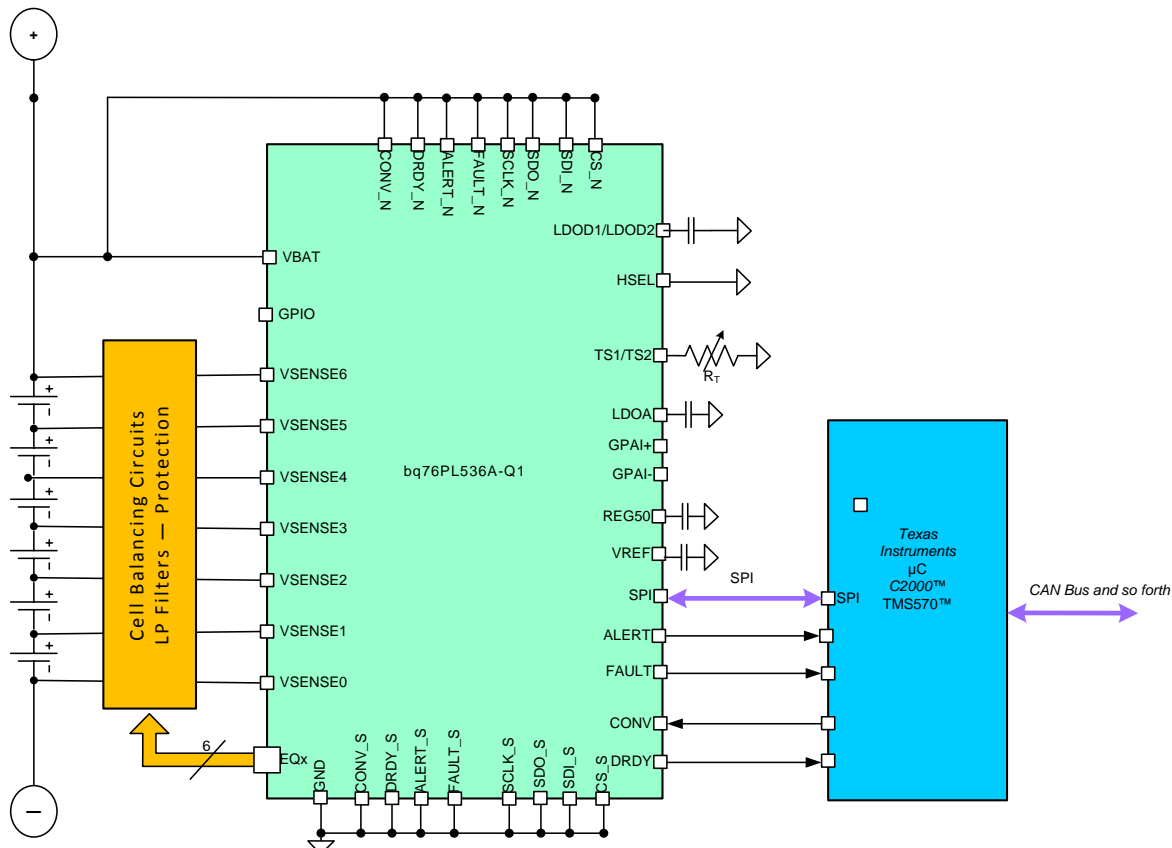
CHECK LIST	PINS	NAMES	SINGLE-ENDED	MULTI-DROP	DAISY CHAIN	
					HOST	SLAVE
35	56	FAULT_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to FAULT_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
36	57	ALERT_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to ALERT_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
37	58	DRDY_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to DRDY_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
38	59	CONV_N	Terminate by connecting to BAT1, BAT2 as shown in Figure 15.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 16.	Connect to CONV_S (slave) as shown in Figure 17.	Terminate by connecting to local BAT1, BAT2 as shown in Figure 17.
39	60 and 61	TS1+, TS-	Float, if not used. See Figure 11 for the reference circuit.	Float, if not used. See Figure 11 for the reference circuit.	Float, if not used. See Figure 11 for the reference circuit.	Float, if not used. See Figure 11 for the reference circuit.
40	63 and 64	BAT1,2	0.1 $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 3.	0.1 $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 3.	0.1 $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 3.	0.1 $\mu$ F low-ESR, ceramic capacitor to GND as shown in Figure 3.

## 4.7 System Architectures

The bq76PL536A-Q1 can be used in a system in several different ways. This section describes different implementations of a bq76PL536A-Q1 for use in a battery pack.

### 4.7.1 Single IC

Figure 15 shows a single bq76PL536A-Q1 interfaced with a microcontroller (MCU).



**Figure 15. Single-Ended bq76PL536A-Q1**

Stacked ICs

4.7.1.1 Multi-Drop

The bq76PL536A-Q1 can be connected in a multi-drop configuration with an MCU local to each module, as Figure 16 shows.

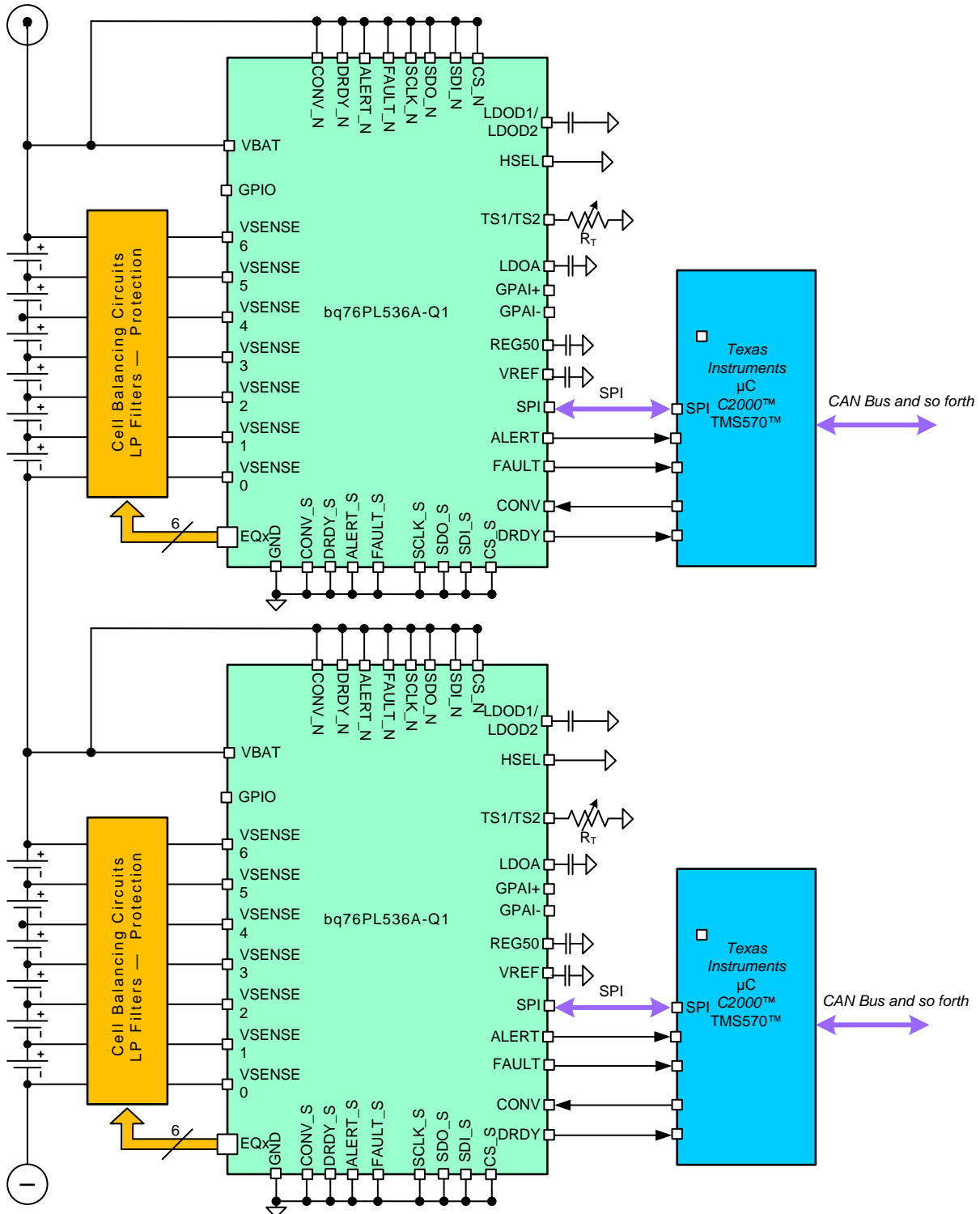


Figure 16. Multi-Drop System Architecture—Local Microcontroller

4.7.1.2 Stacked

The bq76PL536A-Q1 can be connected in a daisy-chain configuration, as Figure 17 shows.

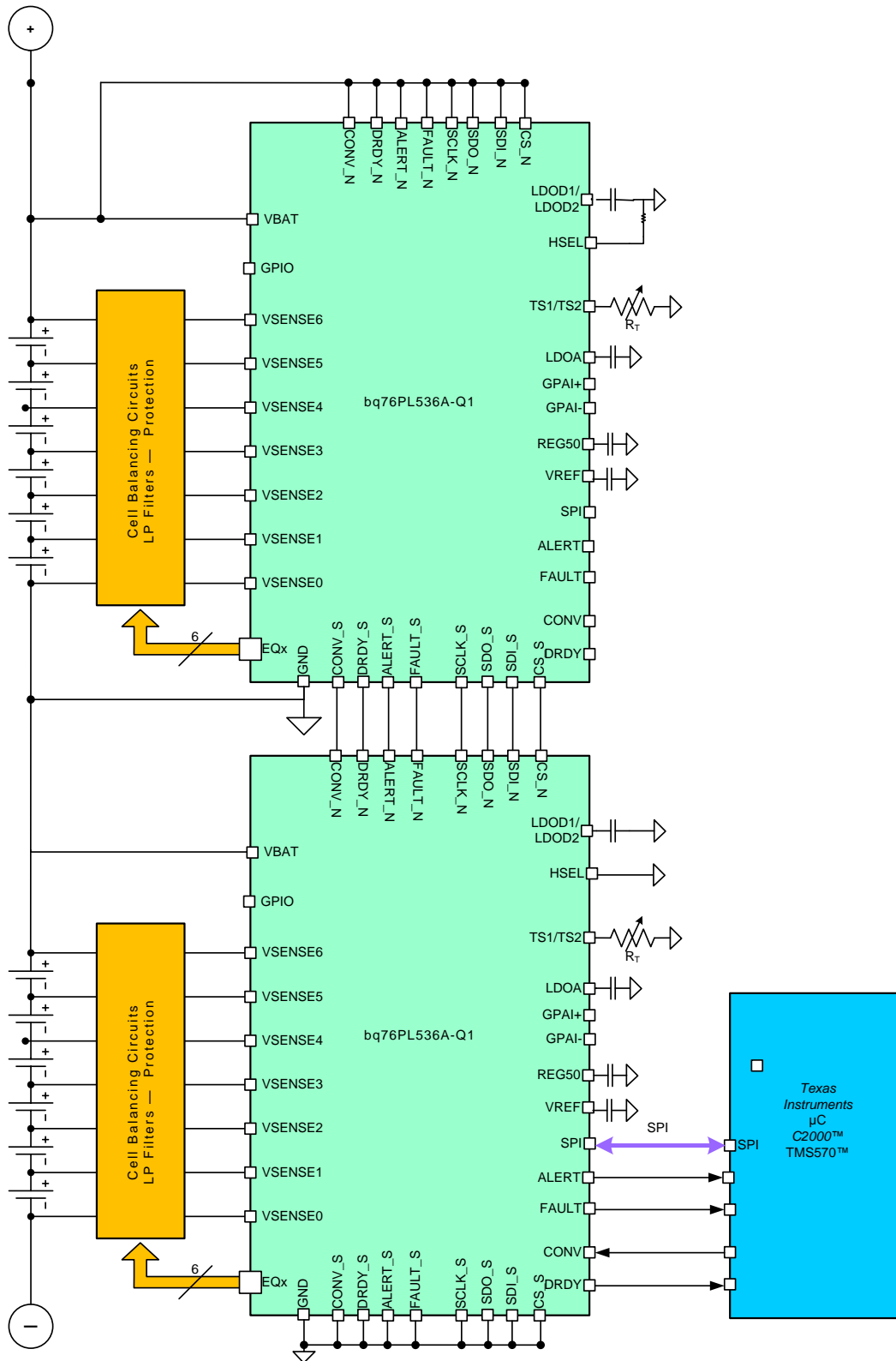


Figure 17. Stacked System Architecture

### 4.7.2 Reduced Cell Count

The minimum  $V_{BAT}$  voltage for a bq76PL536A-Q1 device in a reduced cell count configuration is equal to 7.2 V, so the number of cells depends on the cell operating range. In the example that Figure 18 shows, four cells are connected. Refer to the [SLUSAM3](#) datasheet for more details.

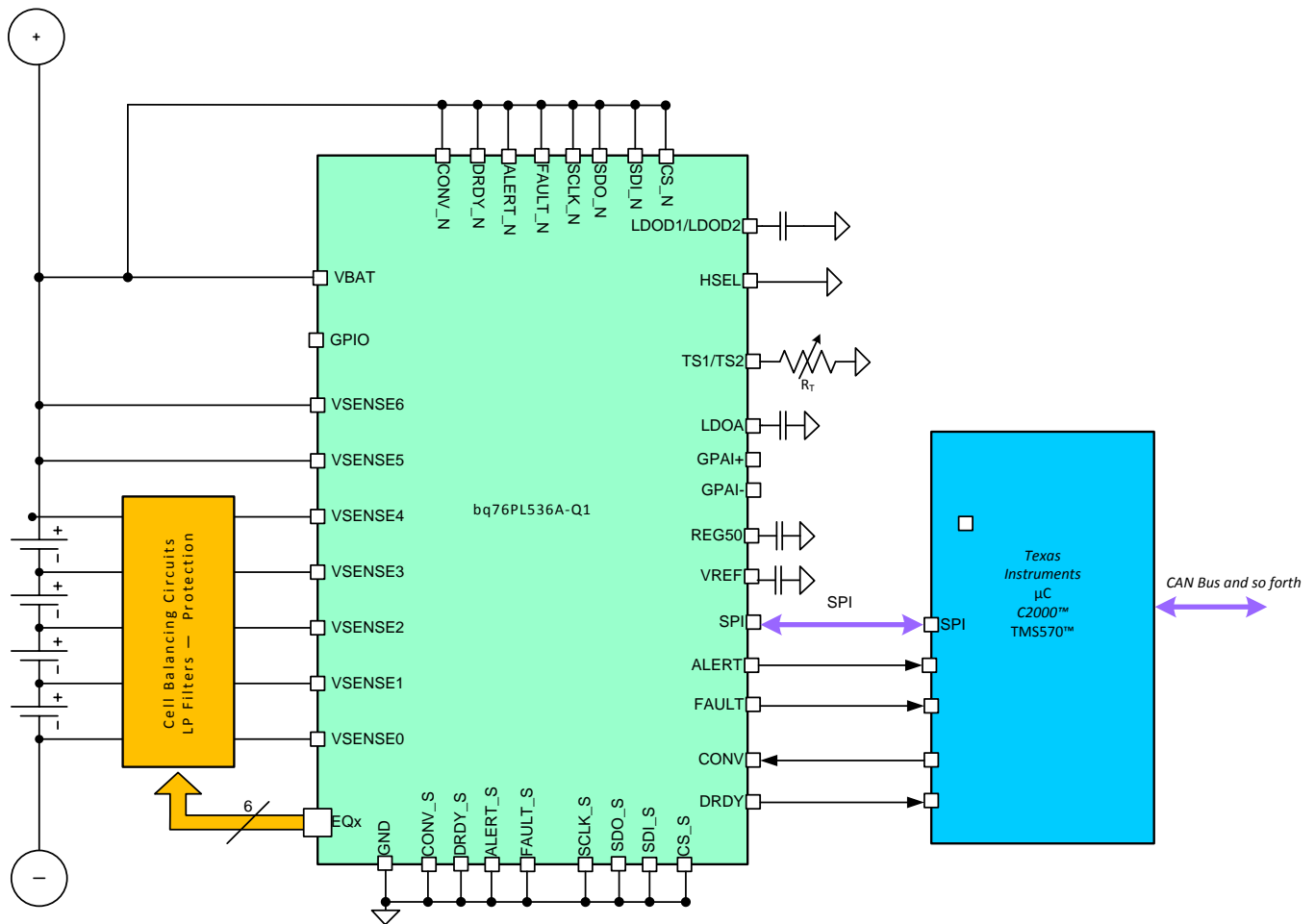


Figure 18. Minimum Cell Count

## 5 Getting Started Hardware

For complete information on the bq76PL536A-Q1 EVM hardware, refer to the [SLUU437](#) user's guide.

### 5.1 EVM Power Supplies Setup

The connection order is as follows: Connect three isolated power supplies to the EVM using the EVM harness. Set the voltage of the power supplies to 20-V DC and current limits to 500 mA.

**NOTE:** Other power schemes, such as using a single power supply, do not provide the correct level of power to the devices under test. Making the connections as the following [Figure 19](#) shows using three isolated supplies is important.

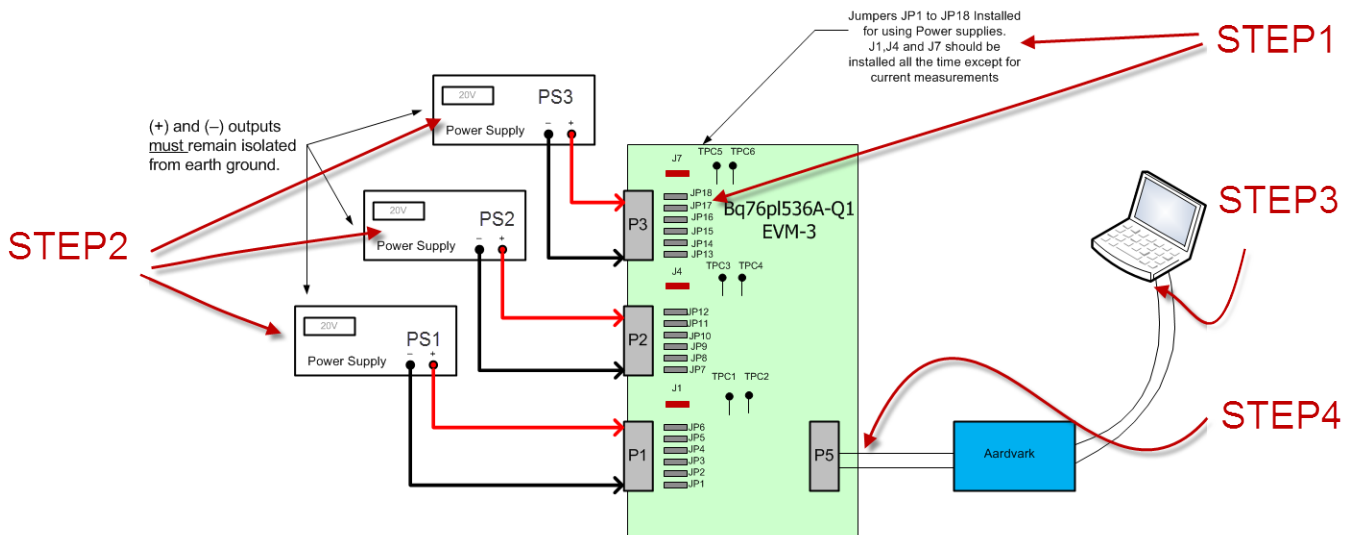


Figure 19. bq76PL536A-Q1 EVM-3 Test Setup

## 6 Getting Started Firmware

The following procedure is an overview describing how the customer can get started with the provided software. For more details, refer to the [SLUU437](#) user's guide.

### 6.1 Aardvark Driver Setup

---

**NOTE:** The Aardvark driver must be installed before attaching the adapter for the first time. Install the Aardvark driver prior to installing the bq76PL536 graphical user interface (GUI) software supplied by Texas Instruments (TI).

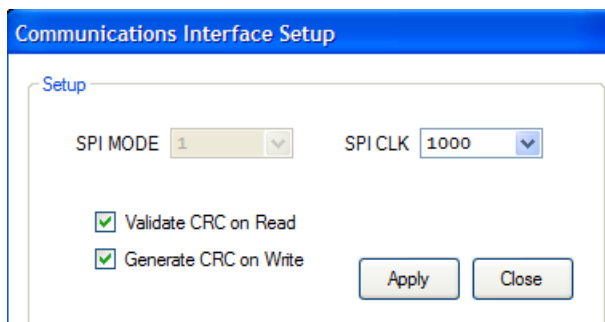
---

Run the *TotalPhaseUSB-v2.0X.exe* to install the drivers. If prompted to do so, plug in the Aardvark adapter to an available USB port using the supplied cable. The port must be a powered port, which the user typically connects directly from a PC. Using a non-powered USB hub may not provide sufficient operating current for the Aardvark adapter or EVM to operate correctly. To access the available software downloads for the Aardvark host adapter family, visit <http://www.totalphase.com/downloads#aardvark>.

### 6.2 bq76PL536A-Q1 Evaluation Software Setup

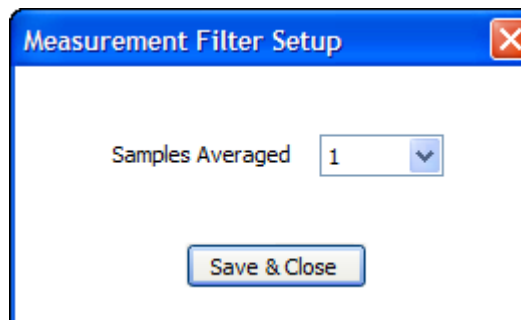
The following steps detail the bq79PL536A evaluation software setup:

1. Run the bq76PL536 *Setup.msi* file to install the GUI software for a Windows-based operating system. As new versions are released, the user may install over the existing version.
2. In the menu bar, navigate to *Tools* → *Interface Setup*. [Figure 20](#) shows the default window. Click the *Apply* button to implement these settings.



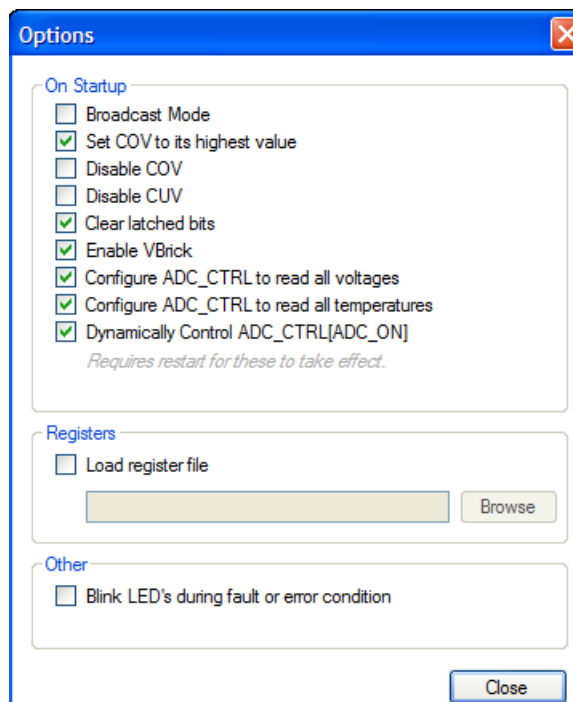
**Figure 20. Communications Interface Setup**

3. In the menu bar, navigate to *Tools* → *Measurement Filter Setup*. [Figure 21](#) shows the default window. The GUI supports up to 500 averages. Click the *Save & Close* button to implement these settings.



**Figure 21. Measurement Filter Setup**

4. In the menu bar, navigate to *Tools* → *Options*. Change the recommended settings to match the settings as the following [Figure 22](#) shows. Close and restart the application after making changes for the new settings to take effect. Changing the settings is only necessary when the user starts the application for the first time after installation; the settings are saved for subsequent application startups.



**Figure 22. Recommended Options**



## 7 Test Setup

### 7.1 Software Installation

If not already installed, install the software using the following procedure.

1. Download and install the *USB Drivers - Windows* from the Aardvark web site: <http://www.totalphase.com/downloads#aardvark>.
2. To install the bq76PL536A and bq76PL536A-Q1 evaluation software, refer to the [SLUU437](#) user's guide.

### 7.2 Connections

**WARNING**

Do not remove any of the jumpers JP1-JP18, J1, J4, or J7 while using the EVM in this configuration. Remove these jumpers only after powering down the power supplies. Lethal DC voltages may be present for these configurations. Contact with these voltages may result in serious injury or death. Use appropriate safety precautions. Refer to the bq76pl536a-Q1 user's guide for details.

The following list details the connection order:

1. Configure the EVM jumpers as [Figure 23](#) shows.
2. Connect the EVM to the power supplies or cells and turn on the supplies at the recommended specification, which is approximately 12 V to 24 V. The absolute maximum voltage per IC is 36 V and must not be exceeded. The recommended maximum continuous voltage is 27 V.
3. Connect the USB cable to the Aardvark adapter and a PC.
4. Connect the Aardvark ribbon cable to the ten-pin header on the EVM board.
5. Start the WinGUI user interface software supplied with the EVM that has been previously installed during the software installation process (see [Figure 24](#)).

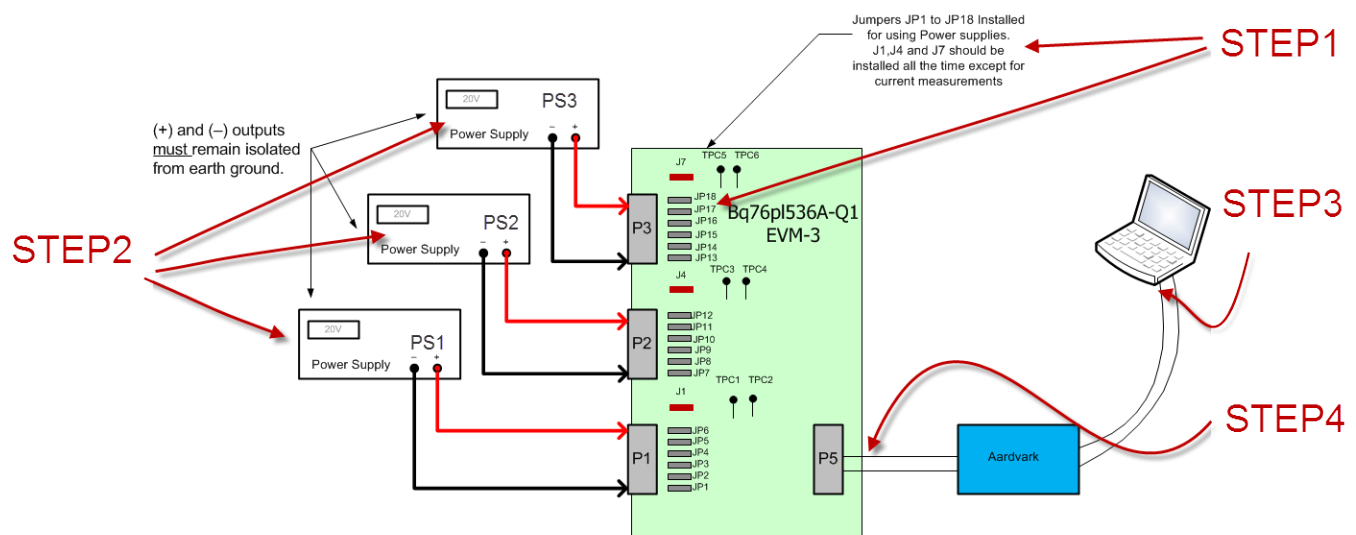


Figure 23. bq76PL536A-Q1 EVM-3 Correct Test Setup

### 7.3 Setting Address

The first step in communicating with the bq76PL536A-Q1 device is to set a unique address for each device in the stack. This setup is required even if the user is only using a single device. As Figure 24 shows, navigate to *Command* → *Auto Address* in the menu bar (shortcut key CTRL + A). This action implements a software process, which interrogates the stack of bq76PL536A-Q1 devices, finds all available devices, and assigns a unique address to each device beginning with address 0x01. The 0x00 address is reserved for unaddressed devices.

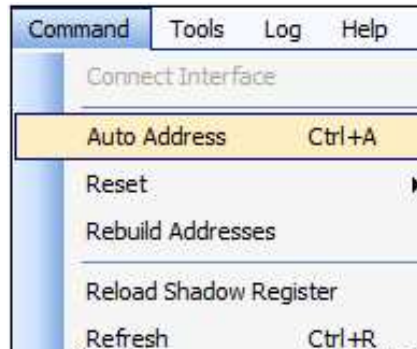


Figure 24. Command—Auto Address Menu Item

After the addressing process is complete, the user can view the number of located devices and the total combined voltage of all cells being monitoring displayed in the *Stack Height* and *V Stack* windows (see Figure 25). In this example, three bq76PL536A-Q1 devices are connected together and monitoring 18 cells of about 20 V for each module. Refer to the [SLUU437](#) user's guide for more details and tests.

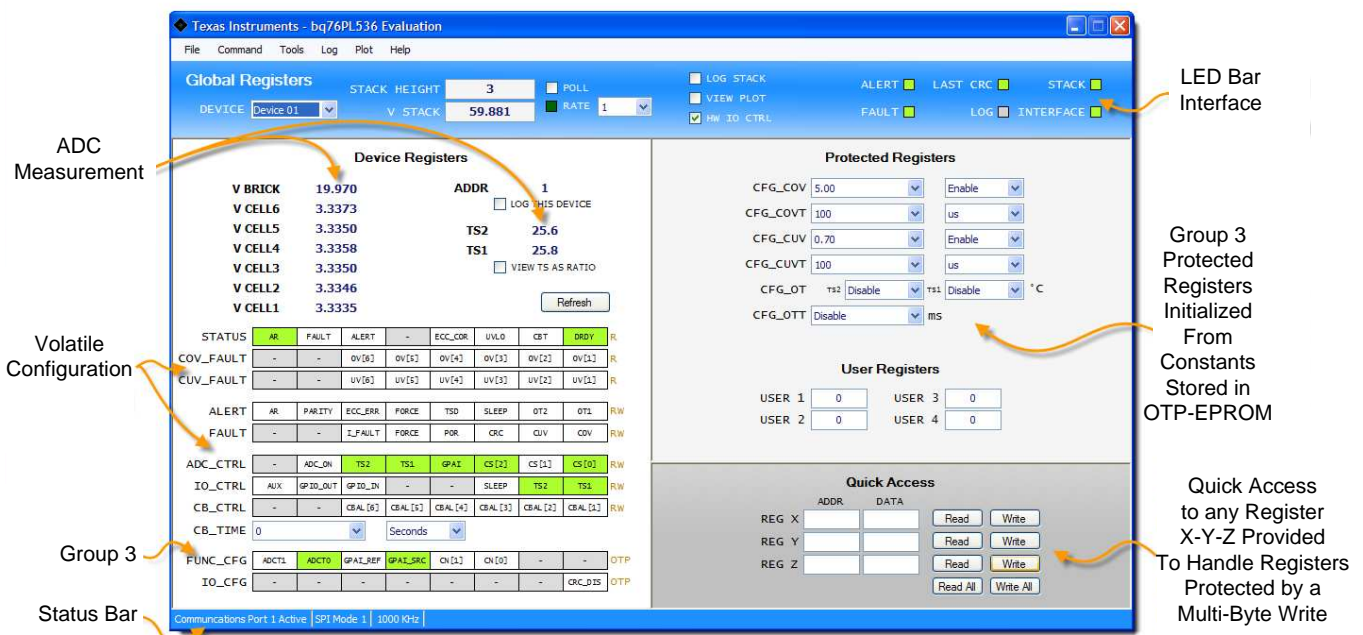


Figure 25. bq76PL536A-Q1 WinGUI

## 7.4 Tests

### 7.4.1 ADC—Total Channel Accuracy

The bq76PL536A-Q1 has a 14-bit SAR ADC converter, which uses an integrated band-gap reference voltage (VREC) for the cell and brick measurements. The ADC has a front-end multiplexer for nine inputs: six cells, two temperature sensors, and one general-purpose analog input (DPAI). The ADC and reference have been factory trimmed to compensate for gain, offset, and temperature-induced errors for all inputs. The purpose of this test is to check over all channels for the accuracy of cell inputs.

The test procedure for the channel accuracy is as follows:

1. Set PS1, PS2, and PS3 to 12 V (see preceding [Figure 23](#)).
2. Start the WinGUI as the following [Figure 24](#) shows.

V BRICK	11.951
V CELL6	2.0020
V CELL5	2.0001
V CELL4	2.0009
V CELL3	2.0005
V CELL2	2.0001
V CELL1	1.9994

Figure 26. Channel Measurement Error

### 7.4.2 Protection—Overvoltage Protection

The bq76PL536A-Q1 integrates dedicated overvoltage detection inputs for each device. The protection circuits use a separate band-gap reference from the ADC system and operate independently. The protector also uses a separate hardware pin, FAULT\_H, from the main SPI bus. Because this pin is separate, it is capable of signaling faults in the hardware without intervention from the host CPU.

The test procedure for the overvoltage protection is as follows:

1. Set PS1, PS2, and PS3 to 13.2 V. Each cell is about 2.2 V.
2. Set the overvoltage protected registers to 3.0 V (see [Figure 27](#)).
3. Set PS1, PS2, and PS3 to 24 V. Each cell is about 4 V, which exceeds the overvoltage threshold.
4. Verify that the fault indicator on the GUI appears as solid red, as [Figure 28](#) shows.
5. View the fault signal assertions, which are identical to the assertions that [Figure 32](#) shows.

The screenshot shows a 'Protected Registers' window with the following settings:

- CFG\_COV: 3.00, Enable
- CFG\_COVT: 1000, ms
- CFG\_CUV: 2.00, Enable
- CFG\_CUVT: 1000, ms
- CFG\_OT: T<sub>s2</sub> 55, T<sub>s1</sub> 55 °C
- CFG\_OTT: 1000, ms

Figure 27. Overvoltage, Undervoltage, and Overtemperature Protection Settings

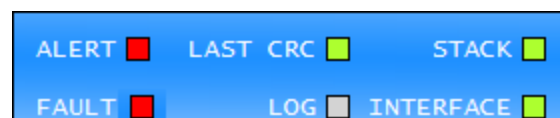


Figure 28. Fault and Alert Alarming

### 7.4.3 Protection—Undervoltage Protection

The bq76PL536A-Q1 integrates dedicated undervoltage detection inputs for each device. The protection circuits use a separate band-gap reference from the ADC system and operate independently. The protector also uses a separate hardware pin, FAULT\_H, from the main SPI bus. Because this pin is separate, it is capable of signaling faults in the hardware without intervention from the host CPU.

The test procedure for the undervoltage protection is as follows:

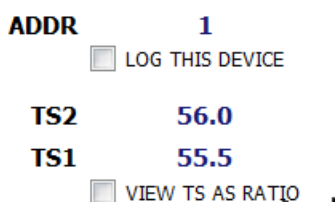
1. Set PS1, PS2, and PS3 to 19.2 V.
2. Set the undervoltage protected registers to 2.0 V as [Figure 27](#) shows.
3. Set PS1, PS2, and PS3 to 10.8 V.
4. Verify that the fault indicator on the GUI appears as solid red, as [Figure 28](#) shows.
5. View the fault signal assertions, which are to be asserted after 1 s as [Figure 33](#) shows.

### 7.4.4 Protection—Overtemperature Protection

The bq76PL536A-Q1 integrates two overtemperature fault detection. The protection circuits use a separate band-gap reference from the ADC system and operate independently. The protector also uses a separate hardware pin, ALERT\_H, from the main SPI bus. Because this pin is separate, it is capable of signaling faults in the hardware without intervention from the host CPU.

The test procedure for the overtemperature protection is as follows:

1. Set PS1, PS2, and PS3 to 18 V as [Figure 23](#) shows.
2. Set the overtemperature to 55°C as [Figure 27](#) shows.
3. Set the temperature chamber to 60°C.
4. Verify that the alert indicator on the GUI appears as solid red, as [Figure 29](#) shows.
5. The alert signal has been asserted when the IC reads above 55°C, as [Figure 31](#) shows.



**Figure 29. Temperature Reading**

### 7.4.5 ADC Conversion—Automatic versus Manual Control

The ADC conversion time is fixed at approximately 6  $\mu$ s per converted channel in addition to 6  $\mu$ s overhead at the start of the conversion. The total conversion time (in  $\mu$ s) is approximately  $6 \times \text{num\_channels} + 6$ .

#### Manual control

The ADC\_CONTROL[ADC\_ON] bit controls the powering up of the ADC section and the main bandgap reference. If the bit is set to 1, the internal circuits are powered on and the current consumption by the part increases. Conversions begin immediately on command. The host CPU must wait more than 500  $\mu$ s before initiating the first conversion after setting this bit. Set the ADC\_CONTROL[ADC\_ON] to 0 when the ADC conversion has completed. If this setting is not changed, then the bq76PL536A-Q1 device continuously consumes excessive current (see [Figure 35](#)).

#### Automatic start

If the ADC\_CONTROL [ADC\_ON] bit is set to 0, an additional 500  $\mu$ s is required. The bq76PL536A-Q1 device automatically turns on the ADC system. The ADC system turns off when the ADC conversion has been completed; therefore, an additional 500  $\mu$ s is required every time the ADC conversion has been initiated.

## 8 Test Data

The following Figure 30 through Figure 36 show the test results.

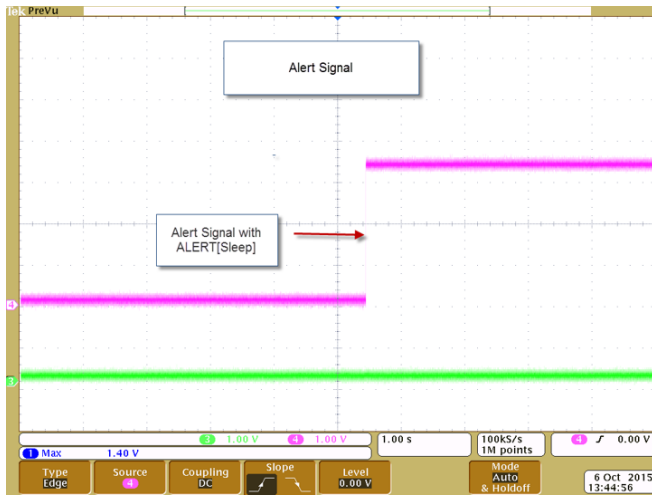


Figure 30. ALERT Signal From ALERT [Sleep]

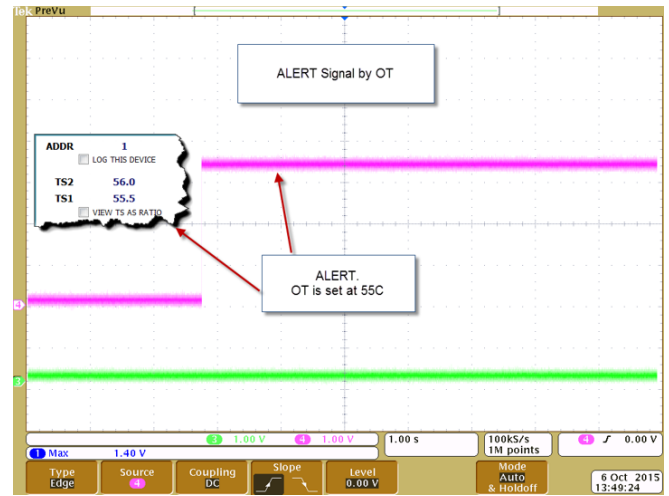


Figure 31. ALERT From Overtemperature

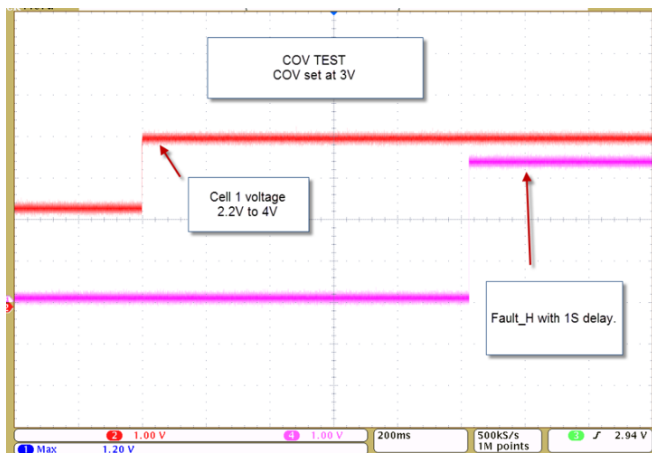


Figure 32. Fault Signal by Cell Overvoltage

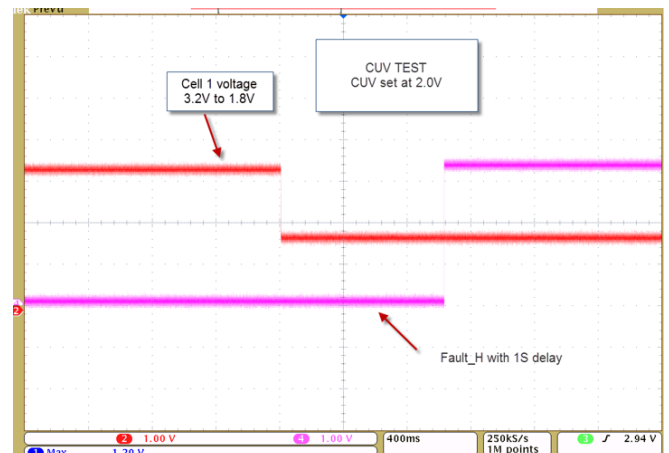
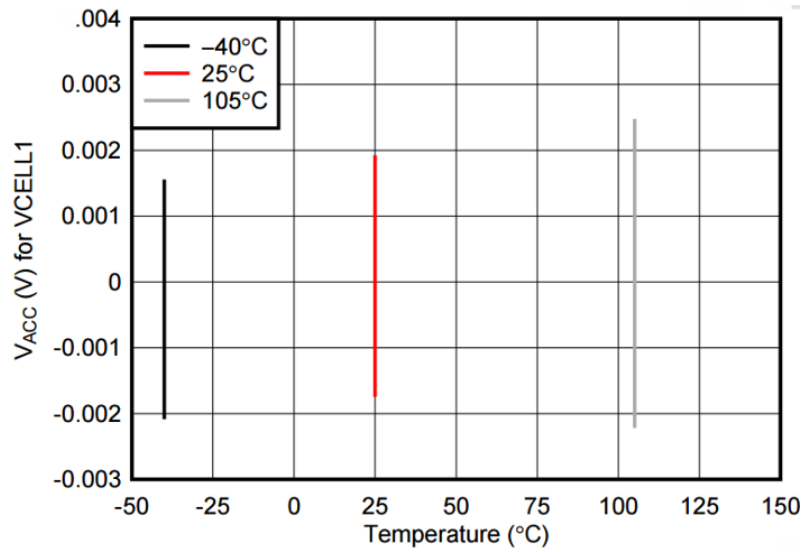


Figure 33. Fault by Cell Undervoltage



V<sub>BAT</sub> = 27 V

Figure 34. Total Channel Accuracy (V) for VCELL1

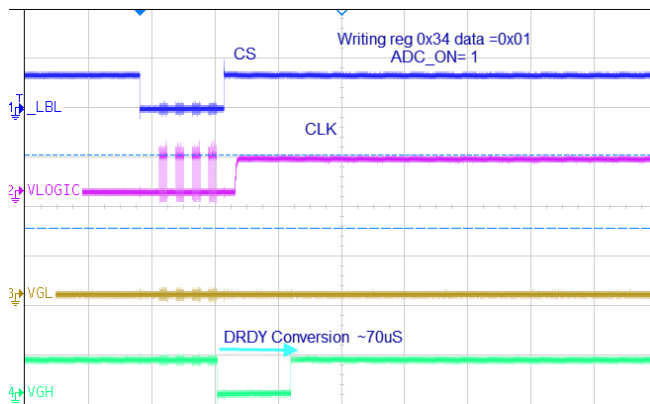


Figure 35. ADC Conversion Timing With ADC\_ON = 1

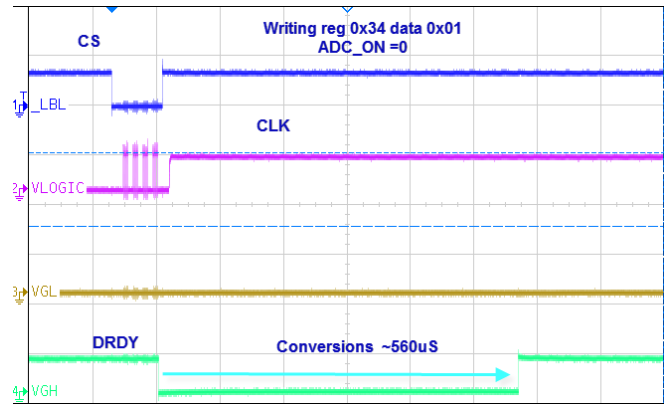


Figure 36. ADC Conversion With ADC\_ON = 0

## 9 Design Files

### 9.1 Schematics

To download the schematics for each board, see the design files at [TIDA-00821](#).

### 9.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at [TIDA-00821](#).

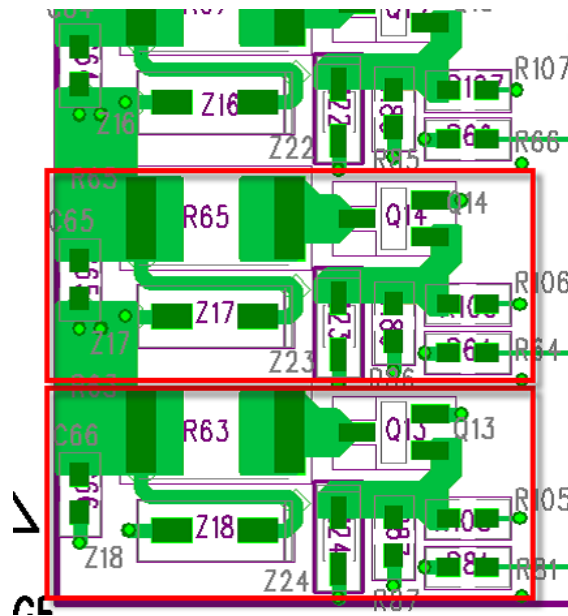
### 9.3 Layer Plots

To download the layout prints for each board, see the design files at [TIDA-00821](#).

### 9.4 Layout Guidelines

#### 9.4.1 General Layout Guidelines

- Keep the cell-balancing circuit components in a tight group.
- Use tracks sized to carry the current and help dissipate heat.
- The tracks must be large enough to handle the current of the cell balancing with less than a 10°C rise.
- For the purposes of balancing, several power resistors in parallel perform better than a single resistor by dissipating heat over a larger surface area.
- The vertical-bus communications connections between the ICs must be as short and direct as possible. Keep these connections away from other noise sources in the system and on the board.

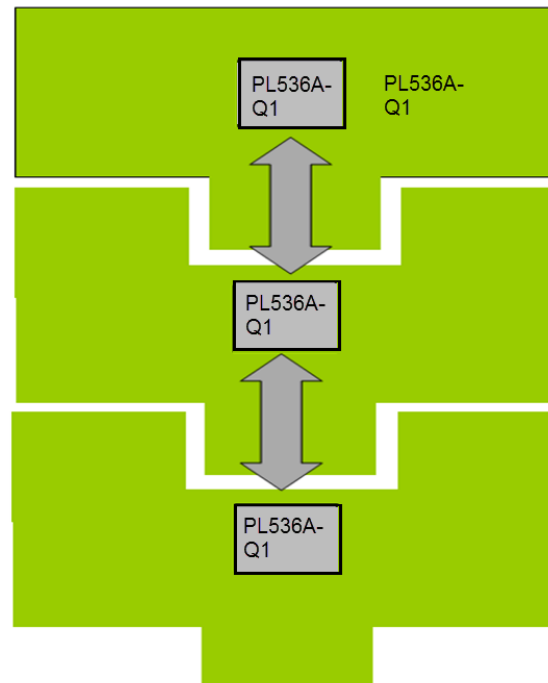


**Figure 37. General PCB Layout**

### 9.4.2 Ground Planes

Proper ground plane design is necessary to protect signal integrity and keep the noise impact on the EMC performance to a minimum.

- Each chip in the circuit must have its own ground plane, referenced to the cell1 negative terminal of the lowest cell in its six-cell stack.
  - For the bottom-most circuit, the ground reference is cell1–.
  - For the second circuit, the ground plane reference is cell7– (cell6+).
  - The third circuit uses cell13– (cell12+) for its ground plane and so forth.
- Each ground plane must be separate and isolated from the other ground planes physically, but must be connected through a capacitor electrically.
- A good ground (GND) plane must have a dedicated layer and extend from the upper IC under its vertical-communications tracks down to the next IC at the lower end in the stack.



**Figure 38. Simplified Layout Guideline**

### 9.5 Gerber Files

To download the Gerber files for each board, see the design files at [TIDA-00821](#).

### 9.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at [TIDA-00821](#).

### 10 Software Files

To download the software files, see the design files at [TIDA-00821](#).



## 11 References

1. Texas Instruments, *3 to 6 Series Cell Lithium-Ion Battery Monitor and Secondary Protection IC for EV and HEV Applications*, bq76PL536A-Q1 Data Sheet ([SLUSAM3](#))
2. Texas Instruments, *bq76PL536A and bq76PL536A-Q1 EVM Quick Start Guide*, User's Guide ([SLUU437](#))

## 12 Terminology

**ADC**— Analog-to-digital converter

**AFE**— Analog front end

**BCI**— Bulk current injection

**BIST**— Built-in self-test

**BMS**— Battery management system

**BSP**— Battery stack protection

**CAN**— Controller area network

**DAC**— Digital-to-analog converter

**EEPROM**— Electrically erasable programmable read only memory

**EMI**— Electromagnetic interference

**FET**— Field-effect transistor

**GPIO**— General purpose input-output

**MCU**— Microcontroller unit

**Module**— Series connection of cells managed by the bq76PL536A-Q1

**PWM**— Pulse width modulation

**Stack**— Series connection of modules managed by the pack controller

**SPI**— Serial peripheral interface

**TVS**— Transient suppression diode

**UART**— Universal asynchronous receiver and transmitter

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