

TI Precision Designs: Verified Design Software Pacemaker Detection Reference Design



TI Precision Designs

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Circuit Description

This circuit is designed to condition and digitize an electrocardiogram signal output from the integrated PACE_OUT buffer on the ADS129x to detect artifacts of a pacemaker. This circuit includes an op amp which serves as a signal conditioner and input driver for a fast-sampling SAR ADC. The ADC communicates using an SPI compatible interface. This document also discusses developing a detection algorithm and other digital signal processing considerations.

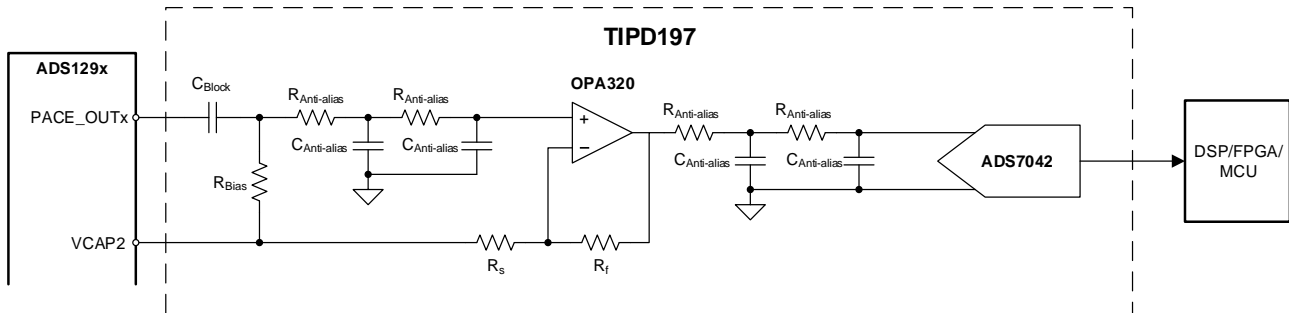
Design Resources

- [TIPD197](#)
- [TINA-TI™](#)
- [ADS7042](#)
- [OPA320](#)
- [ADS1298](#)

- All Design files
- SPICE Simulator
- Product Folder
- Product Folder
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1 Design Summary

The design requirements are to resolve pacemaker signals with the following characteristics such that they can be detected with a strong software pace detection algorithm:

- 0.5 ms – 2 ms pacemaker signal width
- ± 2 mV – ± 250 mV pacemaker signal magnitude
- 100 μ s maximum rise time

This design showcases a topology which has proven to provide a user with the ability to detect the presence of a pacemaker. The specific values of the gains, target cutoff frequencies, thresholds, etc. are flexible to allow systems with inherent variations to find a reliable combination.

Figure 1 shows an electrocardiogram signal with a pacemaker present (top) and after being output from a digital high pass filter showing thresholds used to trigger detection (bottom).

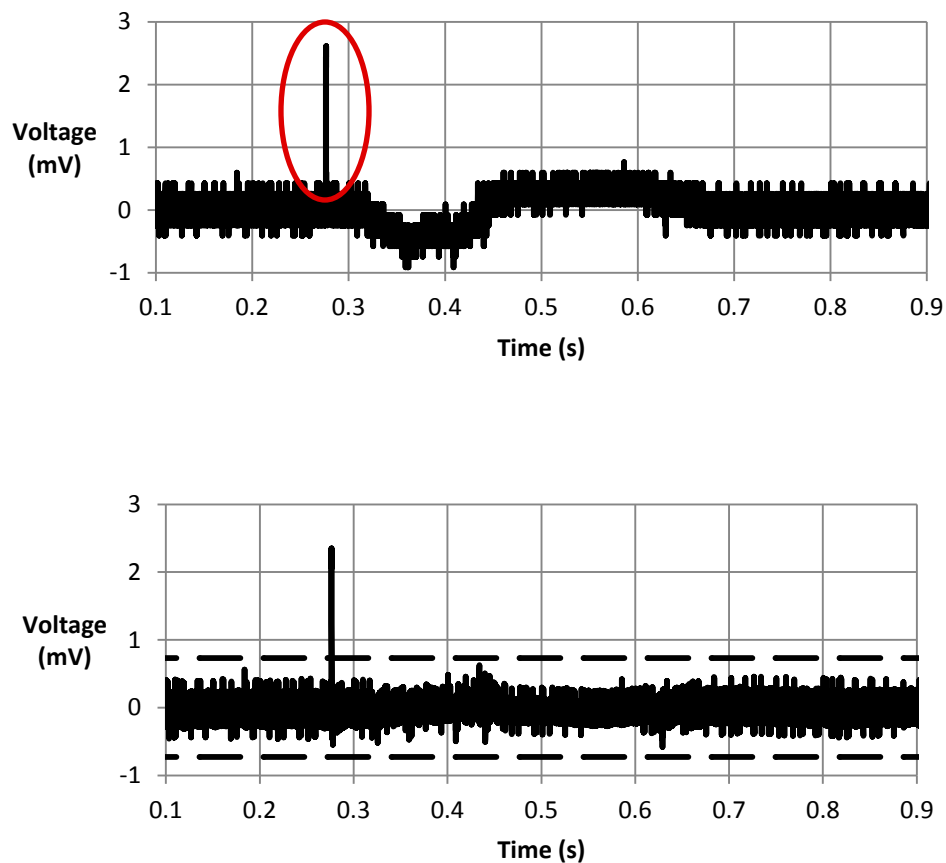


Figure 1: Example pacemaker signal capture using TIPD197 (top) and after detection algorithm (bottom)

2 Theory of Operation

According to AAMI EC11, medical instrumentation must be capable of displaying pacemaker pulses with amplitudes between 2 and 250 mV, durations between 0.5 and 2 ms, and a rise time of less than 100 μs. These parameters will be used as the basis for defining the signal that this solution aims to detect. Figure 2 shows a circuit that may be used to detect a pacemaker pulse.

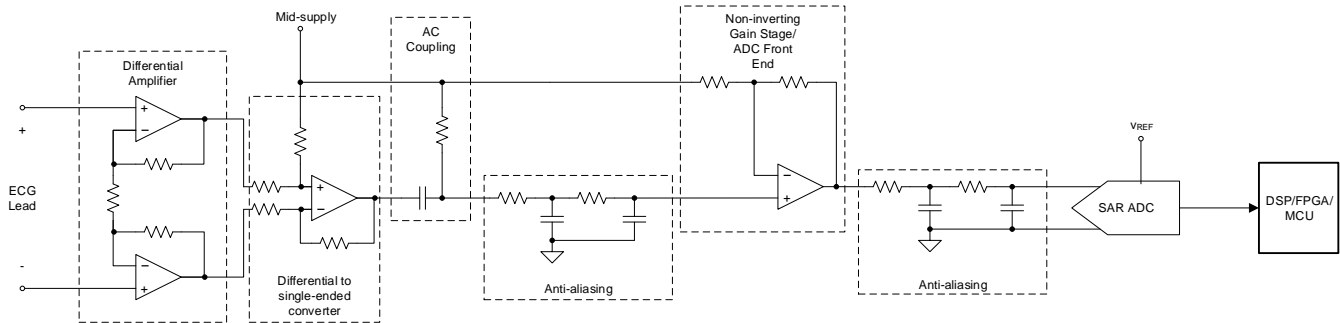


Figure 2: Pacemaker detection circuit

The transfer function measured as the output digital code of the ADC is shown in Equation (1). The quantity G_{total} represents the total gain from all of the amplifier stages.

$$\text{OutputCode} = v_{Lead} \frac{G_{total} 2^N}{V_{Ref}} \quad (1)$$

2.1 Understanding a Pacemaker Pulse

A pacemaker artifact will appear as a narrow pulse in an ECG waveform. The amplitude at which the pacemaker signal appears in the ECG signal depends on the lead.

The characteristic of a pacemaker pulse which separates it from other biopotential signals is its fast rise time and narrow width. In general, these characteristics will be leveraged in detection, but also they provide constraints on the design. Figure 3 shows an example Lead II ECG waveform with a ventricular pacer present.

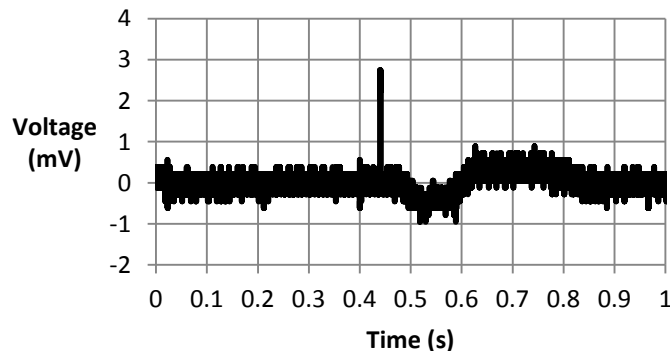


Figure 3: Example ECG signal with pacemaker present

Such a narrow pulse would intuitively suggest a wide bandwidth. In this design, the narrowest pulse targeted for detection measures 0.5 ms. A bandwidth of 4 kHz is sufficient to resolve the pulse. The Nyquist inequality dictates that systems must sample more than twice as fast as the bandwidth. In practice the signals should be well oversampled to produce a better reconstruction.

In addition to the constraint created by the speed of the pulse, it also has the potential to be small in magnitude. The input referred noise must be less than 2 mV if the pulse is to be identified. Ideally it should be significantly smaller than 2 mV to prevent a false detection. How much margin is needed exactly will depend largely on the detection algorithm.

2.2 Signal Conditioning

An ECG signal needs to be conditioned to be made ideal for pacemaker detection. The signal may need gain, electrode offset needs to be removed, and the signal should be biased at the mid-supply voltage of the ADC to provide the signal with the maximum possible range within the ADC's conversion range.

2.2.1 ECG Front End

A typical ECG lead is comprised of the difference between potentials at two electrodes. For instance Lead I is defined as LA – RA. This means the front end of any ECG sensor must be differential. The front end must also comply with medical regulatory standards which limit the amount of current that can flow in or out of electronic medical equipment. A differential amplifier with a high impedance input is a natural choice for ECG front end since it meets both requirements.

Figure 4 shows a differential amplifier as an ECG front end. Gain can be provided by selecting R_f and R_g using Equation (2).

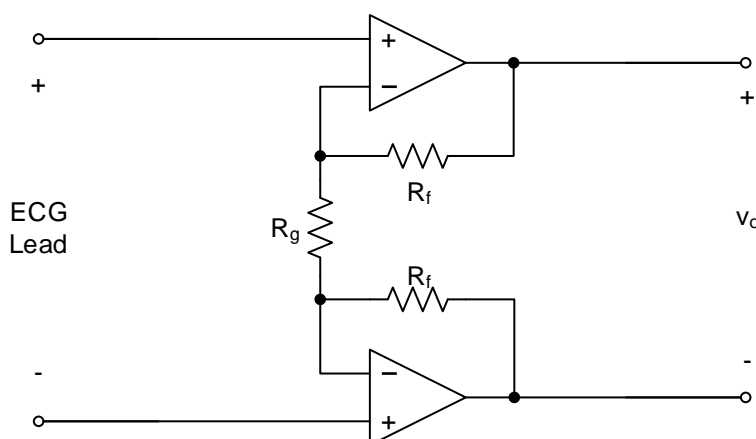


Figure 4: Fully differential amplifier as ECG front end

Equation (2) describes the transfer function of this amplifier scheme. The output can conveniently be routed to a typical ECG acquisition channel as well as a pacemaker detection channel.

$$v_o = v_{Lead} \left(\frac{2R_f}{R_g} \right) \quad (2)$$

2.2.2 Differential to Single-Ended Conversion

It is convenient for pacemaker detection for the lead which is being probed for a pacemaker signal to be single ended and referenced to a known potential. An amplifier can be used to take the output from the fully differential amplifier and refer it to some voltage which is constant with respect to the board supplies.

Figure 5 shows a differential to single ended converter whose output is referred to mid-supply. The resistor values will define the gain according to Equation (3).

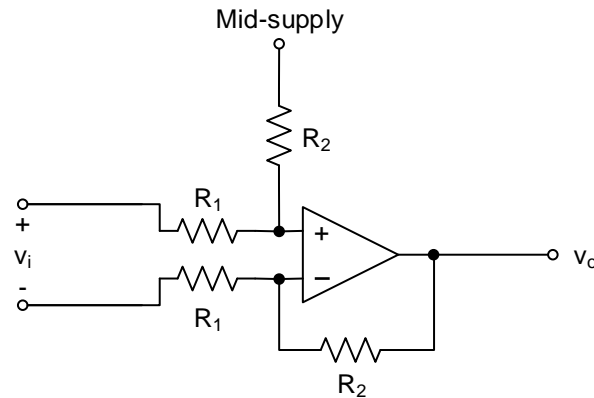


Figure 5: Differential to single-ended converter

$$v_o = \frac{R_2}{R_1} v_i \quad (3)$$

2.2.3 AC Coupling

Even after the output has been referred to mid-supply, it may still have dc content. In ECGs, dc offset can range up to a few hundred millivolts. It's important to remove it so that the input to the pacemaker detection ADC is centered at mid-supply giving it the most range within the rails of the converter.

This can easily be done by placing a capacitor in series with the input and biasing to mid-supply with a large shunt resistor as shown in Figure 6.

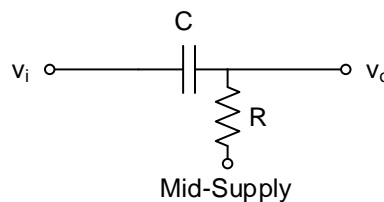


Figure 6: AC coupling circuit

This circuit forms a high-pass filter. The cutoff filter should be placed as low as possible if the designer intends to preserve the QRS complex of the ECG waveform. The constraint placed on the cutoff frequency can be relaxed if the QRS complex is not needed on the pacemaker channel. Equation (4) describes the half-power frequency of the circuit.

$$f_{-3dB} = \frac{1}{2\pi RC} \quad (4)$$

2.2.4 Non-Inverting Gain Stage/ADC Front End

Another amplifier is needed to drive the ADC's sampling circuitry. This amplifier must have sufficient bandwidth to successfully resolve the high bandwidth pacemaker pulse as well as charge the SAR ADC's sample and hold circuitry. Since an anti-aliasing filter will be placed at the output of the amplifier, the bandwidth should be at least 4 times as large as the anti-aliasing filter's cutoff frequency. This will minimize harmonic distortion and improve overall stability of the circuit.

The amplifier can also provide an additional gain stage. Therefore, it should be configured in a non-inverting topology as shown in Figure 7. Note that the gain-setting resistor R_s shunts to mid-supply, preserving the common-mode of the signal.

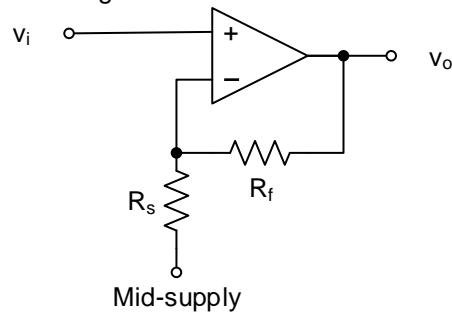


Figure 7: Non-inverting gain stage

The transfer function is shown in Equation (5). If no gain is needed, then R_s may be depopulated and R_f shorted out to configure the op amp as a simple buffer.

$$v_o = v_i \left(1 + \frac{R_f}{R_s} \right) \quad (5)$$

2.3 Anti-Aliasing

Anti-aliasing in front of the ADC limits the band of the system to prevent the fold-back of unwanted high frequency signals as well as broadband noise. Steep anti-aliasing roll-off is critical in this design where the noise may indeed be close in magnitude to the signal of interest. A simple RC filter may not provide satisfactory attenuation outside of the signal band. A second order RC filter provides faster roll off. Figure 8 shows an example two-pole RC filter. The transfer function for the circuit is shown in Equation (6).

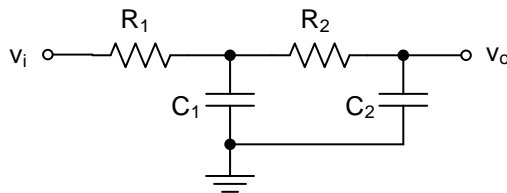


Figure 8: Second order RC filter

$$H(\omega) = \frac{1}{1 + (j\omega)[C_1 R_1 + C_2 (R_1 + R_2)] + (j\omega)^2 R_1 R_2 C_1 C_2} \quad (6)$$

If necessary, roll-off can be improved by adding another second order RC anti-aliasing in front of the amplifier which drives the ADC. Assuming very high input impedance and an amplifier bandwidth much larger than that of the passive filters, there will be no interaction between the two anti-aliasing filters and their transfer functions can be multiplied. Refer to Figure 9 for an example. The op amp has been configured as a unity gain buffer for illustration, but this does not have to be the case. The op amp may also be configured in the non-inverting gain scheme to provide gain.

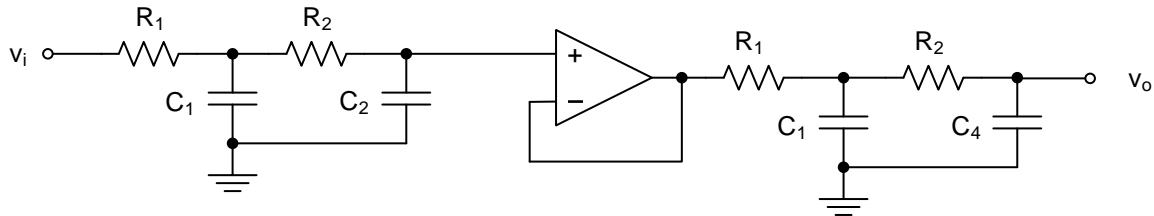


Figure 9: Two second order RC filters isolated by op amp

$$H(\omega) = \left(\frac{1}{1 + (j\omega)[C_1R_1 + C_2(R_1 + R_2)] + (j\omega)^2 R_1R_2C_1C_2} \right)^2 \quad (7)$$

A designer could provide additional anti-aliasing by intentionally using a lower bandwidth amplifier in one of the stages before the ADC input drive amplifier. The ADC driver should remain high bandwidth to prevent THD degradation and to ensure stability. Equation (8) describes the transfer function of an amplifier with one low pole where G corresponds to the closed loop gain of the amplifier and ω_1 is the cutoff frequency. The total anti-aliasing transfer function can be obtained by multiplying this with the Equation (7).

$$H(\omega) = \frac{G}{1 + j\omega / \omega_1} \quad (8)$$

The ADC samples with a switch-capacitor circuit like that shown in Figure 10. Generally R_s will be small. The capacitor directly in front of the ADC C_1 should be at least 10 times as large as the sampling capacitor C_s in order to provide sufficient charge with each sample.

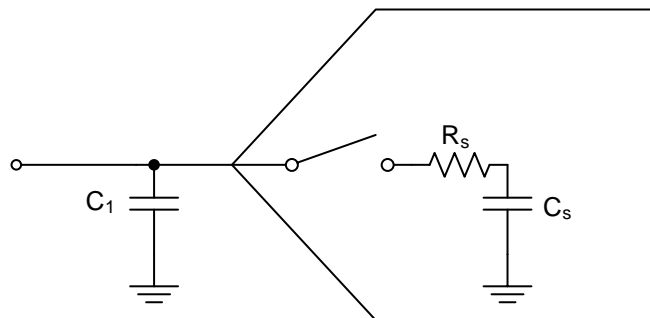


Figure 10: ADC sampling approximation

2.4 Sampling

The ADC quantizes input voltages into a finite number of “bins”. With the potential for very small signals it is important to ensure that even the smallest pacemaker signal will appear larger than the surrounding noise following quantization. Equation (9) shows the transfer function for an ADC where N is the number of bits.

$$\text{OutputCode} = v_{in} \left(\frac{2^N}{V_{\text{Ref}}} \right) \quad (9)$$

2.5 Digital Signal Processing

Once the ECG has been converted, a strong digital signal processing algorithm can detect the presence of a pulse. Many designers have proprietary algorithms to detect the presence of a pacemaker or provide additional diagnostic information.

Consider an algorithm which puts magnitude thresholds on the output data and sets a flag if data exceeds the thresholds indicating that a pacemaker pulse was present in the data. Output data will be centered about a voltage near the middle of the ADC's input range since the pacemaker could be as large as a few hundred millivolts. Since the source providing the bias to the signal could have error, setting the thresholds with respect to the calculated mid-supply output code is unreliable. This offset must be calibrated out so the thresholds can be set about zero.

Once that has been done, the algorithm faces another problem. The peak of the patient's QRS complex can be larger than the smallest possible pacemaker pulse. Figure 11 shows an example of such an ECG.

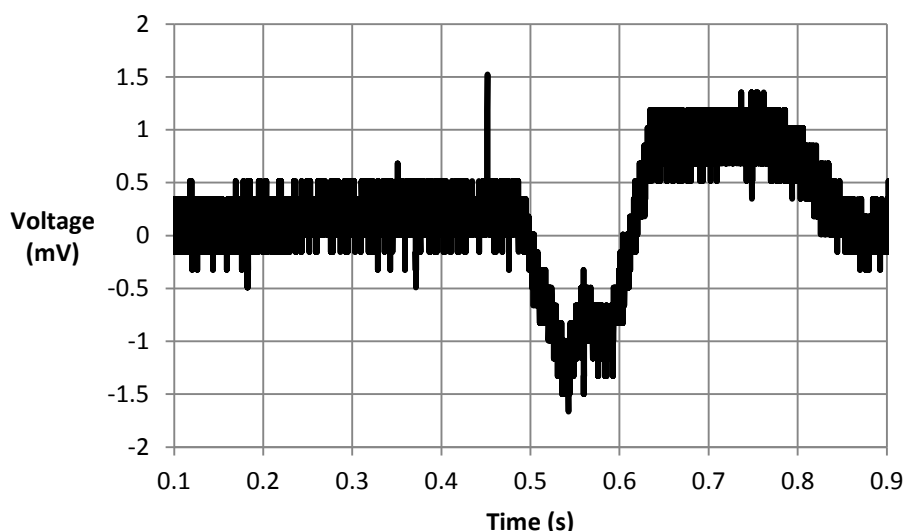


Figure 11: Paced ECG with similar magnitude QRS complex

The QRS complex can be removed by digitally high pass filtering the data. This can be done in conjunction with the offset calibration by choosing a digital filter which has a zero present at dc. The choice of filter will depend on several factors including processor bandwidth, tolerance for non-linear phase response, and processor resolution. Once the QRS complex has successfully been filtered out, the ECG may look like it does in Figure 12. The plot shows dashed lines representing a threshold where if the data exceeds the threshold in either direction, detection is triggered. A designer should take a statistical approach to choosing such a threshold. They should take data across different boards and environmental parameters to choose a threshold that will minimize the likelihood of a false detection while also ensuring that pulses can be detected with sufficient probability.

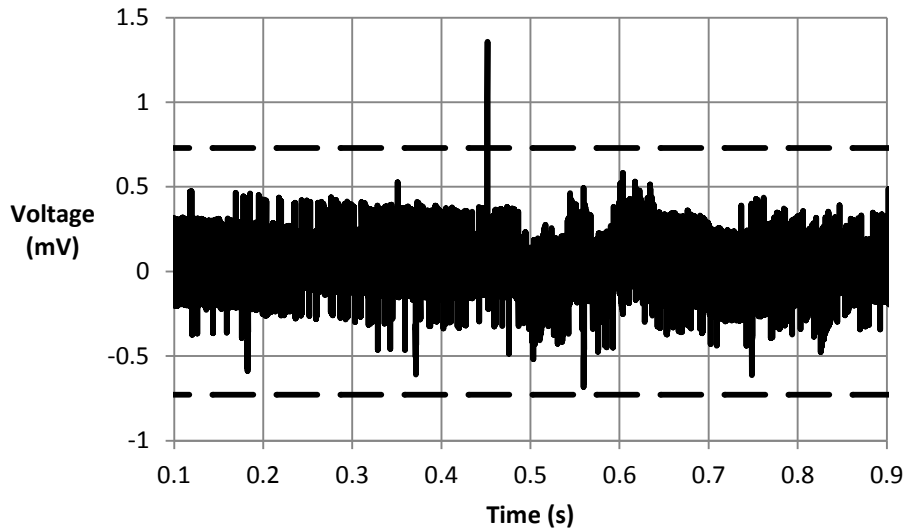


Figure 12: Paced ECG following high pass filtering

3 Component Selection

Figure 13 shows a schematic with the components chosen for this design. The dotted boundary indicates which blocks are included in the PCB design.

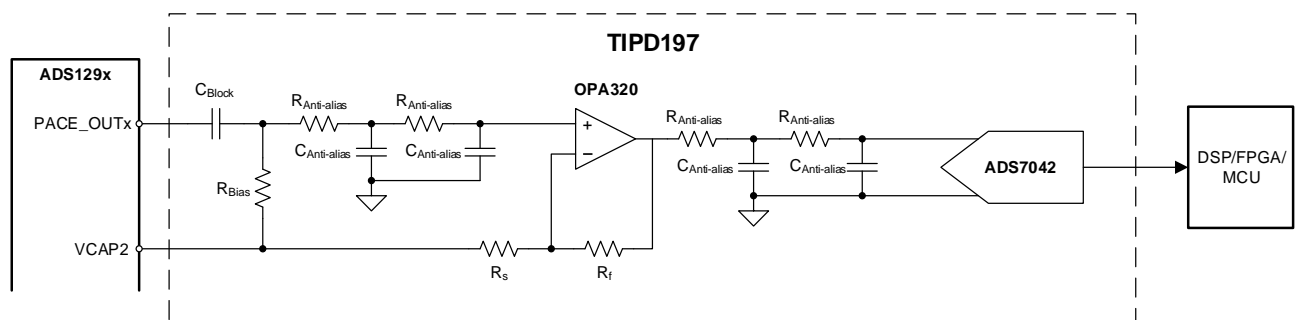


Figure 13: Schematic showing components selected for this design

3.1 ECG Front End

The ADS129x family of devices is a group of integrated low noise ECG front end delta sigma ADCs. They feature up to 8 simultaneous sampling ADC channels with data rates up to 32 kSPS, each with a dedicated programmable-gain amplifier (PGA) with gains as high as 12. Each of the devices also possess two integrated pacemaker detection buffers which output a single-ended version of the analog input signal after being amplified by the PGA. This device provides the first two functional blocks of this design: an ECG front-end differential amplifier provided by the channel configurable PGAs, and a differential to single-ended converter which outputs a signal referred to mid-supply. Channels can individually be routed to the pacemaker buffers through device register settings. The device also has a regulated mid-supply voltage with limited current drive which may be used to bias the pacemaker detection circuit.

The designer may use the ADS129x's low noise simultaneous sampling conversion channels for measuring ECG, providing a right leg drive and a Wilson Central Terminal (WCT) voltage, and use the pacemaker output to detect and/or measure high bandwidth pacemaker signals discretely.

Figure 14 shows a schematic representation of a generic conversion channel's PGA routed to one of the two pacemaker detection buffers. In this schematic, the PGA is configured to have a gain of 6. The PGA is designed to have intentionally low bandwidth which aids in anti-aliasing. To collect the data to verify this design, the PGA gain was set to 12. Note that the pacemaker buffer provides a gain of 0.4.

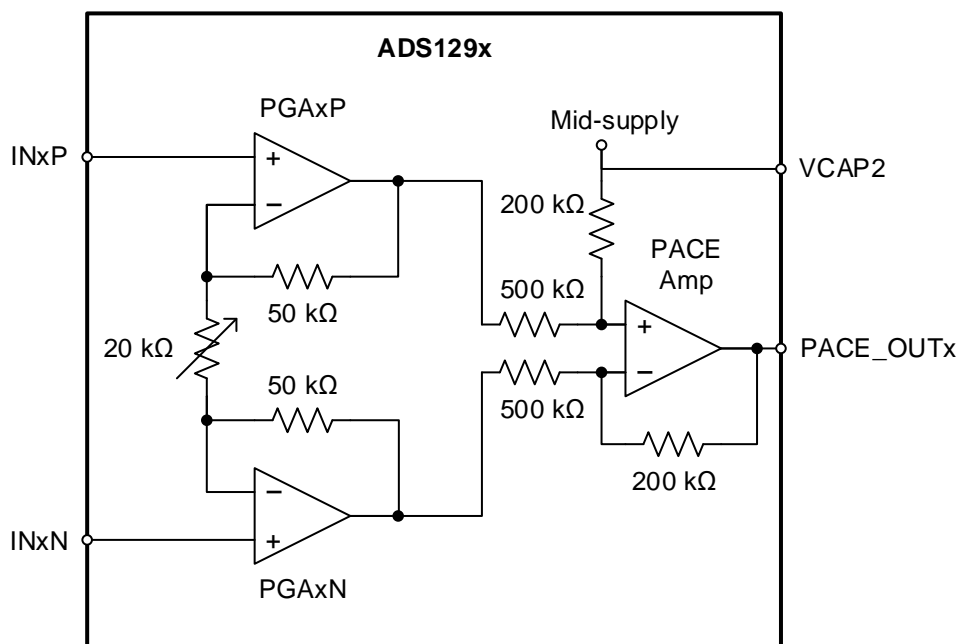


Figure 14: Schematic showing PGA output routed to a pace buffer on the ADS129x

3.2 ADC Input Drive Amplifier

The parameters for choosing the amplifier to drive the ADC for this design are bandwidth, noise, and input bias current. The OPA320 was chosen since it has a gain bandwidth product of 20 MHz which will provide ample bandwidth even for configurations where high gain is needed and/or heavy oversampling is used. The broadband (10 kHz) voltage noise spectral density is especially low: 7 nV/ $\sqrt{\text{Hz}}$. Finally, input bias current is important since offset from rather large anti-aliasing resistors is undesirable. The OPA320 is a CMOS amplifier and has input bias current of ± 0.2 pA.

For the data that was collected to verify this design, the amplifier was configured in the simple buffer scheme since gain was provided by the ADS129x PGA.

3.3 ADC

When selecting a SAR ADC, the primary considerations are resolution and bandwidth. The ADS7042 has a maximum sample rate of 1 MSPS making it flexible for high levels of oversampling. Data was collected with a sample rate of 32 kSPS. The device has 12-bit resolution. It conveniently uses its analog supply as its reference voltage. For this design, an analog supply voltage of 3.3 V was used giving the ADC an LSB voltage of 805.7 μV . The chip's size is notable – it consumes a 2.25 mm² area of board space.

3.4 Passive components

The passive components in this design couple the power supplies for the ICs, anti-aliasing, and AC coupling. Refer to Figure 15 for references to specific components.

The high-pass filter formed by C_{Block} and R_{Bias} were set as $0.18 \mu F$ and $10 M\Omega$, respectively. The cutoff for this filter is less than 1 Hz. The anti-aliasing networks which are formed by combinations of $R_{Anti-alias}$ and $C_{Anti-alias}$ were chosen to be $1.5 k\Omega$ and $1 nF$ in all cases. The capacitor directly in front of the ADC is large enough to supply the input sampling capacitor with the instantaneous charge necessary for precise conversion. This creates a -3 dB point near 45 kHz.

The feedback network surrounding the OPA320 was chosen to be a simple buffer scheme where R_s was depopulated and R_f was installed as a 0Ω resistor. However if gain is needed, the series combination of R_s and R_f should be higher than $100 k\Omega$ since the VCAP2 output has limited drive strength. The supply bypass capacitor for the op amp, C_{OPABYP} , is set to $2.2 \mu F$ as is recommended in that device's datasheet. Both the analog and digital supply bypass capacitors for the ADS7042, C_{ADCBYP} , were selected to be $1 \mu F$ as recommended by the datasheet.

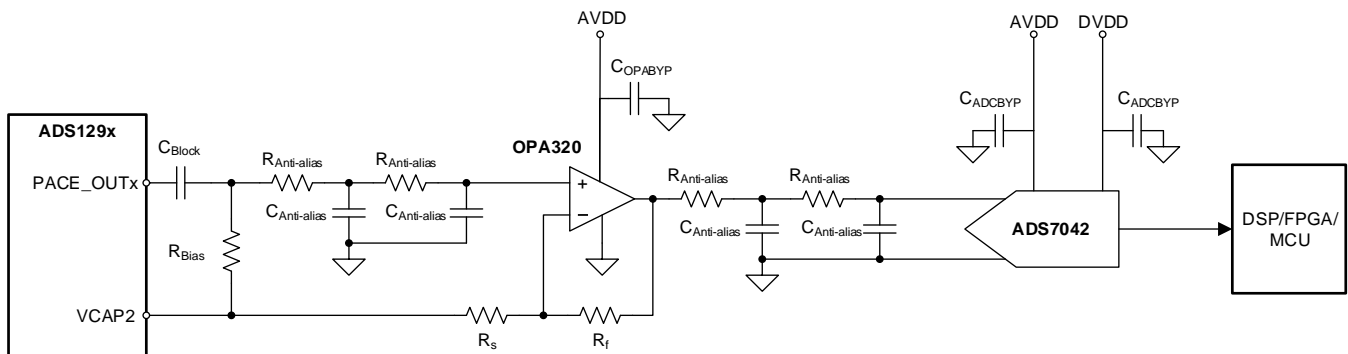


Figure 15: Schematic diagram identifying passive components

4 Simulation

Simulation was performed using TINA-TI. Figure 16 shows the simulation schematic of the circuit. All op amps used in the circuit are “ideal op amps”. This is acceptable for the pace buffer IOP3 and the OPA320 since the bandwidth of those amplifiers well exceeds the signal band. The PGA’s frequency response had to be approximated using RC filters formed by R_{13} , R_{14} , C_1 , and C_2 . Since additional components were placed, they had to be buffered by IOP5 and IOP6 to prevent them from interacting with the pace buffer. The PGA gain-setting resistor R_2 was set to $9.09 k\Omega$ to give the PGA a gain of 12. The input is provided with respect to $1.65 V$ without a DC offset for simplicity, but that does not have to be the case.

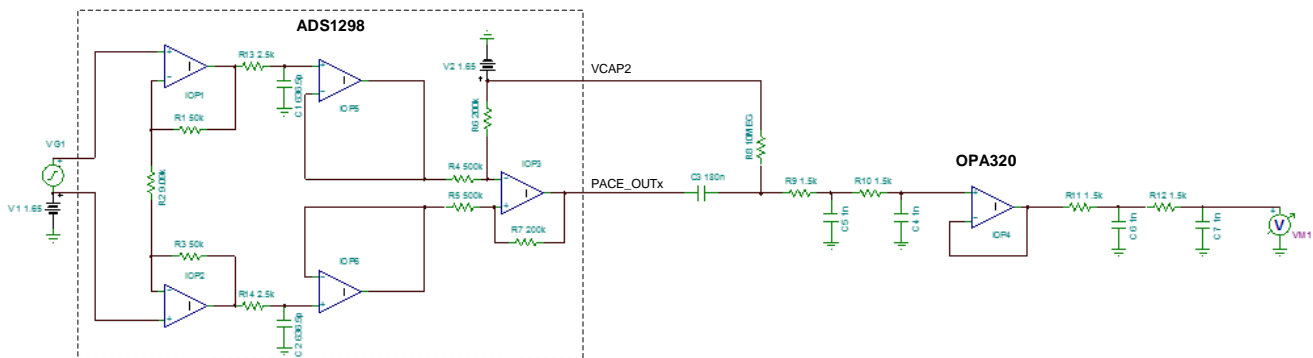


Figure 16: TINA-TI simulation schematic

The AC magnitude characteristics were simulated and are plotted in Figure 17. As expected the passband gain of the circuit is 13.53 dB which corresponds approximately to the PGA and pace buffer total gain. The -3 dB frequency simulates to be close to 25 kHz. The effect of the high pass filter can be seen at very low frequencies where the magnitude begins to decrease.

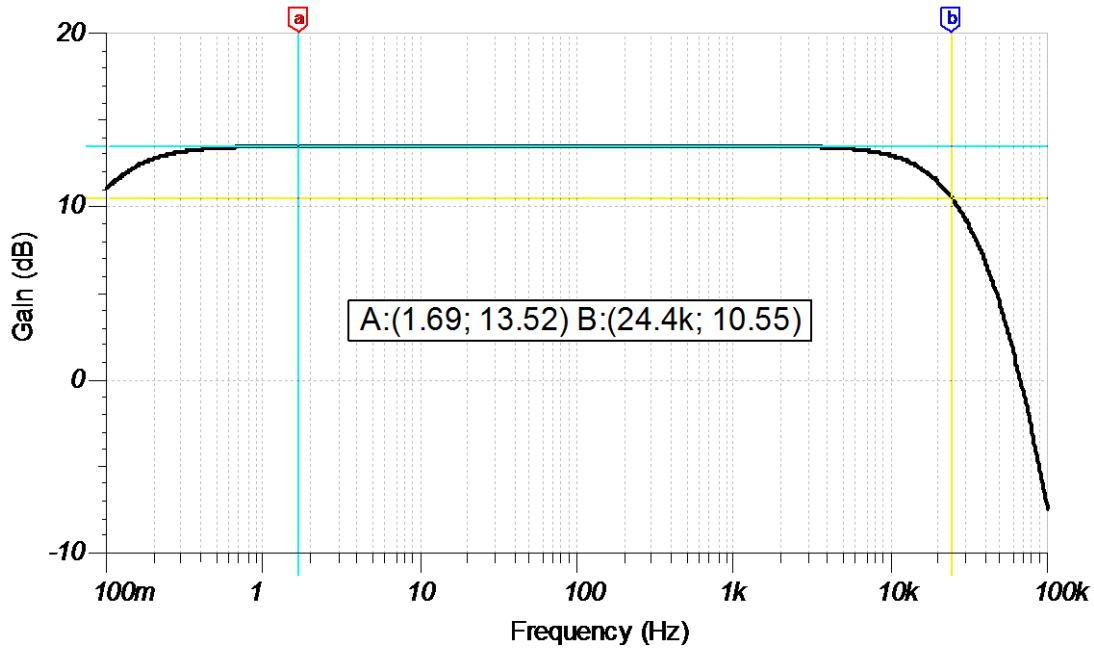


Figure 17: Simulation circuit frequency magnitude response

Finally, the transient response to a 2 mV, 500 μ s pulse was simulated to approximate a small pacemaker signal. It is clear that the pulse propagates to the output recognizably with final amplitude of 9.5 mV (very close to the ideal 9.6 mV) as indicated by the cursors. Note that the output settles to 1.65 V, which is the mid-supply voltage.

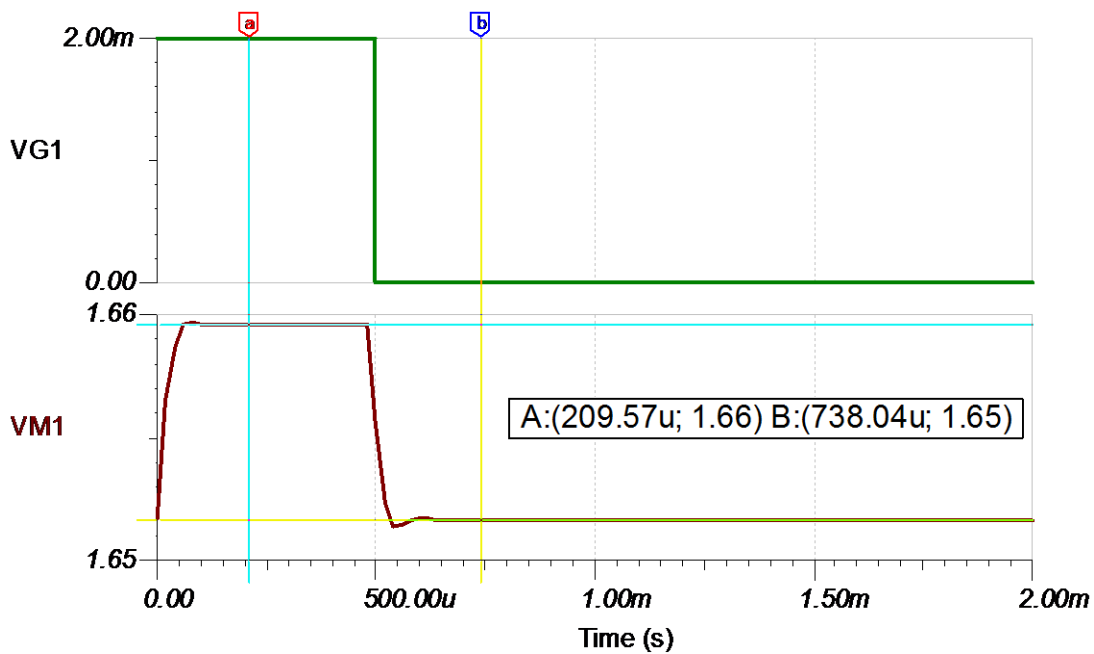


Figure 18: Simulation of pacemaker pulse

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

Place bypass capacitors as close to the ICs as possible to optimize decoupling. This is especially important for the ADS7042 since its supplies also serve as its reference voltage. Allow sufficient room for current to travel to and from board supplies by using wide traces and inserting pours where possible.

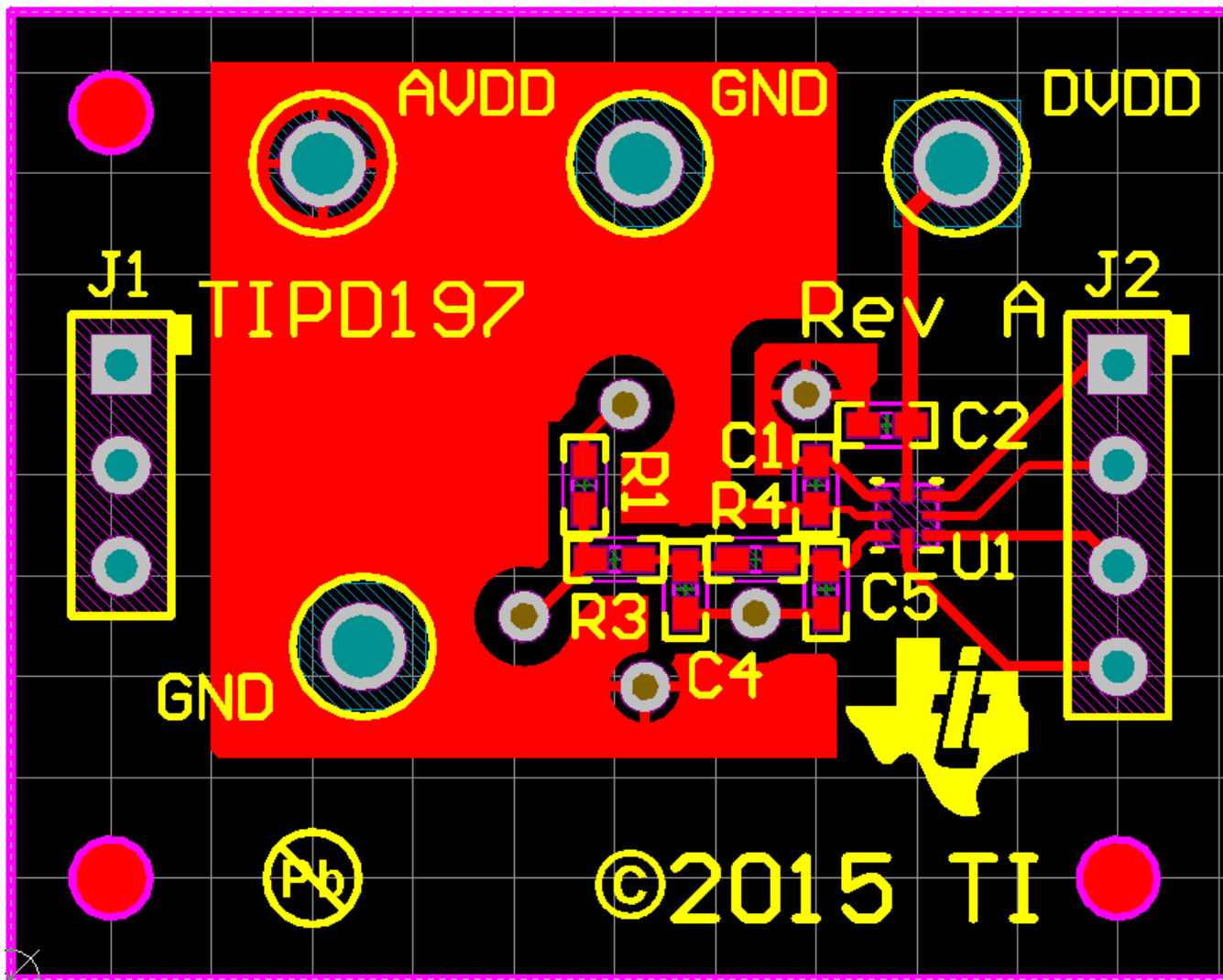


Figure 19: Top

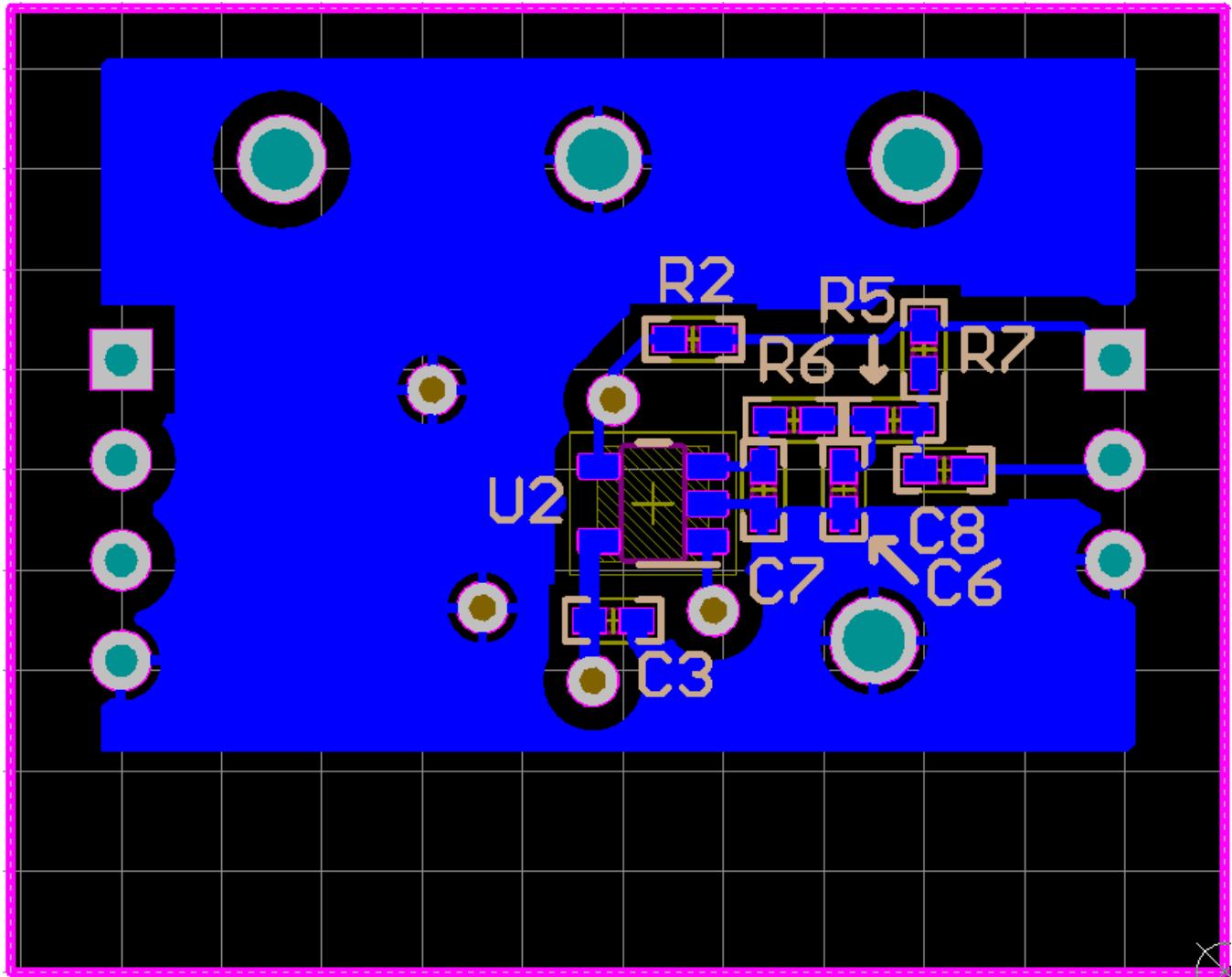


Figure 20: Bottom

6 Verification & Measured Performance

A board was assembled and tested to validate functionality and prove viability. ECG waveforms were generated a patient simulator and input to the ADS1298RECGFE-PDK. The ADS1298R was configured to have a PGA gain of 12 and to route channel 3 (corresponding to ECG Lead II) to the PACEO buffer by assigning bits [2:1] of the PACE register on the ADS1298R to 01. The signal was subsequently taken from the TEST_PACE_OUT2 pin and connected to the PACEOUT input on the TIPD197 board. The VCAP2 output voltage was blue wired from the ADS1298RECGFE-PDK board to the VCAP2 input on the TIPD197 board.

Data was collected by connecting the SPI pins on the design board to the SPI connectors on a modified ADS7042EVM-PDK board and leveraging the existing firmware and software for that EVM. Data was collected at a rate of 32 kSPS. The filtering described here was performed after all the samples for a given collection were obtained.

The figures below show conversion data of pacemaker signals collected in the boundary amplitude/width scenarios. The pulse was very easy to identify in scenarios where the magnitude was near the upper limit so that data is not shown. Data was passed through the digital high pass filter described in Equation (10) (using a 64-bit floating-point unit) to show that a strong detection algorithm can make identification simpler. In each case the y-axis is given in the output referred voltage to reflect what data is actually obtained by the processor.

$$y[n] - 0.99y[n - 1] = x[n] - x[n - 1] \tag{10}$$

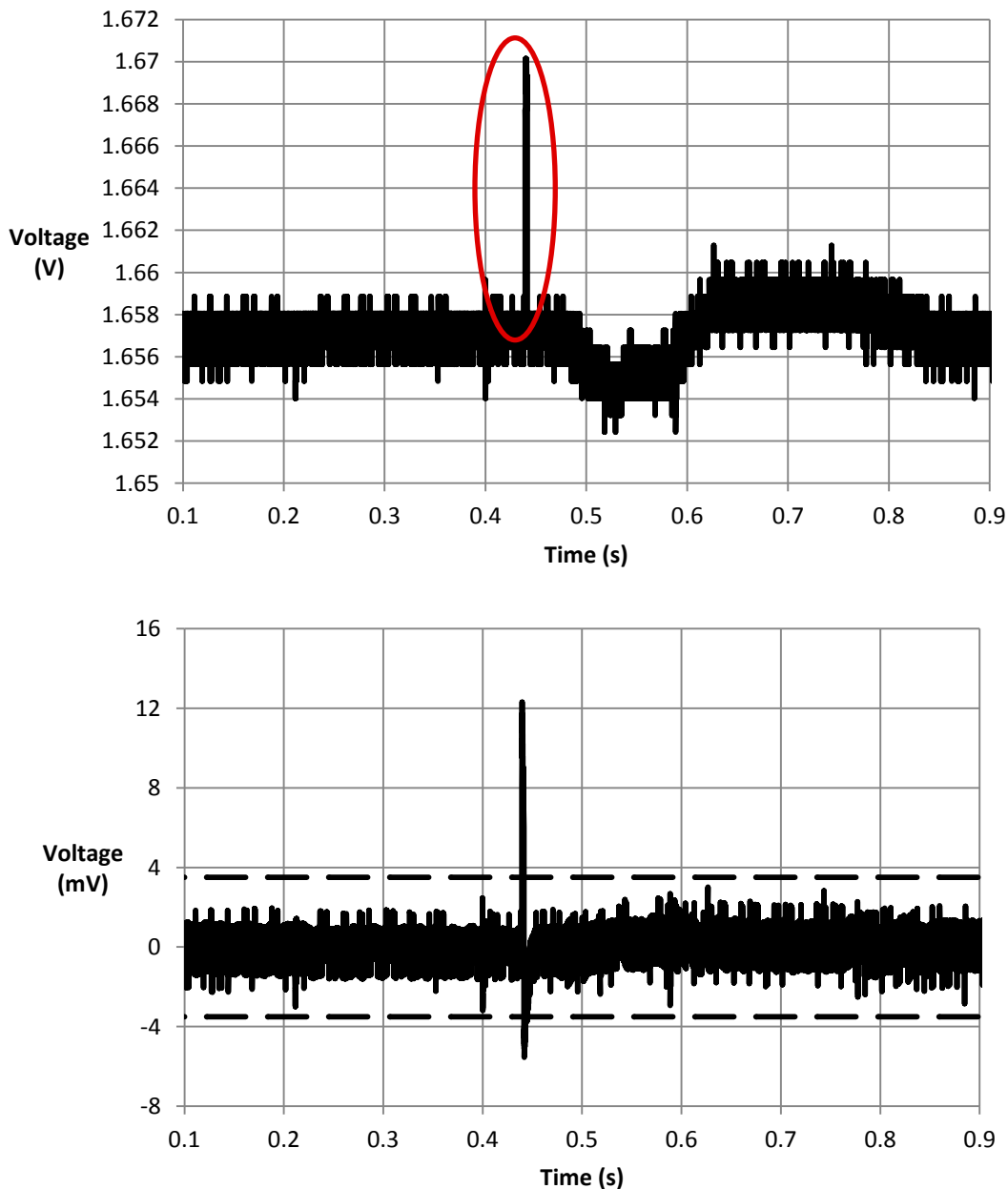


Figure 21: 2 mV, 2 ms pulse raw (top), filtered with threshold indicators (bottom)

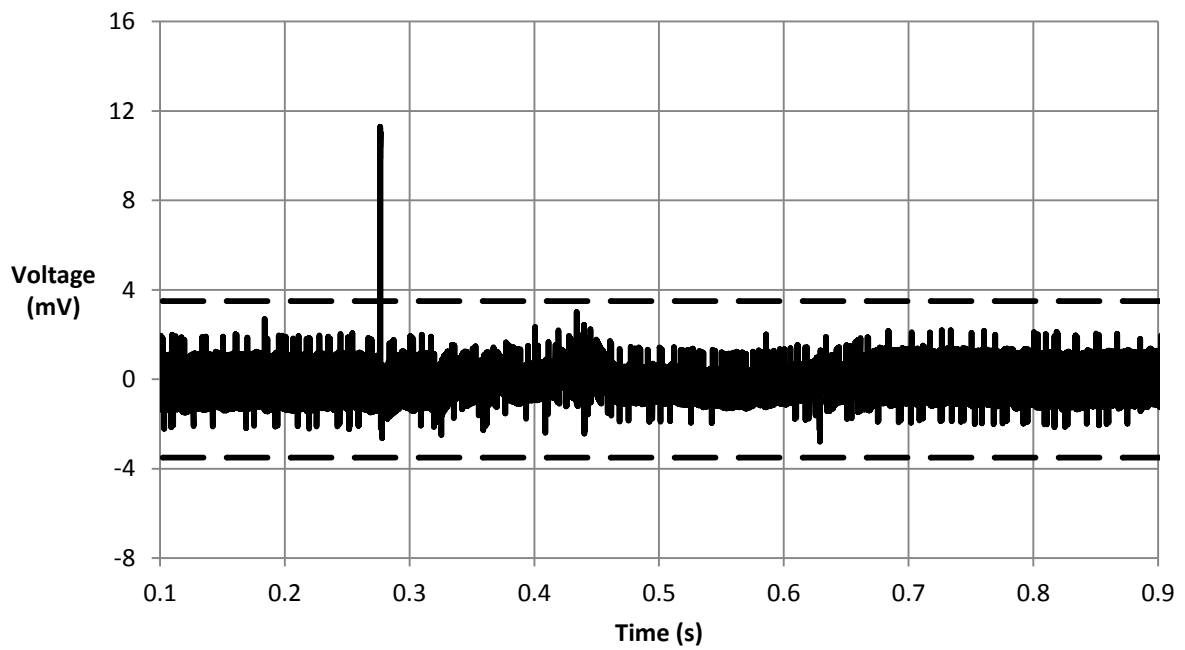
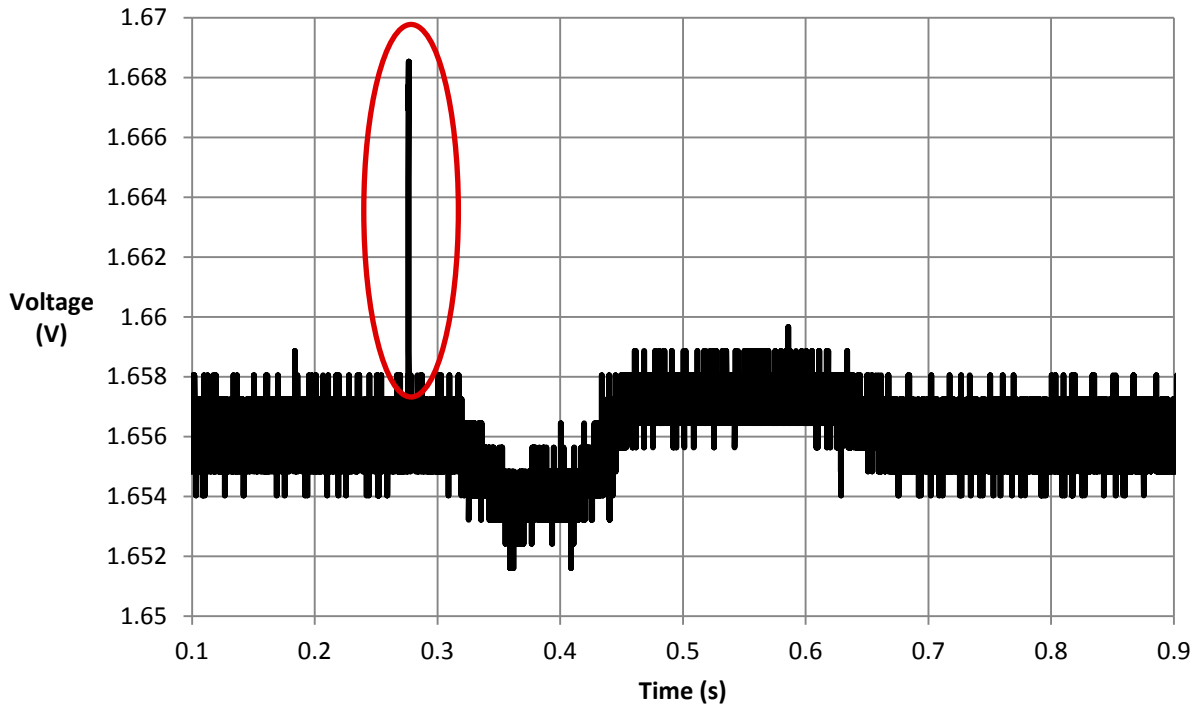


Figure 22: 2 mV, 0.5 ms pulse raw (top), filtered (bottom)

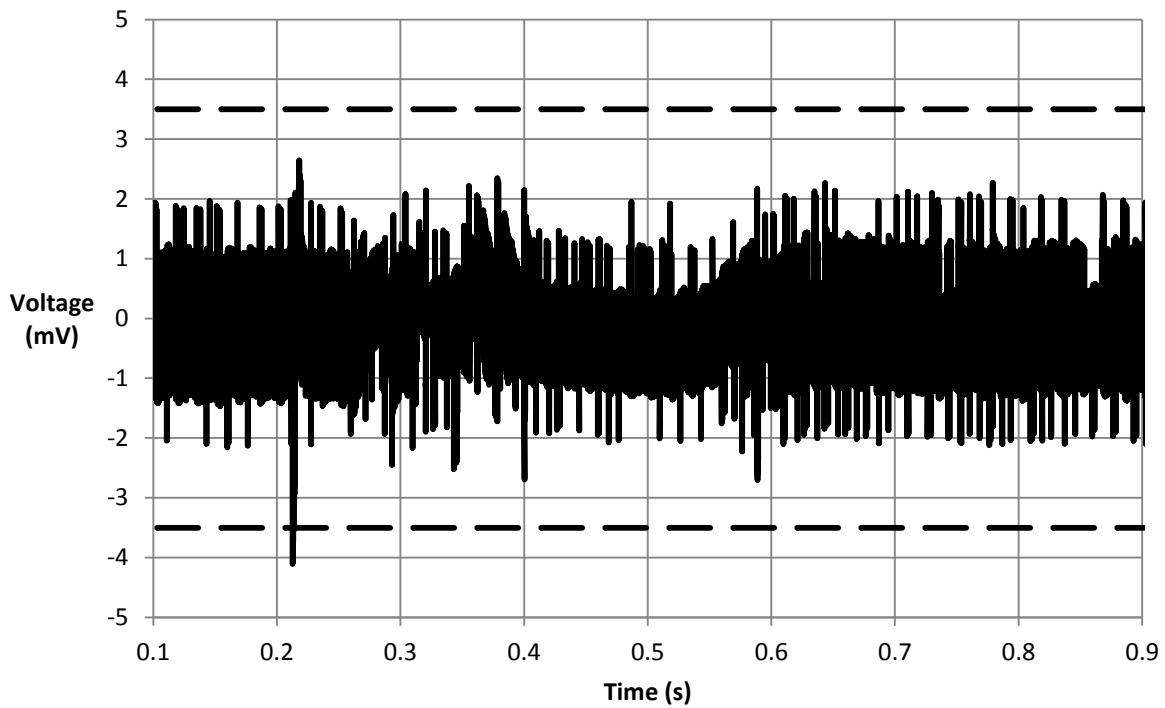
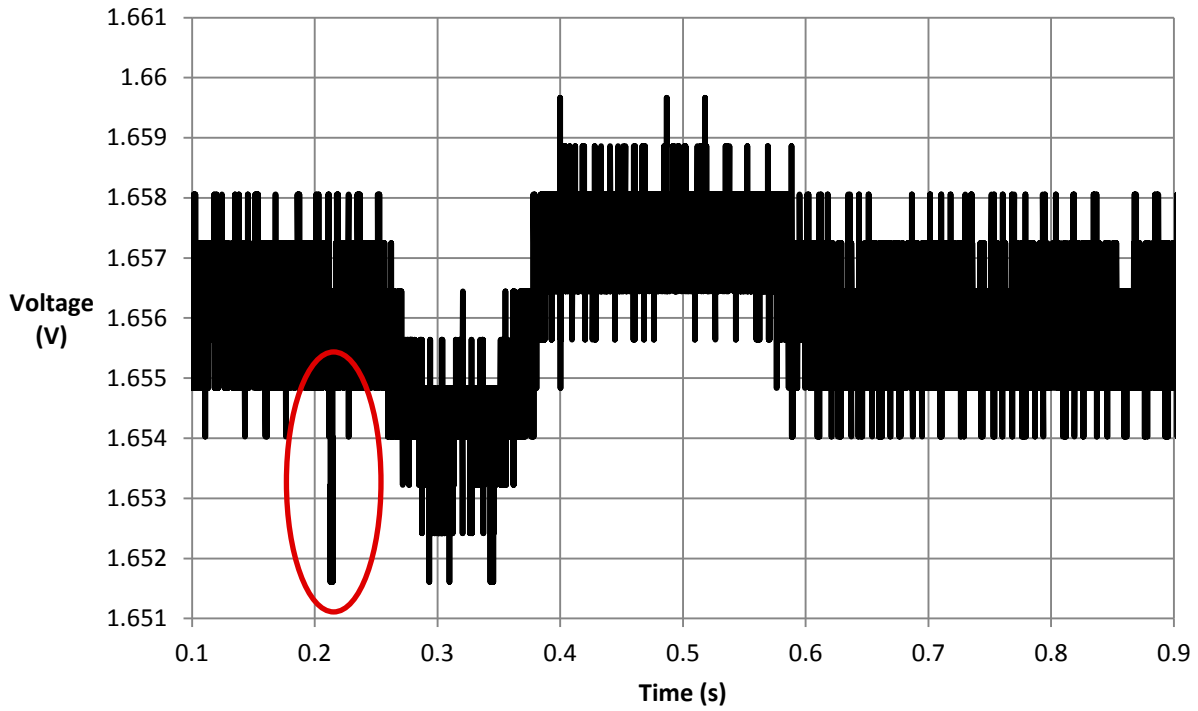


Figure 23: -2 mV, 2 ms pulse raw (top), filtered (bottom)

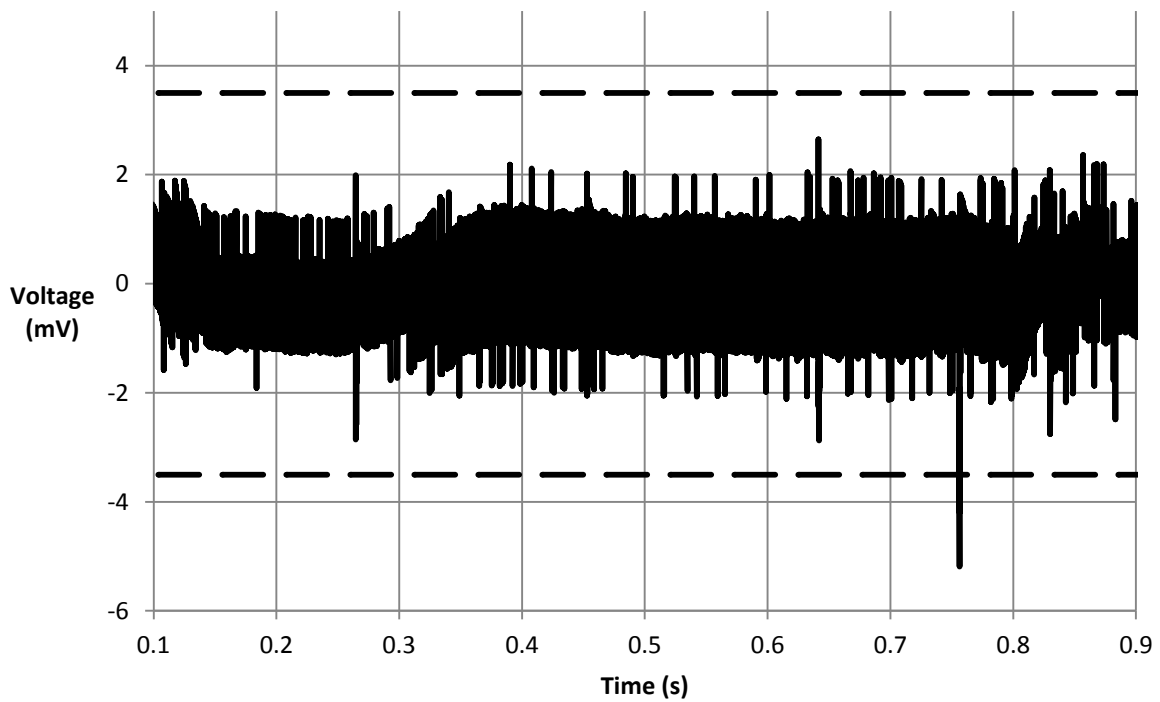
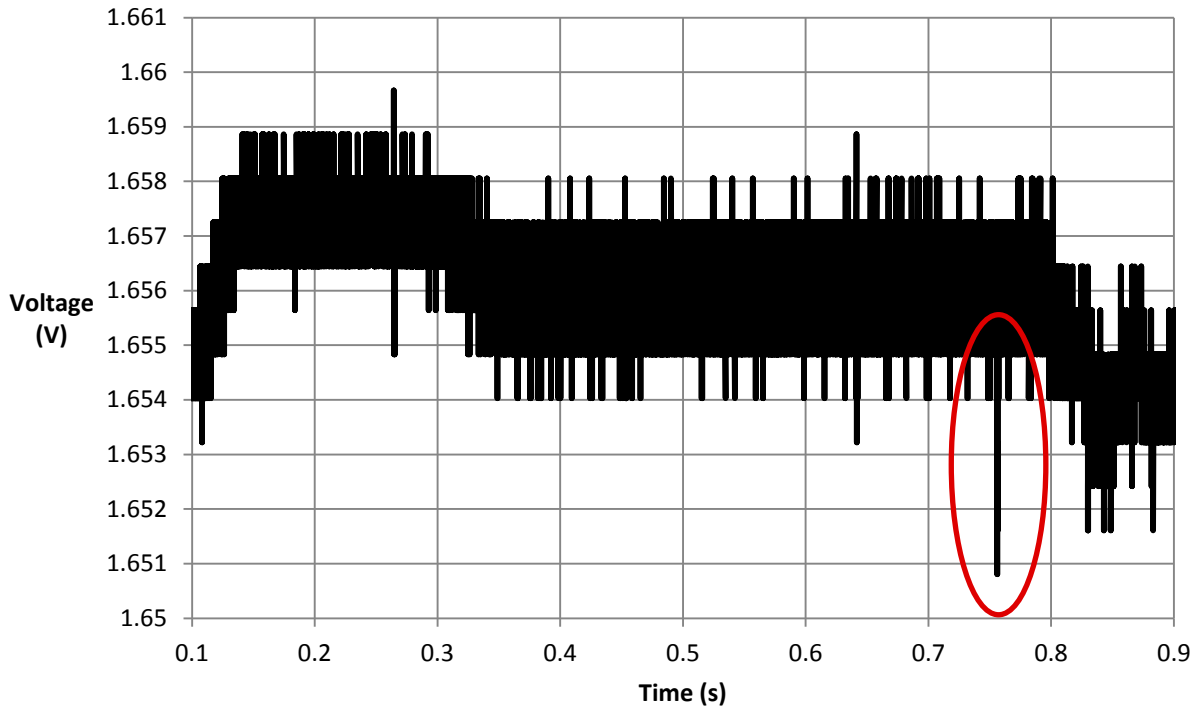


Figure 24: - 2 mV, 0.5 ms pulse raw (top), filtered (bottom)

7 Modifications

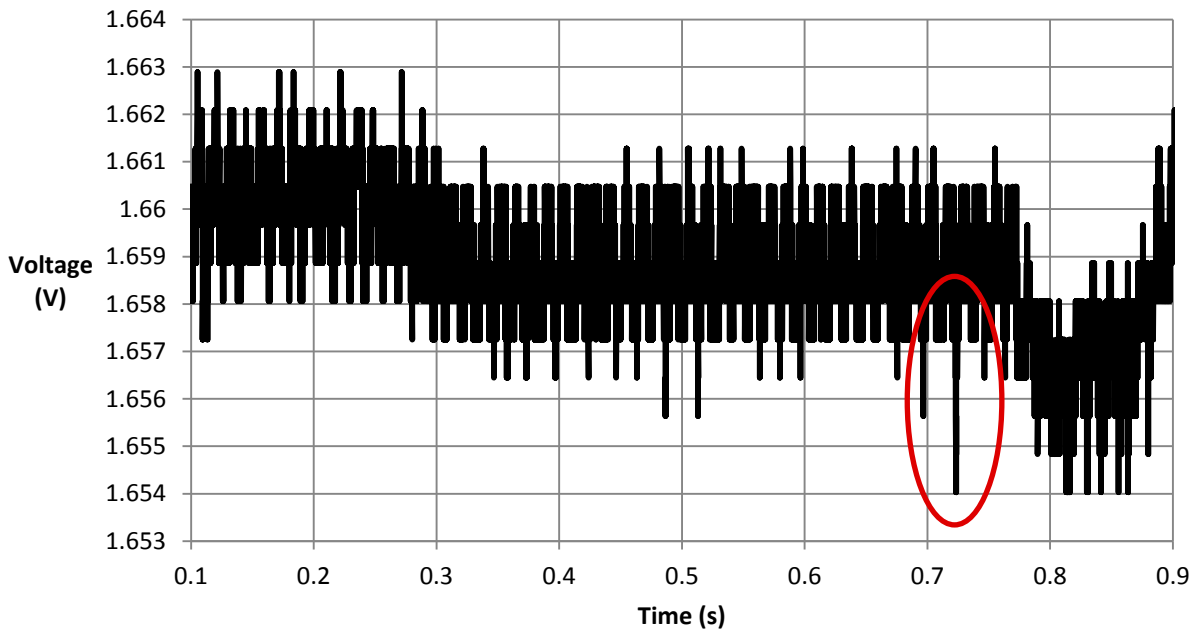
Key hardware modifications which can change the performance or operation of the system are related to the passive components. The anti-aliasing filter may be adjusted in to decrease the wide-band noise level. In some cases, electrode offset will reduce flexibility with the ADS129x PGA gain. In that case it makes sense to increase the gain of the OPA320 using Equation (5).

If there is noise created by some other source present in the system, the anti-aliasing requirement may not be as straightforward as it was described above. This design allows for heavy oversampling and digital low pass filtering to effectively eliminating out of band noise close to the pacemaker's bandwidth.

The designer may also want to use the ADS129xR to measure respiration rate. This feature works by sourcing a 32 kHz or 64 kHz square wave excitation signal to the body to measure body impedance. This signal will exist as an artifact in this pacemaker design. Such a scenario was studied using a 2 kΩ Lead I body impedance simulated using a patient simulator and using the 32 kHz internally generated excitation signal on the ADS1298R.

The strategy for mitigating the effect was to sample at nearly the same frequency as the excitation signal so that it would alias close to dc and would be removed by the digital high pass filter. This can theoretically be the case as long as collection for the pacemaker detection is performed at or near some integer divisor frequency of the excitation signal frequency.

Figure 25 shows a ventricular pacer with an amplitude of -2 mV with a width of 0.5 ms in the presence of the respiration measurement excitation signal – what can be considered to be the worst case. The pulse can be clearly identified and detected from the filtered output without any special consideration.



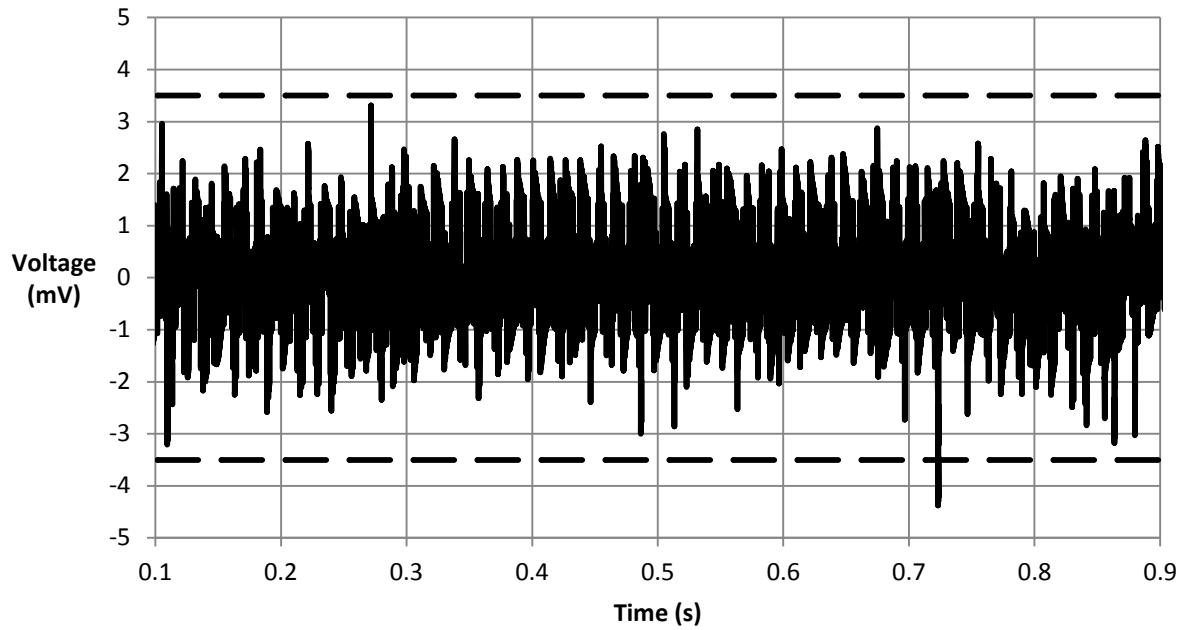


Figure 25: -2 mV, 0.5 ms pulse with respiration excitation signal present raw (top), filtered (bottom)

8 About the Author

Brian Pisani is an applications engineer located in Dallas, Texas specializing in delta-sigma ADCs with a particular interest in digital signal processing. He received his B.S. Electrical Engineering from the University of Wisconsin-Madison.

Appendix A.

A.1 Electrical Schematic

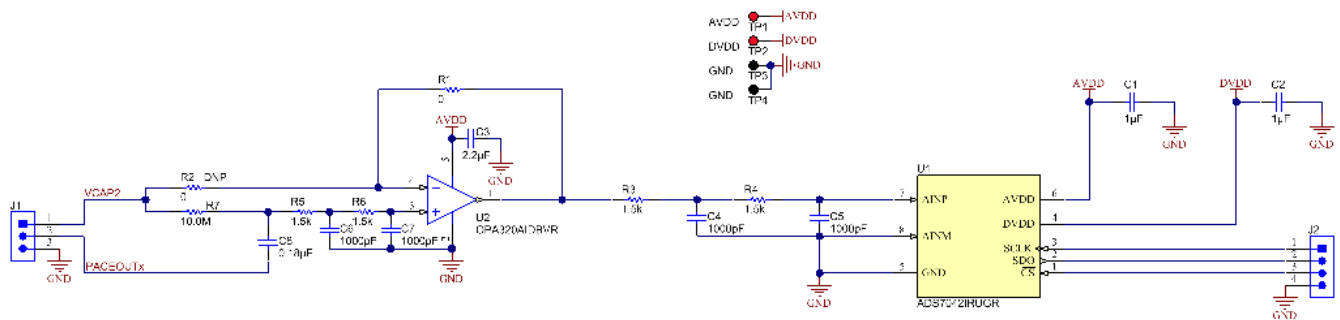


Figure A-1: Electrical Schematic

A.2 Bill of Materials

| Item # | Quantity | Designator | Description | Manufacturer |
|--------|----------|----------------|--|-------------------|
| 1 | 2 | C1, C2 | CAP, CERM, 1 μF, 10 V, +/- 10%, X5R, 0402 | TDK |
| 2 | 1 | C3 | CAP, CERM, 2.2 μF, 10 V, +/- 10%, X5R, 0402 | TDK |
| 3 | 2 | C4, C5 | CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0402 | MuRata |
| 4 | 2 | C6, C7 | CAP, CERM, 1000 pF, 25 V, +/- 5%, C0G/NP0, 0402 | TDK |
| 5 | 1 | C8 | CAP, CERM, 0.18 μF, 10 V, +/- 10%, X5R, 0402 | MuRata |
| 6 | 1 | J1 | Header, 100mil, 3x1, TH | Mill-Max |
| 7 | 1 | J2 | Header, 100mil, 4x1, TH | Mill-Max |
| 8 | 1 | R1 | RES, 0, 5%, 0.063 W, 0402 | Panasonic |
| 9 | 1 | R2 | RES, 0, 5%, 0.063 W, 0402 | Vishay-Dale |
| 10 | 4 | R3, R4, R5, R6 | RES, 1.5 k, 5%, 0.063 W, 0402 | Vishay-Dale |
| 11 | 1 | R7 | RES, 10.0 M, 1%, 0.063 W, 0402 | Vishay-Dale |
| 12 | 1 | TP1 | Test Point, Multipurpose, Red | Keystone |
| 13 | 1 | TP2 | Test Point, Multipurpose, Red | Keystone |
| 14 | 2 | TP3, TP4 | Test Point, Multipurpose, Black | Keystone |
| 15 | 1 | U1 | Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC | Texas Instruments |
| 16 | 1 | U2 | Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier | Texas Instruments |

Figure A-2: Bill of Materials

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