TI Designs

Single-Chip, Loop-Powered 4- to 20-mA RTD Sensor Transmitter

TI Designs

This reference design is a single-chip solution for a two-wire, 4- to 20-mA loop-powered system including a four-wire RTD analog front end. The built-in processor enables the use of compensation algorithms, which increases the system performance. The design is ideally suited for applications with space constraints and operates at high ambient temperatures with a low power performance.

Design Resources

TIDA-00851	Tool Folder Containing Design Files
PGA900	Product Folder
PGA900EVM	Tool Folder

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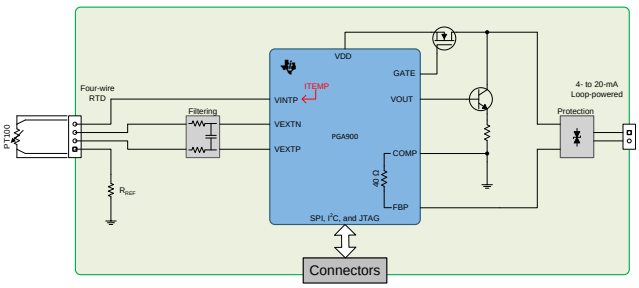
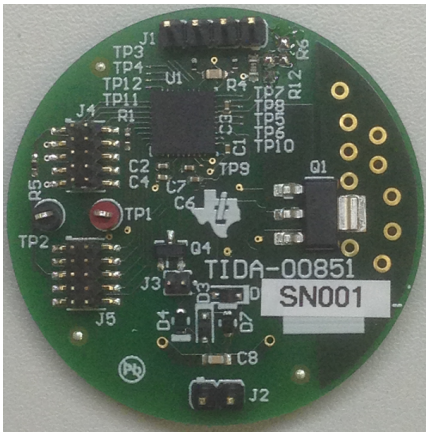
Design Features

- Single-Chip Solution
- Four-Wire RTD Sensors (PT100)
- Loop-Powered 4- to 20-mA Current Interface
- Current Consumption: 1.7 mA
- Ambient Temperature: –40ºC to 150ºC
- Designed to Meet Following Specifications:
  - IEC 61000-4-2
  - IEC 61000-4-4
  - IEC 61000-4-5

Featured Applications

- Sensors and Field Transmitters
- Factory Automation and Process Control
- Building Automation





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS AND FEATURES
Sensor type	Four-wire PT100 probe
Temperature range of RTD sensor	–200°C to 850°C
Output signal	Two-wire, 4- to 20-mA current loop
Power supply voltage range	10 V to 36 V
Current consumption	< 3 mA
Reverse polarity protection	Yes, on power input
Operating temperature	–40°C to +150°C
Form factor	4-cm diameter circular shape

2 System Description

The objective of this reference design is to realize a low-power, single-chip, two-wire, loop-powered, 4- to 20-mA current-output, resistance-temperature detecting (RTD) transmitter. The design focuses on a four-wire PT100 implementation for the analog front end (AFE) and a 4- to 20-mA loop-powered interface with a flexible loop supply voltage. A single device handles the analog front end, temperature calculation, appropriate loop current setting, and power supply. Additional protection circuitry has been used to protect against reverse polarity and has been designed to meet IEC 61000-4 standards.

3 Block Diagram

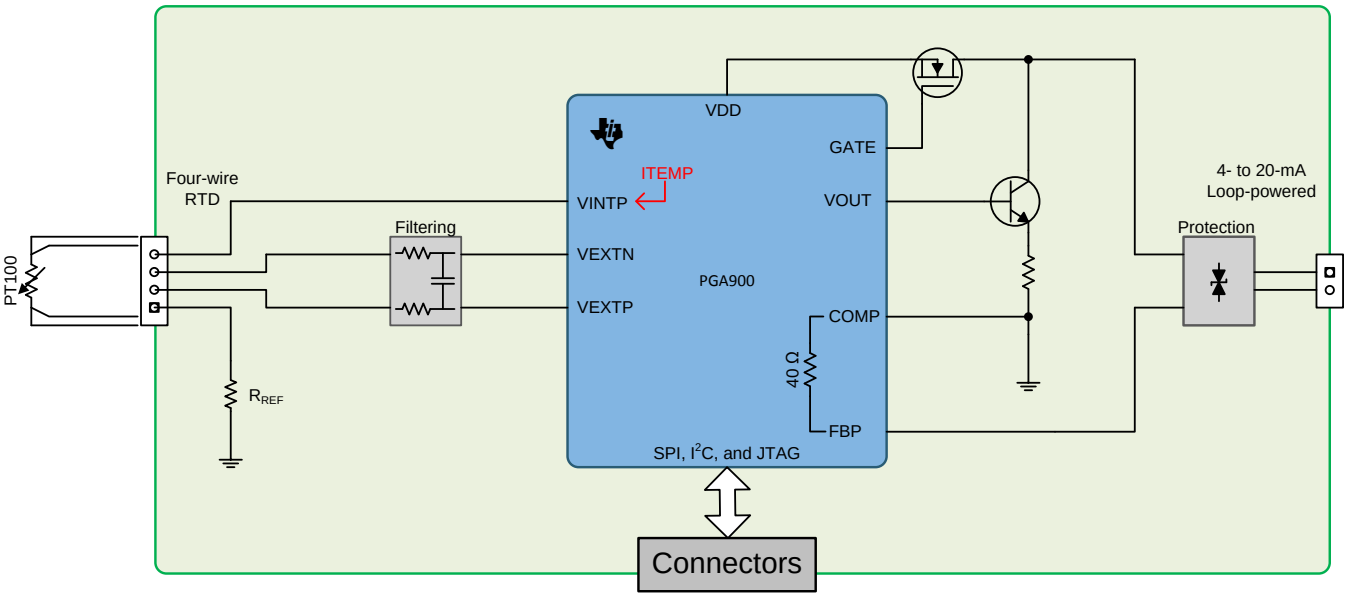

Figure 1. TIDA-00851 Block Diagram

4 Highlighted Products

4.1 PGA900

Description

The PGA900 is a signal conditioner for resistive sensing applications. The device can accommodate various sensing element types. The PGA900 conditions its input signals by amplification and digitization through two analog front-end channels. With the user programmed software in the on-chip ARM® Cortex®-M0 processor, the PGA900 can perform linearization, temperature compensation, and other user-defined compensation algorithms. The conditioned signal can be output as ratiometric voltage, absolute voltage, 4- to 20-mA current loop, or pulse width modulation (PWM). The data and configuration registers can also be accessed through serial peripheral interface (SPI), I^2C, universal asynchronous receiver/transmitter (UART), and two general purpose input/output (GPIO) ports. In addition, the unique one-wire interface (OWI) allows communication and configuration through the power supply pin without using additional lines. The PGA900 operating voltage is from 3.3 V to 30 V and it can operate in temperatures from –40°C to 150°C.

Features

- High-accuracy, low-noise, low-power, small-size, resistive-sensing signal conditioner
- User-programmable temperature and nonlinearity compensation
- On-chip ARM® Cortex®-M0 microprocessor allows users to develop and implement calibration software
- One-wire interface enables the communication through power supply pin without using additional lines
- On-chip power management accepts wide power supply voltage from 3.3 V to 30 V
- Operating temperature range: –40°C to 150°C
- Memory
  - 8-KB software memory
  - 128-byte EEPROM
  - 1-KB data SRAM
- Accommodates sensor sensitivities from 1 mV/V to 135 mV/V
- Two individual analog front end (AFE) chains, each including:
  - Low-noise programmable gain amplifier (PGA)
  - 24-bit $\Delta\sum$ analog-to-digital converter (ADC)
- Built-in internal temperature sensor with option to use external temperature sensor
- 14-bit digital-to-analog converter (DAC) with PGA
- Output options:
  - Ratiometric and absolute voltage output
  - 4- to 20-mA current loop interface
  - One-wire interface (OWI) over power line
  - PWM output
  - SPI
  - Inter-integrated circuit (I^2C)
- Depletion MOSFET gate driver
- Diagnostic functions

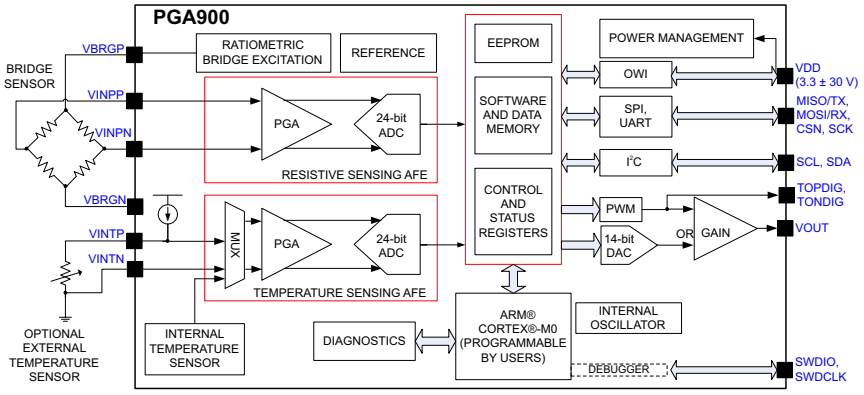

Figure 2. PGA900 Block Diagram

5 System Design Theory

The main component in this design is the PGA900. This design only uses the so-called “T channel” (from the two available signal chains) to minimize the current consumption allowed by switching off the “P channel".

5.1 RTD Front End

Figure 3 shows a schematic of the front end. The PT100 sensor can be connected to J1. Port VINTP provides a constant current (I_{TEMP}) from the PGA900. The device is able to provide different levels of current. In this design, the constant current has been set to I_{TEMP} = 100 µA. Ports VEXTP and VEXTN are the actual inputs to the PGA900 T channel. R4 is a reference resistor, which can be used to bring the common-mode input of the programmable gain amplifier (PGA) to its compliance voltage range (see Equation 1).

$$V_{CM} = R4 \times I_{TEMP} = 4.99\ k\Omega \times 100\ \mu A = 0.499\ V \quad (1)$$

A PT100 sensor covers a temperature range from –200°C to 850°C, which corresponds to 18.52 Ω to 390.481 Ω according to the Callendar-Van-Dusen equation [1].

Equation 2 and Equation 3 show that a constant current of I_{TEMP} = 100 µA results in a voltage span of:

$$V_{PT100\_MIN} = R_{PT100\_MIN} \times I_{TEMP} = 18.52\ k\Omega \times 100\ \mu A = 1.852\ V \quad (2)$$

$$V_{PT100\_MAX} = R_{PT100\_MAX} \times I_{TEMP} = 390.481\ \Omega \times 100\ \mu A = 39.0481\ mV \quad (3)$$

The input stage basically has a common-mode voltage of approximately 0.5 V, on which the PT100 voltage changes by a maximum of approximately 40 mV.

The T channel of the PGA900 has fewer gain settings for the built-in PGA as compared to the P channel. For the application in this design, choose the maximum gain setting of the T channel: Gain = 20 V/V.

This setting results in the following maximum ADC input voltage in Equation 4:

$$V_{IN\_ADC} = 40\ mV \times 20\ V/V = 800\ mV \quad (4)$$

In the standard configuration, R12 is not populated (DNP). PGA900 uses its internal reference voltage of 2.5 V. In this case, the voltage generated by R4 × I_{TEMP} does not provide the ADC reference, thus the calculation of PT100 is not in relation to R4. The calculation of the PT100 value depends on the actual value of I_{TEMP}, as Equation 5 shows:

$$R_{PT100} = \frac{V_{PT100}}{I_{TEMP}} = \frac{ADC_{CODE} \ / \ 2^{BIT-1} \times V_{REF} \ / \ Gain}{I_{TEMP}} = \frac{ADC_{CODE}}{2^{23}} \times \frac{2.5\ V}{20\ V/V \times 100\ \mu A} \quad (5)$$

Measure the actual current I_{TEMP} with an external digital multimeter (DMM) for better accuracy. Because the PGA900 has a second channel, the voltage drop across R4 can also be measured. If using the second channel, R4 should be a precise resistor with low drift over temperature.

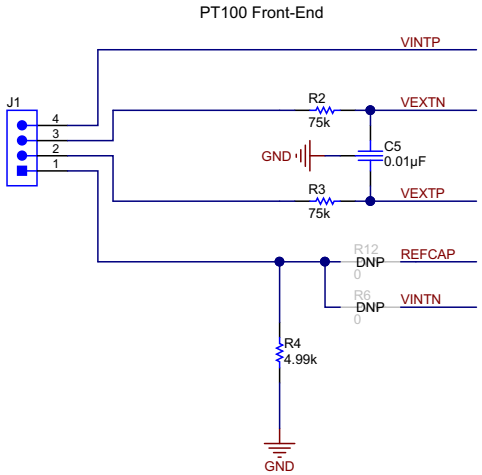

Figure 3. PT100 Front End

5.2 Current Loop (4 mA to 20 mA)

The PGA900 also has a DAC output, which sets the current in the loop. The temperature range of the RTD from –200°C to 850°C is mapped to a current range from 4 mA to 20 mA in a linear fashion.

Consult the *PGA900 as 4- to 20-mA Current Loop Transmitter* application report for a detailed description on how the 4- to 20-mA current loop works with the PGA900 [2].

The loop current can be calculated as shown in Equation 6:

$$I_{LOOP} = 1001 \times \frac{1.25\ V}{40\ k\Omega} \times \frac{DAC_{CODE}}{0x3FFF} \quad (6)$$

5.3 MCU Calculations

Several methods exist to calculate the corresponding temperature. This design uses a look-up table to derive the equivalent temperature. Making the calculation requires knowing the absolute value of V_{REF} = 2.5 V, as well as the constant current I_{TEMP}. Use either the nominal values of these variables, or for more precise results, measure them. The software then maps the minimum temperature to the DAC code representing 4 mA and the maximum temperature value is mapped to 20 mA.

The build in this MCU can utilize additional features, such as offset and gain compensation or correction algorithms.

5.4 Protection

5.4.1 Protection for IEC61000-4

The input overvoltage protection of this design protects all blocks and components of the transmitter that can be considered to have a direct connection to the loop. Figure 4 shows a schematic of the input protection.

The nominal maximum input voltage expected is provided either by dedicated modules of the programmable logic controller (PLC) or by a separate (DIN-rail) power supply. Possible overvoltage events are mainly transients and overvoltage pulses, which can be caused by the following events:

- Supply voltage overshoot during power up of the power supply
- The presence of coupling and crosstalk between the loop cable and adjacent cables with large voltage or current transients on these adjacent cables
- Surge, burst, or electrostatic discharge (ESD) pulses leading to differential mode voltages (such pulses are used, for example, in EMC compliance testing during the approval procedure of the complete transmitter)

Out of these transients, the most critical pulse (according to the EN 61000-4-5 standard) is the 8/20-µs surge pulse, coupled through a total resistance of 42 Ω and through a coupling capacitor of 0.5 µF differentially into the loop input. This power design has been created with the intention of handling this critical surge pulse.

A bidirectional transient-voltage-suppression (TVS) diode (D6) and a ceramic capacitor (C8) are used to clamp any overvoltage transient on the loop input terminal J2 to a safe voltage level that is independent of the transient voltages polarity. This overvoltage clamping provides a safe voltage level to the bipolar junction transistor (BJT) controlled by the 4- to 20-mA DAC inside the transmitter electronics.

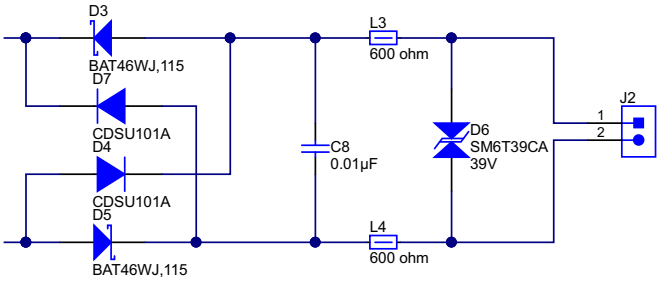

Figure 4. Input Protection

5.4.2 TVS Diode Selection D6

To choose the appropriate TVS diode for this design, be sure to satisfy the following requirements:

1. The TVS standoff voltage V_{RM}, which is the voltage where the TVS does not conduct, must be higher than the maximum nominal loop-input voltage to prevent the TVS from conducting during normal operation. The “does not conduct” condition can be considered to be fulfilled for most projects and applications if the leakage current I_{RM} of the TVS at the given V_{RM} is less than 100 µA. However, the leakage current inside the protection block is not recognized by the DAC current loop control, but adds to the loop current experienced by the loop receiver, which causes an error. To bypass this error, this design targets a leakage current much less than 3 µA. Because the leakage currents usually grow with increased temperature, the I_{RM} specification of the TVS must be given not only at the maximum nominal loop-input voltage, but also at the maximum operating temperature of the design.
2. The TVS peak current and peak pulse power specifications must be higher than the surge current and pulse power under the design-specific conditions. Most of the TVS diode manufacturers specify the device with respect to a 10/1000-µs double-exponential test pulse; however, the pulse used for surge test according to EN 61000-4-5 is an 8/20-µs pulse. Ideally, TVS manufacturers provide the specification for this shorter pulse, as well. If the specification has not been provided, the ’peak pulse power versus pulse time’ graph must be used, which shows how the peak pulse power of the TVS is affected by shorter or longer pulse durations. For shorter pulse widths, the TVS can withstand a higher-peak pulse power. Locate the peak-pulse power versus pulse time graph in the respective TVS diode datasheet.
3. When the TVS conducts and becomes low impedance to clamp the voltage at a safe level, the TVS clamping voltage (V_{CL}) at the specific peak pulse current (I_{PP}) and the V_{CL} at the maximum operating temperature of the design must be lower than the maximum recommended operating voltage of the circuits connected to that voltage.

The TVS selected for this design is an SM6T39CA, which fulfils the following three requirements:

1. I_{RM} (max): 1 µA at V_{RM} = 33.3 V at 85°C
   I_{RM} (max): 0.2 µA at V_{RM} = 33.3 V at 25°C
2. The data sheet specifications for the 8/20-µs pulse are as follows:
   I^{PP} (max): 57 A
   P_{PP} (max): 4 kW
   Both parameters are much higher than the application specific values:
   I_{PP}: approximately 22.6 A
3. V_{CL} (max at 100°C) is approximately 55 V

5.4.3 Selection of Input Capacitor C8

To bypass the higher-frequency transient voltages caused by burst or ESD, a 10-nF ceramic X7R capacitor was selected. With the 100-V DC voltage rating of the capacitor, the device matches the clamping voltage of the TVS with plenty of margin.

5.4.4 Reverse Input Protection

The reverse input voltage protection enables a transmitter to withstand operation at reverse input voltage conditions on the loop input (J2). Examples of such conditions are as follows:

- Interchange of the two wires at the loop input terminals because of miswiring (interchange can last continuously)
- Negative differential-mode surge pulses (can occur because of lightning events or during testing by applying the negative 1-kV surge pulse, according to the EN 61000-4-5 standard)

The positive and negative input terminals are protected separately by protection diodes. Schottky diodes are preferred because of their low forward voltage (VF). The huge, high-temperature reverse currents (IRs) of the Schottky diodes (hundreds of µA at > 85°C) are of no concern if the diodes are forward biased.

One-way rectifiers, or half-wave rectifiers, can provide sufficient protection. One example is a circuit consisting of the diodes D3 and D5 (Figure 4) that does not contain diodes D7 and D4. The disadvantage of half-wave rectifiers is that the rectifier diodes must withstand the sum of the rectifier output voltage (usually stored in the bypass capacitor on the input of the following block or blocks), plus the absolute value of an applied negative voltage. Using this design as an example, the sum of 33 V plus 60 V is close to 100 V.

In the case of using separate diodes for the positive and negative loop-input terminals, this voltage can divide equally. In real cases, this equal splitting cannot be guaranteed because of the wide spread of reverse currents between the two diodes, especially when Schottky diodes are used at high temperatures.

Another disadvantage of the half-wave rectifier configuration is the missing current, which normally keeps the blocks following the protection circuit alive during any negative input-voltage events. Therefore, a better solution is a full-wave rectifier configuration, which provides a perfect voltage clamp across the rectifier diodes to the absolute value of the input voltage. The full-wave rectifier configuration also ensures a continuous current delivery to the following blocks, even during reverse input-voltage events.

Nevertheless, if the rectifier bridge has been built using only Schottky diodes, the hundreds of µA of reverse current (IR) of these diodes add to the 1-µA IR of the TVS diode (D6). Therefore, the total error on the loop current measured by the loop receiver is no longer acceptable.

By using the mix of Schottky diodes and silicon diodes (Figure 4), the advantages of both diode types can be preserved. The two forward-biased Schottky diodes D3 and D5 cause a total worst-case FV drop of only 880 mV at 3.3 mA and –40°C. The two silicon diodes D7 and D4 prevent D3 and D5 from being stressed with more than 60 V during miswiring events or negative-differential surge pulses. D7 and D4 are reverse biased, but add only 1 µA of additional reverse current IR at 85°C on the 1-µA IR of the TVS diode and the resulting 2-µA IR is within the design limit of 3 µA.

Even when the loop input voltage has been applied in reverse direction on J2, the output of the protection circuitry provides a voltage with the correct polarity to the following blocks. In this situation, the silicon diodes D7 and D4 are now forward-biased; however, the total FV drop of those two diodes is now in the worst-case situation (almost 1.9 V), which is more than twice the total drop caused by the Schottky diodes (almost 900 mV total). The two Schottky diodes D3 and D5 are reverse-biased and as a whole contribute an additional 500-µA reverse current to the total leakage current of the protection circuitry.

The transmitter continues to work even with reverse loop-input voltage polarity; however, the transmitter is no longer capable of matching the accuracy specification of the transmitter. Nevertheless, one clear advantage is that the transmitter electronics do not lose power during negative transient events. This advantage means that the transmitter returns back to the full, typical performance after the transient without any time delay that a required restart of the transmitter internal electronics requires.

6 Getting Started Hardware

6.1 Board Description

Refer to Figure 5 for the corresponding description of the TIDA-00851 PCB.

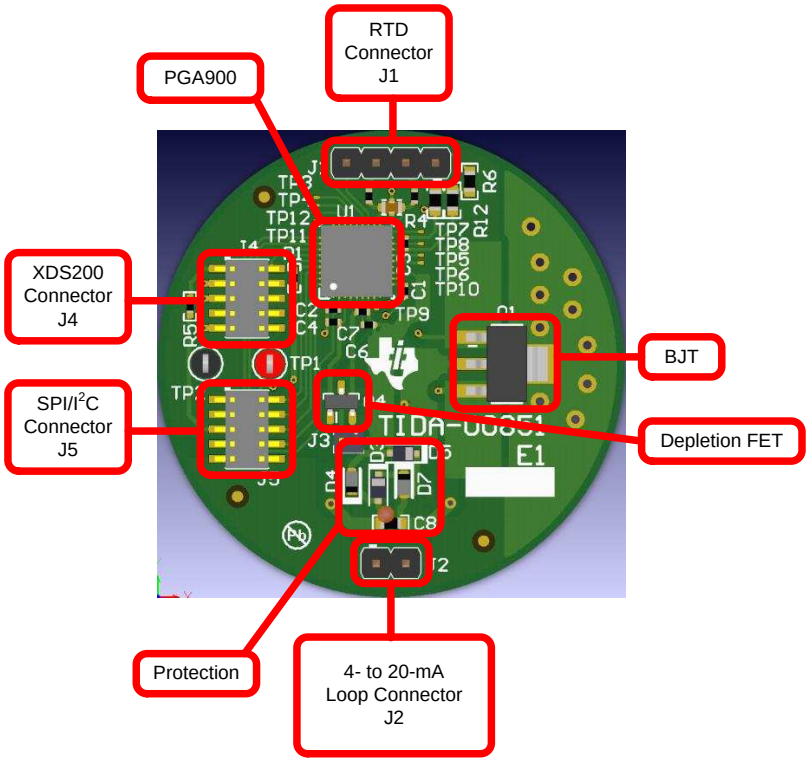

Figure 5. PCB Overview

- *RTD connector J1*: At this four-pin 2.54-mm raster pin header, the user can connect an external RTD. This design uses a PT100 simulator (Time Electronics Type 1049).
- *PGA900*: This is the main device. See details in Section 4.1.
- *XDS200 connector J4*: The XDS200 programmer can be connected at this connector. With the provided adapter, the programmer can be connected directly to J4.

J4 PIN	DESCRIPTION
1	AVDD (through 10-kΩ resistor)
2	SWDIO
3	GND
4	SWDCLK
5	GND
6, 7, 8, and 10	NC
9	GND

- *SPI/I²C connector J5*: The design also has additional interfaces on a dedicated connector for test and debugging purposes. Such connectors can be very useful in examples such as using the design in combination with the PGA900EVM to use it with the existing graphical user interface (GUI).

Table 2. J5 Description

J5 PIN	DESCRIPTION
1	SCK
2	SDA
3	CSN
4	MOSI
5	AVDD
6	MISO
7	DVDD
8	SCL
9	GND
10	GND

- *Protection*: The protection circuitry (in addition to three components on the bottom layer) protects against reverse polarity and surge events.
- *4- to 20-mA loop connector J2*: At this two-pin, 2.54-mm raster pin header, the user can connect the current loop to provide the supply voltage.
- Depletion FET: This FET is required to operate the design at > 30 V from the loop. If this feature is not required, bypass the field-effect transistor (FET) by placing a jumper on J3. The PGA900 requires reprogramming in this situation because the GATE drive is no longer required.
- *BJT*: This is the transistor for driving the 4 mA to 20 mA of the current loop.

The PCB has additional test points to make all available signals of the PGA900 available to the user.

6.2 Required Hardware

The following equipment is required for testing the design:

- TIDA-00851 TI Design
- Digital multimeter (DMM): 6½-DMM is sufficient; 8½-DMM is even better
- Power supply (24 V)
- PT100 simulator (or precision resistors within a PT100 resistor range)
- XDS200 debugger
- UART-to-USB cable (here: FTDI – TTL-232R-3V3)
- PC

6.3 Stand-alone Setup

Figure 6 shows the TIDA-00851 setup, which the following steps briefly outline:

1. Connect the PT100 simulator (or precision resistor) to J1.
2. Connect the XDS200 debugger to J4 and to the user PC.
3. Connect the UART-to-USB cable to J5 and to the user PC.
4. Connect a power supply to J2 with an ammeter in series to measure the loop current.

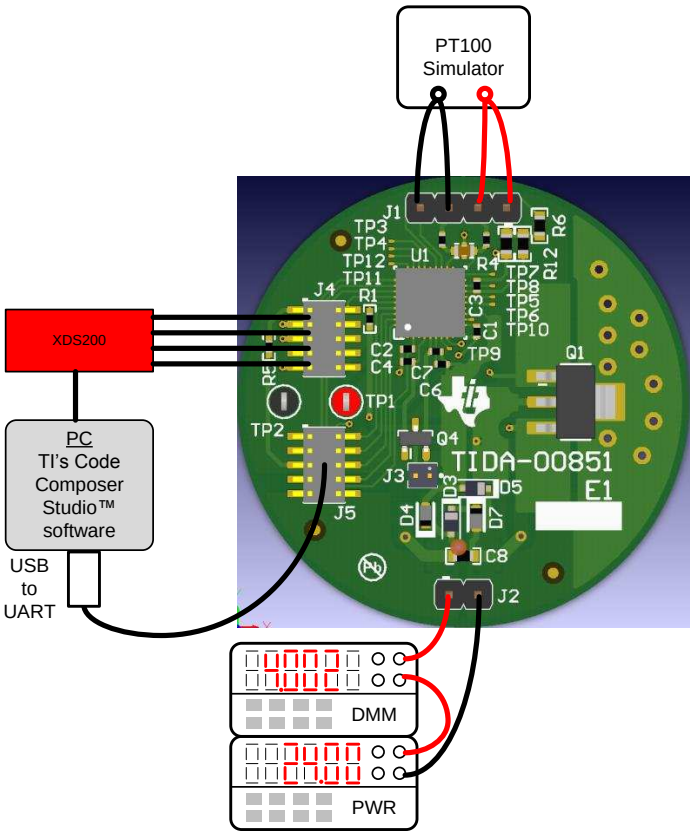

Figure 6. TIDA-00851 Setup

Refer to Section 7 *Getting Started Firmware* for details on loading the firmware into the PGA900 device.

When the design is up and running, the user can observe a loop current change when changing the PT100 value.

6.4 EVM Setup

The TIDA-00851 TI Design can also be used in combination with the existing PGA900EVM and its GUI. With this approach, configuring the PGA900 building blocks like ADC and DAC without using the M0 processor is easy. Because the GUI of the EVM also enables control through Python, automated testing of the different building blocks is easy.

6.4.1 Hardware Setup

The EVM setup requires additional hardware to the hardware listed in Section 6.2:

- PGA900EVM
- USB2ANY board
- No longer requires the XDS200 debugger
- No longer requires the UART-to-USB cable

To connect the PGA900EVM with the TIDA-00851 board, remove the PGA900 device from the socket on the EVM.

Follow the settings in Table 3 for a proper hardware setup.

Table 3. Hardware Setting of TIDA-00851 and PGA90EVM

TIDA-00851	PGA900EVM (HREL017 REV.A)	EVM DESCRIPTION
J2 – PIN1	TP20	VDD(1)
J2 – PIN2	TP42	FBP
J5 – PIN2	TP15	SDA
J5 – PIN3	TP13	CSN
J5 – PIN8	TP16	SCL
X	J1, J2, J3, J4, J5, J7, J9, J10, J13, J24, J25, J26, J27, J28, J30	SHORTED
X	J6, J8, J11, J12, J15, J16	OPEN
X	J14	SHORT PINs 2-3
X	J19	SHORT PINs 1-2

(1) Indicates to place an anmeter in series to measure the loop current.

6.4.2 PGA900 GUI

After following the hardware instructions and installing the PGA900EVM GUI (http://www.ti.com/tool/PGA900EVM), launch the software.

Figure 7 through Figure 11 show the first GUI screen and the following steps for setting up the GUI, which Table 4 describes in further detail.

Table 4. PGA900EVM GUI Settings

GUI BUTTON	DESCRIPTION	REFERENCE
Microcontroller → Digital interface	Enable the digital interface to control the device.	Figure 8
I^2C	Activate the I^2C interface for the communication.	Figure 8
Gain and ADC	Choose gain and ADC selection.	Figure 9
Enable VREF buffer	Enable the internal buffer for the reference voltage.	Figure 9
Analog power	Power up the analog power.	Figure 9
ADC_CFG_1	Enable the ADC.	Figure 9
TEMP_MUX_CTRL	Choose the T channel MUX settings.	Figure 9
TSEM_N	Put the measurement into differential measurement.	Figure 9
TEST_MUX_T_EN	Set the Test MUX to the ADC.	Figure 9
TADC_EN	Enable the TADC.	Figure 9
TADC_EN_24BIT	Set to 24-bit mode.	Figure 9
READ ADC	Read ADC data.	Figure 9
DAC & PWM settings	Select the DAC&PWM settings.	Figure 10
DAC_ENABLE	Enable DAC.	Figure 10
TEST_MUX_DAC_EN	Set the Test MUX to the DAC.	Figure 10
CURRENT AMP	Choose the current output and activate 4-20mA.	Figure 10

Table 4. PGA900EVM GUI Settings (continued)

GUI BUTTON	DESCRIPTION	REFERENCE
DAC REG0	Set the DAC REG0 register to 0x0000 and write the data. The current consumption should decrease. The user can now change the loop current by writing different values to the DAC Register at this location.	Figure 10
ADC Capture	Choose selection ADC Capture.	Figure 11
Mode	Select between Voltage or ADC code to be shown in the graph.	Figure 11
Register	Select between PADC or TADC data to be shown.	Figure 11
Bits	Select between 16 bit or 24 bit.	Figure 11
T_GAIN	Select the gain settings of the channel.	Figure 11
Start/Stop	Start/Stop capturing data from the ADC (max 1024 is buffered).	Figure 11
TADC (graph)	With a right-click on the icon the user can pick the EXPORT function to store the captured data in a file.	Figure 11

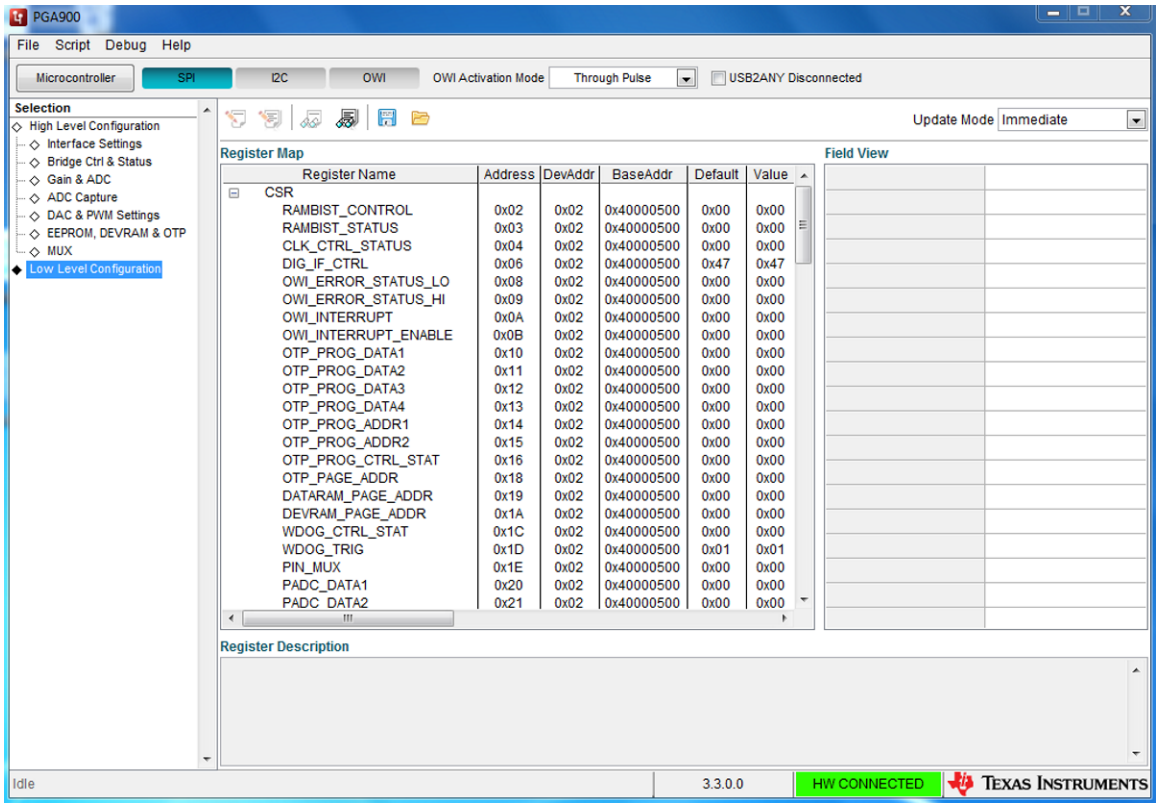

Figure 7. PGA900 GUI Step 1

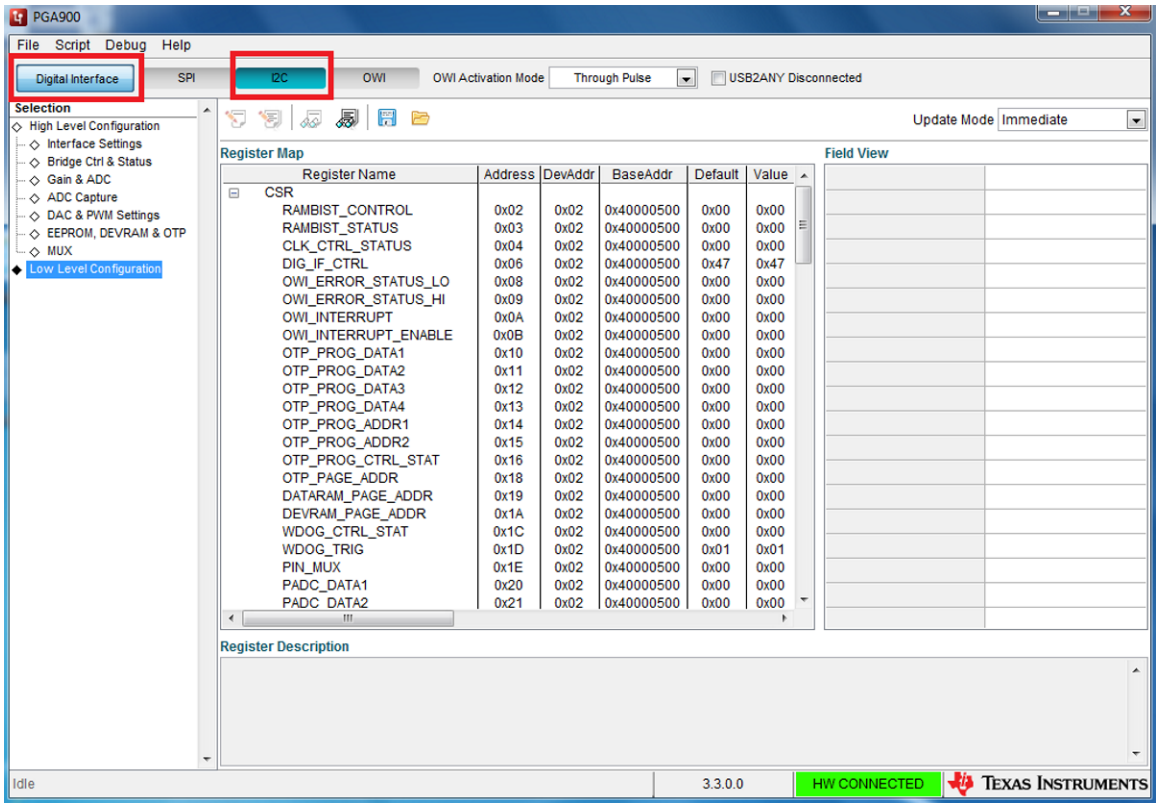

Figure 8. PGA900 GUI Step 2

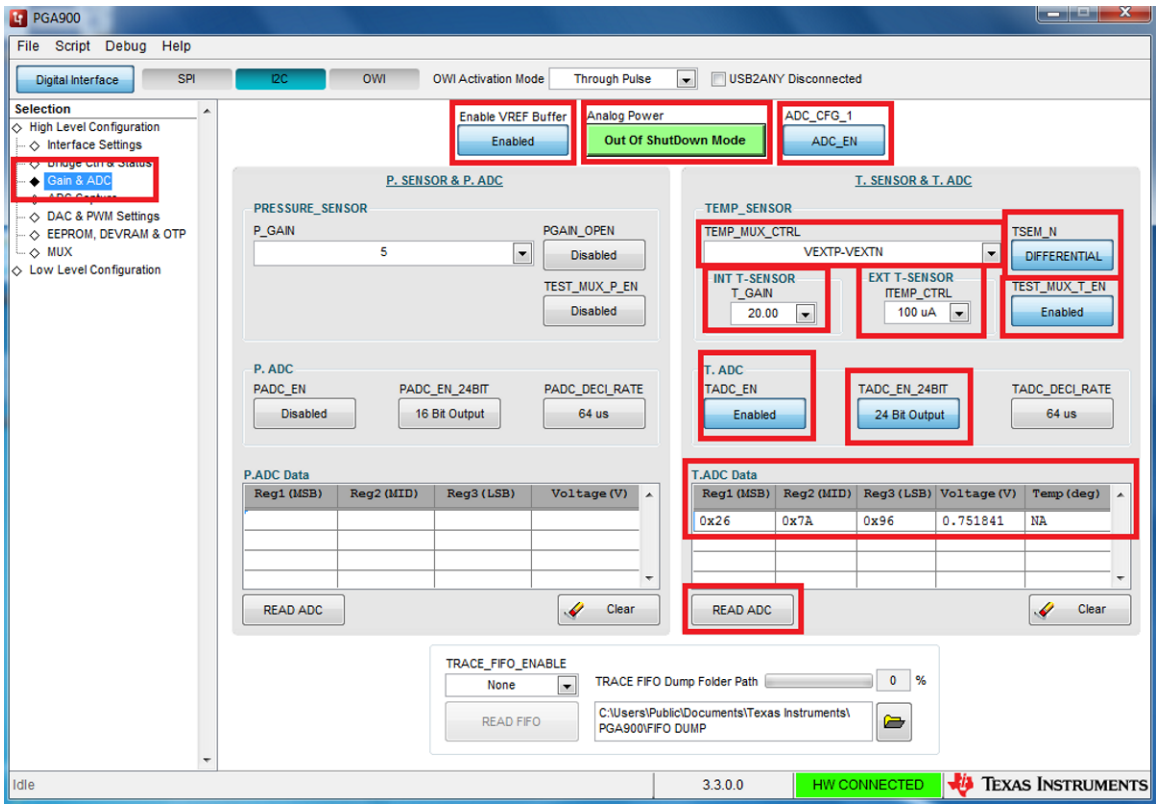

Figure 9. PGA900 GUI Step 3

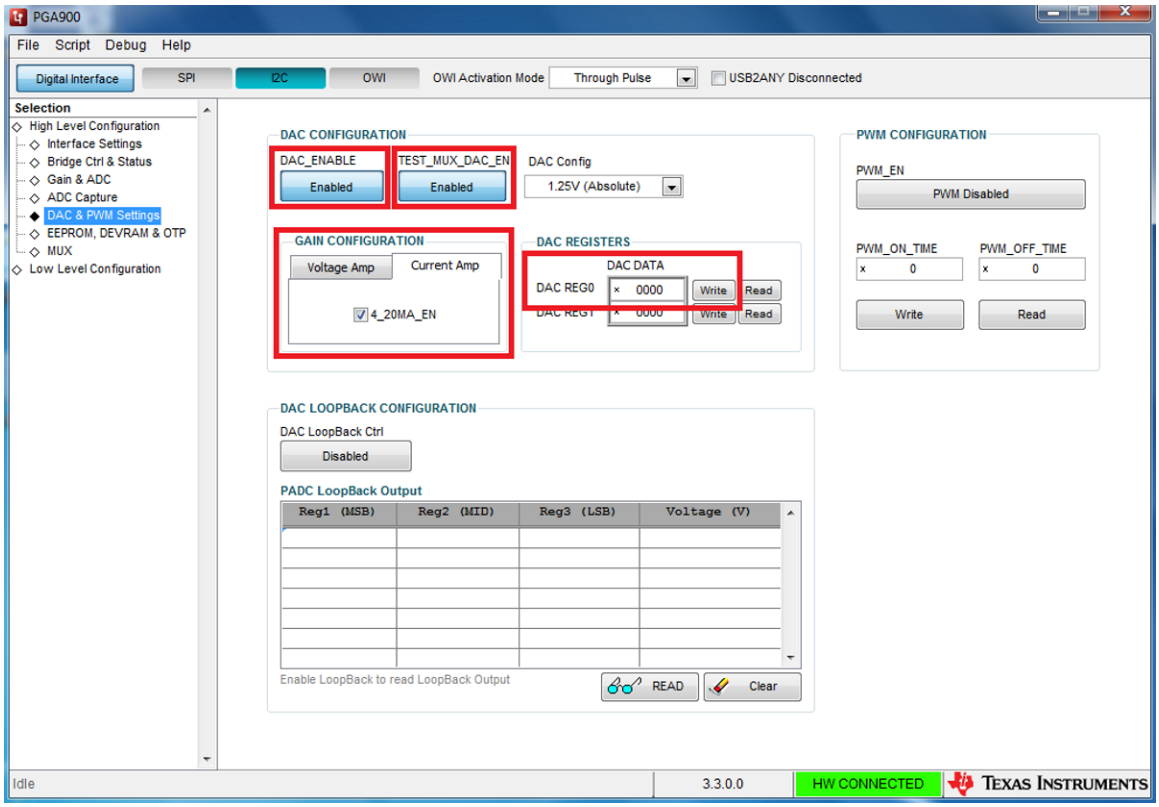

Figure 10. PGA900 GUI Step 4

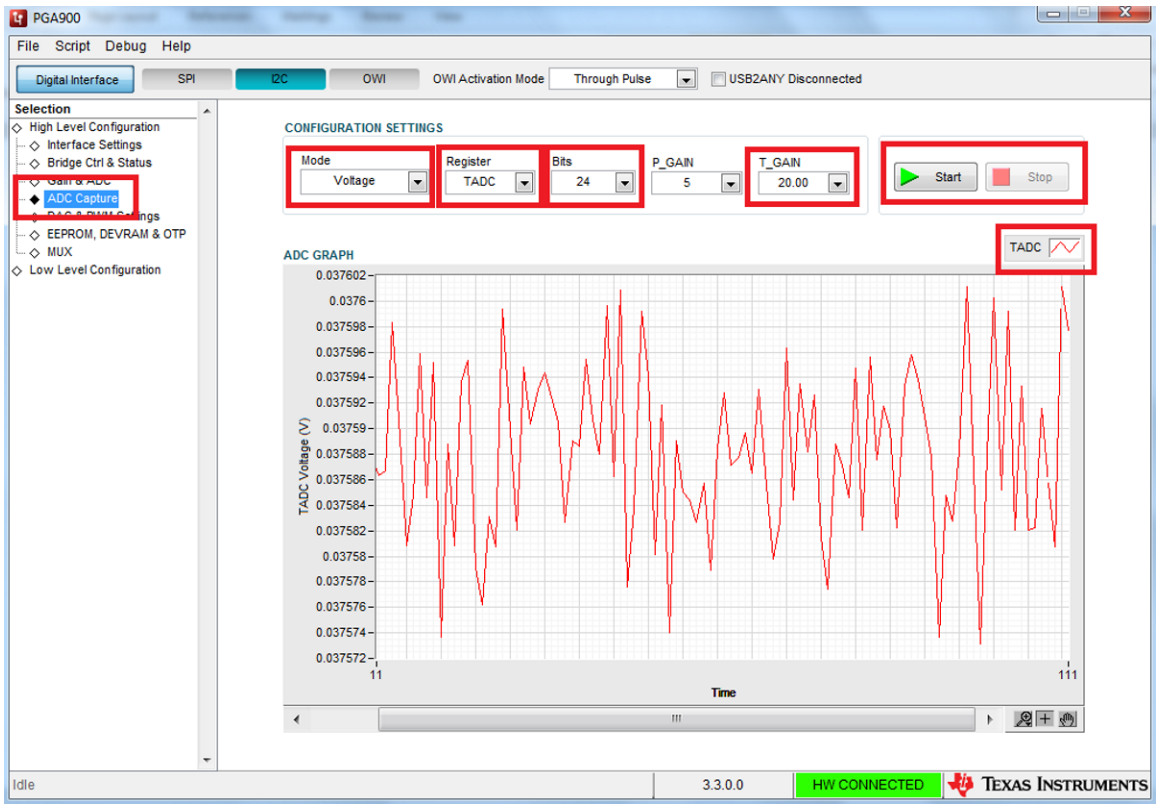

Figure 11. PGA900 GUI Step 5

7 Getting Started Firmware

To download the software files for this reference design, see the link at http://www.ti.com/tool/TIDA-00851.

7.1 Software Setup

For more information on the software setup, see the *PGA900 Software Quick Start Guide* (SLDU015).

7.2 RTD Demo Software

The software is based on the PGA900 generic firmware. For more information on the PGA900 generic firmware, see the *PGA900 Software User's Guide* (SLDU013).

The software code has been designed to implement a temperature-transmitter application to receive data from an RTD temperature probe and send out the temperature reading on a 4- to 20-mA signal. The software code also addresses system level calibration—both offset and gain—that can be implemented to improve ADC and DAC accuracy and also includes linear interpolation to address the nonlinearity of the RTD element.

The file *RTD_Lookuptable.xlsx* can be used to generate the RTD look-up table. The look-up table must be stored in the file *RTD_Math.c*.

In the file *RTD_Math.h*, the offset and gain calibration values can be adjusted for the ADC and the DAC. The following values are used for the calibration:

- DAC_OFFSET
- DAC_GAIN_CORRECTION
- ADC_OFFSET
- ADC_GAIN_CORRECTION

The software also implements the averaging of ADC results. The number of averaged samples can be adjusted with ADC_SAMPLES in the file *pga900_adc.h*.

If the UART_TESTING has been defined, the results are sent on the UART port.

8 Test Setup

The setup that Figure 12 shows has been used to test the design. The following equipment is required for testing the design:

- TIDA-00851 TI Design
- DMM: 6½-DMM is sufficient; 8½-DMM is even better
- Power supply (24 V)
- PT100 simulator (or precision resistors within a PT100 resistor range)
- XDS200 debugger
- UART-to-USB cable (here: FTDI – TTL-232R-3V3)
- PC

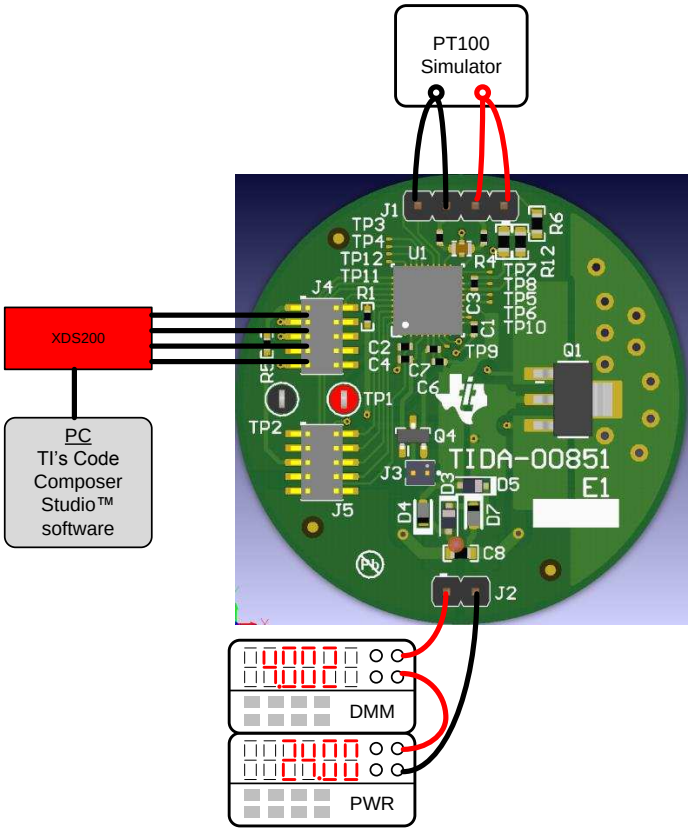

Figure 12. Test Setup

8.1 PT100 Simulator

To specify the accuracy of the system, precise reference resistors are required. A PT100 simulator with fixed resistor values has been used for the testing, representing different temperatures. In Table 5, the first column represents the temperatures that the simulator can select. The second column represents the actual resistor values by measuring with an 8½-DMM. The third column shows the temperature values based on the measured resistor values.

Table 5. Values of PT100 Simulator

PT100 SIMULATOR TEMPERATURE (°C)	MEASURED PT100 SIMULATOR RESISTOR (Ω)	PT100 SIMULATOR BASED ON MEASUREMENTS (°C)
–200	18.566	–199.894
–100	60.291	–99.9132
–50	80.33	–49.9403
0	100.0265	0.067805
50	119.401	50.01006
100	138.598	100.2439
200	175.869	200.0354
500	280.977	499.9985
800	375.7035	799.9983

8.2 Current Loop

Because the TIDA-00851 consists of a loop-powered design, a 24-V power supply is connected in series with an ampere meter at J2.

8.3 Programming and Debugging

The XDS200 programmer is connected to J4 to program the PGA900 device. Additionally, the ADC codes can be read as well as the DAC registers that have been written for test purposes.

9 Test Data

9.1 Analog Front End

The analog front end has been tested by providing several precision resistor values at the input. The following figures show plots for the 1024 captures taken during testing.

Figure 13 is the histogram with shorted inputs.

Figure 14 through Figure 31 show the histograms for the different PT100 values at the input. Figure 32 through Figure 40 show the histograms with the corresponding temperature variation. The provided values are listed in Table 5. Two different histograms have been provided for each resistor value. The first plot shows the results without averaging and the second plot averages 64 values of the captured ADC codes. The averaging is performed in the M0 processor.

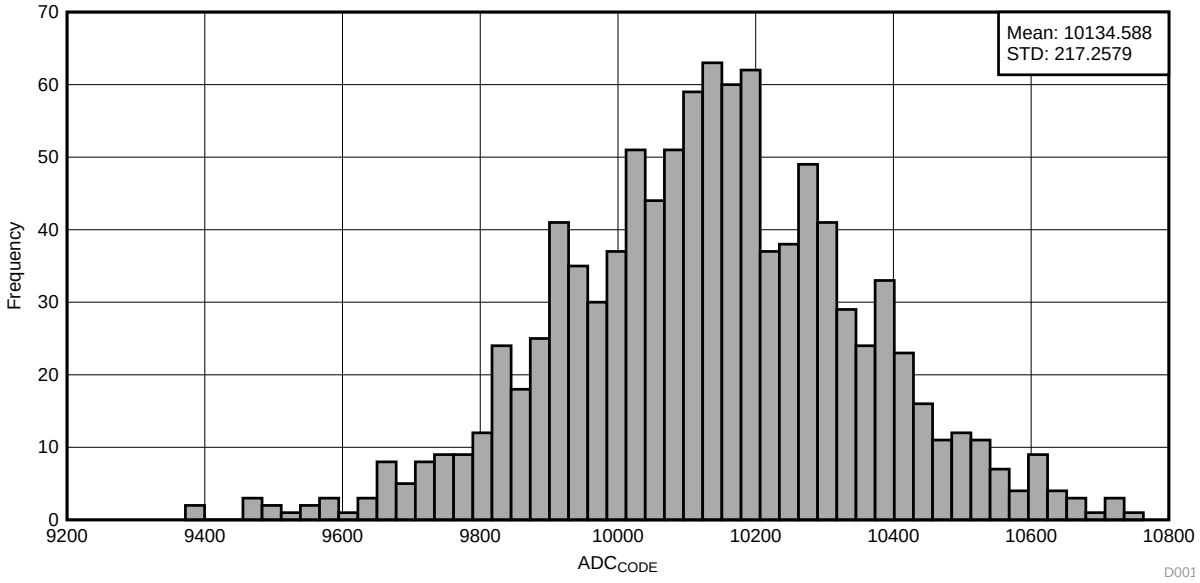

Figure 13. Short Input at J1

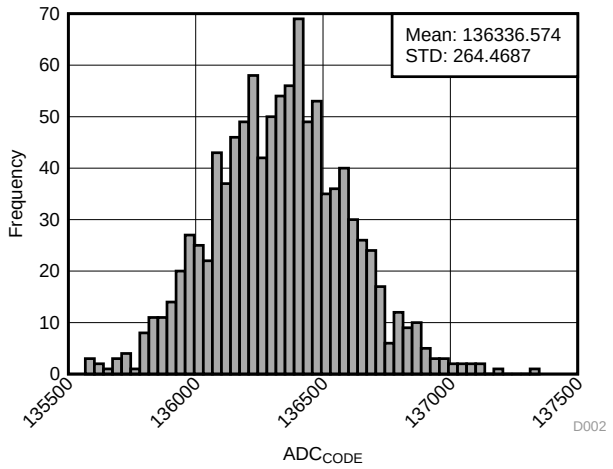

Figure 14. PT100 Simulator: –200°C Without Averaging

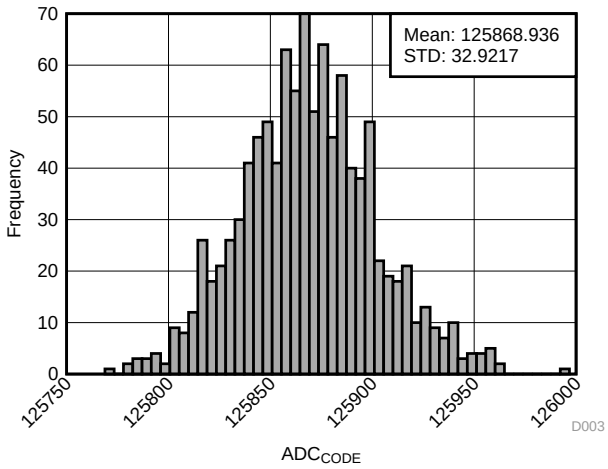

Figure 15. PT100 Simulator: –200°C With Averaging (64×)

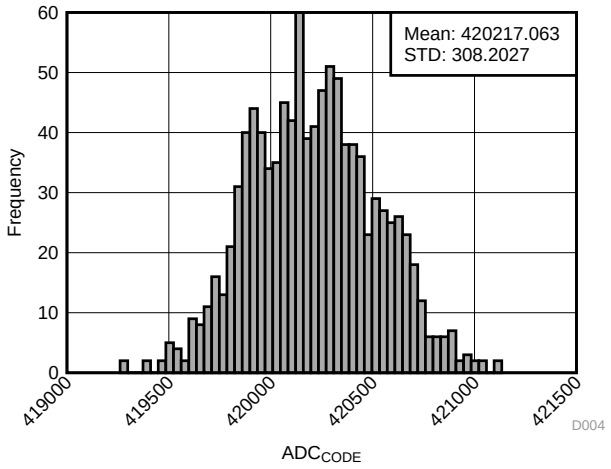

Figure 16. PT100 Simulator: –100°C Without Averaging

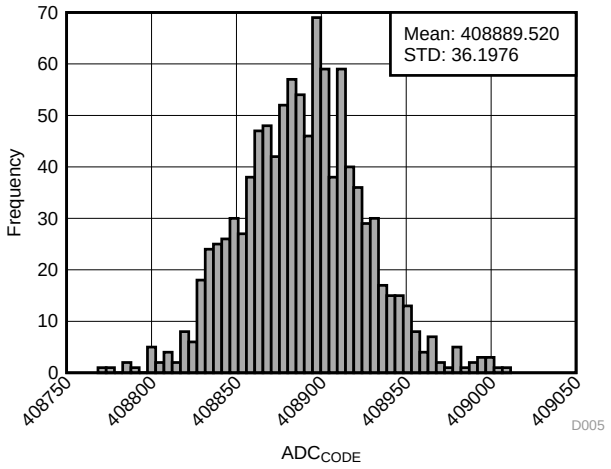

Figure 17. PT100 Simulator: –100°C With Averaging (64×)

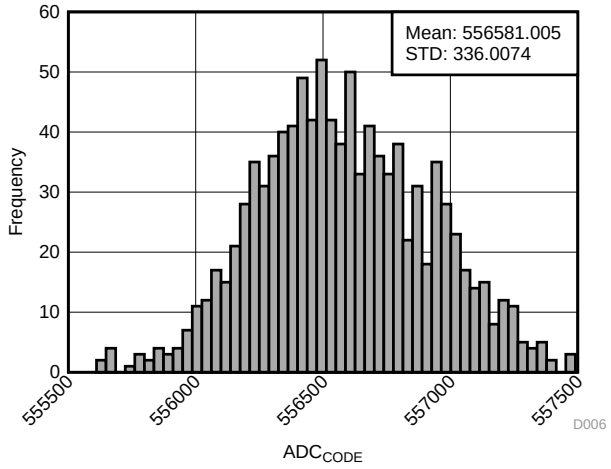

Figure 18. PT100 Simulator: –50°C Without Averaging

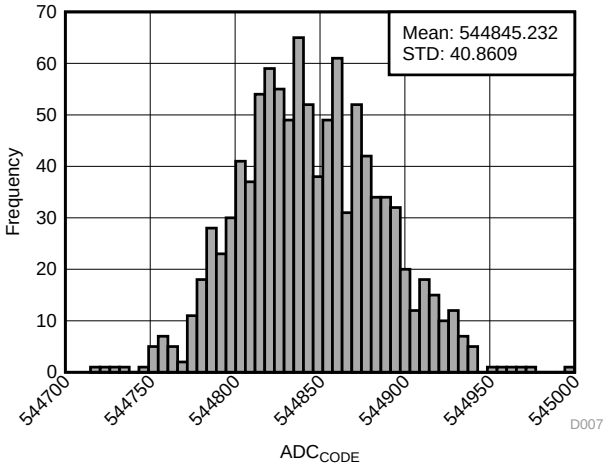

Figure 19. PT100 Simulator: –50°C With Averaging (64×)

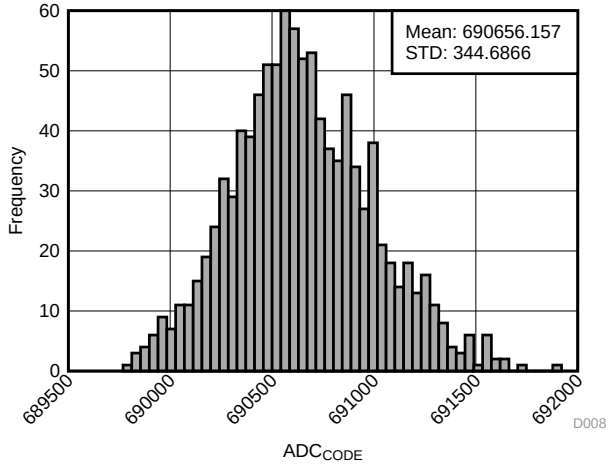

Figure 20. PT100 Simulator: 0°C Without Averaging

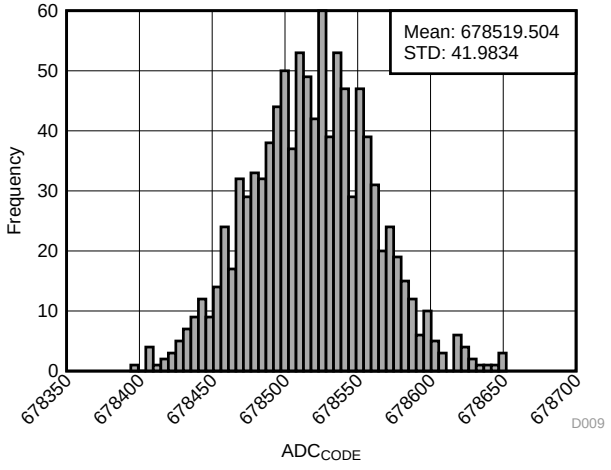

Figure 21. PT100 Simulator: 0°C With Averaging (64×)

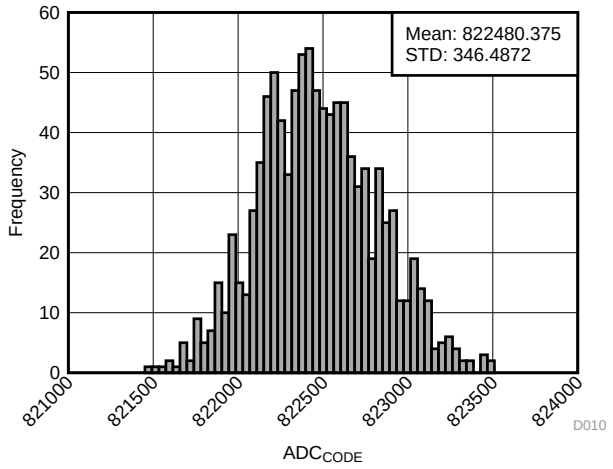

Figure 22. PT100 Simulator: 50°C Without Averaging

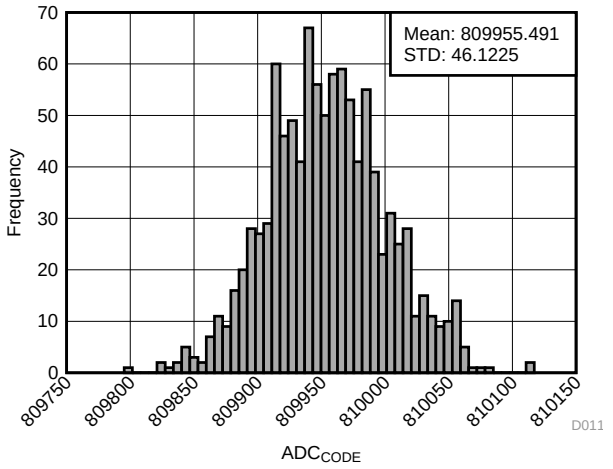

Figure 23. PT100 Simulator: 50°C With Averaging (64×)

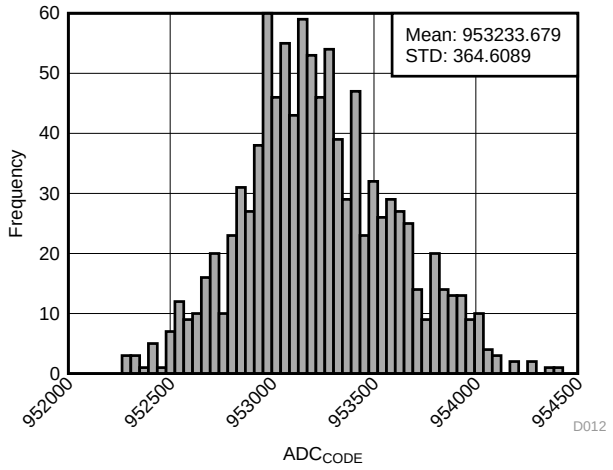

Figure 24. PT100 Simulator: 100°C Without Averaging

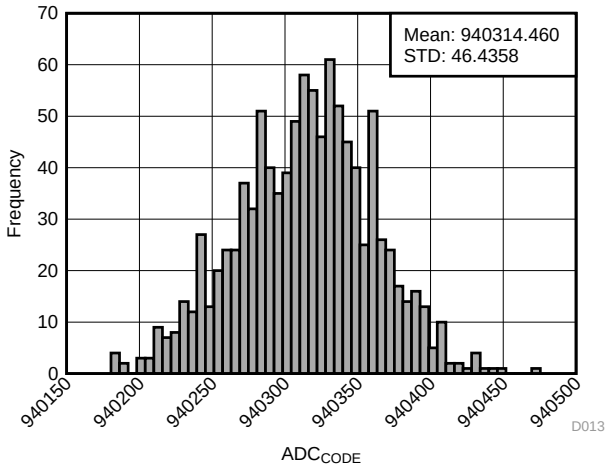

Figure 25. PT100 Simulator: 100°C With Averaging (64×)

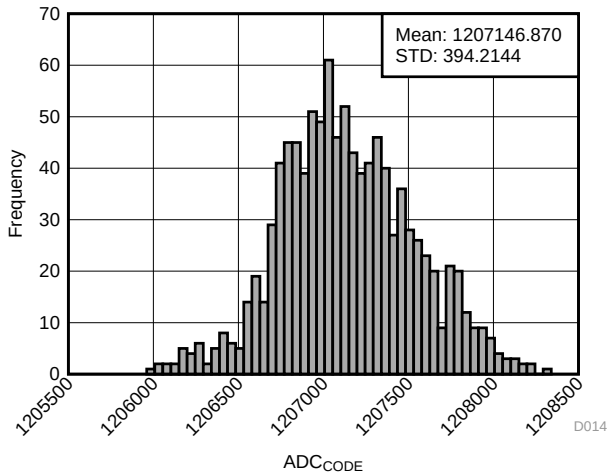

Figure 26. PT100 Simulator: 200°C Without Averaging

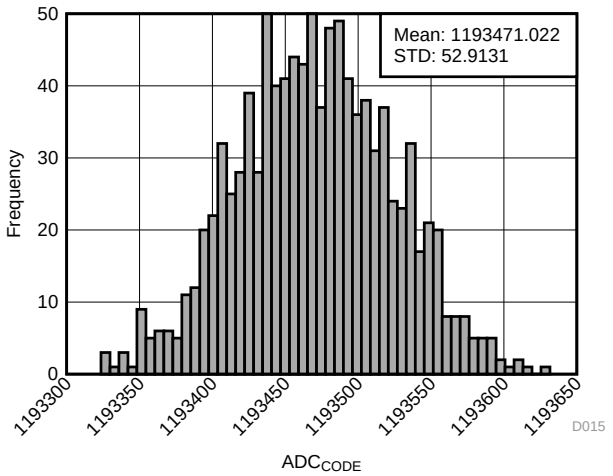

Figure 27. PT100 Simulator: 200°C With Averaging (64×)

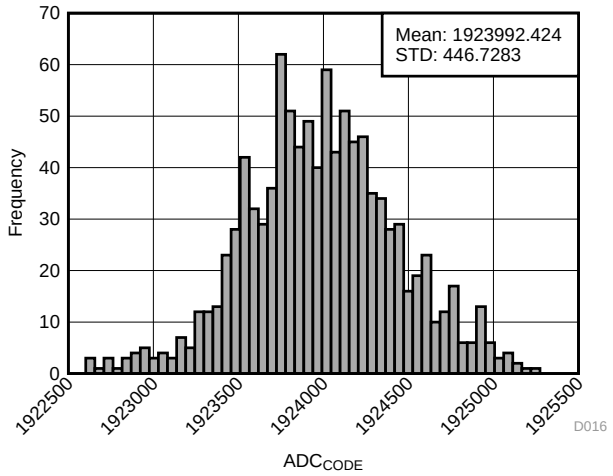

Figure 28. PT100 Simulator: 500°C Without Averaging

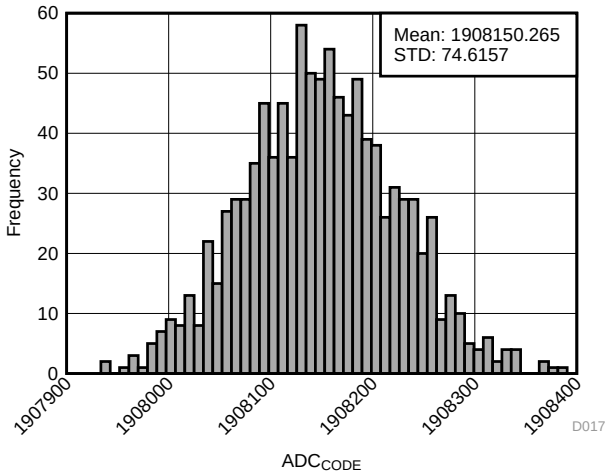

Figure 29. PT100 Simulator: 500°C With Averaging (64×)

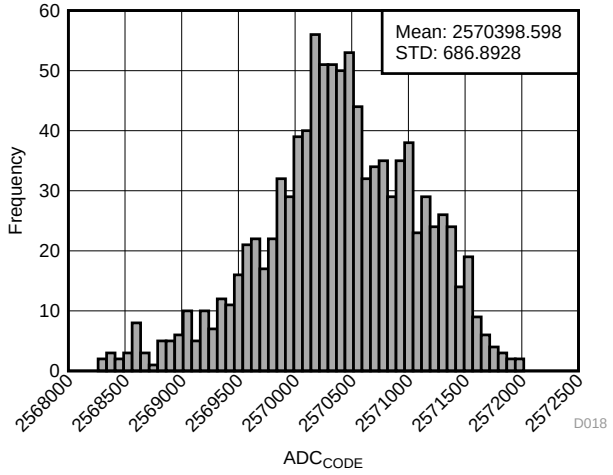

Figure 30. PT100 Simulator: 800°C Without Averaging

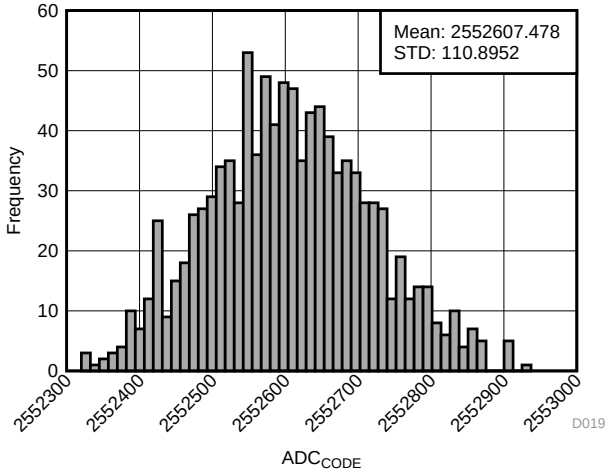

Figure 31. PT100 Simulator: 800°C With Averaging (64×)

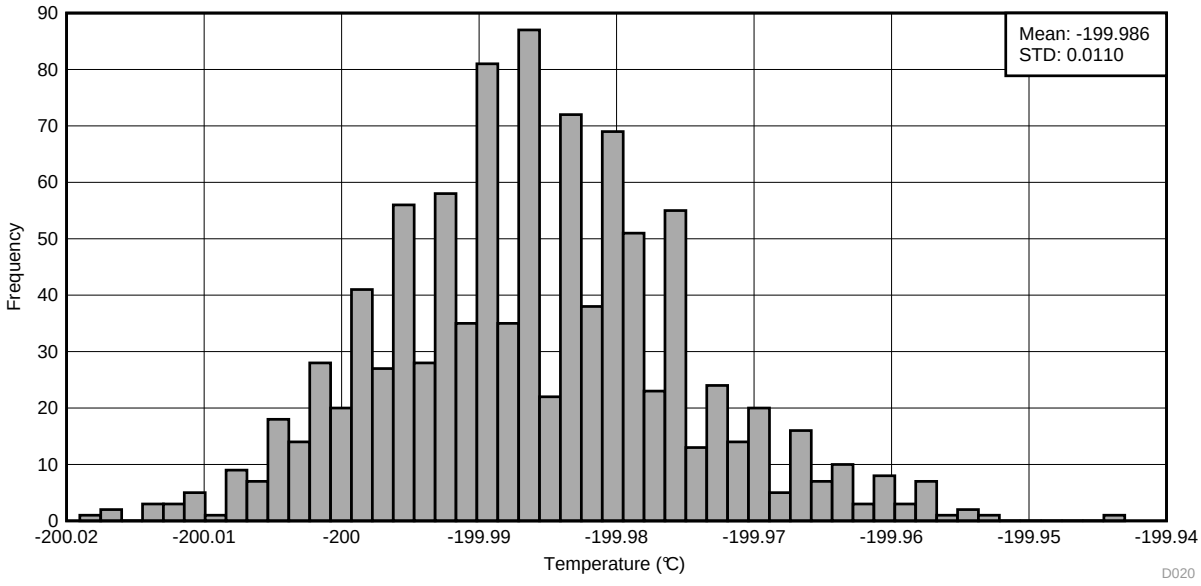

Figure 32. PT100 Simulator: –200°C With Averaging (64×)

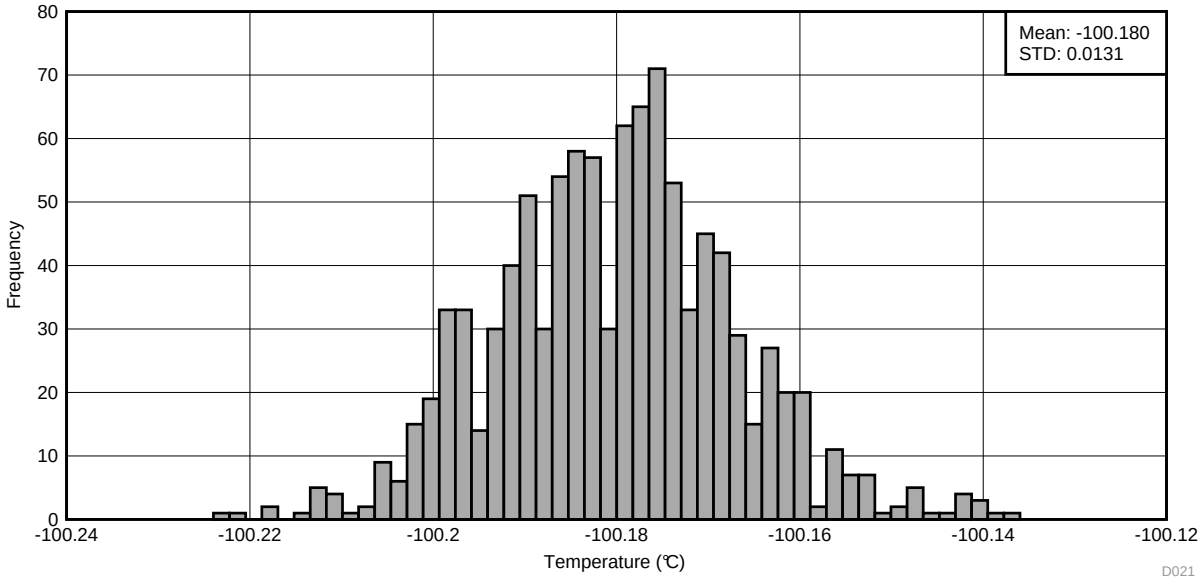

Figure 33. PT100 Simulator: –100°C With Averaging (64×)

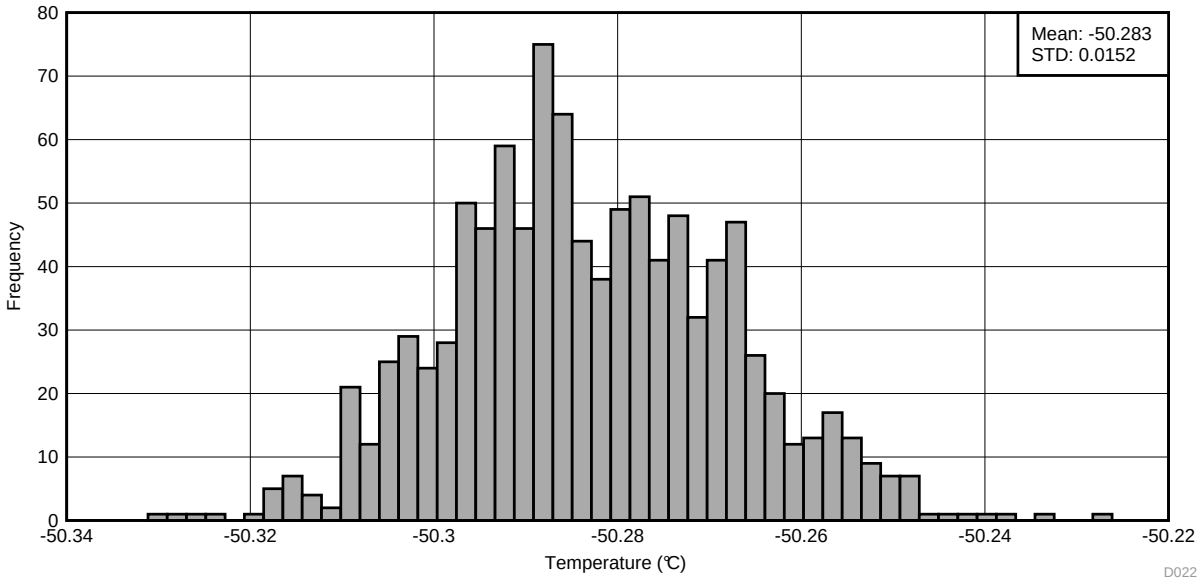

Figure 34. PT100 Simulator: –50°C With Averaging (64×)

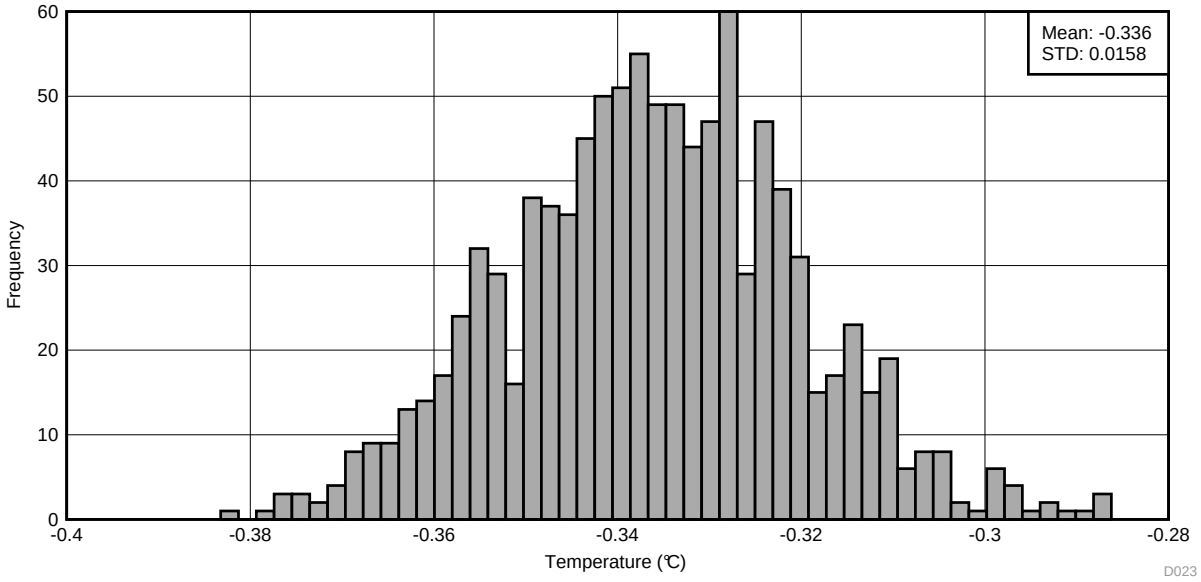

Figure 35. PT100 Simulator: 0°C With Averaging (64×)

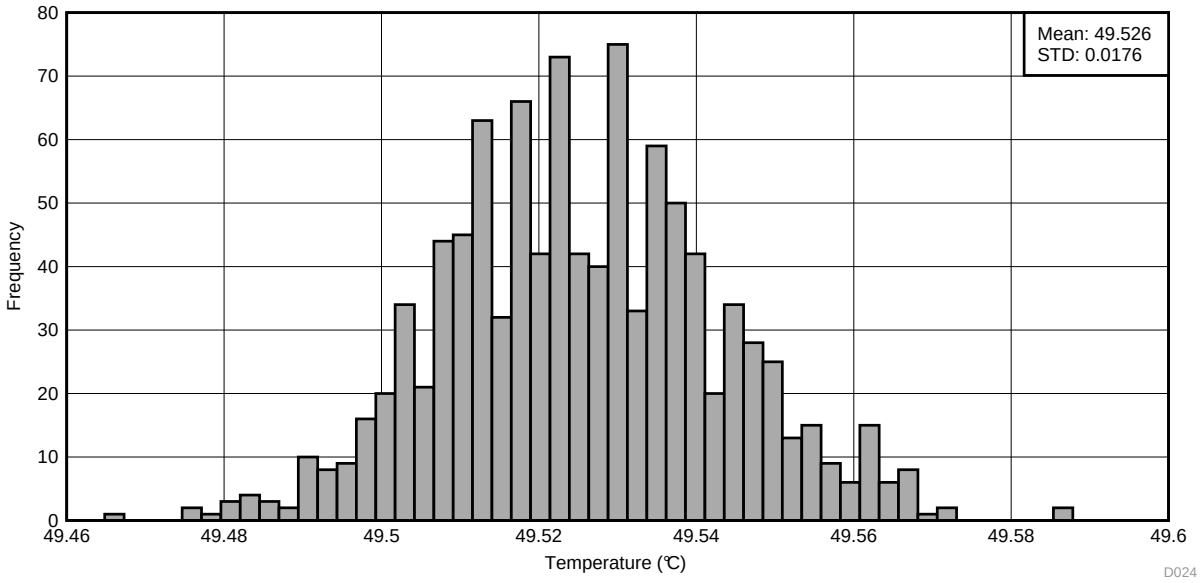

Figure 36. PT100 Simulator: 50°C With Averaging (64×)

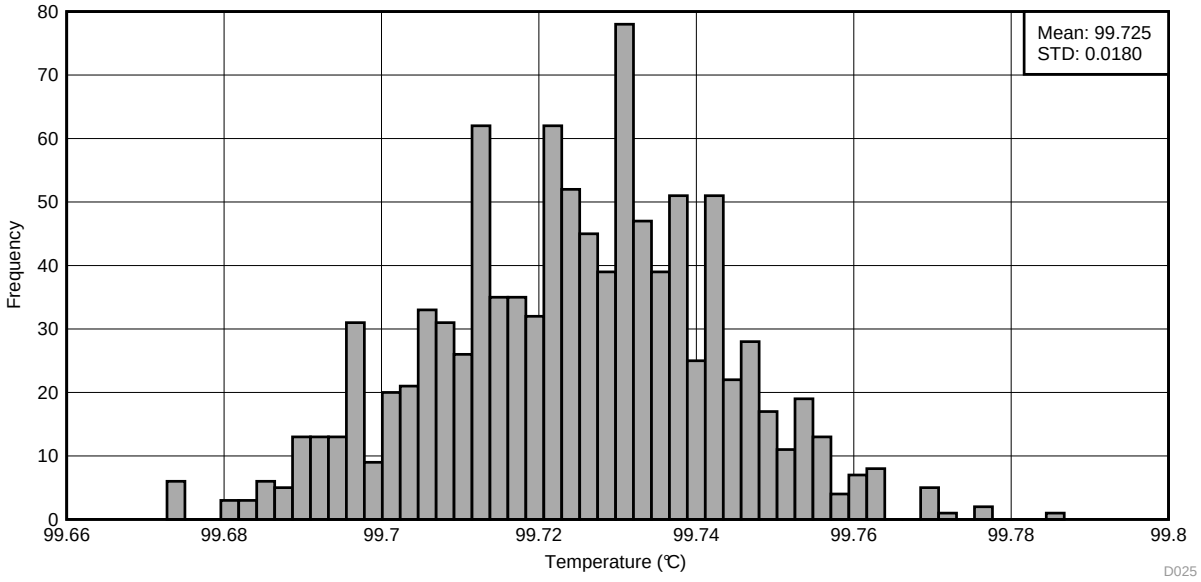

Figure 37. PT100 Simulator: 100°C With Averaging (64×)

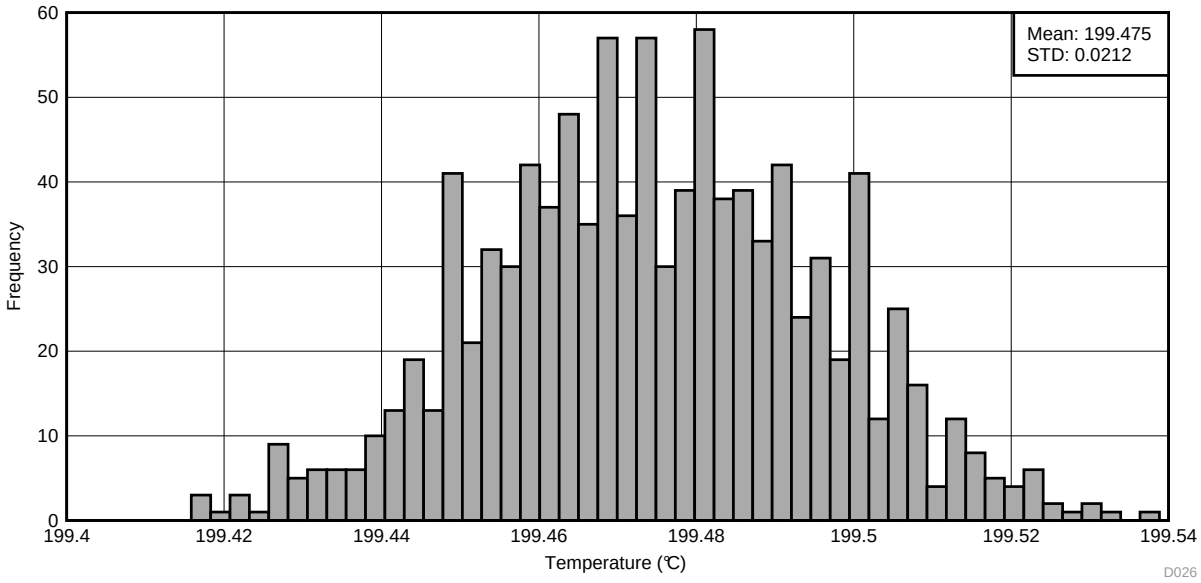

Figure 38. PT100 Simulator: 200°C With Averaging (64×)

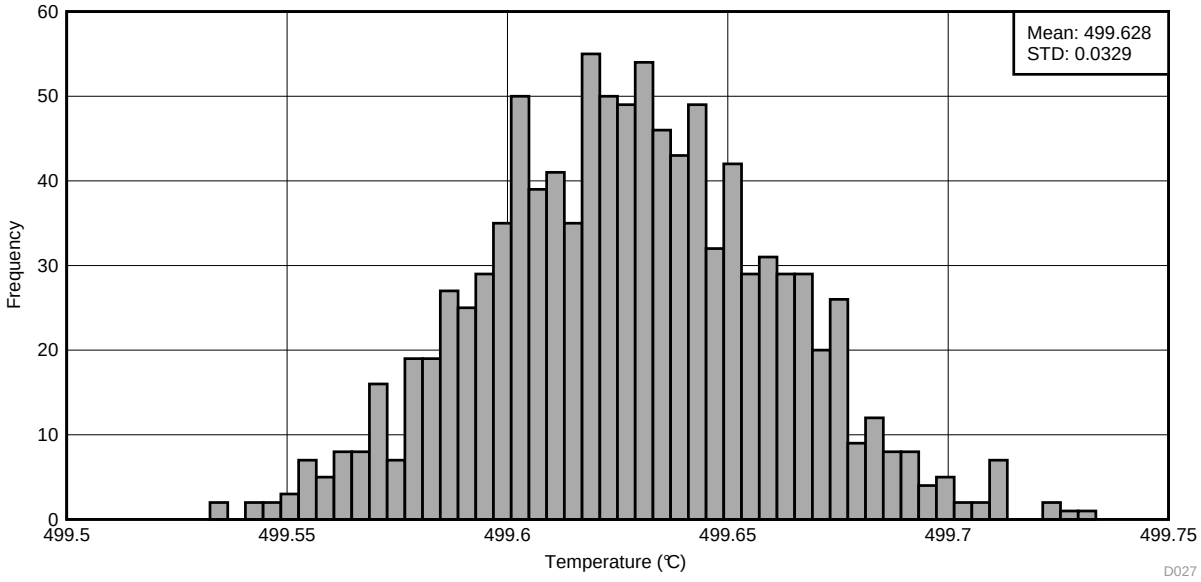

Figure 39. PT100 Simulator: 500°C With Averaging (64×)

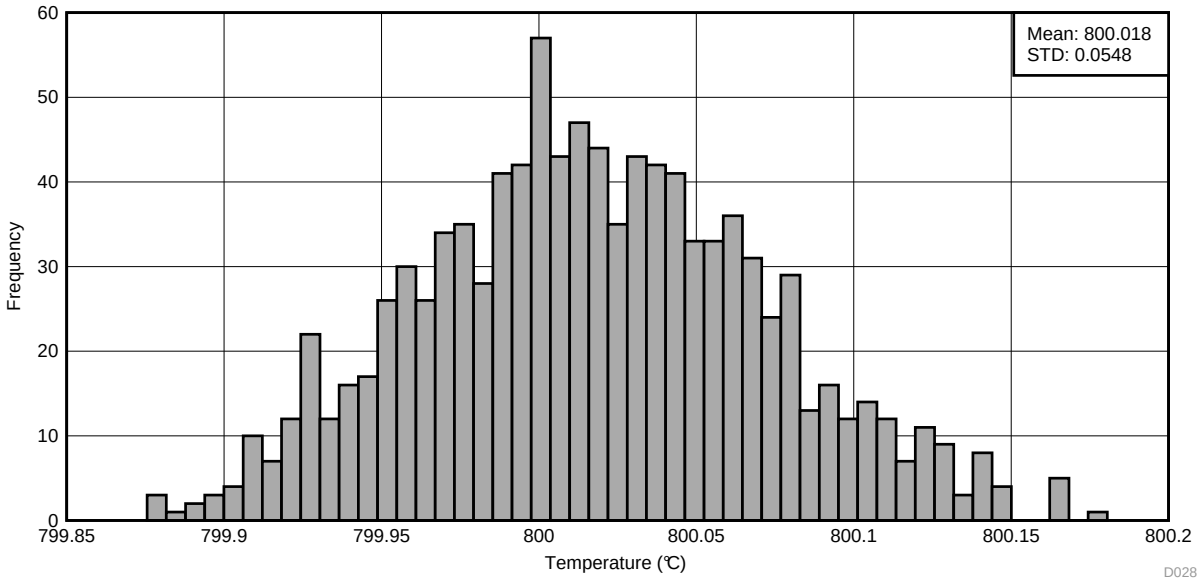

Figure 40. PT100 Simulator: 800°C With Averaging (64×)

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00851.

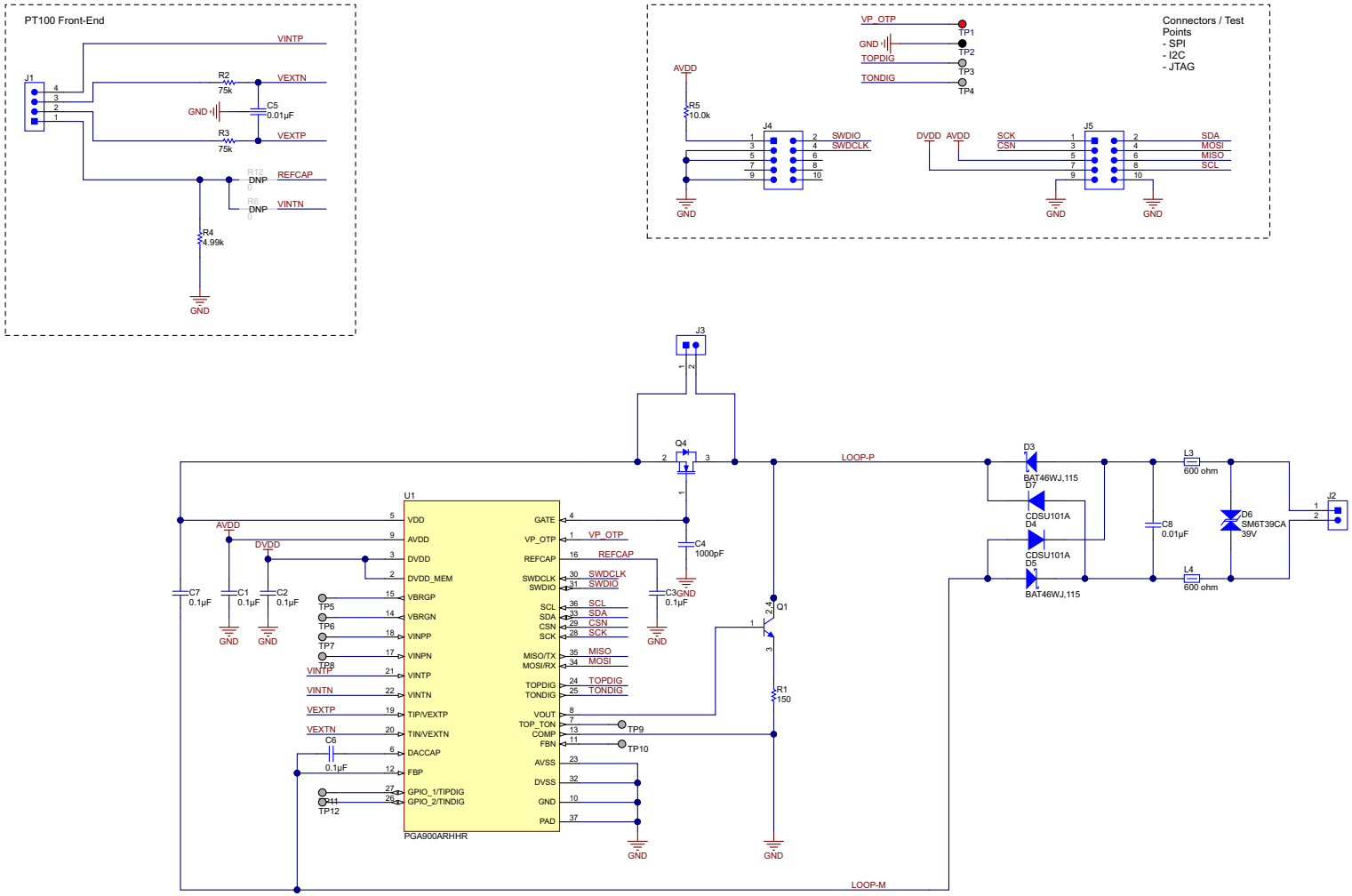

Figure 41. TIDA-00851 Schematic

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00851.

Table 6. TIDA-00851 BOM

ITEM #	DESIGNATOR	QUANTITY	VALUE	PART #	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB	1		TIDA-00851	Any	Printed Circuit Board	
2	C1, C2, C3, C6, C7	5	0.1uF	C1005X7R1H104K050BB	TDK	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402	0402
3	C4	1	1000pF	GRM155R61C102KA01D	MuRata	CAP, CERM, 1000 pF, 16 V, +/- 10%, X5R, 0402	0402
4	C5	1	0.01uF	500X14W103MV4T	Johanson Technology	CAP, CERM, 0.01 µF, 50 V, +/- 20%, X7R, 0603	0603
5	C8	1	0.01uF	C1608X7R2A103K	TDK	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0603	0603
6	D3, D5	2	100V	BAT46WJ,115	NXP Semiconductor	Diode, Schottky, 100 V, 0.25 A, SOD-323F	SOD-323F
7	D4, D7	2	90V	CDSU101A	Comchip Technology	Diode, Switching, 90 V, 0.1 A, SOD-523F	SOD-523F
8	D6	1	39V	SM6T39CA	STMicroelectronics	Diode, TVS, Bi, 39 V, 600 W, SMB	SMB
9	J1	1		61300411121	Wurth Elektronik	Header, 2.54 mm, 4x1, Gold, TH	Header, 2.54mm, 4x1, TH
10	J2	1		61300211121	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH
11	J3	1		GRPB021VWVN-RC	Sullins Connector Solutions	Header, 50mil, 2x1, Gold, TH	2x1 Header
12	J4, J5	2		BB02-BS101-KA8-025B00	GradConn	Header, 1.27mm, 5x2, SMT	Header, 1.27mm, 5x2, SMT
13	L3, L4	2	600 ohm	MI1206K601R-10	Laird-Signal Integrity Products	Ferrite Bead, 600 ohm @ 100 MHz, 1.5 A, 1206	1206
14	Q1	1	80 V	BCP56-16	STMicroelectronics	Transistor, NPN, 80 V, 1 A, SOT-223	SOT-223
15	Q4	1	100V	BSS169H6327XTSA1	Infineon Technologies	MOSFET, N-CH, 100 V, 0.17 A, SOT-23	SOT-23
16	R1	1	150	CRCW0402150RFKED	Vishay-Dale	RES, 150, 1%, 0.063 W, 0402	0402
17	R2, R3	2	75k	CRCW040275K0JNED	Vishay-Dale	RES, 75 k, 5%, 0.063 W, 0402	0402
18	R4	1	4.99k	RG1608P-4991-B-T5	Susumu Co Ltd	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603

Table 6. TIDA-00851 BOM (continued)

ITEM #	DESIGNATOR	QUANTITY	VALUE	PART #	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
19	R5	1	10.0k	CRCW040210K0FKED	Vishay-Dale	RES, 10.0 k, 1%, 0.063 W, 0402	0402
20	TP1	1	Red	5000	Keystone	Test Point, Miniature, Red, TH	Red Miniature Testpoint
21	TP2	1	Black	5001	Keystone	Test Point, Miniature, Black, TH	Black Miniature Testpoint
22	U1	1		PGA900ARHHR	Texas Instruments	PRESSURE SENSOR SIGNAL CONDITIONER, RHH0036C	RHH0036C
23	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
24	R6, R12	0	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603	0603

10.3 Layout Prints

To download the layout prints, see the design files at TIDA-00851.

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00851.

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00851.

10.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00851.

11 Software Files

To download the software files, see the design files at TIDA-00851.

12 References

1. Wikipedia.org, *Callendar–Van Dusen equation*, Wikipedia Entry (https://en.wikipedia.org/wiki/Callendar–Van_Dusen_equation)
2. Texas Instruments, *PGA900 as a 4- to 20-mA Current Loop Transmitter*, Application Report (SLDA030)

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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