TI Designs: TIDA-00779

230-V, 3.5-kW PFC With >98% Efficiency, Optimized for BOM and Size Reference Design

Description

This reference design is a 3.5-kW, cost competitive PFC designed for room air conditioners and other major appliances. This reference design is a continuous-conduction-mode (CCM) boost converter implemented using TI's UCC28180 PFC controller provided with all of the necessary built-in protections. The hardware is designed and tested to pass surge and EFT testing as per the IEC 61000 requirements for household appliances.

The key highlights of this reference design are:

- Provides a ready platform for front-end PFCs to address power level requirements for appliances up to 3.5 kW
- Up to 98.6% peak converter efficiency under 230-V input enable a competitive high power density and small heat sink design
- Robust output supply protected for output overcurrent, output overvoltage, and output undervoltage conditions

Resources

TIDA-00779	Design Folder
UCC28180	Product Folder
UCC27531	Product Folder
LMT01	Product Folder

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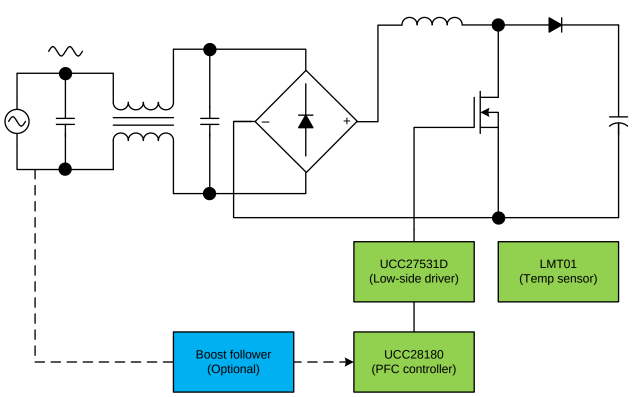
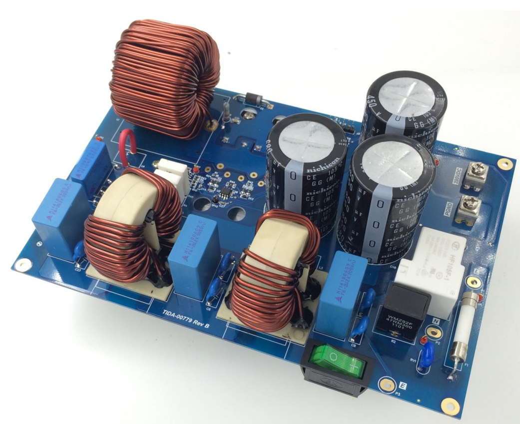
Features

- High Efficiency of > 98% Over Entire Operating Voltage Range, Allowing a Smaller Heat Sink
- Wide Full Load Operating Input Range of 190-V to 270-V AC
- High Power Factor > 0.99 and < 5% THD From Medium-to-Full Load (50 to 100%)
- Up to 3.5-kW High Power Output to Cover Most of Single-Phase Input PFC Application
- 8-Pin PFC Solution (No AC Line Sensing Needed) Enable Very Simple Design
- Reduced Current Sense Threshold Minimizes Power Dissipation
- High Power Density for Smaller Dimension
- Robust Output Supply Protected for Output Overcurrent, Output Overvoltage, and Output Undervoltage Conditions
- Meets Requirements of EFT Norm IEC 6000-4-4 and Surge Norm IEC 61000-4-5
- Simple Use PCB Form Factor (215 × 145 mm)

Applications

- Room Air Conditioners
- Industrial AC/DC > 480 W
- Single-Phase UPS
- Other Major Appliances





1 System Description

Major appliance equipment such as air conditioners, refrigerators, and washers use three-phase, pulse-width modulated BLDC or PMSM drives. These motor drives typically have fractional or low horsepower ratings ranging from 0.25 HP (186 W) to 5 HP (3.75 kW). An electronic drive is required to control the stator currents in a BLDC or PMSM motor. A typical electronic drive consists of:

- Power stage with a three-phase inverter with the required power capability
- Microcontroller unit (MCU) to implement the motor control algorithm
- Motor voltage and current sensing for closed-loop speed or torque control
- Gate driver for driving the three-phase inverter
- Power supply to power up the gate driver and MCU

These drives require a front-end power PFC regulator to shape the input current of the power supply and to meet the standards for power factor and current THD, such as IEC61000-2-3. A PFC circuit shapes the input current of the power supply to be in phase with the mains voltage and helps to maximize the real power drawn from the mains. The front-end PFC also offers several benefits:

- *Reduces RMS input current*
  For instance, a power circuit with a 230-V/5-A rating is limited to about 575 W of available power with a power factor (PF) of 0.5. Increasing the PF to 0.99 almost doubles the deliverable power to 1138 W, allowing the operation of higher power loads.
- *Facilitates power supply hold-up*
  The active PFC circuit maintains a fixed, intermediate DC bus voltage that is independent of the input voltage so that the energy stored in the system does not decrease as the input voltage decreases. This maintenance allows the use of smaller, cost effective bulk capacitors.
- *Improves efficiency of downstream converters*
  The PFC reduces the dynamic voltage range applied to the downstream inverters and converters. As a result, the voltage ratings of rectifiers can be reduced, resulting in lower forward drops. The operating duty cycle can also be increased, resulting in lower current in the switches.

This reference design is a boost PF regulator implemented using the UCC28180 device as a PFC controller for use in all appliances that demand a PF correction of up to 3.5 kW. The design provides a ready platform of an active front-end to operate downstream inverters or DC/DC converters operating on a hi-line AC voltage range from 190-V to 270-V AC.

This design demonstrates a high power density PF stage in a small form factor (215 × 145 mm) that operates from 190-V to 270-V AC and delivers up to 3.5 kW of continuous power output to drive inverters or converters at more than a 98% efficiency rate without an SiC device. This TI Design also provides flexibility for the boost follower configuration, in which the boost voltage can be varied with AC input voltage, but only can work on the boosted voltage when it is above the peak input voltage. The boost follower configuration helps reduce switching losses in the PFC regulator and the downstream inverter or converter. This design also gave an efficiency comparison in using MOSFET and IGBT, which can help customer to choose efficiency or cost is preferred.

Above all, this TI Design meets the key challenges of appliances to provide safe and reliable power with all protections built in while delivering a high performance with low power consumption and a very competitive bill-of material (BOM) cost.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage	V_{IN}	—	85	230	270	V AC
Frequency	F_{AC}	—	47	—	64	Hz
Input UVLO	V_{IN_UVLO}	I_{OUT} = nom	—	80	—	V AC
Power factor	PF	V_{IN} = nom, I_{OUT} = max	—	0.99	—	—
Input current	I_{IN}	V_{IN} = nom, I_{OUT} = max	—	20	—	A
OUTPUT CHARACTERISTICS						
Output voltage	V_{OUT}	V_{IN} = nom, I_{OUT} = min to max	—	390	—	V
Output current	I_{OUT}	V_{IN} = 190-V AC to max	0	—	9	A
Output power	P_{OUT}	V_{IN} = 190-V AC to max	—	—	3.5	kW
Line regulation		V_{IN} = min to max, I_{OUT} = nom	—	—	2	%
Load regulation		V_{IN} = nom, I_{OUT} = min to max	—	—	3	%
Output voltage ripple	V_{OUT_RIPPLE}	V_{IN} = nom, I_{OUT} = max	—	—	17	V
Output overvoltage	V_{OVP}	I_{OUT} = min to max	—	—	430	V
Output overcurrent	I_{OCP}	V_{IN} = min to max	12	—	—	A
SYSTEM CHARACTERISTICS						
Switching frequency	f_{SW}	—	—	45	—	kHz
Peak efficiency	η_{PEAK}	V_{IN} = max, I_{OUT} = 4 A, test with MOSFET	—	—	98.6	%
Operation temperature	T_{NOM}	With air flow	–25	—	65	°C

2 System Overview

2.1 Block Diagram

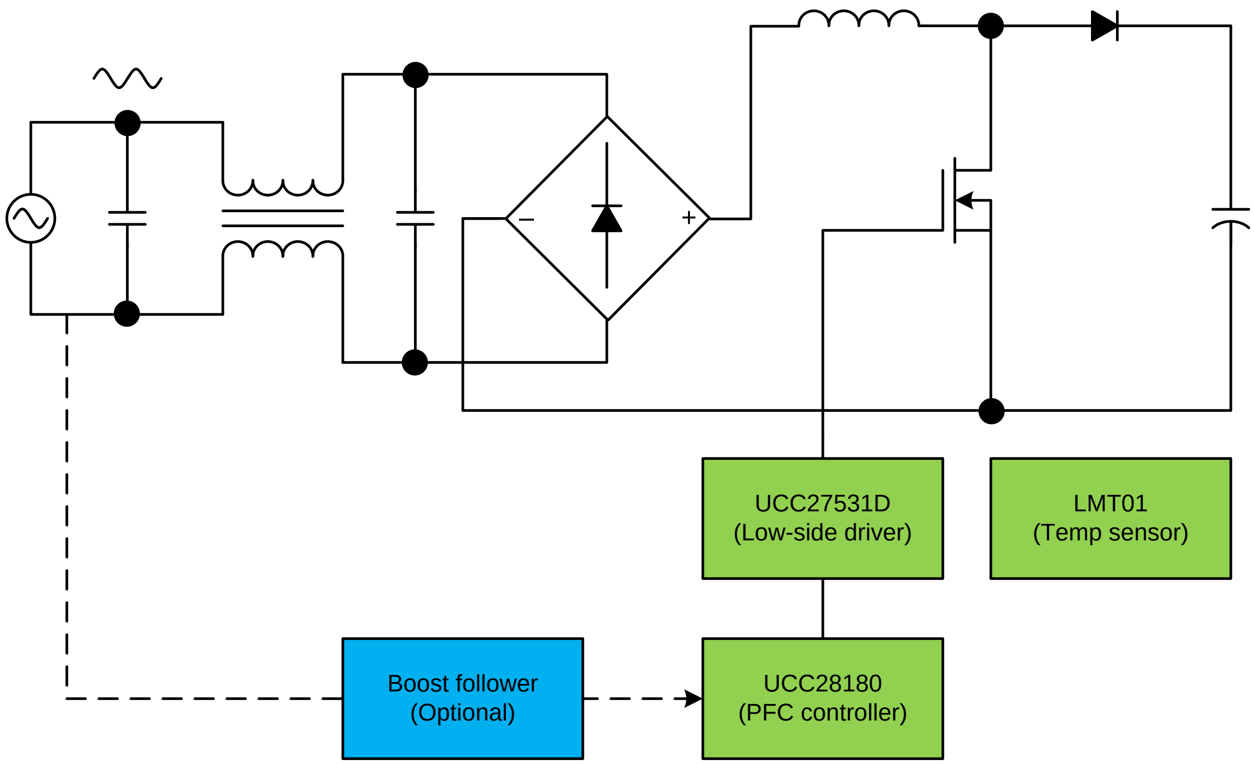


Figure 1. Block Diagram of PFC Regulator

2.2 Highlighted Products and Key Advantages

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. See their respective product datasheets for complete details on any highlighted device.

2.2.1 UCC28180 – PFC Controller

The UCC28180 is a high performance, CCM, 8-pin programmable frequency PFC controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. The UCC28180 uses trimmed current loop circuits to achieve less than a 5% THD from a medium-to-full load (50% to 100%). A reduced current sense threshold enables the UCC28180 to use a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. The UCC28180 also consists of an integrated fast gate driver, with a drive of 2-A source current and −1.5-A sink current, which eliminates the requirement for an external gate driver.

The UCC28180 also has a complete set of system protection features that greatly improve reliability and further simplify the design:

- Soft overcurrent
- Cycle-by-cycle peak current limit
- Output overvoltage
- VCC undervoltage lockout (UVLO) protection
- Open pin protections (ISENSE and VSENSE pins)

2.2.2 UCC27531D – Low-Side Gate Driver

Obtaining a lower level of switching losses is important to achieve high efficiency. The switching losses of a MOSFET are a function of the drive current that is required to quickly pass through the Miller plateau region of the power-MOSFET's switching transition. Placing a high-current gate driver close to a FET allows for a faster turn on and turnoff by effectively charging and discharging voltage across the MOSFET’s gate-to-drain parasitic capacitor (CGD). This placement effectively reduces switching losses.

The UCC27531D is a single-channel, high-speed gate driver can effectively drive MOSFET and IGBT power switch. Using a design that allows for a source of up to 2.5 A and a 5-A sink through asymmetrical drive (split outputs), coupled with the ability to support a negative turn-off bias, rail-to-rail drive capability, extremely small propagation delay (17 ns typical), the UCC27531D are ideal solutions for MOSFET and IGBT power switches. The UCC27531D can also support enable, dual input, and inverting and non-inverting input functionality. The split outputs and strong asymmetrical drive boost the devices immunity against parasitic Miller turn-on effect and can help reduce ground debouncing.

Other key features that make the device ideal for this application are:

- Wide VDD range from 10 to 35 V
- Input and enable pins capable of withstanding up to –5-V DC below ground
- UVLO
- Output held low when input pins are floating or during VDD UVLO

Using an additional gate driver is an optional means to further reduce the switching losses because the UCC28180 controller has an integrated fast gate driver of 2-A source current and −1.5-A sink current, which is sufficient for this design.

2.2.3 LMT01 — Temperature Sensor

The LMT01 is a high-accuracy, 2-pin temperature sensor with an easy-to-use pulse count interface, which makes it an ideal digital replacement for PTC or NTC thermistors both on and off board in industrial and consumer markets. The LMT01 digital pulse count output and high accuracy over a wide temperature range allow pairing with any MCU without concern for integrated ADC quality or availability, while minimizing software overhead. The LMT01 achieves flat ±0.5°C accuracy with very fine resolution (0.0625°C) over a wide temperature range of –20°C to 90°C without system calibration or hardware or software compensation.

Unlike other digital IC temperature sensors, the LMT01’s single-wire interface is designed to directly interface with a GPIO or comparator input, thereby simplifying hardware implementation. Similarly, the LMT01's integrated EMI suppression and simple 2-pin architecture make it ideal for onboard and off-board temperature sensing. The LMT01 offers all the simplicity of analog NTC or PTC thermistors with the added benefits of a digital interface, wide specified performance, EMI immunity, and minimum processor resources. This design uses the LMT01 as the temperature monitor for the MOSFET or IGBT.

Other key features that make the device ideal for this application are:

- Communication frequency: 88 kHz
- Continuous conversion plus data-transmission period: 100 ms
- Conversion current: 34 µA
- Floating 2- to 5.5-V (VP–VN) supply operation with integrated EMI immunity

2.3 System Design Theory

This reference design is a 3.5-kW boost PFC regulator that operates in continuous conduction mode and is implemented using the UCC28180 PFC controller. The design is specifically tailored for inverter fed drives for use in major appliances such as air conditioners. This design serves as a simple and superior alternative to existing bulk, passive PFC circuits that are used to meet the power harmonic standards. The system efficiency is greater than 98% over the wide input operating voltage range from 190-V to 270-V AC under full load conditions. Additionally, this design includes several embedded protections including output overvoltage protection and output short circuit protection.

The main focus of this design is a high efficiency, high PF, and protected DC power rail for targeted applications.

2.3.1 Selecting Switching Frequency

The UCC28180 switching frequency is user programmable with a single resistor on the FREQ pin to GND.

This design uses a 45-kHz switching frequency. Calculate the suitable resistor value to program the switching frequency using Equation 1:

$$R_{FREQ} = \frac{f_{TYP} \times R_{TYP} \times R_{INT}}{\left(f_{SW} \times R_{INT}\right) + \left(R_{TYP} \times f_{SW}\right) - \left(R_{TYP} \times f_{TYP}\right)} \tag{1}$$

where

- f_{TYP}, R_{TYP}, and R_{INT} are constants internally fixed to the controller that are based on the UCC28180 control logic
- f_{TYP} = 65 kHz
- R_{TYP} = 32.7 kΩ
- R_{INT} = 1 MΩ

Applying these constants in Equation 2 yields the appropriate resistor that must be placed between the FREQ and GND pins.

$$R_{FREQ} = \frac{65\text{ kHz} \times 32.7\text{ k}\Omega \times 1\text{ M}\Omega}{\left(45\text{ kHz} \times 1\text{ M}\Omega\right) + \left(45\text{ kHz} \times 32.7\text{ k}\Omega\right) - \left(65\text{ kHz} \times 32.7\text{ k}\Omega\right)} = 47.9\text{ k}\Omega \tag{2}$$

A typical value of 47 kΩ for the FREQ resistor results in a switching frequency of 44 kHz.

2.3.2 Calculating Output Capacitance

Assuming that the percentage of non-conducting period is minimal, the required output capacitance can be calculated as Equation 3 shows:

$$C_O = \frac{2 \times P_{LOAD}}{\pi \times V_O \times \Delta V_O \times f_{LINE}} \tag{3}$$

Where

- ΔV_O = The peak-to-peak voltage ripple on the output
- f_{LINE} = The input line frequency
- P_{LOAD} = The output load power

Insert the values into Equation 3 to obtain the following result:

$$C_O = \frac{2 \times 3500}{\pi \times 390 \times 50 \times 50} = 2286\,\mu\text{F}$$

A capacitance of 2040 µF has been selected to accommodate overload conditions and effects caused by aging.

2.3.3 Calculating PFC Choke Inductor

The UCC28180 is a CCM controller; however, if the chosen inductor allows a relatively high ripple current, the converter becomes forced to operate in discontinuous mode (DCM) at light loads and at the higher input voltage range. High-inductor ripple current affects the CCM/DCM boundary and results in a higher light-load THD. This type of current also affects the choices for the input capacitor, R_{SENSE}, and C_{ICOMP} values. Allowing an inductor ripple current, ΔI_{RIPPLE}, of 20% or less enables the converter to operate in CCM over the majority of the operating range. However, this low-inductor ripple current requires a boost inductor that has a higher inductance value, and the inductor itself is physically large. This design takes certain measures to optimize performance with size and cost. The inductor is sized to have a 40% peak-to-peak ripple current with a focus on minimizing space and the knowledge that the converter operates in DCM at the higher input voltages and at light loads; however, the converter is well optimized for a nominal input voltage of 230-V AC at the full load.

Calculate the minimum value of the duty cycle, D_{MIN}, as Equation 4 shows:

$$D_{MIN} = 1 - \frac{\sqrt{2} \times V_{IN\_MIN} \times \left|\sin\left(2\pi \times f_{LINE} \times t\right)\right|}{V_O} = \frac{\sqrt{2} \times 190 \times 1}{390} = 0.31 \quad (4)$$

Based upon the allowable inductor ripple current of 40%, the PFC choke inductor, L_{BST}, is selected after determining the maximum inductor peak current, I_{PK}, as Equation 5 shows:

$$I_{PK} = \frac{\sqrt{2} \times P_O}{\eta \times V_{IN\_MIN}} = \frac{\sqrt{2} \times 3500}{0.98 \times 190} = 26.6\ \text{A} \quad (5)$$

Calculate the minimum value of the c, L_{MIN}, based upon the acceptable ripple current, I_{RIPPLE}, as Equation 6 shows:

$$L_{MIN} \geq \frac{\sqrt{2} \times V_{IN\_MIN} \times D_{MIN}}{I_{PK} \times 0.4 \times f_{SW}} = \frac{\sqrt{2} \times 190 \times 0.31}{26.6 \times 0.4 \times 45 \times 10^3} = 174\ \mu\text{H} \quad (6)$$

The actual value of the PFC choke inductor used is L_{MIN} = 180 µH

2.3.4 Selecting Switching Element

The MOSFET switch is driven by a gate output that is clamped at 15.2 V internally for VCC bias voltages greater than 15.2 V. An external gate drive resistor is recommended to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit. This resistor also helps by meeting any EMI requirements of the converter. This design uses a 22-Ω resistor; the final value of any design depends on the parasitic elements associated with the layout of the design. To facilitate a fast turnoff, place a standard 100-V, 1-A Schottky diode or switching diode anti-parallel with the gate drive resistor. A 10-kΩ resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect from inadvertent d_V/d_T triggered activations.

The maximum voltage across the FET is the maximum output boost voltage (that is, 425 V), which is the overvoltage set point of the PFC converter used to shut down the output. Considering a voltage de-rating of 30%, the voltage rating of the MOSFET must be greater than 550-V DC.

This design uses an IPW60R099P6 MOSFET of 600 V with 37.9 A at 25°C and 24 A at 100°C. If cost is a concern, this design also can use an IGBT (FGA4060ADF) to replace the MOSFET. This design needs a heat sink of the appropriate size for the MOSFET or IGBT.

2.3.5 Boost Follower Control Circuit

The traditional design of PFC boost converters consists of a fixed output voltage greater than the maximum peak line voltage to maintain boost operation and be able to shape the input current waveform of the power supply. The boost voltage does not have to be fixed, but can be varied based on the AC input voltage provided that the boosted voltage is above the peak input voltage. The boost follower control circuit aids in setting the output voltage based on the peak input voltage.

Varying the output voltage with variations in the peak line voltage provides several benefits.

- *Reduced boost inductor*
  The boost inductor is selected based on the maximum allowed ripple current, at maximum duty cycle, at minimum line voltage, and at minimum output voltage. A decrease in V_{OUT} results in a decrease in the maximum duty cycle, which causes the boost inductor to decrease.
- *Reduced boost switch losses at low line operation*
  In an offline PFC converter, a large amount of converter power loss is due to the switching losses of the boost FET. The boost follower PFC has a much lower output voltage at the low-input line voltage than a traditional PFC boost, which reduces the switching losses.
- *Reduced switching losses in the downstream inverter stage and isolated DC/DC converter stage*
  The switching losses in a three-phase inverter drive or isolated DC/DC converter stage are proportional to the boost regulated voltage. A lower output voltage results in lower switching losses, increasing the overall efficiency of the system, which is more noticeable in the light-load efficiency of the power stage.

2.3.6 Bias Power

The TIDA-00779 design requires an external bias supply to power the UCC28180 PFC controller UCC27531D gate driver, and relay, which is used to shunt the inrush current limiting resistor.

TI recommends powering these devices from a regulated auxiliary supply. These devices are not intended to be used from a bootstrap bias supply. A bootstrap bias supply is fed from the input high voltage through a resistor with sufficient capacitance on the VCC pin to hold the voltage on the VCC pin until the current can be supplied from a bias winding on the boost inductor.

The UCC28180 has a UVLO of 11.5 V and the UCC27531D has a UVLO of 4.5 V, whereas the minimum voltage required to turn on the relay is 9.6 V (for a 12-V relay), so the bias voltage for board operation must be ≥ 12 V. The total current required for these devices is approximately 55 mA.

TI recommends using an external bias power supply of 12 V per 60 mA to power the board independently. The board has been tested and validated with a 12-V bias supply.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Test Conditions

For the input, the power supply source (V_{IN}) must range from 190-V to 270-V AC. Set the input current limit of the input AC source to 25 A.

For the output, use an electronic variable load or a variable resistive load, which must be rated for ≥ 400 V and must vary the load current from 0 mA to 10 A.

3.1.2 Recommended Equipment

Use the following recommended test equipment:

- Fluke 287C (multimeter)
- Chroma 61605 (AC source)
- Chroma 63204 (DC electronic load)
- Voltech PM100 / WT210 (power analyzer)
- Tektronix DPO 3054 (oscilloscope)

3.1.3 Procedure

1. Connect input terminals (P1 and P2) of the reference board to the AC power source.
2. Connect output terminals (P4 and P5) to the electronic load, maintaining correct polarity (P4 is the 390-V DC output and P5 is the GND terminal).
3. Connect an auxiliary supply of 12 V between pin-3 and pin-4 of connector J3, maintaining correct polarity (pin-3 is the bias supply positive input and pin-4 is the GND terminal).
4. Turn on the auxiliary supply and set a voltage of 12 V.
5. Gradually increase the input voltage from 0 V to turn on the voltage of 190-V AC.
6. To test the board independently, short pin-3 and pin-5 of connector J3.
7. Turn on the load to draw current from the output terminals of the PFC.
8. Observe the startup conditions for smooth-switching waveforms.

3.2 Test Results

The following test results cover the steady-state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, surge measurements, and EFT measurements.

3.2.1 Performance Data

3.2.1.1 Efficiency and Regulation With Load Variation

Table 2, Table 3, and Table 4 show the data at inputs of 190-V AC, 230-V AC, and 270-V AC input in using MOSFET and an ultra-fast diode.

Table 2. Performance Data With MOSFET and Ultra-Fast Diode Under 190-V AC Input

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THDi (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	REG (%)
190	0.60	81.7	0.716	15.82	392.8	0.20	78.2	95.68	0
190	0.97	165.9	0.901	11.94	392.7	0.41	160.7	96.84	–0.03
190	1.35	244.6	0.953	3.37	392.6	0.61	237.8	97.20	–0.05
190	1.75	323.1	0.971	5.07	392.6	0.80	314.9	97.45	–0.05
190	2.16	402.0	0.980	6.19	392.6	1.00	392.5	97.63	–0.05
190	4.25	801.0	0.991	4.55	392.6	2.00	784.8	97.98	–0.05
190	6.39	1202.0	0.990	3.28	392.6	3.00	1177.7	97.98	–0.05
190	8.54	1599.0	0.986	3.19	392.7	3.99	1565.8	97.92	–0.03
190	10.75	2003.0	0.981	3.35	392.9	4.99	1959.7	97.84	0.03
190	12.83	2419.4	0.993	1.64	392.9	6.02	2365.3	97.76	0.03
190	14.95	2822.7	0.994	1.76	393.0	7.02	2757.3	97.68	0.05
190	17.06	3225.4	0.995	2.62	393.0	8.01	3147.9	97.60	0.05
190	18.14	3435.1	0.996	2.39	393.1	8.52	3350.0	97.52	0.08

Table 3. Performance Data With MOSFET and Ultra-Fast Diode Under 230-V AC Input

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THDi (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	REG (%)
230	0.62	81.3	0.569	18.74	392.3	0.20	77.2	94.96	–0.05
230	0.90	165.6	0.802	22.51	392.3	0.41	160.2	96.75	–0.05
230	1.18	244.4	0.901	10.20	392.3	0.61	237.6	97.21	–0.05
230	1.49	322.4	0.941	6.39	392.3	0.80	314.8	97.65	–0.05
230	1.82	401.2	0.960	3.54	392.3	1.00	392.4	97.81	–0.05
230	3.52	799.0	0.987	4.88	392.3	2.00	784.6	98.20	–0.05
230	5.26	1198.0	0.990	4.00	392.4	3.00	1177.7	98.31	–0.03
230	7.00	1592.0	0.989	3.65	392.5	3.99	1565.4	98.33	0
230	8.78	1994.0	0.987	3.63	392.6	4.99	1958.5	98.22	0.03
230	10.56	2406.9	0.991	1.67	392.6	6.02	2363.8	98.21	0.03
230	12.30	2808.6	0.993	1.87	392.7	7.02	2755.2	98.10	0.05
230	14.04	3208.3	0.994	2.21	392.7	8.01	3145.9	98.06	0.05
230	15.78	3612.3	0.995	2.40	392.8	9.01	3537.6	97.93	0.08

Table 4. Performance Data With MOSFET and Ultra-Fast Diode Under 270-V AC Input

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THDi (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	REG (%)
270	0.72	81.5	0.421	44.76	392.3	0.20	76.9	94.39	–0.05
270	0.92	165.3	0.663	40.20	392.3	0.41	159.9	96.76	–0.05
270	1.13	243.8	0.801	29.18	392.4	0.61	237.4	97.38	–0.03
270	1.34	321.8	0.886	16.68	392.4	0.80	314.7	97.80	–0.03
270	1.60	400.3	0.927	7.87	392.4	1.00	392.4	98.02	–0.03
270	3.02	797.0	0.978	4.84	392.4	2.00	784.6	98.45	–0.03
270	4.48	1195.0	0.988	4.61	392.4	3.00	1177.6	98.54	–0.03
270	5.94	1588.0	0.990	4.17	392.5	3.99	1565.4	98.57	0
270	7.43	1987.0	0.990	4.10	392.6	4.99	1958.5	98.57	0.03
270	8.96	2399.2	0.992	1.99	392.6	6.02	2363.5	98.51	0.03
270	10.43	2798.1	0.993	2.06	392.6	7.02	2754.5	98.44	0.03
270	11.92	3198.5	0.994	2.35	392.7	8.01	3145.5	98.34	0.05
270	13.41	3599.4	0.994	2.51	392.7	9.01	3536.7	98.26	0.05

Table 5 shows the data at a 230-V AC input in using an IGBT and an ultra-fast diode.

Table 5. Performance Data With IGBT and Ultra-Fast Diode Under 230-V AC Input

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THDi (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	REG (%)
230	0.55	45.0	0.354	16.39	392.5	0.10	41.1	91.33	–0.05
230	1.95	409.3	0.914	8.34	392.5	1.01	398.4	97.34	–0.06
230	3.61	807.2	0.971	5.86	392.4	2.01	790.0	97.87	–0.07
230	5.32	1206.2	0.985	3.90	392.5	3.01	1182.1	98.00	–0.05
230	7.09	1616.4	0.991	3.65	392.5	4.03	1584.8	98.04	–0.05
230	8.83	2017.6	0.993	3.63	392.7	5.02	1977.8	98.03	–0.01
230	10.58	2419.1	0.994	2.64	392.6	6.02	2369.6	97.95	–0.02
230	12.34	2823.2	0.995	1.86	392.8	7.02	2764.0	97.90	0.04
230	14.10	3227.3	0.995	2.47	392.8	8.01	3155.9	97.79	0.03
230	15.88	3637.1	0.996	2.24	393.3	9.00	3551.9	97.66	0.15

3.2.1.2 Efficiency and Regulation With Line Variation

Table 6 and Table 7 show the data for the efficiency and line regulation of the output with AC input voltage variation in using a MOSFET.

Table 6. Performance Data With Fixed Output Voltage in Using MOSFET

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
190	17.18	3247.7	0.995	392.9	8.01	3147.5	96.92
200	16.52	3288.1	0.995	393.1	8.13	3193.9	97.14
210	15.87	3316.6	0.995	393.2	8.21	3228.2	97.33
220	15.33	3356.9	0.995	393.2	8.32	3273.0	97.50
230	14.99	3432.6	0.996	393.3	8.52	3351.7	97.64
240	14.68	3508.1	0.995	393.3	8.72	3429.6	97.76
250	14.54	3619.1	0.996	393.2	9.00	3540.7	97.83
260	13.97	3614.5	0.995	393.3	9.00	3540.8	97.96
270	13.43	3610.5	0.996	393.3	9.00	3540.8	98.07

Table 7. Performance Data With Boost Follower Configuration in Using MOSFET

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
190	17.30	3267.6	0.994	333.1	9.51	3169.1	97.08
200	16.75	3331.4	0.994	340.2	9.52	3240.1	97.26
210	16.24	3392.2	0.995	347.2	9.52	3305.5	97.44
220	15.76	3450.0	0.995	353.5	9.52	3366.0	97.56
230	15.33	3508.5	0.995	360.0	9.52	3427.1	97.68
240	14.95	3568.2	0.995	366.6	9.52	3489.2	97.79
250	14.46	3597.0	0.995	373.2	9.43	3520.0	97.86
260	13.81	3570.0	0.995	380.0	9.20	3496.8	97.95
270	13.23	3552.6	0.995	386.9	9.00	3483.3	98.05

Table 8 and Table 9 show the data for the efficiency and line regulation of the output with AC input voltage variation in using an IGBT.

Table 8. Performance Data With Fixed Output Voltage in Using IGBT

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
190	17.20	3253.0	0.995	392.8	8.01	3144.9	96.68
200	16.55	3295.3	0.995	393.1	8.12	3192.8	96.89
210	15.90	3324.4	0.995	393.3	8.21	3227.8	97.09
220	15.36	3364.5	0.995	393.3	8.32	3272.6	97.27
230	15.02	3439.9	0.996	393.3	8.52	3350.9	97.41
240	14.71	3515.2	0.995	393.3	8.72	3428.7	97.54
250	14.56	3625.3	0.996	393.2	9.00	3540.0	97.65
260	13.98	3620.8	0.996	393.2	9.00	3540.0	97.77
270	13.45	3616.2	0.996	393.2	9.00	3540.0	97.89

Table 9. Performance Data With Boost Follower Configuration in Using IGBT

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
190	17.05	3214.5	0.992	327.2	9.52	3113.6	96.86
200	16.57	3290.6	0.993	335.5	9.52	3192.6	97.02
210	16.12	3363.2	0.993	343.5	9.52	3267.9	97.17
220	15.71	3435.0	0.994	351.4	9.52	3343.6	97.34
230	15.32	3504.1	0.994	358.8	9.52	3414.4	97.44
240	14.97	3571.7	0.994	366.2	9.52	3484.7	97.56
250	14.51	3607.9	0.995	373.7	9.43	3524.0	97.67
260	13.88	3589.1	0.995	381.4	9.20	3509.6	97.79
270	13.31	3574.5	0.995	388.6	9.00	3498.6	97.88

3.2.1.3 No Load Power

The no load power was noted at multiple AC input voltages with the PFC controller enabled. Table 10 and Table 11 show the tabulated results with the fixed output and boost follower configuration.

Table 10. No Load Power With Fixed Output

V_{INAC} (VAC)	I_{INAC} (mA)	P_{INAC} (W)	V_{OUT} (V)	P_{OUT} (W)	NO LOAD POWER (W)
120	260.0	2.3	389.5	0.69	1.61
150	320.0	2.4	389.5	0.69	1.71
180	379.0	2.3	389.5	0.69	1.61
230	476.0	2.3	389.5	0.69	1.61
270	557.0	2.5	389.5	0.69	1.81

Table 11. No Load Power With Boost Follower Configuration

V_{INAC} (VAC)	I_{INAC} (mA)	P_{INAC} (W)	V_{OUT} (V)	P_{OUT} (W)	NO LOAD POWER (W)
120	259.0	1.3	292.0	0.39	0.91
150	317.0	1.4	315.7	0.45	0.95
180	377.0	1.6	336.1	0.51	1.09
230	477.0	2.3	370.3	0.62	1.68
270	558.0	2.6	397.7	0.72	1.88

3.2.2 Performance Curves

3.2.2.1 Efficiency Curves

Figure 2, Figure 3, Figure 4, and Figure 5 show the measured efficiency in the system with AC input voltage variation with and without boost follower configurations. These graphs also compare the efficiency improvement between using a MOSFET and using an IGBT.

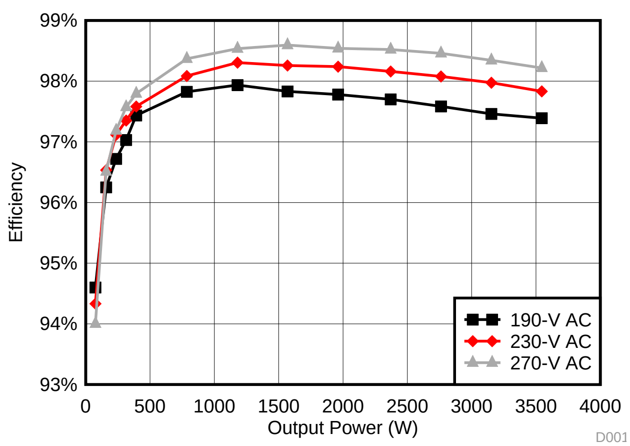


Figure 2. Efficiency With Load Variation in Using MOSFET

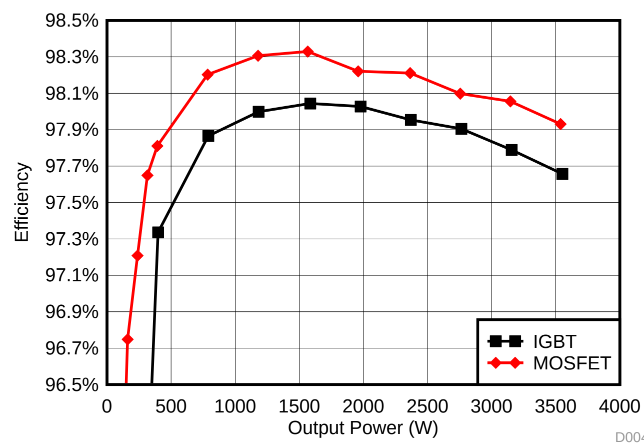


Figure 3. Efficiency Compared Between MOSFET and IGBT

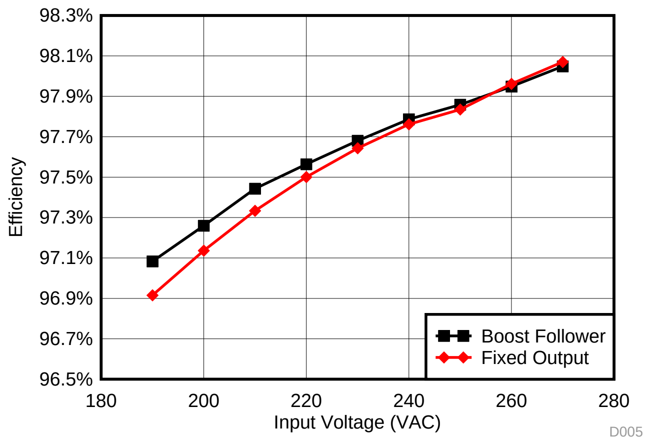


Figure 4. Efficiency versus AC Input Voltage in Using MOSFET

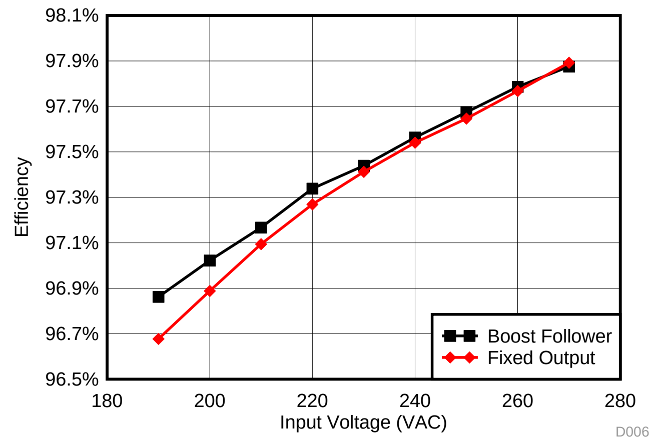


Figure 5. Efficiency Versus AC Input Voltage in Using IGBT

3.2.2.2 PF and THDi Curves

Figure 6 and Figure 7 show the measured PF value and THDi in the system with load variation.

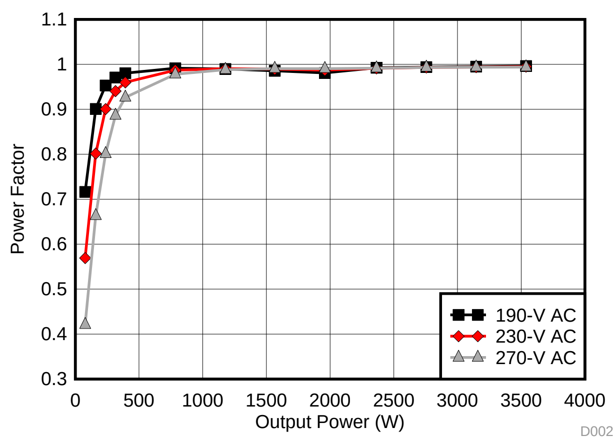


Figure 6. Power Factor With Load Variation

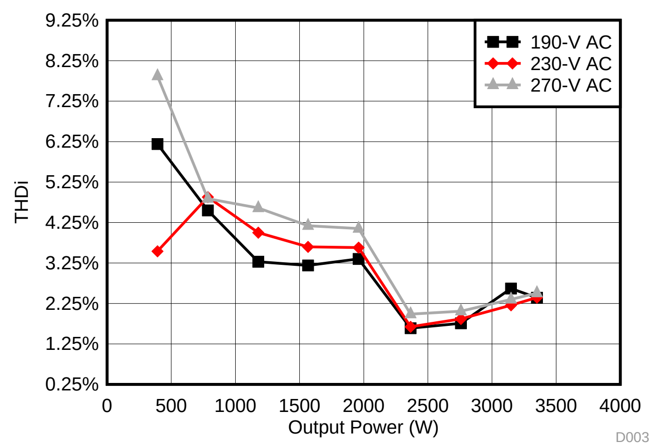


Figure 7. THDi With Load Variation

3.2.3 Functional Waveforms

3.2.3.1 Startup and Shutdown Waveform

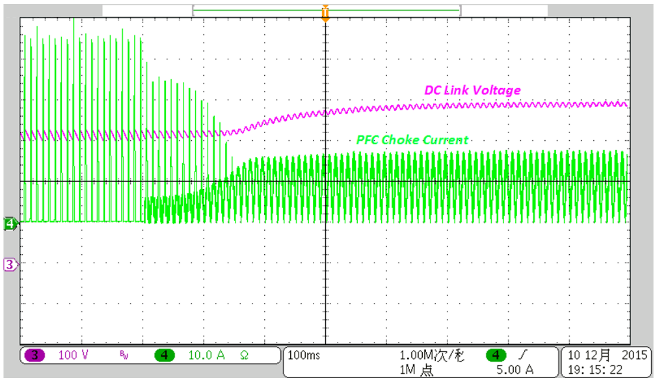


Figure 8. Start-up With Fixed Output Under 230-V AC Input

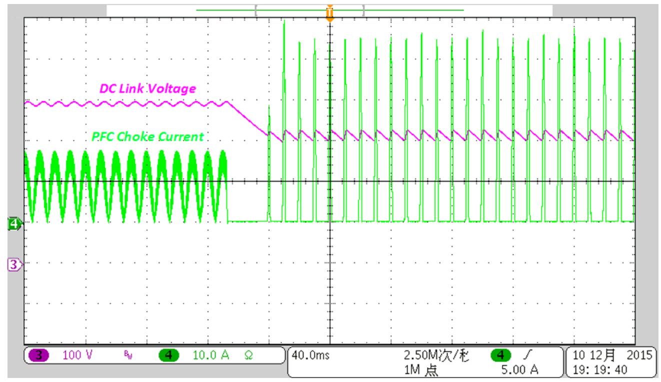


Figure 9. Shutdown With Fixed Output Under 230-V AC Input

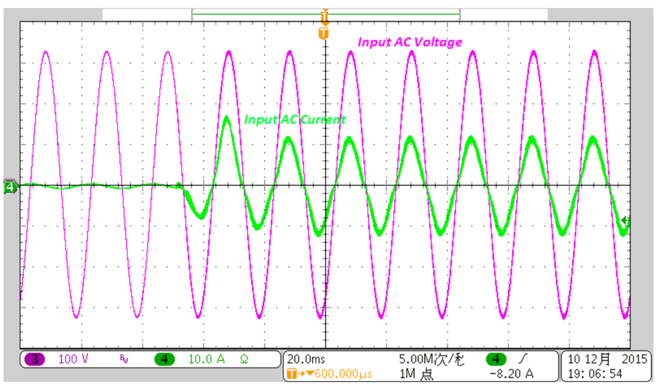


Figure 10. Input Voltage versus Input Current Under Half Load

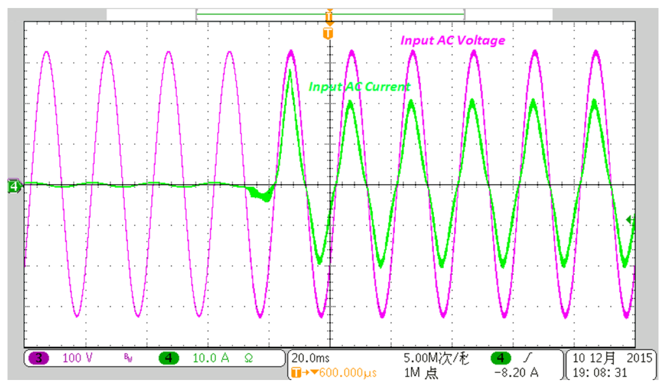


Figure 11. Input Voltage versus Input Current Under Full Load

3.2.3.2 Inrush Current Waveform

Figure 12 and Figure 13 show the inrush current drawn by the system. The inrush current was observed and recorded at a input voltage of 230-V and 270-V AC.

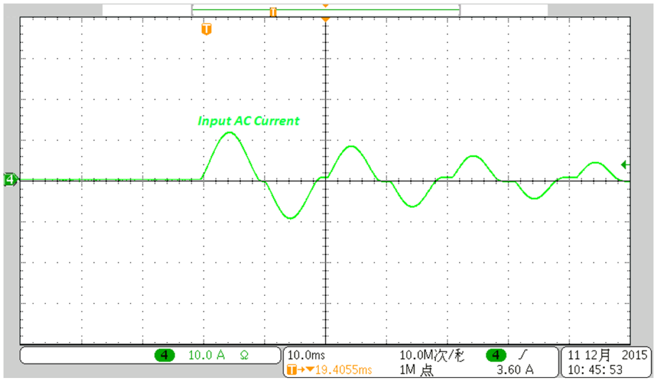


Figure 12. Inrush Current Under 230-V AC Input With No Load

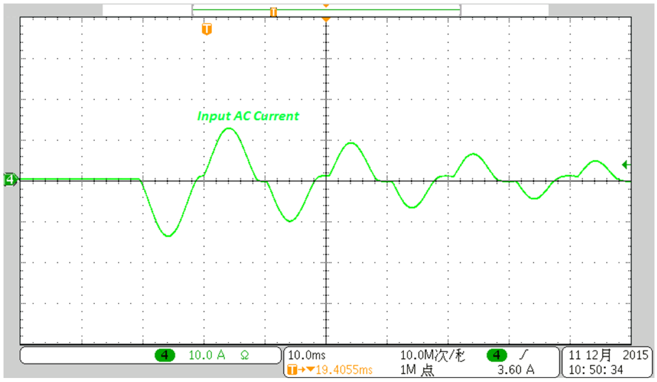


Figure 13. Inrush Current Under 270-V AC Input With No Load

3.2.3.3 Input Voltage and Current Waveform

Figure 14 and Figure 15 show the input current waveform at 230-V AC with a half and full-load condition.

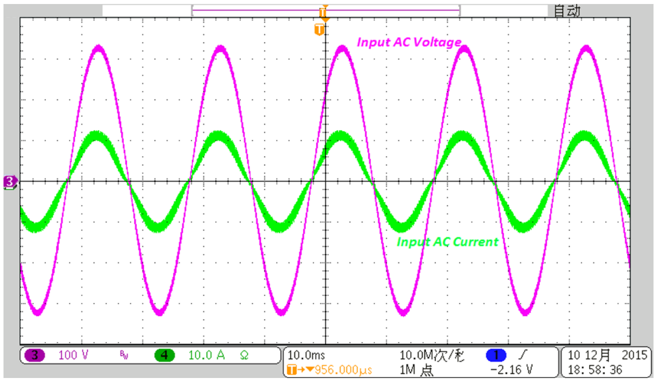


Figure 14. Input Voltage and Current With Half Load Under 230-V AC Input

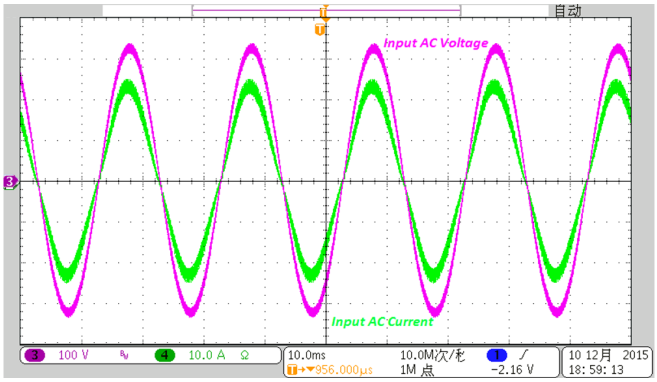


Figure 15. Input Voltage and Current With Full Load Under 230-V AC Input

3.2.3.4 Output Ripple

As Figure 16 and Figure 17 show, the ripple was observed at a 390-V DC output with half load and full load, respectively.

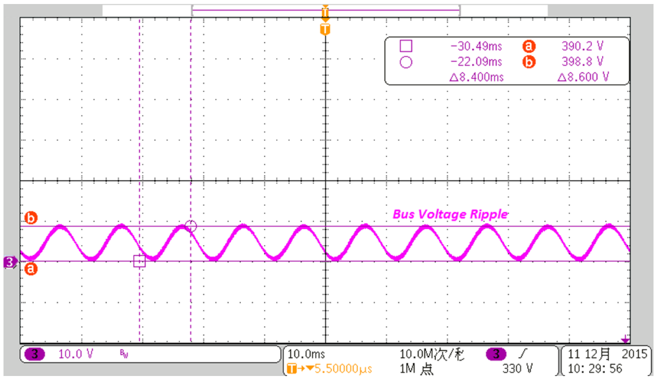


Figure 16. Bus Voltage Ripple Under Half Load

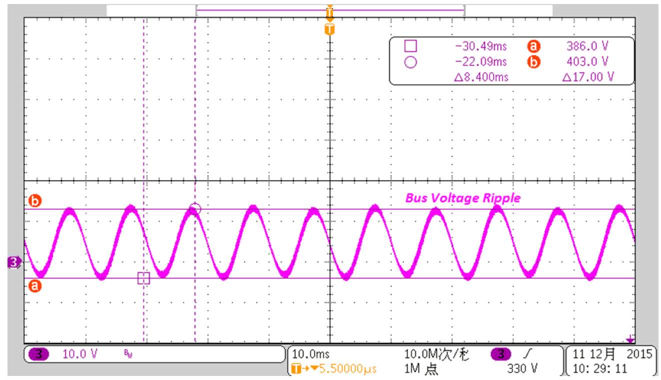


Figure 17. Bus Voltage Ripple Under Full Load

3.2.3.5 Switching Node Waveform

Figure 18, Figure 19, Figure 20, and Figure 21 show the waveforms at the switching node, which were observed along with the MOSFET and IGBT for 230-V AC under full-load conditions.

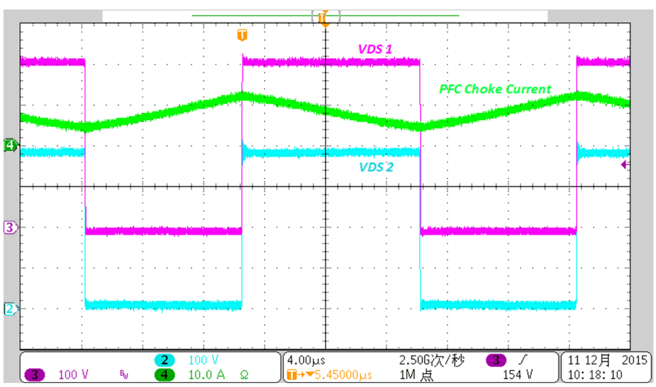


Figure 18. VDS1, VDS2, and PFC Choke Current (MOSFET)

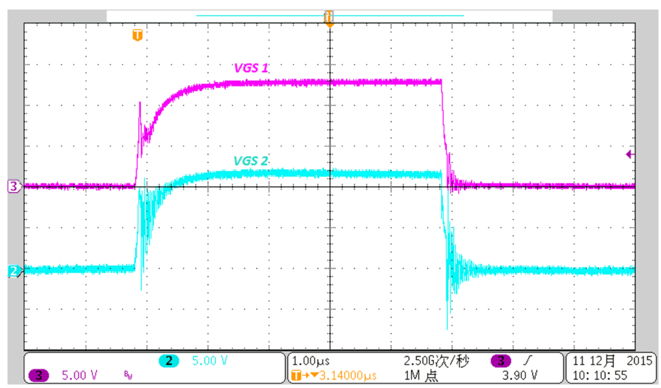


Figure 19. VGS1 and VGS2 (MOSFET)

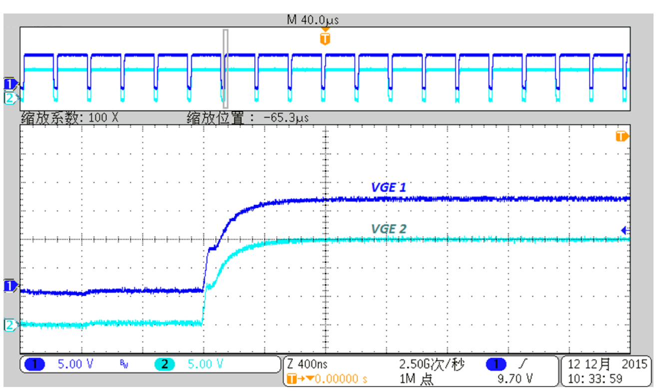


Figure 20. Turn on of VGS1 and VGS2 (IGBT)

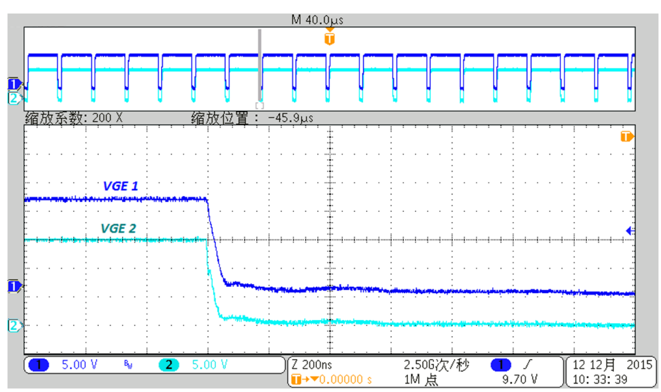


Figure 21. Turn off of VGS1 and VGS2 (IGBT)

3.2.3.6 Transient Waveform

The load transient performance was observed with the load switched at a 0.2-m wire length. The output load is switched using an electronic load.

Figure 22 and Figure 23 show the load transient waveforms for V_{IN} = 230-V AC and a step load transient from 0.5 A to 8 A. Figure 22 shows a step change from 0.5 A to 8 A, and Figure 23 shows a load step down from 8 A to 0.5 A.

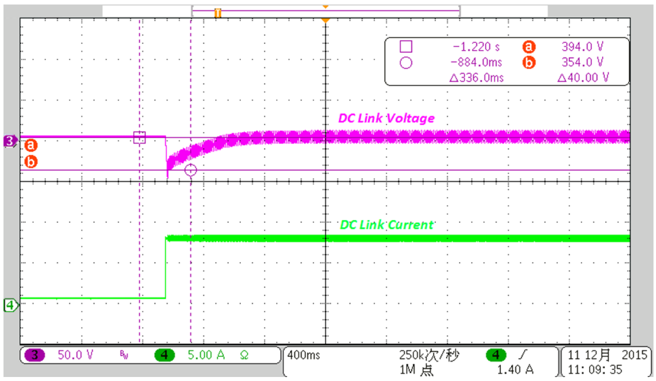


Figure 22. DC Link Voltage versus DC Link Current Under 0.5 A to 8 A

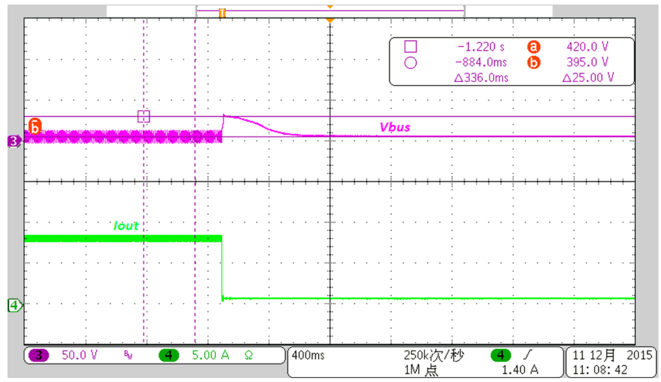


Figure 23. DC Link Voltage versus DC Link Current Under 8 A to 0.5 A

3.2.4 Thermal Measurements

To better understand the temperature of power components and maximum possible operating temperature, the thermal images were plotted at room temperature (25°C) with a closed enclosure, no airflow, and at full-load conditions. The board was allowed to run for 30 minutes before capturing a thermal image.

Figure 24 shows the temperature of power components at input voltage of 230-V AC with the 3.5-kW power output.

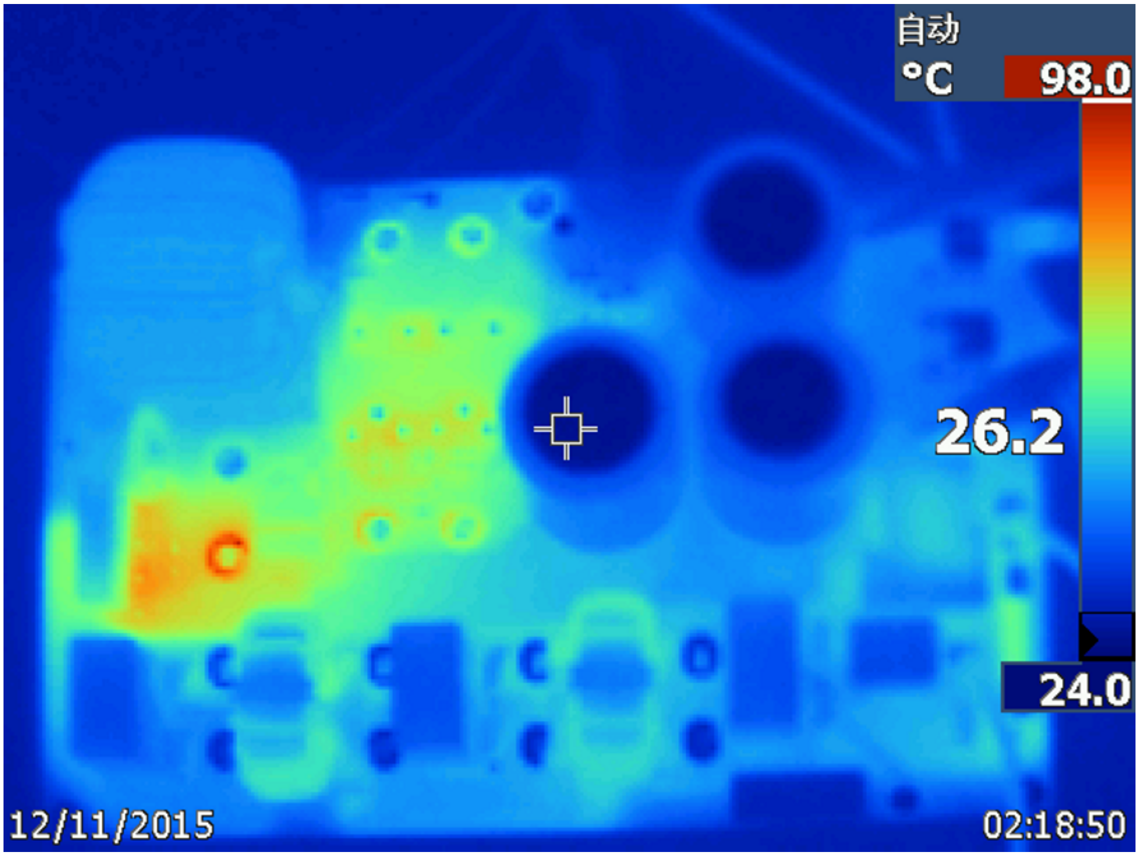


Figure 24. Top-Side Temperatures at 230-V AC Input and 3.5-kW Output

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00779.

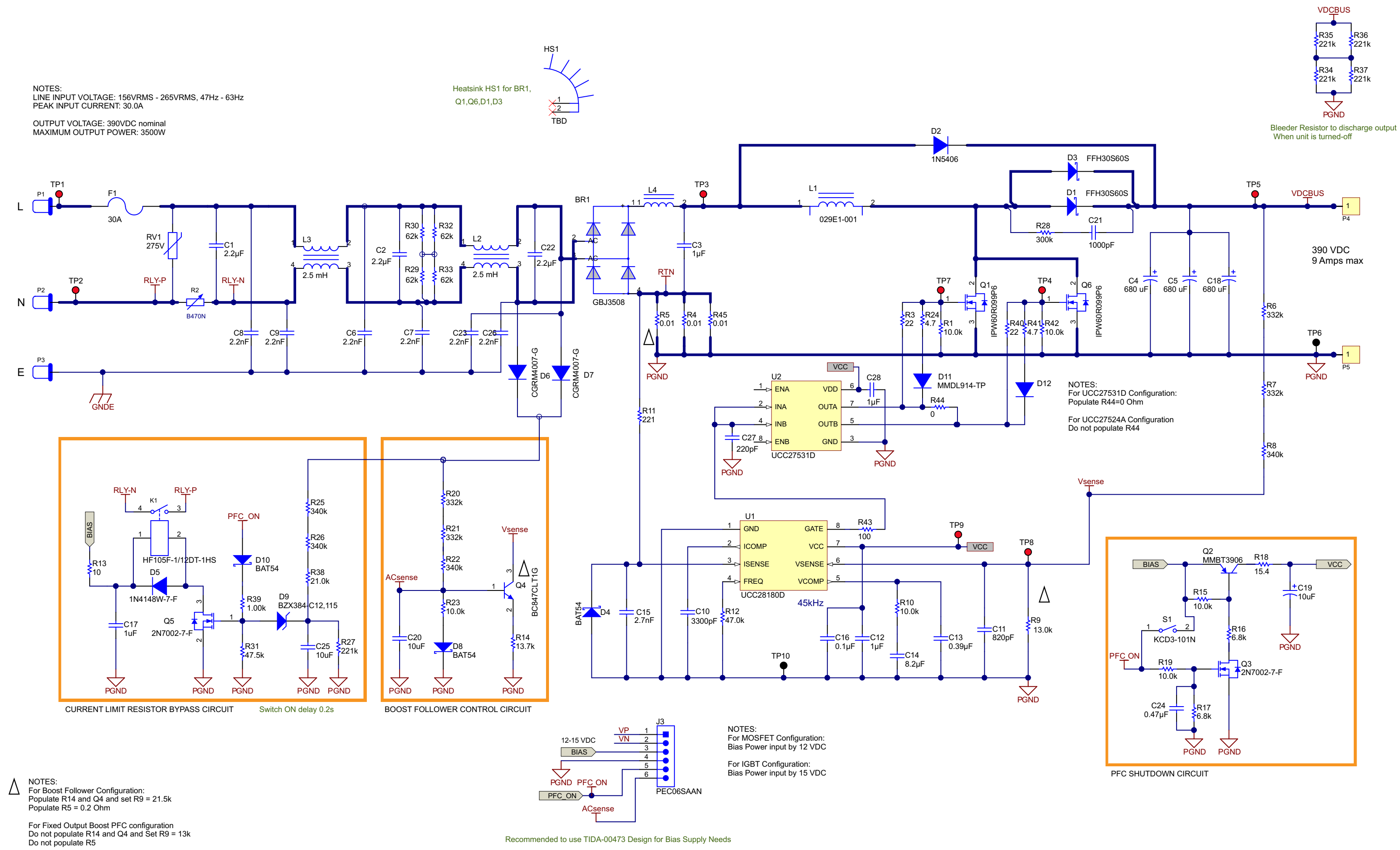


Figure 25. TIDA-00779 Schematics

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00779.

4.3 Layout Prints

To download the layout prints, see the design files at TIDA-00779.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00779.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00779.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00779.

5 References

1. Texas Instruments, *230-V, 900-W, Power Factor Regulator Converter (PFC) for Inverter-Fed Drives and Appliances*, TIDA-00443 Design Guide
2. Texas Instruments, *Using the UCC28180EVM-573 360-W Power Factor Correction Module*, UCC28180EVM-573 User's Guide
3. Texas Instruments, *UCC28180 Programmable Frequency, Continuous Conduction Mode (CCM), Boost Power Factor Correction (PFC) Controller*, UCC28180 Datasheet

5.1 Trademarks

6 About the Author

YUAN (JASON) TAO is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Yuan brings to this role his extensive experience in power electronics, high frequency DC/DC, AC/DC converters, and analog circuit design. Yuan earned his master of IC design and manufacture from Shanghai Jiao Tong University in 2007.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (May 2016) to C Revision	Page
• Changed formatting to fit current design guide template	1
• Changed THD from more than 5% to less than 5%	1

Changes from A Revision (March 2016) to B Revision	Page
• Changed title	1

Changes from Original (January 2016) to A Revision	Page
• Changed from preview page	1

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