**TI Designs**

**12-Gbps BERT Board Reference Design**

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**Design Overview**

The DS125DF1610 BERT board is a small, convenient, and low-cost alternative to a traditional bit error rate tester (BERT). The onboard DS125DF1610 retimer allows for eight channels of pattern generation and eight channels of pattern checking, exceeding the capabilities of most standard BERTs. The retimer locks to an input clock signal from either the onboard LMX2581 clock or an external reference clock and generates a pseudo-random binary sequence. The DS125DF1610 can lock to any frequency in the 9.8- to 12.5-Gbps range or any divide-by-2, divide-by-4, or divide-by-8 sub-multiples of this range.

**Design Features**

- Eight Pattern Generation Channels
- Eight Pattern Checking Channels
- Onboard Low-Jitter Reference Clocks
- Optional External Reference Clock Inputs
- Onboard USB-to-I^2^C for Easy Device Programming
- Status Display LEDs

**Featured Applications**

- Pattern Generation up to 12.5 Gbps
- Pattern Checking up to 12.5 Gbps

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**Design Resources**

- TIDA-00426 Design Folder
- DS125DF1610 Product Folder
- LMX2581 Product Folder
- TCA6424 Product Folder
- MSP430F5529 Product Folder

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**Inputs**

- 2x Onboard Ref Clock
- LMX2581 Clock
- 2x External Ref Clock
- 8x Pattern Checker

**Outputs**

- DS125DF1610 Retimer
- 8x Pattern Generator
- External Power 2.5 V, 3.3 V
- MSP430™ USB2ANY
- TCA6424 GPIO Expander

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1 Key System Specifications

Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rates</td>
<td>DS110DF1610: 8.5 Gbps to 11.3 Gbps</td>
<td>Divide-by-2, divide-by-4, and divide-by-8 also supported</td>
</tr>
<tr>
<td></td>
<td>DS125DF1610: 9.8 Gbps to 12.5 Gbps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DS150DF1610: 12.5 Gbps to 15 Gbps</td>
<td></td>
</tr>
<tr>
<td>Output amplitude</td>
<td>350 mVppd to 1002 mVppd</td>
<td>The step size is approximately 50 mVppd</td>
</tr>
<tr>
<td>FIR</td>
<td>Positive and negative precursor and postcursor, as well as de-emphasis</td>
<td>—</td>
</tr>
<tr>
<td>Data patterns</td>
<td>PRBS7, PRBS9, PRBS15, and PRBS31</td>
<td>—</td>
</tr>
<tr>
<td>Input equalization</td>
<td>Auto-adapting CTLE and DFE</td>
<td>—</td>
</tr>
</tbody>
</table>
2 System Description

The 12-Gbps BERT board is a small, convenient, and low-cost alternative to a traditional bit error rate tester (BERT). The onboard DS125DF1610 retimer allows for eight channels of pattern generation and eight channels of pattern checking, exceeding the capabilities of most standard BERTs. The retimer locks to an input clock signal from either the onboard LMX2581 frequency synthesizer or an external reference clock and generates one of four pseudo-random bit sequences: PRBS7, PRBS9, PRBS15 or PRBS31. The DS125DF1610 can lock to any frequency in the 9.8- to 12.5-Gbps range or any divide-by-2, divide-by-4, or divide-by-8 sub-multiples of this range.

Three pin-compatible parts may be used to generate and check different data rates:

- DS150DF1610 device allows for 12.5 Gbps to 15 Gbps (plus divide-by-2, divide-by-4, or divide-by-8 sub-rates)
- DS125DF1610 device allows for 9.8 Gbps to 12.5 Gbps (plus divide-by-2, divide-by-4, or divide-by-8 sub-rates)
- DS110DF1610 device allows for 8.5 Gbps to 11.3 Gbps (plus divide-by-2, divide-by-4, or divide-by-8 sub-rates)

2.1 DS125DF1610

The DS125DF1610 is a sixteen-channel, multi-rate retimer with integrated signal conditioning features. The device has built-in pattern generation and checking capabilities as well as four 4 × 4 non-blocking crosspoint switches.

In this design, two quads (four-channel blocks) of the retimer are used for pattern generation and two quads are used for pattern checking. Each of the pattern generation quads can lock to either an external clock input or an input from the onboard frequency synthesizer (the LMX2581 in this design). The locked inputs can be broadcasted to one or more of the quad’s outputs and transformed into a pseudorandom binary sequence (PRBS) signal. The DS125DF1610 can output the following patterns: PRBS7, PRBS9, PRBS15, PRBS31, and a 16-bit custom pattern. The other two quads are used to lock to an input signal and check for bit errors.

![Figure 1. DS125DF1610 Simplified Data Path Diagram](image-url)
2.2 **LMX2581**

The LMX2581 is a low-noise, wideband frequency synthesizer that integrates a delta-sigma (ΔΣ) fractional N PLL, multiple core voltage-controlled oscillator (VCO), programmable output divider, and two differential output buffers. The VCO frequency range is from 1880 MHz to 3760 MHz and can be sent directly to the output buffers or divided down by even values from 2 to 38.

In this design, the LMX2581 device provides a low-jitter input onto which the DS125DF1610 device locks. This input is a sub-multiple of the desired lock frequency. For example, for a 10.3125-Gbps signal (5.156-GHz Nyquist), the LMX2581 device may be set to output 5.156 GHz / 2 = 2.578 GHz or 5.156 GHz / 4 = 1.289 GHz.

2.3 **TCA6424A**

This 24-bit input/output (I/O) expander for the two-line bidirectional bus (I²C) has been designed to provide general-purpose remote I/O (GPIO) expansion for a microcontroller (MCU) through the I²C interface.

In this design, the TCA6424 device provides more GPIOs for the onboard MSP430™ MCU from Texas Instruments (TI). These GPIOs are used for various light-emitting diode (LED) indicators for the purpose of showing which pattern generator channels have been enabled and the error status of the pattern-checking channels.

2.4 **MSP430F5529**

The MSP430F5529 is an ultra-low-power MCU with integrated USB and PHY, which supports USB 2.0 as well as many other features.

In this design, the MSP430 MCU provides a USB-to-I²C and a USB-to-MICROWIRE interface to program the devices mentioned in Section 2.1, Section 2.2, and Section 2.3. The USB2ANY firmware is used to interface with the device graphical user interfaces (GUIs).
3 Block Diagram

Figure 2. TIDA-00426 Block Diagram

3.1 Highlighted Products

The TIDA-00426 TI Design features the following devices:

- DS125DF1610
- LMX2581
- TCA6424A
- MSP430F5529

For more information on each of these devices, see their respective product folders at www.ti.com.

3.1.1 DS125DF1610

- Pin-compatible family
  - DS150DF1610: 12.5 Gbps to 15 Gbps
  - DS125DF1610: 9.8 Gbps to 12.5 Gbps
  - DS110DF1610: 8.5 Gbps to 11.3 Gbps
- 4×4-analog crosspoint switch for each quad
- Fully-adaptive continuous-time linear equalizer (CTLE)
- Self-tuning decision feedback equalizer (DFE), with optional continuous adaption
- Configurable VGA
- Adjustable transmit VOD
- Adjustable three-tap transmit FIR filter
- On-chip AC coupling on receive inputs
3.1.2 LMX2581

- Output frequency from 50 MHz to 3760 MHz
- Phase detector frequency up to 200 MHz
- Supports fractional and integer modes
- \(-229 \text{ dBc/Hz}\) normalized PLL phase noise
- \(-120.8 \text{ dBc/Hz}\) normalized PLL 1/f noise
- \(-137 \text{ dBc/Hz}\) VCO phase noise at 1 MHz offset for a 2.5-GHz carrier
- 100-fs RMS jitter in integer mode
- Programmable fractional modulator order
- Programmable fractional denominator
- Three-wire serial interface and readback
- Single-supply voltage from 3.15 V to 3.45 V

3.1.3 TCA6424A

- Operating power-supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P port
  - 2.5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P port
  - 3.3-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P port
  - 5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P port
- \(I^2C\)-to-parallel port expander
- Low standby current consumption of 1 \(\mu\text{A}\)
- 5-V tolerant I/O ports
- 400-kHz fast \(I^2C\) bus
- Input and output configuration registers
- Polarity inversion register
3.1.4 MSP430F5529

- Low supply voltage range: 3.6 V down to 1.8 V
- Ultra-low-power consumption
  - Active mode (AM):
    - All system clocks active:
      - 290 µA/MHz at 8 MHz, 3 V, flash program execution (typical)
      - 150 µA/MHz at 8 MHz, 3 V, RAM program execution (typical)
  - Shutdown mode (LPM4.5):
    - 0.18 µA at 3 V (typical)
- Wake up from standby mode in 3.5 µs (typical)
- Flexible power management system
  - Fully-integrated low-dropout regulator (LDO) with programmable regulated core supply voltage
  - Supply voltage supervision, monitoring, and brownout
- Full-speed universal serial bus (USB)
  - Integrated USB-PHY
  - Integrated 3.3-V and 1.8-V USB power system
  - Integrated 3.3-V and 1.8-V USB power system
  - Eight input and eight output endpoints
4 System Design Theory

The 12-Gbps BERT board uses a DS125DF1610 retimer as an eight-channel pattern generator and checker. For the retimer to be able to perform these functions, the retimer requires a clean, low-jitter source for the CDR to lock to, which is provided by the LMX2581 device or from an external source. Locking requires a clock equal to the Nyquist frequency of the desired data rate divided by 2, 4, or 8.

To optimize the output signal quality, the differential traces have been carefully designed to stay at a 100-Ω differential characteristic impedance to minimize reflections. Megtron6 material has also been used to minimize insertion loss from the board itself.

5 Getting Started Hardware

5.1 Board

Figure 3 shows the important sections of the board. The input references for the DS125DF1610 device are highlighted in green. These references either come from the onboard LMX2581 or from the SMA connectors. The Input Clock Ref 0 section can only be used for pattern generator channels 0 through 3 and the Input Clock Ref 1 section can only be used for pattern generator channels 4 through 7.

The eight-pattern checking inputs are highlighted in yellow. The connectors used are Huber Suhner MXP connectors which require a mate that adapts into SMA connectors. Note that the right side (channels 4 through 7) is not populated in Figure 3.

Figure 3. DS125DF1610BERT Top View
5.2 Board Power Up

Figure 4 shows where to connect power to the terminal block of the board. Two voltages are required: 2.5 V for the DS125DF1610, device and 3.3 V for the LMX2581 device. The MSP430 MCU and TCA6424A device are powered from the USB port. If not using the LMX device as a reference to the DS125DF1610 device (and if only using external clocks in their place), the 3.3-V supply is not required. Note that this design does not have an on-board regulator option (U2 and U3 are not populated and not operational for this board design). Figure 4 shows how external power must be supplied.

5.3 Cable Assemblies

The design EVM uses Huber+Suhner 1x8-MXP cable assemblies (see Figure 5). These assemblies are required to connect the pattern-generator outputs and pattern-checker inputs.

Figure 4. DS125DF1610 Power Inputs

Figure 5. Huber+Suhner 1x8-MXP Cable Assemblies
6 Getting Started Software

6.1 CodeLoader 4

Install the CodeLoader 4 software from the following link: http://www.ti.com/tool/CODELOADER. This software allows for programming of the LMX2581 device. When the board has been plugged in and this software is running, the software may ask to update the firmware of the MSP430 MCU. Follow through the prompts and update the firmware. After having updated, in the Port Setup tab, a device called USB2ANY appears in the drop-down menu (see Figure 6.) Clicking the Identify button makes the LED D9 blink to ensure that communication is in place.

![Figure 6. CodeLoader 4—Port Setup](image-url)
Ensure that the LMX2581 has been selected by clicking the Select Device option in the File menu followed by PLL + VCO and LMX2591, as Figure 7 shows.

![Figure 7. CodeLoader 4—Select Device](image.png)

When the device has been selected, navigate to the File menu and then the Restore option and select one of the files provided with the TI Design download. These files provide the necessary frequencies to lock to common data rates. Alternatively, the device may be manually configured by navigating to the Bits/Pins tab and PLL tab.

### 6.2 SigCon Architect

The SigCon Architect software can be downloaded from the following location: [http://www.ti.com/tool/sigconarchitect](http://www.ti.com/tool/sigconarchitect). This software allows programming for the DS125DF1610 device. After plugging the board in and running this software, the software may ask to update the firmware of the MSP430 MCU. Follow through the prompts and update the firmware. Run the device profile installer provided and select Configuration tab underneath DS125DF1610 in the Selection window (see Figure 8). Select a Slave Address of 0x44 and REF_CLOCK of 312.5 MHZ in the drop-down fields and click the Apply button.
Select the Low Level Page option in the left-side Selection window and click the Load Config button, which Figure 9 highlights with a red box. Load one of the configuration files provided based on the desired configuration (see Table 2).

Table 2. Configuration Files

<table>
<thead>
<tr>
<th>FILE NAME</th>
<th>CLOCK INPUT</th>
<th>DATA RATE</th>
<th>PATTERN GENERATOR OUTPUT(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMX_10G_Config.cfg</td>
<td>LMX2581</td>
<td>10.3125 Gbps</td>
<td>PRBS31: All channels</td>
</tr>
<tr>
<td>LMX_12G_Config.cfg</td>
<td>LMX2581</td>
<td>12 Gbps</td>
<td>PRBS31: All channels</td>
</tr>
<tr>
<td>EXT_10G_Config.cfg</td>
<td>External Input</td>
<td>10.3125 Gbps</td>
<td>PRBS31: All channels</td>
</tr>
<tr>
<td></td>
<td>Clock Ref 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Ref 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXT_12G_Config.cfg</td>
<td>External Input</td>
<td>12 Gbps</td>
<td>PRBS31: All channels</td>
</tr>
<tr>
<td></td>
<td>Clock Ref 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Ref 1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
After having completed the configuration, select the **High Level Page** option in the left-side **Selection** window and then click the **CDR** tab (highlighted with a red box in Figure 10). Click the **Reset CDR All Channels** button and select a channel such as RX/TX 3B, which maps to the pattern generator inputs that Table 3 lists. If the input frequency has been set correctly, the channel indicator displays **CDR Locked**.

This tab may also be used to select custom data rates.
Table 3. Channel Map

<table>
<thead>
<tr>
<th>PATTERN GENERATOR CHANNEL</th>
<th>RETIMER CHANNEL</th>
<th>PATTERN CHECKER CHANNEL</th>
<th>RETIMER CHANNEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG0</td>
<td>CH3B (Quad 1)</td>
<td>PC0</td>
<td>CH0A (Quad 0)</td>
</tr>
<tr>
<td>PG1</td>
<td>CH2A (Quad 1)</td>
<td>PC1</td>
<td>CH1B (Quad 0)</td>
</tr>
<tr>
<td>PG2</td>
<td>CH2B (Quad 1)</td>
<td>PC2</td>
<td>CH0B (Quad 0)</td>
</tr>
<tr>
<td>PG3</td>
<td>CH3A (Quad 1)</td>
<td>PC3</td>
<td>CH1A (Quad 0)</td>
</tr>
<tr>
<td>PG4</td>
<td>CH4A (Quad 2)</td>
<td>PC4</td>
<td>CH6B (Quad 3)</td>
</tr>
<tr>
<td>PG5</td>
<td>CH4B (Quad 2)</td>
<td>PC5</td>
<td>CH7A (Quad 3)</td>
</tr>
<tr>
<td>PG6</td>
<td>CH5B (Quad 2)</td>
<td>PC6</td>
<td>CH6A (Quad 3)</td>
</tr>
<tr>
<td>PG7</td>
<td>CH5A (Quad 2)</td>
<td>PC7</td>
<td>CH7B (Quad 3)</td>
</tr>
</tbody>
</table>

Select the **TX FIR/VOD** tab (see Figure 11) and adjust the FIR taps as required. Ensure that the correct channel has been selected and click the **Apply to Channel** button.

![Figure 11. SigCon Architect—TX FIR/VOD Config](image_url)
To modify the pattern, select the PRBS Gen/Checker tab for the desired channel and modify the pattern type or polarity. The Enable button turns this feature on or off (see Figure 12).

![Figure 12. SigCon Architect—PRBS Gen Config](image)

To check the bit error rate, ensure that one of the pattern generator outputs has been connected to one of the pattern checker inputs through a channel. After performing this step, select the pattern checker channel and click the Reset CDR button so that it locks. If the CDR does not lock, the channel may be too long or there may be an issue with the connections. Select the PRBS Gen/Checker tab and edit the capture period to a finite time or infinite amount of time (see Figure 13). Click the Reset Checker button to ensure that any errors from previous tests have been erased, and click the Turn On button to begin error checking. The PRBS pattern is automatically detected; if it has detected the wrong pattern, too many bit errors must be occurring. Try lowering the amount of insertion loss in the signal path and double check that the input has been configured correctly. The plot displays the number of errors over time. Click the Clear Checker button to clear the graph.

![Figure 13. SigCon Architect—PRBS Checker Config](image)
To evaluate the input signal for a given channel, select the Eye Monitor Page in the left-side Selection window. Select the desired channel and EOM_SEL_VRANGE (400 mV recommended for large inputs) and click the Single Capture button (see Figure 14). The graph displays the eye diagram and the horizontal eye opening (HEO) and vertical eye opening (VEO) values are also displayed, which are very useful parameters to determine the quality of the input. If the eye is very small or closed, the FIR taps at the output may be changed to compensate for insertion loss.

![Figure 14. SigCon Architect—Eye Monitor Page](image-url)
7 Test Setup

As Figure 15 shows, this board was tested with two different configurations. The first configuration is a simple loopback configuration where the DS125DF1610 device checks for bit errors for a given FR4 channel. In the second configuration, the DS125DF1610 device was connected to an oscilloscope. Section 8 shows the oscilloscope screen captures.

Figure 15. Test Setups
8 Test Data

8.1 Eye Diagram

Figure 16 shows the output of one of the PRBS generator channels with no channel other than the board trace and cable. The pattern generator was configured for a 10.3125-Gbps signal with 1.2-Vppd and PRBS7 output, as well as a precursor tap of –2 and postcursor tap of –5.

![Eye Diagram](image)

Figure 16. PRBS7 Eye Diagram

8.2 Time Domain Signal

Figure 17 shows the time domain signal of one of the PRBS generator channels with no channel other than the board trace and cable. The pattern generator is configured for a 10.3125-Gbps signal with 1.2 Vpp and PRBS7 output, as well as a precursor tap of –2 and postcursor tap of –5.

![Time Domain Signal](image)

Figure 17. PRBS7 Time Domain Signal
9 Design Files

9.1 Schematics
To download the schematics, see the design files at TIDA-00426.

9.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-00426.

9.3 PCB Layout Recommendations
The following guidelines must be followed when designing the layout:
• Decoupling capacitors must be placed as close to the VDD pins as possible. Placing them directly underneat the device is one option if the board design permits.
• High-speed differential signals must be tightly coupled, skew matched, and impedance controlled.
• Vias must be avoided when possible on the high-speed differential signals. When vias must be used, take care minimizing the via stub, either by transitioning through mostor all layers, or by back drilling.
• GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
• GND vias must be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

9.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-00426.

9.4 Altium Project
To download the Altium project files, see the design files at TIDA-00426.

9.5 Gerber Files
To download the Gerber files, see the design files at TIDA-00426.

9.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-00426.

10 Software Files
To download the software files, see the design files at TIDA-00426.

11 References

12 About the Author
GUI BORBA is an Applications Engineer at Texas Instruments, where he is responsible for defining, testing, and supporting high-speed signal conditioning and port management devices for data center switch, router, server, and wireless infrastructure systems. Gui earned his Master of Science in Electrical Engineering (MSEE) from Lehigh University in Bethlehem, Pennsylvania. In his spare time, Gui enjoys snowboarding, hiking, and swimming.
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