

PMP11670 Test Results

1 General

1.1 Purpose

This test report is to provide the detailed data for evaluating and verifying the PMP11670 which employs one Buck Converter ---- LM73605 and two USB Charging Port Controllers ---- TPS2549-Q1.

1.2 Reference Documentation

Schematic: PMP11670_Sch.pdf

Gerber: PMP11670_GerberNCdrills.zip

Layer Plot: PMP11670_PCBlayers.pdf

Assembly Drawing: PMP11670_Assy.pdf

CAD File: PMP11670_CAD.zip

BOM: PMP11670_BOM.pdf

1.3 Test Equipment

Multi-meter (current): Fluke 287C

Multi-meter (voltage): Fluke 287C

DC Source: Chroma 62012P-600-8

E-Load: Chroma 63105A module

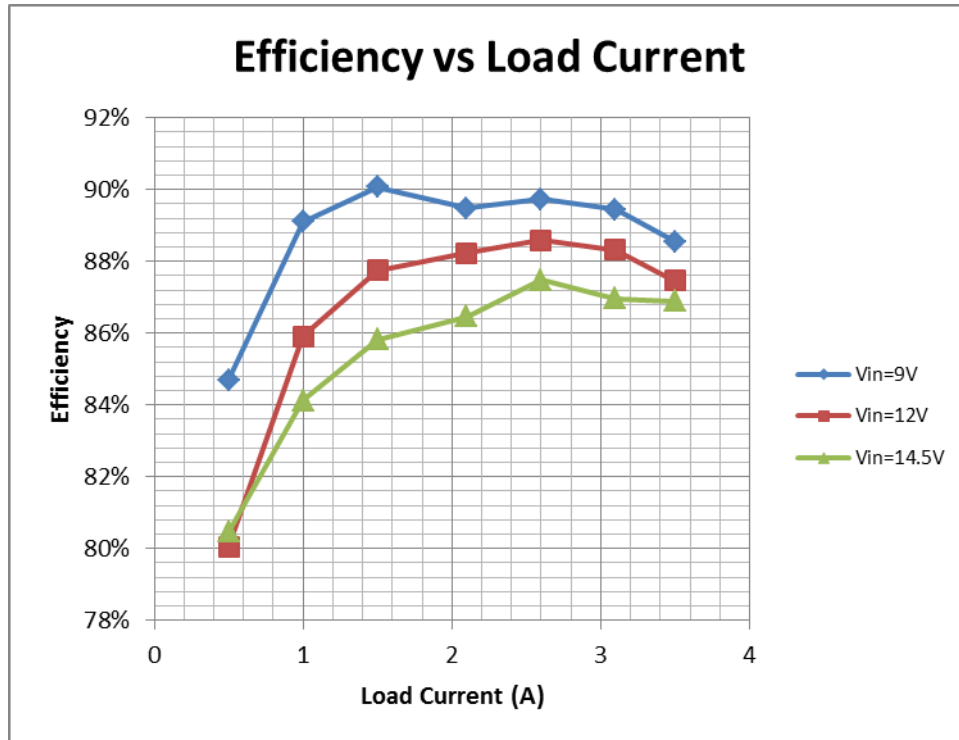
Oscilloscope: Tektronix DPO3054

Electrical Thermography: Fluke Ti9

2 Performance Data and Waveform

2.1 Efficiency

Vin (V)	Iin (A)	Vo1 (V)	Io1 (A)	Vo2 (V)	Io2 (A)	Efficiency
8.98	0.01	5.22	0.01	5.22	0.00	56.99%
8.97	0.34	5.13	0.50	5.17	0.00	84.70%
8.94	0.64	5.09	1.00	5.17	0.00	89.10%
8.91	0.94	5.05	1.50	5.17	0.00	90.06%
8.87	1.32	5.00	2.10	5.16	0.00	89.48%
8.84	1.65	5.00	2.10	5.13	0.50	89.74%
8.81	1.98	4.99	2.10	5.10	1.00	89.45%
8.78	2.25	4.96	2.40	5.08	1.10	88.54%
12.01	0.01	5.22	0.01	5.22	0.00	49.96%
12.00	0.27	5.13	0.50	5.16	0.00	80.06%
11.97	0.50	5.09	1.00	5.16	0.00	85.90%
11.94	0.72	5.05	1.50	5.16	0.00	87.75%
11.90	1.00	5.00	2.10	5.16	0.00	88.24%
11.89	1.24	5.00	2.10	5.12	0.50	88.58%
11.87	1.49	5.00	2.10	5.09	1.00	88.33%
11.85	1.69	4.97	2.40	5.08	1.10	87.46%
14.50	0.01	5.21	0.01	5.22	0.00	49.22%
14.49	0.22	5.13	0.50	5.16	0.00	80.46%
14.47	0.42	5.10	1.00	5.16	0.00	84.12%
14.45	0.61	5.06	1.50	5.16	0.00	85.83%
14.43	0.85	5.02	2.10	5.16	0.00	86.46%
14.40	1.04	5.02	2.10	5.12	0.50	87.49%
14.39	1.25	5.01	2.10	5.07	1.00	86.96%
14.37	1.40	4.96	2.40	5.07	1.10	86.89%

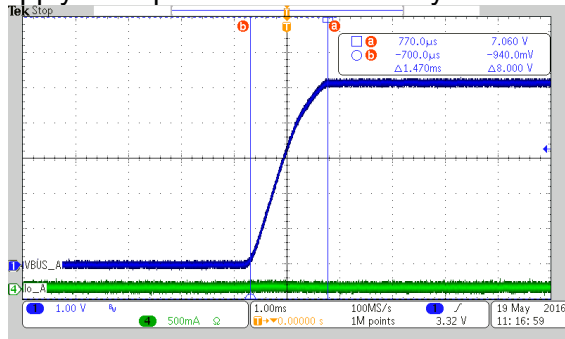


2.2 Standby Current

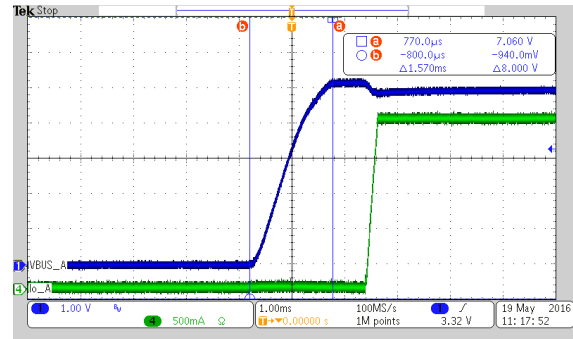
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I _{STD}	Standby current	Vin=9V, All ports unattached		346		uA
	Standby current	Vin=12V, All ports unattached		297		uA
	Standby current	Vin=14.5V, All ports unattached		258		uA

2.2 Start Up

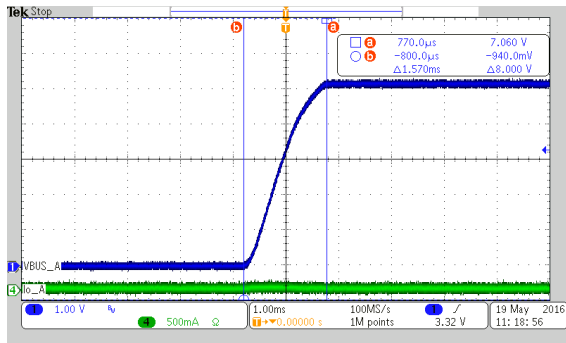
Apply the input source to check system's the soft start.



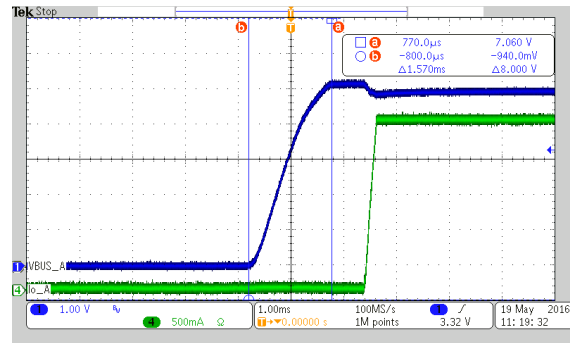
Vin=9V and No Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



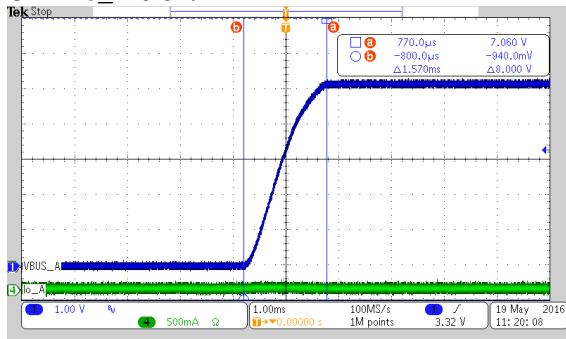
Vin=9V and Full Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



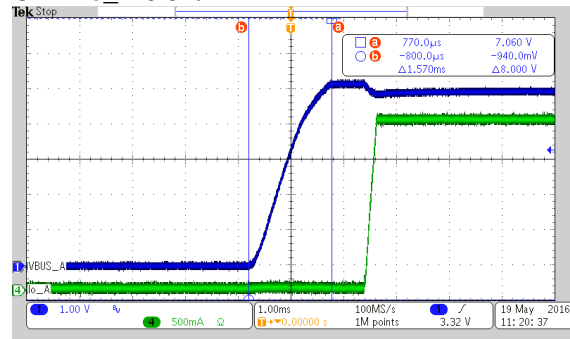
Vin=12V and No Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



Vin=12V and Full Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



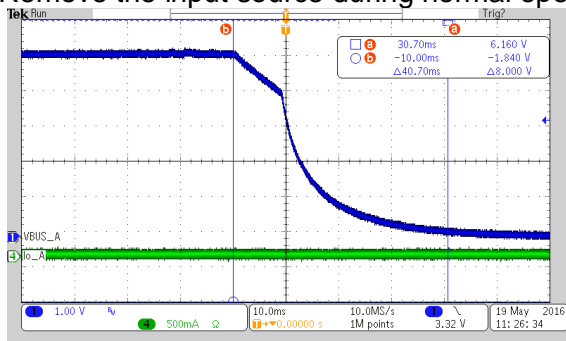
Vin=14.5V and No Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



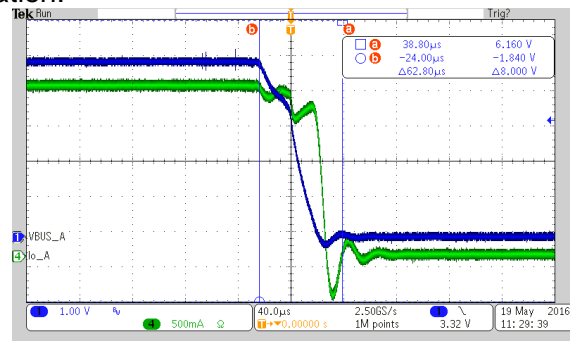
Vin=14.5V and Full Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div

2.3 Shut Down

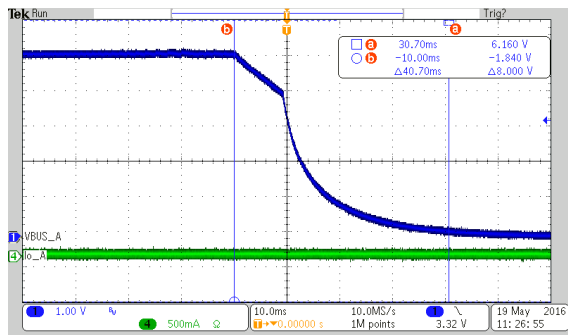
Remove the input source during normal operation.



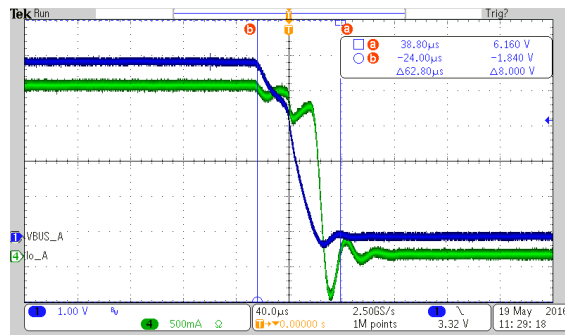
Vin=9V and No Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



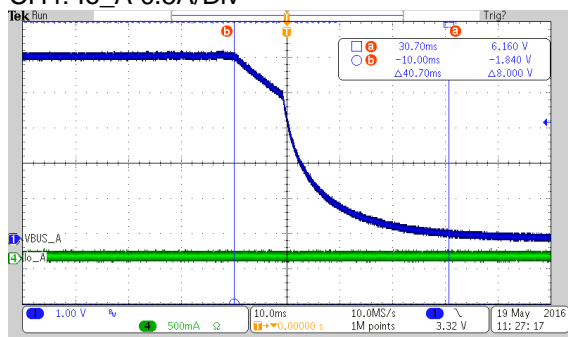
Vin=9V and Full Load
CH1: VBUS_A 1V/Div
CH4: Io_A 0.5A/Div



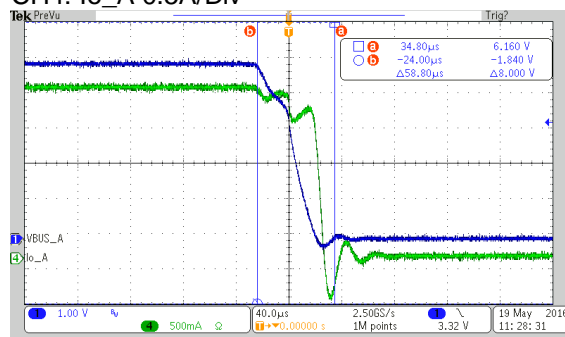
Vin=12V and No Load
CH1: VBUS_A 1V/Div
CH4: io_A 0.5A/Div



Vin=12V and Full Load
CH1: VBUS_A 1V/Div
CH4: io_A 0.5A/Div

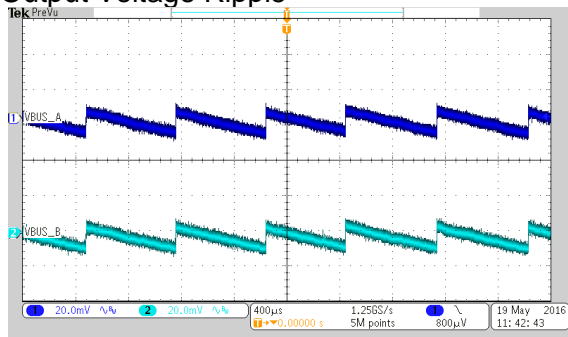


Vin=14.5V and No Load
CH1: VBUS_A 1V/Div
CH4: io_A 0.5A/Div

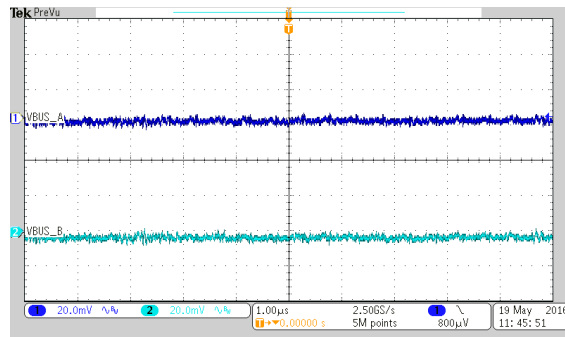


Vin=14.5V and Full Load
CH1: VBUS_A 1V/Div
CH4: io_A 0.5A/Div

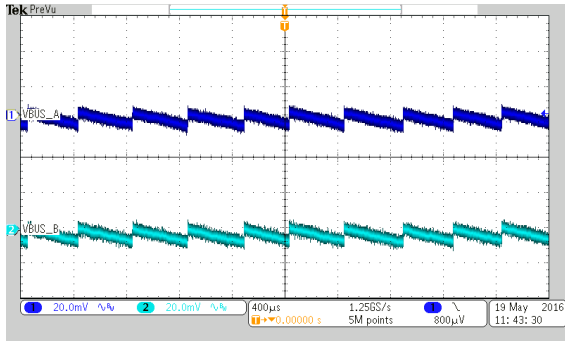
2.4 Output Voltage Ripple



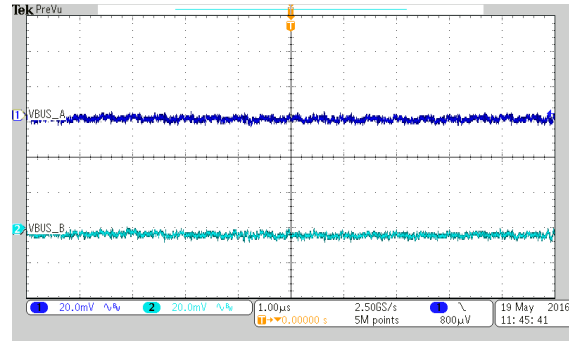
Vin=9V and No Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div



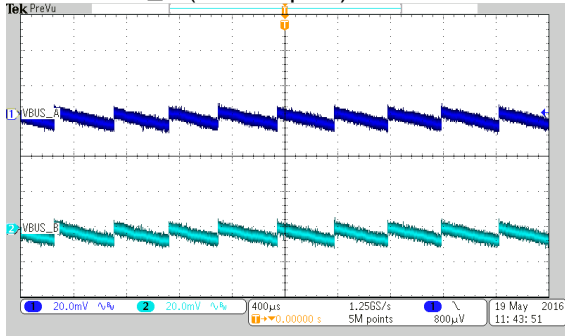
Vin=9V and Full Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div



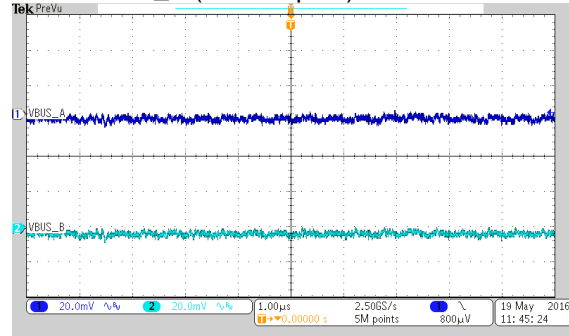
Vin=12V and No Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div



Vin=12V and Full Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div



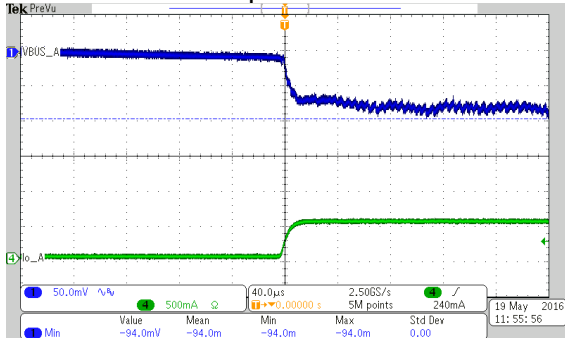
Vin=14.5V and No Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div



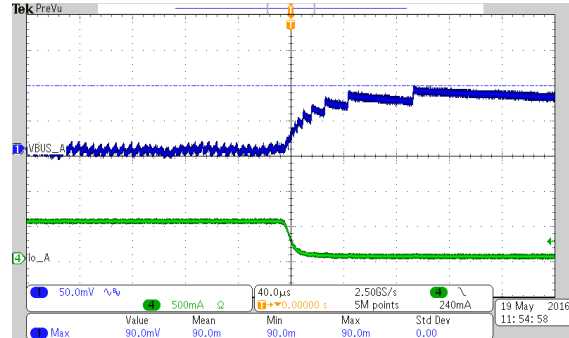
Vin=14.5V and Full Load
CH1: VBUS_A (AC Coupled) 20mV/Div
CH2: VBUS_B (AC Coupled) 20mV/Div

2.5 Dynamic Performance

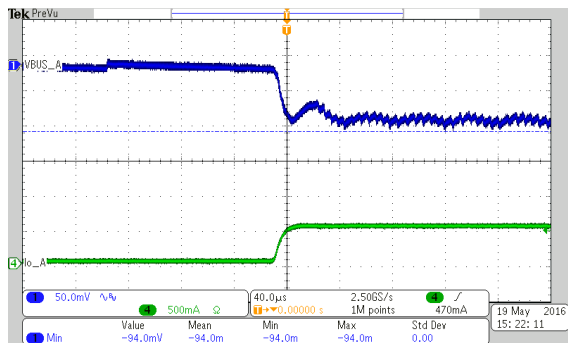
0A↔0.5A Load Step @100mA/µs



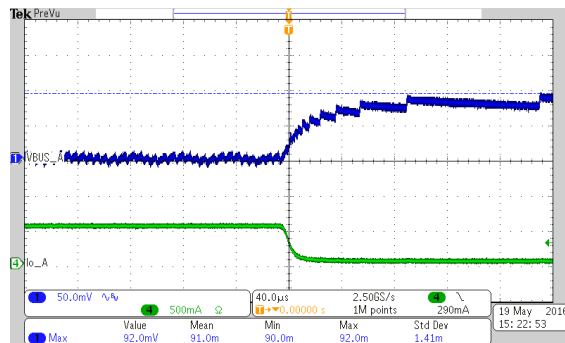
Vin=9V, io_B=0A and Load switching for io_A from 0A to 0.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: io_A 0.5A/Div



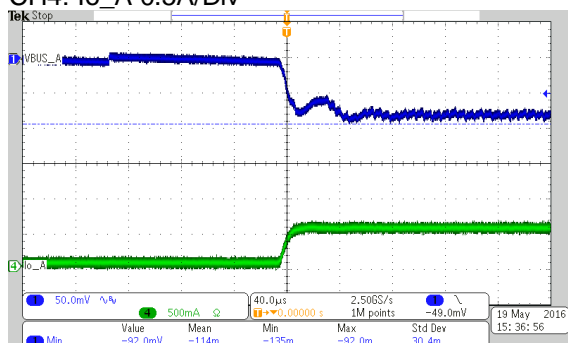
Vin=9V, io_B=0A and Load switching for io_A from 0.5A to 0A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: io_A 0.5A/Div



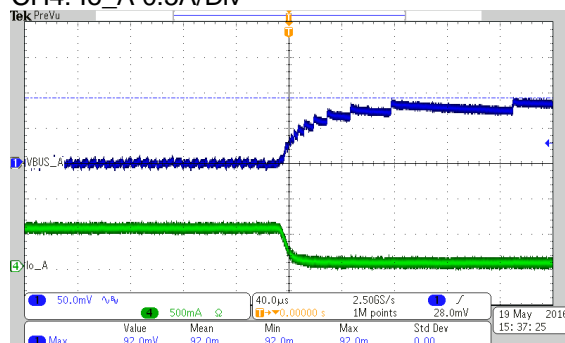
Vin=12V, Io_B=0A and Load switching for Io_A from 0A to 0.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=12V, Io_B=0A and Load switching for Io_A from 0.5A to 0A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

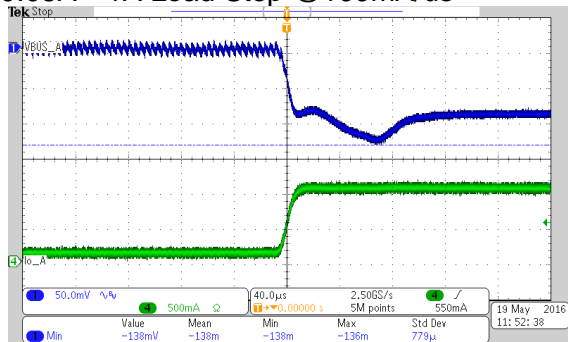


Vin=14.5V, Io_B=0A and Load switching for Io_A from 0A to 0.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

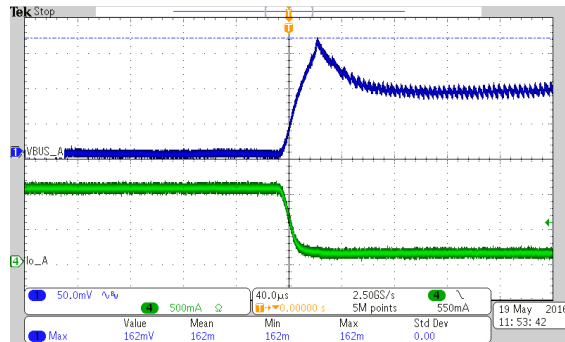


Vin=14.5V, Io_B=0A and Load switching for Io_A from 0.5A to 0A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

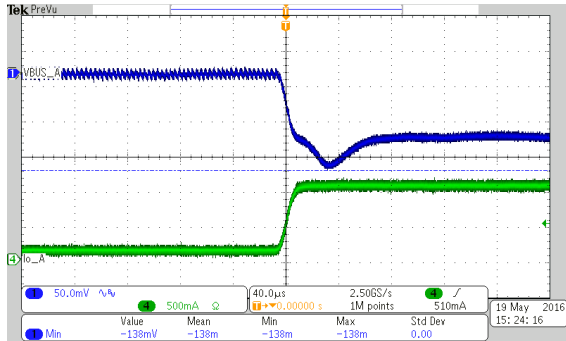
0.08A↔1A Load Step @100mA/us



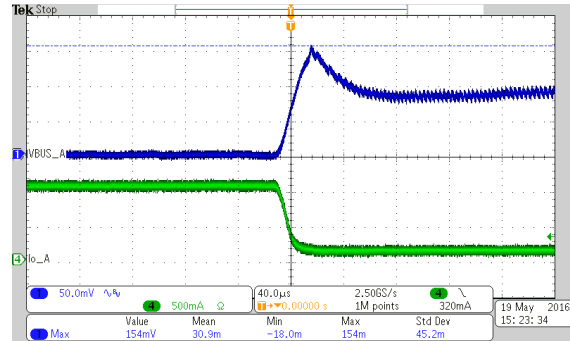
Vin=9V, Io_B=0A and Load switching for Io_A from 0.08A to 1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



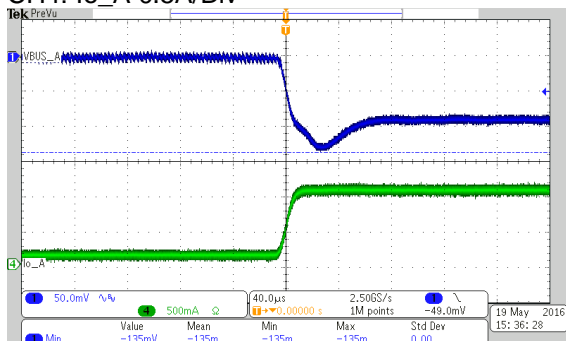
Vin=9V, Io_B=0A and Load switching for Io_A from 1A to 0.08A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



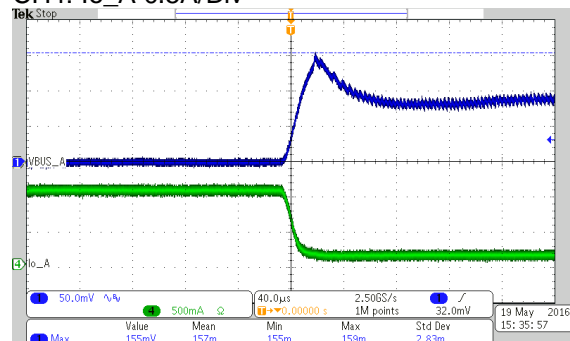
Vin=12V, Io_B=0A and Load switching for Io_A from 0.08A to 1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=12V, Io_B=0A and Load switching for Io_A from 1A to 0.08A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

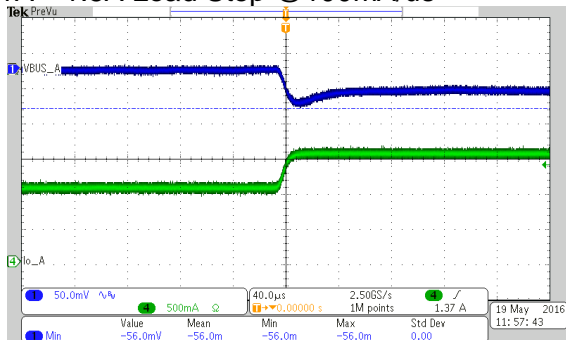


Vin=14.5V, Io_B=0A and Load switching for Io_A from 0.08A to 1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

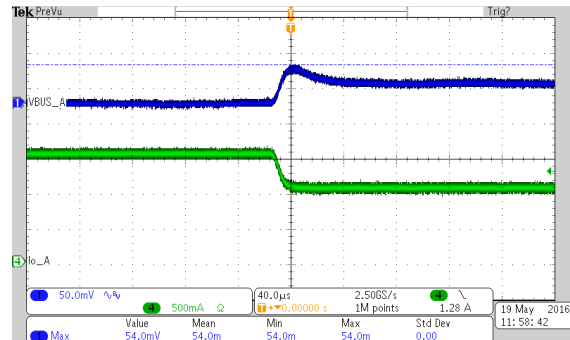


Vin=14.5V, Io_B=0A and Load switching for Io_A from 1A to 0.08A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

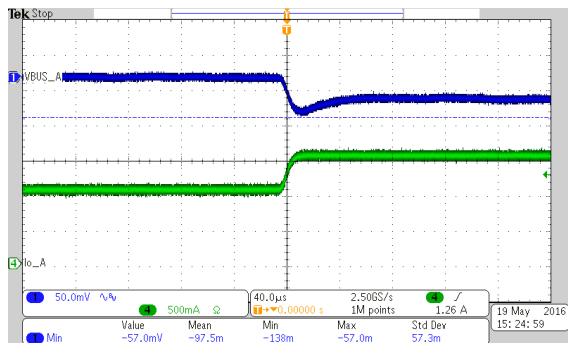
1A↔1.5A Load Step @100mA/us



Vin=9V, Io_B=0A and Load switching for Io_A from 1A to 1.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

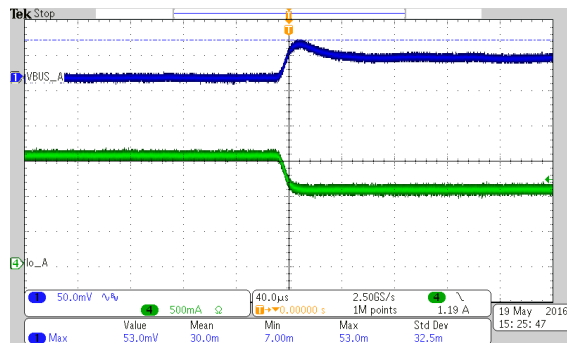


Vin=9V, Io_B=0A and Load switching for Io_A from 1.5A to 1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



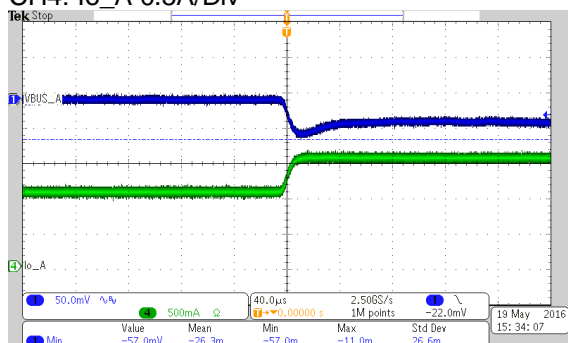
Vin=12V, Io_B=0A and Load switching for Io_A from 1A to 1.5A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



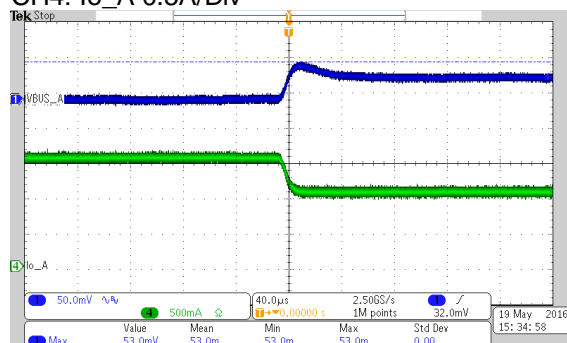
Vin=12V, Io_B=0A and Load switching for Io_A from 1.5A to 1A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=14.5V, Io_B=0A and Load switching for Io_A from 1A to 1.5A

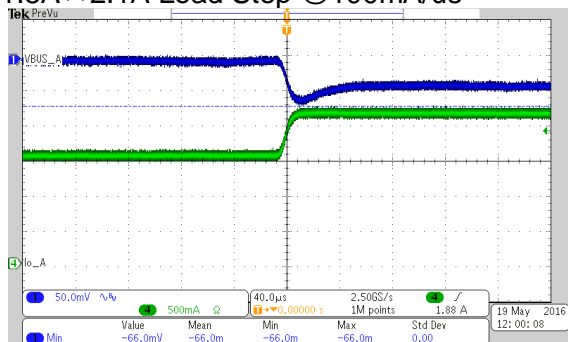
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=14.5V, Io_B=0A and Load switching for Io_A from 1.5A to 1A

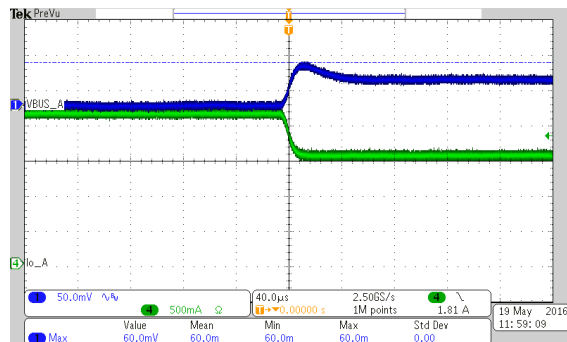
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

1.5A↔2.1A Load Step @100mA/us



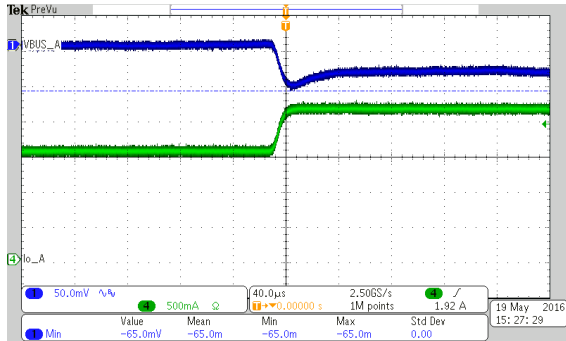
Vin=9V, Io_B=0A and Load switching for Io_A from 1.5A to 2.1A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

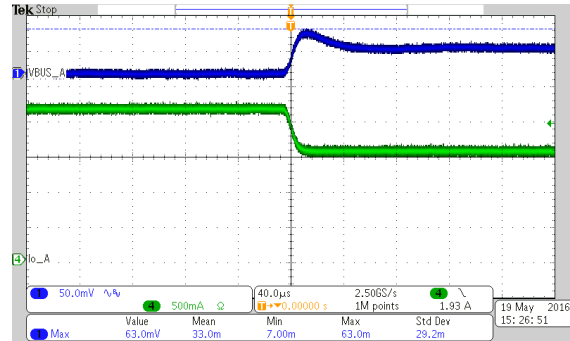


Vin=9V, Io_B=0A and Load switching for Io_A from 2.1A to 1.5A

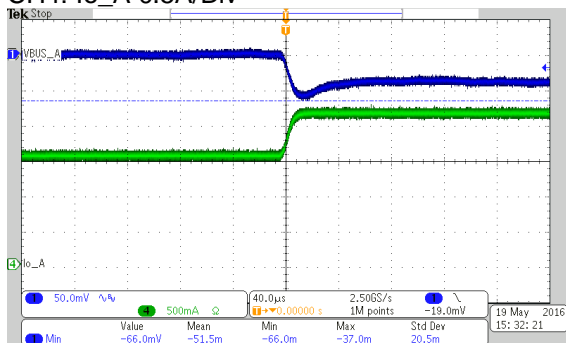
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



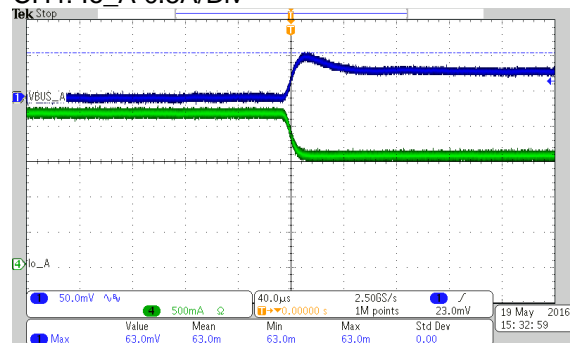
Vin=12V, Io_B=0A and Load switching for Io_A from 1.5A to 2.1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=12V, Io_B=0A and Load switching for Io_A from 2.1A to 1.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

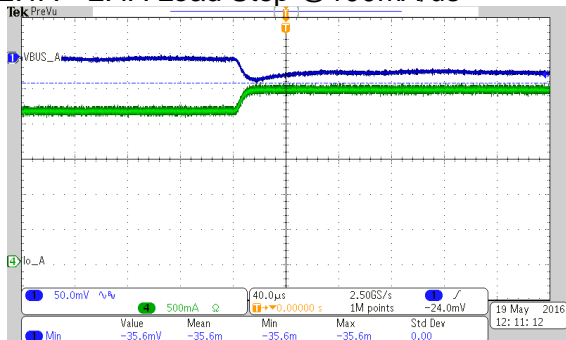


Vin=14.5V, Io_B=0A and Load switching for Io_A from 1.5A to 2.1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

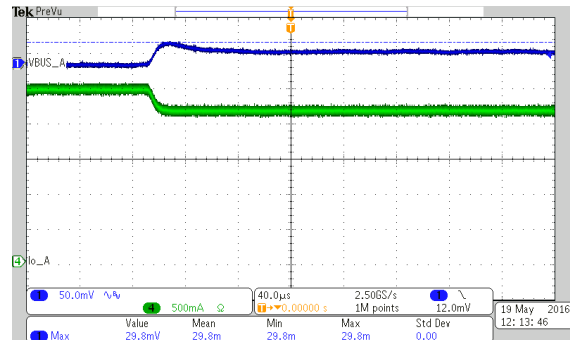


Vin=14.5V, Io_B=0A and Load switching for Io_A from 2.1A to 1.5A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

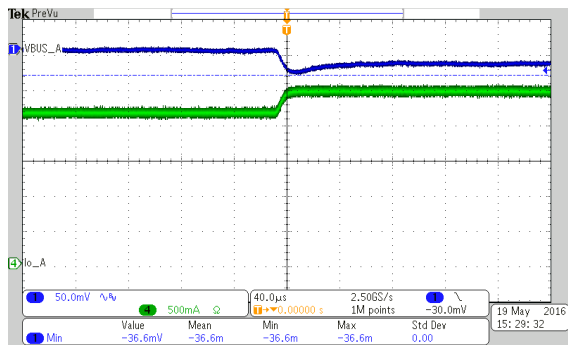
2.1A↔2.4A Load Step @ 100mA/us



Vin=9V, Io_B=0A and Load switching for Io_A from 2.1A to 2.4A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

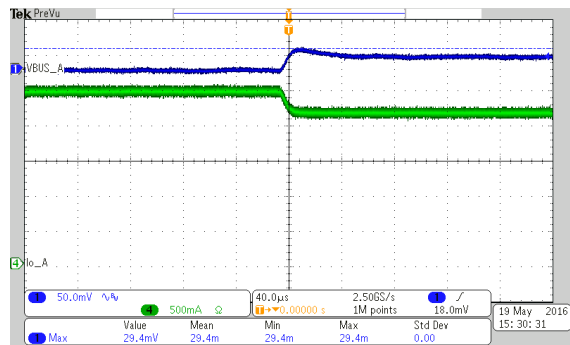


Vin=9V, Io_B=0A and Load switching for Io_A from 2.4A to 2.1A
CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



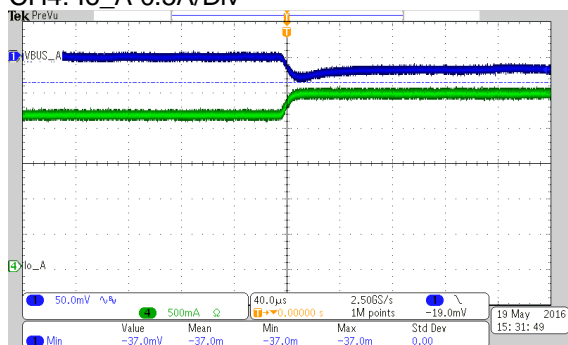
Vin=12V, Io_B=0A and Load switching for Io_A from 2.1A to 2.4A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



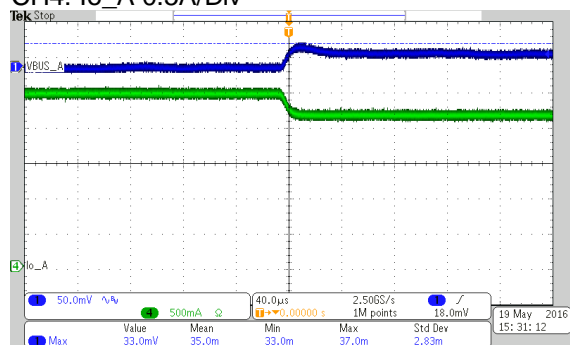
Vin=12V, Io_B=0A and Load switching for Io_A from 2.4A to 2.1A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div



Vin=14.5V, Io_B=0A and Load switching for Io_A from 2.1A to 2.4A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

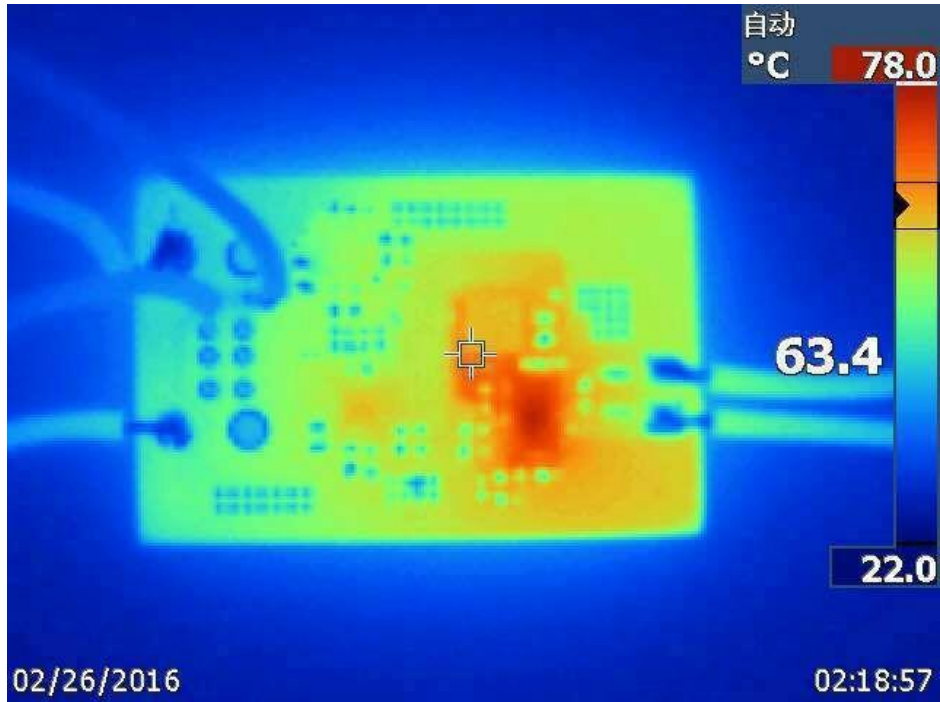


Vin=14.5V, Io_B=0A and Load switching for Io_A from 2.4A to 2.1A

CH1: VBUS_A (AC Coupled) 50mV/Div
CH4: Io_A 0.5A/Div

2.6 Thermal Performance

The board is applied a 12V DC voltage and 3.5A load current for both outputs. Run about 10min for warming up.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated