**Overview**

This TI Design provides a solution for EMC-compliant resolver-to-digital converter (RDC) with a single-chip PGA411-Q1 with a 12-bit angle resolution. The PGA411-Q1’s integrated boost converter and exciter amplifier reduces system cost and board space compared to traditional RDC solutions. On-chip protection and diagnostic improve robustness against short-circuit and increase safety by detecting external fault conditions. A high-speed 3.3-V SPI allows PGA411-Q1 configuration, diagnostics, angle, and velocity information. Example firmware on a C2000™ MCU allow for easy real-time evaluation of the TI Design with angle data available at a 16-kHz sample rate for angle data read-out and register configuration through virtual COM port.

**Features**

- Single-Chip RDC With Typical Accuracy Better Than ±0.2 degrees
- Exceeds IEC61800-3 EMC Immunity
  - ±8-kV ESD CD per IEC 61000-4-2
  - ±4-kV EFT per IEC 61000-4-4
  - ±2-kV Surge per IEC 61000-4-5
- Integrated Exciter Amplifier With 150-mA Output Current and Programmable (10 to 17 V) Boost Power Supply Enables 60% PCB Size Reduction
- 24-V Input With Wide Input Voltage Range (12 to 42 V/60 V) and Reverse Polarity Protection
- SPI (8-MHz, 3.3-V I/O), Parallel and ABZ/UVW Output Interface
- Option to Use External 15-V Exciter Supply and External Exciter Amplifier
- Example Firmware With C2000 MCU to Read Angle at 16-kHz Sample Rate

**Applications**

- Industrial Drives
- Servo Drives
- Multi Axis Robotics Control
- Factory Automation and Control
1 System Overview

1.1 System Description

Industrial drives like servo drives require accurate and high-reliable position feedback. Especially in harsh industrial environment with dust and temperatures above 100°C, resolvers are often used.

This TI Design provides a solution for EMC-compliant resolver-to-digital converter (RDC) with a single-chip PGA411-Q1 with a 12-bit angle resolution. The PGA411-Q1’s integrated boost converter and exciter amplifier reduces system cost and board space compared to traditional RDC solutions. On-chip protection and diagnostic improve robustness against short-circuit and increase safety by detecting external fault conditions. A high-speed 3.3-V SPI allows for PGA411-Q1 configuration, diagnostics, angle, and velocity information. Example firmware on a C2000 MCU allow for easy real-time evaluation of the TI Design with angle data available at a 16-kHz sample rate for angle data read-out and register configuration through virtual COM port.

The major building blocks of this TI Design are:
- The single-chip RDC PGA411-Q1, with integrated RDC, exciter amplifier, and exciter amplifier power supply
- The power management with a 24-V input and 5-V and 3.3-V output
- The interface connector to the resolver
- The host processor interface for PGA411-Q1 configuration and angle and velocity read-out

A simplified system block diagram is shown in Figure 1, with the TI hardware design represented by the box in green. To allow for an easy evaluation of this TI Design, an example firmware is provided for the TMS320F28069M MCU to evaluate the TIDA-00363 performance with the TMS320F28069M InstaSPIN™-MOTION LaunchPad™.

Figure 1. Simplified System Block Diagram of TIDA-00363 With Piccolo™ F28069M LaunchPad

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.
1.2 Introduction to Resolver-to-Digital Conversion

1.2.1 Resolver Basics

A resolver is an absolute mechanical angle sensor. It typically operates as variable coupling transformers, with the amount of magnetic coupling between the primary winding and two secondary windings varying according to the position of the rotating element (rotor), which is typically mounted on the motor shaft. Employed in industrial motor controls, servos, robotics, power-train units in hybrid- and full-electric vehicles and many other applications that require precise shaft rotation, resolvers can withstand severe conditions for a very long time, making them the perfect choice for industrial systems in harsh environments.

As shown in Figure 2, a resolver sensor has one rotor winding (R1-R2) with the exciter sine wave that is AC-coupled to two stator windings. The stator windings, a sine coils (S2-S4) and a cosine coil (S1-S3), are mechanically positioned 90 degrees out-of-phase. As the rotor spins, the rotor position angle ($\theta$) changes with respect to the stator windings. The rotor and stator windings have a turns ratio in the order of 30%. The resulting amplitude modulated signals shown in Figure 1 are typical resolver output signals. These signals must be conditioned, demodulated and post processed to extract angle and velocity information.

![Figure 2. Representation of Resolver Signals: Exciter, Sine, and Cosine](image)

For more details on the basics on resolver and conversion principle, see the application report *Design considerations for resolver-to-digital converters in electric vehicles* (SLYT661).
1.2.2 Resolver-to-Digital Conversion—Theory of Operation

For a resolver, the primary winding is excited with the sine wave reference signal, and two output signals, sine and cosine, are electromagnetically induced on the secondary windings. An RDC generates the resolver excitation signal and decodes the absolute angle and optional angular speed from the sine and cosine amplitude modulated signals.

There are typically two different methods applied to demodulate the resolver’s sine and cosine output signals and calculate the angle.

One method leverages the arctangent method with optional Type-II low-pass tracking filter for improving angular resolution and angular speed at zero velocity lag in steady state. This method is often implemented with microcontrollers like the C2000 MCU. A simplified block diagram is shown in Figure 3. This method typically requires a dual, simultaneous sampling 12-bit ADC and buffers and amplifiers for the analog signal chain. For more details on this method, see the white paper Reduce system costs with RDC implementation on C2000™ Delfino™ microcontrollers (SPRY212).

The other method, as implemented on the PGA411-Q1 and used with this TI Design, leverages analog multiply and subtract along with a Type-II PI digital tracking loop to perform angle and velocity calculations. Type-II loops use a second-order filter to ensure that steady-state errors are zero for stationary or constant-velocity input signals. This architecture enables the PGA411-Q1 to support up to 200,000 RPM in 10-bit mode. This method does not require analog-to-digital converters. For a detailed block diagram, see the PGA411-Q1 datasheet (SLASE76).
1.3 **Block Diagram**

The system block diagram for the TIDA-00363 is shown in Figure 3.

The major building blocks of this TI Design are the RDC, the power management, and the interfaces to the resolver and host microcontroller for display of angle position. To allow for easy evaluation of the TIDA-00363 design, an example firmware is provided for the F28069M Piccolo LaunchPad, which outputs the angle position through virtual COM port. The PGA411-Q1 is single-chip RDC IC with an integrated excitation amplifier and 10- to 17-V boost converter for excitation amplifier. This integration eliminates need for an external power supply and exciter amplifier (until a 150-mA output current) and reduces the bill of material (BOM) and PCB size by nearly 60%. The fault diagnostics feature of the PGA411-Q1 eliminates need for external monitoring, supervisors, and protection circuits. Its wide input voltage range from 15 to 42 V/60 V (typical 24 V) with reverse polarity protection provides the necessary voltages for the PGA411-Q1. The power supply uses non-isolated buck converter TPS54140A, which has a pin-drop option for the 60-V input device TPS54160A as well. A jumper selects between internally generated boost supply (default) or external provided 15-V supply for the PGA411-Q1 excitation amplifier. The TPS79933 is used for generating an IO voltage of 3.3 V for the PGA411-Q1. A Sub-D9 connector and an additional 6-pin header provide flexibility to connect a resolver. Two 20-pin connectors are provided to provide multiple interface options (SPI, parallel, ABZ, UVW) to the host processor.

1.4 **Highlighted Products**

The following subsections highlight key features of the highlighted devices.
1.4.1 PGA411-Q1

The PGA411-Q1 is a highest integration RDC accepting up to 20-kHz sine and cosine signals from the resolver sensor to output a 10- or 12-bit digital word representing angle or velocity. The resolver can be excited by the PGA411-Q1 on-chip excitation amplifier with sine wave input referenced to internally or externally generated clock. Optionally, an external amplifier can be used to extend the output current capability beyond 150 mA. The PGA411-Q1 is also equipped with a boost regulator supplying power to the onboard excitation amplifier. A tracking loop employing a Type-II PI Controller is integrated to determine the angle and velocity value based on the input signals. The maximum tracking rate of the device is 200,000 rpm. The integrated continuous diagnostics monitor and the internal diagnostics engine can signal a fault condition by a dedicated pin, which can be used as an MCU interrupt.

1.4.2 TPS54140A

The TPS54140A device is a 42-V, 1.5-A, step down regulator with an integrated high-side MOSFET. Current mode control provides simple external compensation and flexible component selection. A low-ripple pulse skip mode reduces the no-load, regulated output supply current to 116 μA. Using the enable pin, shutdown supply current is reduced to 1.3 μA. Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow start pin that can also be configured for sequencing/tracking. An open-drain power good signal indicates the output is within 94% to 107% of its nominal voltage. A wide switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition.

1.4.2.1 Drop-in Compatible Version to 60 V—TPS54160A

The TPS54160A is pin-to-pin compatible DC/DC buck converter with an input voltage up to 60 V. For applications requiring 60-V input voltage, this device is a drop-in replacement for the TPS54140A.

1.4.3 TPS79933

The TPS799 family of low-dropout (LDO), low-power linear regulators offers excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40-μA (typical) ground current. The TPS799 is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of typically 100 mV at a 200-mA output. The TPS799 uses a precision voltage reference and feedback loop to achieve an overall accuracy of 2% over all load, line, process, and temperature variations. The TPS799 features inrush current protection when the EN toggle is used to start the device, immediately clamping the current.
2 System Specifications and Design Features

The TI Design TIDA-00363 realizes an industrial temperature range, EMC-compliant, single-chip solution for RDCs. The major building blocks of this TI Design are the PGA411-Q1 (single-chip RDC), the power management block and interfaces to resolver as well as the serial SPI and optional parallel interface to a host microcontroller for displaying accurate angle position.

To allow for evaluation of this TI Design, an example firmware is provided for the example firmware is provided for the TMS320F28069M MCU to evaluate the TIDA-00363 performance with the TMS320F28069M InstaSPIN™-MOTION LaunchPad™. The TMS320F28069M displays the 10- or 12-bit angle position for resolver through a USB virtual COM port.

The TIDA-00363 has following design features:

- Single-chip RDC with an integrated boost converter for exciter amp supply and integrated exciter amp with a 150-mA output current
- Single-chip R2D with programmable fault detection thresholds and filters, analog and logic BIST, protection against short to power supply
- EMC immunity: Meets IEC61000-4-2, 4-4, and 4-5 (ESD, EFT, and surge) as specified in the standard IEC61800-3 EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems
- Wide input voltage range: 24 V (15 to 42 V/60 V) with reverse polarity protection provides the necessary voltages for the PGA411-Q1. The power supply uses non-isolated buck converter, which has pin-drop option for 60-V input device as well
- Option to use an external 15-V supply and external exciter
- Flexible I/O: 3.3-V or 5-V I/O (default 3.3 V)
- Interface to host processor with a 3.3-V digital interface signals to MCU SPI and ABZ/UVW outputs and optional 10- or 12-bit parallel interface to host processor
- Resolver interface: Sub-D9 female connector or 6-pin header interface to resolver
- Programmable angle position with a 10- or 12-bit resolution, cable length tested up to 20 m
- Evaluation firmware: Example firmware for Piccolo F28069M MCU. The user interface is through USB virtual COM port for easy performance evaluation.

2.1 Input Supply Specifications and Other Power Supply Rails

Table 1 shows different characteristics of the input power supply. This TI Design features a 24-V DC input with wide input voltage range from 12 to 42 V (or 60 V with drop-on compatible DC-DC) and reverse-polarity protection.

<table>
<thead>
<tr>
<th>CHARACTERISTICS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>15 to 42 V, 24 V (nominal), or 60 V using drop-in compatible DC/DC buck converter IC</td>
</tr>
<tr>
<td>Max. input current</td>
<td>400 to 500 mA</td>
</tr>
<tr>
<td>Reverse polarity protection</td>
<td>Yes</td>
</tr>
<tr>
<td>Input EMI filter</td>
<td>No</td>
</tr>
<tr>
<td>Connector</td>
<td>2-pin header (2.54 mm)</td>
</tr>
</tbody>
</table>

The onboard power management is split into a DC-DC buck that generates a 5-V rail and an LDO, which generates a 3.3-V rail. Table 2 shows the voltage rails and the required currents on these rails.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VOLTAGE</th>
<th>CURRENT</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V_VCC</td>
<td>5 V (+5%)</td>
<td>1.5 A</td>
<td>High efficiency (&gt;80%) DC/DC asynchronous buck power supply</td>
</tr>
<tr>
<td>3.3V_VIO</td>
<td>3.3 V (+5%)</td>
<td>200 mA</td>
<td>IO supply generated using LDO</td>
</tr>
</tbody>
</table>
2.2 Resolver Interface

The TIDA-00363 has a DSub-9 female connector as well as a 6-pin male header to connect the resolver as shown in Table 3.

Table 3. Sub-D9 Female and 6-Pin Male Header Assignment

<table>
<thead>
<tr>
<th>PIN NO ON CONNECTOR J3</th>
<th>PIN NO ON Connector J4</th>
<th>SIGNAL NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>SIN−</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>SIN+</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>COS+</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>COS−</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>EXC−</td>
</tr>
<tr>
<td>9</td>
<td>6</td>
<td>EXC+</td>
</tr>
</tbody>
</table>

2.3 3.3-V I/O Host Processor Interface

As per the PGA411-Q1 datasheet, the default output data interface for the device is parallel out. The angle and velocity data are also available in the register memory space and can be polled through the SPI. This TI Design TIDA-00363 has options to use both the interfaces. The SPI signals are available on connector J1 whereas the parallel port data is available on connector J2 as shown in Figure 14. Table 4 and Table 5 show the signals on connectors J1 and J2, respectively.

Table 4. Signals on Connector J1 (SPI Port)

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>PIN NO</th>
<th>PIN NO</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGND</td>
<td>1</td>
<td>2</td>
<td>AMODE</td>
</tr>
<tr>
<td>SDO</td>
<td>3</td>
<td>4</td>
<td>OUTZ</td>
</tr>
<tr>
<td>DGND</td>
<td>5</td>
<td>6</td>
<td>OUTA</td>
</tr>
<tr>
<td>SDI</td>
<td>7</td>
<td>8</td>
<td>OUTB</td>
</tr>
<tr>
<td>DGND</td>
<td>9</td>
<td>10</td>
<td>NCS</td>
</tr>
<tr>
<td>SCLK</td>
<td>11</td>
<td>12</td>
<td>FAULT</td>
</tr>
<tr>
<td>DGND</td>
<td>13</td>
<td>14</td>
<td>PRD</td>
</tr>
<tr>
<td>FAULTRES</td>
<td>15</td>
<td>16</td>
<td>NRST</td>
</tr>
<tr>
<td>ECLKSEL</td>
<td>17</td>
<td>18</td>
<td>BMODE</td>
</tr>
<tr>
<td>DGND</td>
<td>19</td>
<td>20</td>
<td>NC</td>
</tr>
</tbody>
</table>

On the TIDA-00363, per default, OMODE is pulled-down, which disables the parallel interface and selects the encoder emulation mode with the TIDA-00363. To select the parallel interface, the host processor should drive OMODE high.

Table 5. Signals on Connector J2 (Parallel Port)

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>PIN NO</th>
<th>PIN NO</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>INHB</td>
<td>1</td>
<td>2</td>
<td>ORD8</td>
</tr>
<tr>
<td>DGND</td>
<td>3</td>
<td>4</td>
<td>ORD7</td>
</tr>
<tr>
<td>DGND</td>
<td>5</td>
<td>6</td>
<td>ORD6</td>
</tr>
<tr>
<td>DGND</td>
<td>7</td>
<td>8</td>
<td>ORD5</td>
</tr>
<tr>
<td>OMODE</td>
<td>9</td>
<td>10</td>
<td>ORD4</td>
</tr>
<tr>
<td>DGND</td>
<td>11</td>
<td>12</td>
<td>ORD3</td>
</tr>
<tr>
<td>VA0</td>
<td>13</td>
<td>14</td>
<td>ORD2</td>
</tr>
<tr>
<td>DGND</td>
<td>15</td>
<td>16</td>
<td>ORD1</td>
</tr>
<tr>
<td>VA1</td>
<td>17</td>
<td>18</td>
<td>ORD0</td>
</tr>
<tr>
<td>DGND</td>
<td>19</td>
<td>20</td>
<td>ORD13</td>
</tr>
</tbody>
</table>
### 2.4 Indicator LEDs

The availability of the input power supply $V_{\text{IN}}$ (12 to 42 V, 24 V nominal), $V_{\text{VCC}}$ and $V_{\text{IO}}$ are indicated using three LEDs. Apart from these, there are five LEDs used for indications for specific functions related to the PGA411. These functions include: availability of $V_{\text{EXT}}$ (= 15 V for 7-V$_{\text{RMS}}$ mode), selection of AMODE (acceleration mode), selection of OMODE (output format mode—parallel or SPI), selection of BMODE (output type mode—angle or velocity) and the selection of an external clock for the PGA411-Q1.

### 2.5 EMC Immunity

The design meets ESD, EFT and surge requirements per IEC61000-4-2, 4-4, and 4-5 with levels specified in the IEC 61800-3 standard “EMC immunity requirements for adjustable speed, electrical-power drive systems”. It is assumed only the Sub-D9 connector to the resolver can be accessed and shielded cables are used to connect to the resolver. Because the resolver cable can exceed 20 m, ESD, EFT, and surge apply per Table 6 for use in Environment 2.

### Table 5. Signals on Connector J2 (Parallel Port) (continued)

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>PIN NO</th>
<th>PIN NO</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORD9</td>
<td>21</td>
<td>22</td>
<td>ORD12</td>
</tr>
<tr>
<td>ORD10</td>
<td>23</td>
<td>24</td>
<td>ORD11</td>
</tr>
</tbody>
</table>

### Table 6. EMC Immunity Requirements

<table>
<thead>
<tr>
<th>PORT</th>
<th>EMC TEST</th>
<th>EMC STANDARD</th>
<th>LEVEL</th>
<th>PERFORMANCE (ACCEPTANCE) CRITERION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolver interface connector</td>
<td>ESD</td>
<td>IEC61000-4-2</td>
<td>±4 kV CD or 8kV AD, if CD not possible</td>
<td>B</td>
</tr>
<tr>
<td>Electrical fast transient (EFT)</td>
<td>IEC61000-4-4</td>
<td>±2 kV/5 kHz, capacitive coupling clamp</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>Surge 1.2/50 µs, 8/20</td>
<td>IEC61000-4-5</td>
<td>±1 kV, since shielded cable &gt; 20 m, direct coupling to shield (2-Ω source impedance)</td>
<td>B</td>
<td></td>
</tr>
</tbody>
</table>

The performance (acceptance) criterion is defined as per Table 7:

### Table 7. Performance Criterion

<table>
<thead>
<tr>
<th>PERFORMANCE (ACCEPTANCE) CRITERION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The module must continue to operate as intended. No loss of function or performance even during the test</td>
</tr>
<tr>
<td>B</td>
<td>Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.</td>
</tr>
<tr>
<td>C</td>
<td>During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart, or power off, or power on.</td>
</tr>
</tbody>
</table>
### 2.6 Evaluation Firmware

To allow for quick evaluation of the TIDA-00363 design, an example firmware for Piccolo F28069M MCU is provided. A user interface through USB virtual COM port at 115000 baud allows for easy performance evaluation.

The user interface menu supports the following features:
- Configuration (read/write) of PGA411-Q1 registers and AMODE, BMODE0 pins
- Continuous angle display (10- or 12-bit mode) with a 10-Hz update rate
- Real-time angle data dump at a 16-kHz sample rate
- Histogram analysis at a 16-kHz sample rate
- Continuous monitoring of faults from the PGA411-Q1

### 2.7 Details About LTN Resolver Used to Test TIDA-00363

Figure 4 (taken from the datasheet of the LTN Resolver, part number R58CURE151B04-021-07AX) shows the specifications. Three important parameters to be noted are:
- Input voltage = 7 V\(_{\text{RMS}}\)
- Input frequency range = 5 to 10 kHz
- Angle accuracy = ±10' / 20' spread
- Transformation ratio = 0.5 ± 10%

![Figure 4. Electrical Parameters for LTN Resolver](image)
3 Circuit Design

This section explains the design theory (and equations, if required) for each of the devices used in the design.

3.1 4.1 Power Management

The PGA411-Q1 requires two different rails for operation. Table 8 shows the recommended operating voltages on Pin 60 (VCC) and Pin 61 (VIO).

Table 8. PGA411-Q1 Recommended Voltage Rails

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC} / QVCC</td>
<td>4.75</td>
<td>5.00</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>V_{EXT} Exciter supply input</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>V</td>
</tr>
<tr>
<td>V_{CCSW} Boost regulator input</td>
<td>14</td>
<td>15</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>V_{IO} I/O supply input</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>V_{IZ} Differential amplitude input</td>
<td>4.5</td>
<td>5.0</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>T_A Operating fee-air temperature</td>
<td>–40</td>
<td>125</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>T_J Operating junction temperature</td>
<td>–40</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

3.1.1 24-V Input to 5-V Rail (5V\_VCC)

A switching DC-DC converter is provided to generate the voltage rail of 5 V for VCC of the PGA411-Q1. This is a basically mandatory choice since the high $V_{IN}/V_{OUT}$ ratio makes any LDO unsuitable for the power conversion. Indeed the efficiency of any LDO could be easily calculated as $V_{OUT}/V_{IN}$ that, in the worst case (maximum $V_{IN}$) would lead to $5 \text{ V}/42 \text{ V} = 11.9\%$. The remaining $\approx 88\%$ of the power consumption is dissipated by the LDO package: having indeed a maximum current of 200 mA would lead to $42 \text{ V} \times 200 \text{ mA} \times 88\% = 7.4 \text{ W}$ of power dissipated on the LDO package that would simple and quickly blow up any reasonable package.

The DC-DC buck converter has been designed to meet the following specifications:
- Input voltage: $V_{IN} = 12$ to 42 V, 24 V nominal
- Drop-in compatible version with $V_{IN} = 12$ to 60 V
- Output voltage: 5 V at 1.5 A
- Switching frequency: 1 MHz nominal
- Output voltage ripple: 25 mV(P-P) max
- Efficiency: > 80% at full load
- Non-isolated topology

The TPS54140A is selected for the purpose: this is a buck converter with an integrated FET, 3.5- to 42-V input voltage, and 0.8- to 39-V output voltages at a 1.5-A output current. Its frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. It can also be enabled and disabled by using EN pin. These features make the TPS54140A a very good fit to these requirements and specifications.

NOTE: The TPS54140A is pin-to-pin compatible with the TPS54160A, which is a high-voltage version of the TPS54140A. The TPS54160A has input voltage range up to 60 V with all other specifications and similar performance.
NOTE: The TPS54140A is pin-to-pin compatible also with the TPS54240, TPS54340, and TPS54540: this widens the part selection and offers the possibility to modulate costs and power level (in case of future system upgrades).

3.1.1.1 Simulation Using WEBENCH® Designer

The design of the TPS54140A and corresponding component selection was verified and simulated using TI’s WEBENCH Designer. Figure 5 shows the simulated efficiency of buck converter at different $V_{IN}$ values. Figure 6 shows the simulated power dissipation for efficiency of buck converter at different $V_{IN}$ values. Figure 7 shows the simulated loop response (gain and phase plots) for the buck converter.
3.1.1.2 Schematic and Components Selection

For a detailed explanation of the design process, see the TPS54140A datasheet (SLVSB55). The schematic of the 24-V to 5-V DC-DC Buck Converter with the TPS54140A is shown in Figure 8.

![Schematic of 24-V to 5-V DC-DC Buck Converter Using TPS54140A](image)

Figure 8. Schematic of 24-V to 5-V DC-DC Buck Converter Using TPS54140A

On a typical application the output voltage is set using a simple resistor divider network. Equation 1 gives the value of the upper resistor according to the output voltage, the reference voltage (0.8 V for the TPS54140A) and the lower resistor (with R57 usually fixed to 10 kΩ).

\[
R60 = R57 \times \frac{V_{OUT} - 0.8 \text{ V}}{0.8 \text{ V}}
\]  

(1)

With \( V_{OUT} = 5 \text{ V} \) and \( R57 = 10 \text{ kΩ} \), \( R60 \) yields 52.3 kΩ.

The tolerance of the 5-V output voltage will be 5 V ±2.1%. This assumes feedback resistors with a 0.1% tolerance and the internal bandgap tolerance from the TPS54140A of ±2%.

The converter start-up voltage can be programmed using the voltage divider connected to EN pin. \( R44 = 174 \text{ kΩ} \) and \( R46 = 24.3 \text{ kΩ} \) are used to set the start-up voltage to 10 V. The switching frequency is set with \( R48 = 113 \text{ kΩ} \) to 1 MHz. The soft-start time is set to 1 ms using \( C42 = 6800 \text{ pF} \).

3.1.2 5-V Input to 3.3-V Rail (3.3V_VIO)

The VIO pin can be powered using 3.3 V or 5 V based on the controller that will be interfaced with the PGA411. In this TI Design, the PGA411 is interfaced with a Piccolo controller from TI, which works on 3.3 V. The LDOs do not need a specific description, except for the allowed range of output cap and ESR for stability purposes, while the main design involves the SMPS, as this affects all the main performances (noise, EMI, efficiency, cost, and board space). The TPS79933 is selected for the following reasons:

1. Input voltage range: 2.7 to 6.5 V (7-V absolute maximum)
2. Output current: up to 200 mA
3. Temperature range: –40°C to 125°C

Check the thermal stress on the LDO. The total power it has to dissipate is:

\[
P_{LDO(max)} = (V_{LDO(IN)} - V_{LDO(OUT)}) \times I_{LDO(max)} = (5 \text{ V} - 3.3 \text{ V}) \times 200 \text{ mA} = 0.34 \text{ W}
\]

(2)

For package selection,

\[
\theta_{JA(max)} = \frac{(T_J - T_A)}{P_{D(max)}} = \frac{(125°C - 85°C)}{0.34} = 117.64°C/W
\]

(3)

The LDO should have package with \( \theta_{JA} \leq 117.64°C/W \). Looking at Table 9 taken from the TPS79933 datasheet, the DRV (SON) package is suitable.
### Table 9. Thermal Information for TPS79933

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPS799 DDC (SOT)</th>
<th>TPS799 DRV (SON)</th>
<th>TPS799 YZU (DSBGA)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{thJA} Junction-to-ambient thermal resistance</td>
<td>225.3°C/W</td>
<td>74.2°C/W</td>
<td>143.3°C/W</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

The schematic of 5-V to 3.3-V conversion using the LDO TPS79933 is shown in Figure 9. R12 and R3 are provided for easy connection and disconnection of U1 to the PGA411-Q1. The TPS799 is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. C3 is input capacitor and C2 is output capacitor. Although an input capacitor is not required for the stability of the TPS79933, C3 can help improving the source impedance, noise or PSRR for the LDO. In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (CNR) is used with the TPS79933, the band gap does not contribute significantly to noise. C1 (0.1 μF) is used as noise-reduction capacitance.

**Schematic tips:**
1. Do connect a 0.1-μF to 1-μF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.
2. Do not exceed the absolute maximum ratings of the device.

**Figure 9. Schematic of 5-V to 3.3-V Converter Using TPS79933**

#### 3.1.3 QVCC Generation for PGA411-Q1

The analog front-end (AFE) in the PGA411-Q1, together with the tracking loop, performs the RDC functionality. The AFE block connects to the resolver sensor SIN and COS coils where the SIN (IZ2/IZ4) and the COS (IZ1/IZ3) signals are amplified by differential input amplifiers with programmable gain. The AFE is referenced to the quiet ground pin QGND and powered by the quiet voltage supply QVCC pin.

**Figure 10. QVCC Generation**

Quiet VCC (QVCC) is generated by providing more filtering to 5V_VCC. As shown in Figure 10, a resistor (R63) with two capacitors C33 (10 μF) and C34 (0.1 μF) form a filter. QVCC_5V is connected to Pin 39 of PGA411-Q1. QVCC_5V_FE is further filtered using an RC filter (R43 and C37) to provide to the input circuitry (explained in Section 3.5.1), which connects the PGA411-Q1 to the resolver. R63 can be also replaced with a 0805 package ferrite bead if further filtering is required.
3.2 **LED Indications**

The design uses some LEDs to indicate different conditions related to power supply as well as the PGA411-Q1 setup. Table 10 shows the summary of LED indications used on TIDA-00363 board.

**Table 10. LED Indications**

<table>
<thead>
<tr>
<th>LED</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D17</td>
<td>$V_{IN}$ (24 V nominal)</td>
</tr>
<tr>
<td>D18</td>
<td>$5V_{VCC}$</td>
</tr>
<tr>
<td>D19</td>
<td>$3.3V_{VIO}$</td>
</tr>
<tr>
<td>D20</td>
<td>Excitation voltage $V_{EXT}$</td>
</tr>
<tr>
<td>D21</td>
<td>AMODE</td>
</tr>
<tr>
<td>D22</td>
<td>OMODE</td>
</tr>
<tr>
<td>D23</td>
<td>BMODE</td>
</tr>
<tr>
<td>D24</td>
<td>External clock mode</td>
</tr>
</tbody>
</table>

3.2.1 **LED Indications—Power**

Figure 11 shows the LED indications used for power supplies. There are in total four LEDs (D17, D18, D19, and D20) that indicate the input power supply $V_{IN}$ (12 to 42 V, 24 V nominal), $5V_{VCC}$, $3.3V_{VIO}$, and the excitation supply for the PGA411-Q1, respectively. D20 indicates availability of $V_{EXT}$ (= 15 V for 7-$V_{RMS}$ mode). It can either be generated from internal boost converter from the PGA411-Q1 or externally provided.

![Figure 11. LED Indications for Power Supplies](image)

3.2.2 **LED Indications—PGA411-Q1**

Figure 12 shows the LED indications used for specific functions related to the PGA411-Q1. There are in total four LEDs (D21 through D24).

- D21 indicates the selection of AMODE.
- D22 indicates the selection of OMODE.
- D23 indicates the selection of BMODE.
- D24 indicates the selection of External Clock for PGA411-Q1.

For more information on these modes, see Section 3.4.
3.3 **Ground Topology**

A proper ground topology is very important in any good design. The PGA411-Q1 has three ground pins, namely:

- **PGND**: Power ground
- **DGND**: Digital ground
- **QGND**: Quiet ground

The TIDA-00363 implements STAR ground topology and all three grounds are connected to each other as shown in Figure 13. For placement of R41 in layout, see Figure 96.

![Figure 13. Star Ground Topology](image)

3.4 **Host Processor Interface**

3.4.1 **Connection to Host Processor—Parallel Port**

To enable the Parallel Output interface, the OMODE pin has to be set high (VDD). Otherwise, if OMODE is low (DGND), then the device is configured in the encoder emulated output mode (described in Section 3.7.7).

![Figure 14. Connection to Host Processor—Parallel Port](image)

**NOTE:** If parallel mode is not used, place a jumper between Pin 1 and Pin 3 of Connector J2.
Figure 14 shows the connection to host processor through a parallel port (Connector J2). The following signals are available on Connector J2:

1. **ORDx parallel data**: The digital parallel output provides an angle or velocity sample value update every 100 ns at the ORD[11:0] pins, which can be expressed as a 10-MSPS output update rate. When the parallel output interface is enabled, the angle and velocity data is read from the ORD11 (MSB) to ORD0 (LSB) pins. The digital data at the parallel output is in 2’s complement format. While this is not important for the angle output because value is always positive, the velocity output can be either positive or negative depending on the resolver rotation direction. If the resolver sensor rotation is clockwise (CW), then the digital parallel output velocity value is positive, while if the resolver sensor rotation is counter clockwise (CCW), then the output value is negative. If the device is used in 10-bit mode (BMODE0 is low), the ORD10 and ORD11 pins will be low (zero’s) on a positive angle and velocity output or high (one’s) on a negative velocity.

2. **OMODE pin**: The OMODE selection pin switches the ORD[11:0] pins between the parallel data output and the emulated encoder output. In this design, by default OMODE pin is connected to LOW (DGND) through resistor R51 (= 10 kΩ) as shown in Figure 16.

3. **INHB pin**: The INHB pin controls the data output update on the PGA411-Q1. When this pin is high (VIO), the output data is being sampled at the ORD[11:0] pins as soon as it becomes available. If the INHB pin is set low (DGND), the data output at ORD[11:0] pins is held at the last sampled output. In a synchronous data transfer system, by applying a clock signal at the INHB input with a frequency lower than 10 MHz, it is possible to sample the data at the output of the PGA411 on every clock period.

4. **VA0 and VA1 pins**: These pins enable and disable the ORD[11:0] pins while also selecting the output parameter. The VA0 and VA1 pins configuration is described in Table 11:

   Table 11. Selection of Output Parameter on ORD[11:0]

<table>
<thead>
<tr>
<th>VA0</th>
<th>VA1</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ORD[11:0] set to high-Z</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Angle output at ORD[11:0]</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Velocity output at ORD[11:0]</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

5. **DGND**: All the signals on connector J2 are referenced to digital ground (DGND).

**NOTE**: The signals connected to Connector J2 are not in a particular order. They are connected in a sequence so as to optimize for the best layout.
**3.4.2 Connection to Host Processor—SPI Port**

The angle and velocity data are available in the register memory space and can be polled through the SPI. **Figure 15** shows the connection to the host processor through an SPI port (Connector J1).

![Figure 15. Connection to Host Processor—SPI Port](image)

The following signals are available on the connector J1:

1. **SPI pins (SDI, SDO, SCLK, and NCS):** The PGA411-Q1 interface includes a four-pin SPI using the pins: NCS (active low spi chip select), SCLK (SPI clock), SDI [SPI slave in/master out (SIMO)] and SDO [SPI slave out / master in (SOMI)]. The RDC is always configured as a slave device. The SPI frame size is 32 bits long, with MSB-first alignment. For an SPI timing diagram, see the PGA411-Q1 datasheet (SLASE76). It is important to note that SDO pin on connector J1 is has a 22-Ω resistor for series termination.

2. **AMODE:** This pin is an "accelerated mode select" input. The acceleration helps the tracking loop to improve the dynamic performance as a result of high angular acceleration effects. The PGA411-Q1 implements a configurable loop acceleration block as well as an external enable control through the AMODE pin. The advantage of accelerated mode is that the loop settling time is significantly reduced. For this TI Design, by default, AMODE is connected to LOW (DGND) through resistor R5 (= 10 kΩ) as shown in **Figure 16**.

3. **BMODE:** BMODE is for the "resolution selection" input. Basically there are two pins: BMODE0 and BMODE1. Since the BMODE1 pin is reserved and needs to be connected to DGND (as shown in **Figure 16**)—BMODE1 is connected to DGND through 0-Ω resistor R49), only BMODE0 can decide the output data resolution. When the BMODE0 pin is low (DGND), the device operates in a 10-bit mode and the output data range is between 0 and 1023 and extracted from the ORD9 to ORD0 pins when parallel output mode is selected. If BMODE0 is high (VIO), the device operates in a 12-bit mode and the output data range is 0 to 4095 extracted from the ORD11 to ORD0 pins when parallel output mode is selected. In this TI Design, by default, BMODE is connected to HIGH (VIO_3.3V) through resistor R47 (= 10 kΩ) as shown in **Figure 16**.
4. **FAULT and FAULTRES**: The FAULT signal is output signal from the PGA411-Q1, and the FAULTRES signal is the input signal to the PGA411-Q1. For more details about these signals, see Section 3.7.4 and Section 3.7.5, respectively.

5. **PRD**: For increased safety, the PGA411-Q1 provides a data parity check output. This is available through the parallel data output by using the PRD bit in register DEV_STAT5 (angle output) or register DEV_STAT6 (velocity output).

6. **NRST**: This is the RESET signal for the PGA411-Q1. For more details on this, see Section 3.7.3.

7. **CLKSEL**: For this design, by default, the ECLKSEL pin is connected to LOW (DGND) through resistor R8 (= 22 kΩ) as shown in Figure 15. The external clock option was not used with the PGA411-Q1.

8. **Encoder emulation signals (OUTA, OUTB, OUTZ)**: The PGA411-Q1 is capable of emulating quadrature encoder output signals with an index pulse, as well as emulating commutation signals. For more details on the encoder emulation, see Section 3.7.7.

9. **DGND**: All the signals on connector J1 are referenced to DGND.

---

**NOTE**: It is important to note that the signals connected to Connector J1 are not in a particular order as per the pin configuration of PGA411-Q1. They are connected in a sequence so as to optimize for best layout.

### 3.5 Connection to Resolver and Feedback From Resolver

Together with the tracking loop, the analog front-end (AFE) in the PGA411-Q1 is performing the RDC functionality. The AFE block connects to the resolver sensor SIN and COS coils where the SIN (IZ2/IZ4) and the COS (IZ1/IZ3) signals are amplified by a differential input amplifiers with variable gain.

#### 3.5.1 Input Front-End Circuit

Because the PGA411-Q1 tracking loop is fed by the SIN and COS signals (through the AFE) from the resolver sensor, conditioning these signals properly is important. Therefore, selecting external components is critical to operate the device. The SIN and COS signals must be amplified properly without causing distortion. Noise must also be suppressed in the monitored frequency range.

#### 3.5.1.1 Calculations for Input Front-End Circuit

By taking into consideration different types of resolver sensors, each of these has a different transformation ratio and is usually in the range of 0.35 to 0.5. Therefore, if needed, additional resistance can be implemented in the input signal path to further attenuate the input signal, which otherwise would cause the OSIN and OCOS outputs to saturate.

Figure 17 and Figure 18 show the EMC protection circuit for the AFE for SIN signals and COS signals, respectively.
**Figure 17. Front-End Protection Circuit for SIN+ and SIN– Inputs From Resolver**

In Figure 17:
- Capacitors C13 and C7 (both 68 pF, 0603 packages), Capacitors C14 and C8 (both 10 pF, 0402 package): These are common-mode filtering capacitors. When using large and small cap in parallel, it is good to use smaller footprint with smaller capacitor, to optimize for ESR at higher frequencies.
- Resistors R21 (= 49.9 kΩ) and R14 (= 49.9 kΩ): Diagnostics and fault detection resistors.
- Capacitors C9 and C10 (68 pF, 0603 package) and C11 and C12 (22 pF, 0402 package): These capacitors are combined together for differential input capacitor.
- Resistors R20, R22, R16, and R17 (each 30 kΩ): These are input resistors for setting the gain. The resistors should have a tolerance of 0.1% to reduce any error due to gain mismatch (see Figure 85, which shows gain error due to high tolerance resistors).
- The protection diodes (D1 through D4) play a vital role, and they should be selected so that their maximum leakage (reverse) current is a small as possible (lower than 10 nA at a 10-V reverse voltage) in order not to impact the offset value of the input signals. For this design, BAS70_1PS7XSB70 from NXP is used. It has a maximum reverse current of 4 nA at 10 V and 25°C.
- The input front-end circuit is designed to have a low pass filter characteristic cut-off frequency of 10 kHz (–3 dB) assuming a resolver with a stator impedance around 100- to 500-Ω DC impedance. The TINA-TI simulation for the same is shown in Figure 18.

**Figure 18. Front-End Protection Circuit for COS+ and COS– Inputs From Resolver**
The AFE gain can be selected between the ranges of 0.75 to 3.5. This is achieved by selecting a different value for the resistance RF as described in Table 12 [taken from the PGA411-Q1 datasheet (SLASE76)].

Table 12. RF Resistance for Gain Levels

<table>
<thead>
<tr>
<th>GAIN LEVEL</th>
<th>R\textsubscript{F} RESISTANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Taking an example of the LTN resolver (part number R58CURE151B04-021-07AX):

- Transformation ratio = 0.5
- External resistors connected as input resistors = 30 kΩ + 30 kΩ = 60 kΩ
- Internal SINCOS (software) gain = 1, which corresponds to an internal feedback resistor of RF = 20 kΩ.

As per the PGA411-Q1 datasheet:

\[
\text{Effective Gain} = \frac{1 \times 20\text{kΩ}}{30\text{kΩ} + 30\text{kΩ} + 20\text{kΩ}} = 0.25
\]

For a 7-V\textsubscript{RMS} mode, the peak-to-peak value of the signal is 17.76 V. The output of the PGA411 then equals 17.76 × 0.5 × 0.25 = 2.2207 V.

The protection circuit for front-end is referenced to QVCC_5V_AFE and QGND (which are quiet references as explained in Section 3.1.3).

The time constant is one of the contributors to phase shift between the exciter signal and the SIN and COS signals. Therefore, an optimum value needs to be derived to keep the phase shift in the PGA411-Q1 correction range. In order for the open input diagnostic to be operational, the external resistors R\textsubscript{FH\textsubscript{L}} and R\textsubscript{FL\textsubscript{L}} are implemented, which provide DC bias to the IZx inputs when the input coil is disconnected. The estimated values of these are shown in Table 13 for some assumed voltages at the VEXT pin (taken from the PGA411-Q1 datasheet).

Table 13. Selection of Open Fault Resistors

<table>
<thead>
<tr>
<th>VEXT (V)</th>
<th>R\textsubscript{FH\textsubscript{L}} (kΩ)</th>
<th>R\textsubscript{FL\textsubscript{L}} (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>24</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>
3.5.1.2 TINA-TI Simulations for Input Front-End Circuit

The input front-end structure is simulated in TINA-TI. Figure 19 shows the simulation schematic. VG1 is set at 2 V(p-p) at 10 kHz. R10 and R20 were set to zero and the resolver stator DC impedance was selected at 100 Ω.

Figure 19. Simulated Front-End Circuit

Figure 20 shows the simulated waveform at the input of the PGA411-Q1.

Figure 20. Simulation Waveforms
Figure 21 shows the frequency response, gain, and phase plots for the signal input to the PGA411-Q1.

Figure 21. Gain and Phase Plots

From Figure 20 and Figure 21, the phase delay from input to output is 2.71 µs (which corresponds to 9.756°).

3.5.2 Connection to Resolver

Figure 22 shows the connection of the TIDA-00363 to the resolver by using a DSub-9 connector. Diodes D9, D10, D13, and D14 are used to protect the OE1 and OE2 (also IE1 and IE2) pins of the PGA411-Q1. The shield of the DSub-9 connector is connected to EARTH.

Figure 22. Connection to Resolver Using DSub-9 Connector
The signals connected to the DSub-9 connector are also connected to a 6-pin connector J4 as shown in Figure 23. This connector is used for monitoring and capturing waveforms as well as another option to add a resolver for test and debug purpose, however without a shield connected to Earth.

![Figure 23. Connection to Resolver Using 6-pin Connector](image)

### 3.5.3 Feedback From Resolver

The IE1 and IE2 inputs are implemented to be used as a feedback from the exciter signal path for monitoring and diagnostics of the exciter signal. This exciter monitor circuit is also used by the phase offset correction circuit for detecting and synchronizing the exciter signal together with the SIN and COS signals in the tracking loop. For monitoring the exciter signal, the IE1 and IE2 signals are conditioned as shown in Figure 24 (taken from the PGA411-Q1 datasheet).

![Figure 24. Signal Conditioning of IEx Pins](image)

Referring to the input specification for these pins (as shown in Table 14), the recommended voltage input swing must always be less than 4 V(p-p) when measured between pin to ground. Depending on the exciter amplifier output setting, there might be a need for additional signal attenuation by using external resistors.

### Table 14. Specifications for IEx Pins [Exciter Signal Monitor (IE1, IE2)]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IECM}$</td>
<td>Input voltage range</td>
<td>—</td>
<td>0.5</td>
<td>4.5</td>
<td>V</td>
</tr>
</tbody>
</table>

With this configuration, the voltage level on IEx pins is:

$$V_{IEX} = V_{OEX} \times \frac{20k\Omega + 20k\Omega}{20k\Omega + 20k\Omega + R}$$

(5)

The system is designed to work in 4 $V_{RMS}$ and 7 $V_{RMS}$ modes. The maximum voltage on the OEx pin is defined per Equation 6 where EXTOUT is programmable in the range 0.5 to 2 V, and VOEX(p-p) corresponds to the single-ended peak-to-peak voltage of the excitation signal.

$$V_{OEX(min)} = EXTOUT + V_{OEX(p-p)}$$

(6)
The minimum voltage on OEx pins is defined by EXTOUT only as per Equation 7.

\[ V_{OEx(min)} = EXTOUT \]  

(7)

Combining Equation 5, Equation 6 and Equation 7, the minimum and maximum values on the IEx pins can be calculated.

For the TIDA-00363, as shown in Figure 25, R39 and R29 (each 68 kΩ) are used for signal conditioning of the IE1 and IE2 pins. The resistors (R40 and R28) and capacitors (C24 and C27) are provided for further signal attenuation and filtering of IEx signals. These are currently marked as "DNP" for the TIDA-00363 design.

3.6 **Exciter Amplifier Power Supply (Internal Boost)**

The exciter power supply implemented in the PGA411-Q1 is supplied by the VCCSW pin for the internal driver logic and error correction and the VSW pin as a switch pin for creating a higher voltage rail. Both of these pins can be supplied by the same power supply when connected to the main device supply VCC, or these can be connected to a separate power source. A stabilization loop feedback pin VEXTS is implemented and must be connected to the output of the exciter power supply. Figure 26 shows the schematic of the boost section. The switching frequency for the exciter power supply is internally set to 400 kHz.
As per the PGA411-Q1 datasheet, the input supply to the boost (VCCSW) should range from 4.75 to 8.5 V. Typically, VCCSW can be supplied with the same 5-V rail as VCC and QVCC; however, in applications where high voltages and high currents are needed out of the boost, it is recommended to increase the voltage on VCCSW to achieve desired performance.

### 3.6.1 Setting up Output Voltage of Boost Circuit

The output voltage selection is done by setting the MODEVEXT bits in the DEV_CONFIG1 register. Regardless of the exciter output mode (4 V₉₀ and 7 V₉₀), the exciter power supply can be adjusted for output voltage in the range from 10 to 17 V as per Table 15 (taken from the PGA411-Q1 datasheet).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEXPS</td>
<td>MODEVEXT = 0x00; IEXTPS = 150 mA; VCCSW ≥ 4.75 V; nBOOST_FF = 1</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x01; IEXTPS = 150 mA; VCCSW ≥ 4.75 V; nBOOST_FF = 1</td>
<td>9</td>
<td>11</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x02; IEXTPS = 150 mA; VCCSW ≥ 5 V; nBOOST_FF = 1</td>
<td>10</td>
<td>12</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x03; IEXTPS = 150 mA; VCCSW ≥ 5 V; nBOOST_FF = 1</td>
<td>11</td>
<td>13</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x04; IEXTPS = 150 mA; VCCSW ≥ 5 V; nBOOST_FF = 1</td>
<td>12</td>
<td>14</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x05; IEXTPS = 150 mA; VCCSW ≥ 6 V; nBOOST_FF = 1</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x06; IEXTPS = 150 mA; VCCSW ≥ 6 V; nBOOST_FF = 1</td>
<td>14</td>
<td>16</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODEVEXT = 0x07; IEXTPS = 150 mA; VCCSW ≥ 7 V; nBOOST_FF = 1</td>
<td>15</td>
<td>17</td>
<td>19</td>
<td></td>
</tr>
</tbody>
</table>

For the TIDA-00363, the exciter power supply output is set to 15 V using the DEV_CONFIG1 register, bits 2, 1, and 0, as per Figure 31 (taken from the PGA411-Q1 datasheet).

---

**Figure 26. Boost Section for PGA411-Q1**

---
### 3.6.2 Selection of L and C for Boost Circuit

The maximum output current from the boost power supply is 150 mA. Given the fixed switching frequency of the boost converter (414 kHz), the PGA411 datasheet recommends using 56 μH of boost inductance along with 10 μF of output capacitance. As shown in Table 17 (taken from datasheet of PGA411-Q1), the recommended values for inductor and output capacitor for internal boost circuit are 56 μH and 10 μF.

#### Table 17. Recommended Values of L and C for Boost Converter

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L&lt;sub&gt;EXCPS&lt;/sub&gt;</td>
<td>Exciter power supply inductor range</td>
<td>56</td>
<td></td>
<td>10</td>
<td>μH</td>
</tr>
<tr>
<td>C&lt;sub&gt;EXCPS&lt;/sub&gt;</td>
<td>Exciter power supply capacitor range</td>
<td>10</td>
<td></td>
<td></td>
<td>μF</td>
</tr>
</tbody>
</table>

### 3.6.3 Use of VEXTS for Diagnostics

VEXTS pin is the sense input for exciter boost DC/DC feedback and amplifier diagnostic.

### 3.6.4 Selection of Exciter Amplifier Power Supply—Internal or External

The internal boost of the PGA411-Q1 can be disabled, and the VEXT voltage can be set to 15 V by connecting it directly to VIN (and reducing the VIN voltage to 25 V). As shown in Figure 26, Connector J7 can be used to select between internal or external exciter amplifier power supplies.

### 3.7 PGA411-Q1 and Related Signals

#### 3.7.1 Clocking the PGA411-Q1

The PGA411-Q1 is able to generate a digital system clock through an internal oscillator or an external crystal oscillator. This is done by setting the state of the ECLKSEL pin low (GND) for the internal 20-MHz oscillator selection, or high (VDD) for the external oscillator selection. (Note that the oscillator circuit is referenced to the VDD power supply.) In the case of an external crystal oscillator, a 20-MHz quartz crystal or resonator is connected between the XIN and XOUT pins along with capacitors (15 pF) connected to DGND. The schematic section for external crystal clock is shown in Figure 27.

As explained in Section 3.2.2, LED D24 indicates the selection of an external clock for the PGA411-Q1.

![Figure 27. Clocking PGA411-Q1 Using External Crystal Oscillator](image-url)
3.7.2 VDD Regulator

The VDD regulator receives a 5-V input supply voltage from the VCC pin and generates a stable 1.8-V supply for internal digital logic circuits. The reference for the VDD regulator is generated by the PGA411-Q1 internal bandgap circuit. The VDD regulator can supply up to a 10-mA current from the VDD pin for powering external circuits. The VDD pin is used for filtering and requires an external filtering capacitor. As shown in Figure 28, a 10-µF/16-V capacitor is connected to Pin 58 (VDD) for filtering.

![Figure 28. VDD Regulator Filtering](image)

3.7.3 RESET Signal for PGA411-Q1

For the PGA411-Q1, the NRST pin asserts nPOR in the device logic. When the NRST pin is low (DGND), the PGA411-Q1 logic is frozen and the device is in RESET. When the NRST pin is pulled up, the logic is enabled after a 70-µs deglitch period and the device is operational. During RESET condition, all functional blocks inside the PGA411-Q1 are disabled. This includes the exciter boost regulator, the exciter output amplifier, digital tracking loop, AFE, the VDD regulator, and the oscillator. The FAULT pin state is low. During active device operation in any state, the PGA411-Q1 can cause an internal reset in the case of:

- Undervoltage on the VCC pin
- VDD regulator undervoltage on the VDD pin
- An oscillator fault condition signaled by the loss of clock monitor
- A thermal shutdown signal generated by the thermal protection circuit in case of a device over-temperature condition

The PGA411-Q1 resumes normal operation when the fault has been cleared and the NRST pin state is high (VIO), in which case the nPOR is removed.

In this TI Design, by default, the device is in RESET mode until a microcontroller brings it out of RESET. As shown in Figure 29, R59 (= 10 kΩ) pulls NRST pin to DGND.

![Figure 29. Default Conditions for NRST and FAULTRES Signals](image)
3.7.4 FAULT Reporting

Fault reporting in the PGA411-Q1 is signaled through the FAULT pin. The FAULT pin is an open drain output structure. The pin is in an active low state when there is not fault that needs to be reported, while the pin is Hi-Z when a fault is present in the system. To know more about all the fault conditions supported by PGA411-Q1, see the PGA411-Q1 datasheet (SLASE76).

In this TI Design, the following faults are tested (the test results are provided in Section 6.6.3):
- Resolver disconnected
- SIN input or COS input disconnected
- Exciter output disconnected
- Exciter connected to GND
- SIN input or COS input connected to GND
- SIN input mutual short
- COS input mutual short

3.7.5 FAULT RESET Signal for PGA411-Q1

The FAULTRES pin is the input signal. All the faults are reset when this pin is low. To clear the fault state in the system, when all fault conditions have been removed, the FAULTRES pin needs to be toggled (high-low-high) and the PGA411-Q1 will transition back into normal mode of operation. As shown in Figure 29, the FAULTRES pin is, by default, pulled high (VIO_3.3V) through R6 (= 10 kΩ).

3.7.6 Analog Output

Analog representation of the angle output can be monitored at the AOUT pin. The PGA411-Q1 implements a 10-bit DAC to convert the ORD digital parallel output into an analog value with range between 0.5 and 4.5 V. Because the analog DAC is limited to 10 bits at the input, in 12-bit resolver mode only ORD[11:2] are ported into the input of the DAC. The analog voltage representation of the angle is illustrated in Figure 30.

![Figure 30. Analog Angle Output](image)

For the TIDA-00363 design, AOUT is taken out on a test point (TP3) as shown in Figure 31. The measured AOUT signal is shown in Figure 71.

For external signal monitoring, the PGA411-Q1 outputs the amplified SIN and COS signals at their dedicated OSIN and OCOS pins. These output pins are referenced to the COMAFE pin. In the schematic, these signals are available on test points TP1 and TP2, respectively (as shown in Figure 71). The measured OSIN and OCOS signals are shown in Figure 74.
3.7.7 Encoder Emulation

The PGA411-Q1 is capable of emulating quadrature encoder output signals with index pulse, as well as emulating commutation signals. The quadrature encoder output and index pulse output A, B, and Z signals are permanently available at the OUTA, OUTB, and OUTZ pins, while also multiplexed on the ORD6, ORD7, and ORD8 pins. The commutation output U, V, W, U1, V1, and W1 signals are multiplexed onto the ORD0 through ORD5 pins only. When the OMODE pin is set low (DGND), the PGA411-Q1 is configured in encoder emulator mode, and the ORD0 through ORD5 output their assigned emulator signal. This signal multiplexing allows the MCU to switch between the parallel output interface and the encoder emulator output by changing the state of the OMODE pin. Depending on the resolution set by the BMODE0 pin, the quadrature encoder will provide 256 pulses on OUTA and OUTB when the device is operating in a 10-bit mode, or 1024 pulses on OUTA and OUTB when operating in a 12-bit mode. The index pulse on OUTZ is generated once per revolution, whenever the angle output is at 0 degrees. The measured encoder emulation signals OUT-A, OUT-B, and OUT-Z are shown in Figure 72 and Figure 73.

3.8 Excitation Signal to Resolver

The PGA411-Q1 exciter signal path is optimized for driving highly inductive loads such as the exciter coil of the resolver sensor. It is designed for 4-V_{RMS} or 7-V_{RMS} operation selected by the EXTMODE bits in register DEV_PHASE_CFG. The exciter signal is generated by reading a digital sine wave stored in the device memory and then passed through a 9-bit differentially balanced DAC for generating a differential analog exciter signal. The frequency of the exciter signal is in the range of 10 to 20 kHz and selected by the SELFEXT bits in the DEV_CONFIG1 register. A custom frequency setting is available by feeding an external clock signal at the EXTCLKIN pin whenever a non-standard exciter frequency is desired.

The sine wave passes through three stages (for more details about each stage, see the PGA411-Q1 datasheet):
1. Pre-amplifier stage
2. Power amplifier stage
3. ORS buffer stage

Figure 31. Test Points for OSIN, OCOS, and AOUT
3.9 **Connection to External Amplifier**

Internal to the PGA411-Q1, a differentially balanced pre-amplifier does the signal conditioning of the exciter signal to the appropriate level for further output amplification. In the pre-amplifier block, the amplification level of the exciter signal can be adjusted while common mode voltage is defined by the voltage at the COMAFE pin (typically 2.5 V). The pre-amplifier gain (selectable though the EXTOUT_GL bits in DEV_OVUV1 register) affects both the pre-amplifier ORS output and power amplifier outputs. For signal monitoring or different exciter topologies, the output signal from the exciter pre-amplifier is available at the ORS pin of the PGA411-Q1. The output voltage is referenced to the voltage on the COMAFE pin.

Figure 32 shows connector J6, which can be used to connect external amplifier, in case the excitation needs to be strengthened. Power to the exciter power amplifier is supplied by the VEXT and PGND pins.

The internal output power amplifier consists of two identical Class AB amplifier units that are independently input inverted to form a bridge tied load (BTL) output topology. The exciter coil of the resolver sensor is connected at the output of the power amplifier (that is, between the OE1 and OE2 pins). Power to the exciter power amplifier is supplied by the VEXT and PGND pins.

![Figure 32. Connection to External Amplifier](image)

3.10 **C2000 LaunchPad Adapter Board**

The TIDA-00363 was tested with InstaSPIN Motion LaunchPad. Because the TIDA-00363 was developed having minimum board size and a single header in mind, the SPI connector J1 is not exactly matching to LaunchPad connectors. To connect to a C2000 LaunchPad, it is necessary to have a mediator, which can connect both the boards. One adapter board is designed for this purpose.

3.10.1 **Signals Required From LaunchPad**

From connectors J5 and J7 of LaunchPad, the following signals are taken out as shown in Table 18 and Figure 33.

![Image of Table 18](image)

**Table 18. LaunchPad Signals (J5 and J7)**

<table>
<thead>
<tr>
<th>MUX VALUE</th>
<th>J5 PIN</th>
<th>J7 PIN</th>
<th>MUX VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>+3.3V</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NC</td>
<td>62</td>
</tr>
<tr>
<td></td>
<td></td>
<td>J7.3</td>
<td>63</td>
</tr>
<tr>
<td></td>
<td></td>
<td>J7.4</td>
<td>64</td>
</tr>
<tr>
<td>EQEP1A</td>
<td>GPIO20</td>
<td>65</td>
<td>ADCINB5</td>
</tr>
<tr>
<td></td>
<td>NC</td>
<td>66</td>
<td>ADCINA5</td>
</tr>
<tr>
<td>TZ3</td>
<td>GPIO14</td>
<td>67</td>
<td>ADCINA3</td>
</tr>
<tr>
<td>EQEP1B</td>
<td>GPIO21</td>
<td>68</td>
<td>ADCINB3</td>
</tr>
<tr>
<td>EQEP1I</td>
<td>GPIO23</td>
<td>69</td>
<td>ADCINA4</td>
</tr>
<tr>
<td>SPI5MOA</td>
<td>GPIO54</td>
<td>70</td>
<td>NC</td>
</tr>
</tbody>
</table>
Figure 33. LaunchPad Signals (J5 and J7) Mapped on Adapter Board

From Connectors J6 and J8 of LaunchPad, the following signals are taken out as shown in Table 19 and Figure 34.

Table 19. LaunchPad Signals (J6 and J8)

<table>
<thead>
<tr>
<th>MUX VALUE</th>
<th>J8 PIN</th>
<th>J6 PIN</th>
<th>MUX VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>EPWM4A</td>
<td>GPIO6</td>
<td>80</td>
<td>GPIO6</td>
</tr>
<tr>
<td>EPWM4B</td>
<td>GPIO7</td>
<td>79</td>
<td>GPIO27</td>
</tr>
<tr>
<td>EPWM5A</td>
<td>GPIO8</td>
<td>78</td>
<td>GPIO26</td>
</tr>
<tr>
<td>EPWM5B</td>
<td>GPIO9</td>
<td>77</td>
<td>GPIO26</td>
</tr>
<tr>
<td>EPWM6A</td>
<td>GPIO10</td>
<td>76</td>
<td>GPIO25</td>
</tr>
<tr>
<td>EPWM6B</td>
<td>GPIO11</td>
<td>75</td>
<td>GPIO24</td>
</tr>
<tr>
<td>NC</td>
<td>74</td>
<td>72</td>
<td>GPIO52</td>
</tr>
<tr>
<td>DAC3</td>
<td>72</td>
<td>52</td>
<td>GPIO53</td>
</tr>
<tr>
<td>DAC4</td>
<td>71</td>
<td>51</td>
<td>GPIO55</td>
</tr>
</tbody>
</table>

Copyright © 2016, Texas Instruments Incorporated

Figure 34. LaunchPad Signals (J6 and J8) Mapped on Adapter Board
3.10.2 Connection to TIDA-00363

The TIDA-00363 and TIDA-00363 adapter board are connected through connector J1_TIDA-00363 on the adapter board as shown in Figure 35.

**Figure 35. Connector to Connect Both Boards**
4 Software Design

4.1 C2000 Peripherals Assignment

The TIDA-00363 example firmware has a simple command line interface for easy evaluation through USB virtual COM port. Figure 36 shows the hardware peripherals used on the TMS320F28069M. The ePWM1 timer is used to generate a periodic interrupt to read a new angle data from the PGA411-Q1. The interrupt frequency is chosen as 16 kHz. The SCI-A peripheral implements the UART interface at 115000 baud through the USB virtual COM port provided on the LaunchPad. Users can interact with the firmware using a terminal application. The firmware has been tested with Tera Term.

Figure 36. TMS320F28069M Peripheral Module and Pin Assignment to TIDA-00363 Interface

4.2 C2000 Software Flow Chart

The firmware uses the C2000 controlSUITE™ libraries. The demo firmware has to synchronously read the angle from the PGA411-Q1 and handle the UART terminal-based user interface. The firmware has two components. There is a background thread to handle the PC terminal interaction and a foreground thread which is the ISR of the ePWM1. This is shown in Figure 37.
The initialization sets TMS320F26069M CPU clock to 80 MHz, the GPIO multiplexers, the peripherals SPI-B, SCI-A (UART), and ePWM1-based periodic timer and interrupt. The SPI-B is configured as the SPI master with the serial clock of 8 MHz. This is the maximum SPI clock supported by the PGA411-Q1. After initialization, the program invokes the UART-based user interface and serves the period interrupt service routine (ISR). The period ISR implements reading the PGA411-Q1 angle data, buffering, and histogram calculation, and counts the SPI faults bits and CRC errors.

The angle data read from the PGA411-Q1 is in hexadecimal format it is an unsigned 16-bit integer, and only the lower 12 bits (12-bit mode) or lower 10 bits (10-bit mode) contain the angle information. The digital value 0 represents 0 degrees and 4096 for 12-bit mode (or 1024 for 10-bit mode) could represent 360 degrees, equivalent to 0 degrees. The angle degree can be computed as:

12-Bit Equation:
\[
\text{Angle (degrees)} = 360 \times \frac{\text{Angle (decimal)}}{4096}
\]

10-Bit Equation:
\[
\text{Angle (degrees)} = 360 \times \frac{\text{Angle (decimal)}}{1024}
\]

The resolver angle is internally processed as 32-bit integer fractional Q28 numbers in per unit (PU) and Q22 per degree (0 to 360 degrees) using TI's IQmath library. The advantage of 32-bit fractional numbers versus 32-bit IEEE floating point is that the resolution remains constant independent of the data range. Because the data range is limited from 0 to 1 for the angle (per unit), Q28 numbers with an integer range ±8, and Q22 numbers with an integer range of ±512 provide enough headroom, while accuracy remains constant for all data.
4.3 Default TIDA-00363 Configuration

The initial (default) PGA411-Q1 settings with the TIDA-00363 are listed in this section. If not mentioned, the settings are identical to the PGA411-Q1 factory setting, per the PGA411-Q1 datasheet (see Section 7.6.2: REGMAP Registers):

- 12-bit angle mode (BMODE0 = High default, can be changed using key "m")
- 4-V\text{RMS} exciter mode (can be changed using Key "j")
- 1-bit angle hysteresis (can be changes using key "j")
- Tracking loop in normal mode (AMODE = Low)
- Internal clock oscillator (ECLKSEL = Low)

**NOTE:** The pin settings and register settings can be changed as explained in Section 5.2.

Table 20 lists the changes versus factory settings.

<table>
<thead>
<tr>
<th>REGISTER</th>
<th>FACTORY SETTINGS</th>
<th>TIDA-00363 SETTINGS</th>
<th>CHANGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV_OVUV1</td>
<td>8B40h</td>
<td>8B40h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_OVUV2</td>
<td>00EDh</td>
<td>00EDh</td>
<td>—</td>
</tr>
<tr>
<td>DEV_OVUV3</td>
<td>FCFFh</td>
<td>FCF0h</td>
<td>OSIN/OCOS Open circuit low threshold level select: 000: VCC × 0.25 V OSIN/OCOS Open circuit high threshold level select: 000: VCC × 0.75 V</td>
</tr>
<tr>
<td>DEV_OVUV4</td>
<td>07E2h</td>
<td>07E2h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_OVUV5</td>
<td>1C00h</td>
<td>1C00h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_OVUV6</td>
<td>038Fh</td>
<td>038Fh</td>
<td>—</td>
</tr>
<tr>
<td>DEV_TLOOP_CFG</td>
<td>0514h</td>
<td>0514h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_AFE_CFG</td>
<td>0005h</td>
<td>0005h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_PHASE_CFG</td>
<td>1400h</td>
<td>1400h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_CONFIG1</td>
<td>0002h</td>
<td>0002h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_CONTROL1</td>
<td>0000h</td>
<td>0000h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_CONTROL2</td>
<td>0000h</td>
<td>0000h</td>
<td>—</td>
</tr>
<tr>
<td>DEV_CONTROL3</td>
<td>0000h</td>
<td>0000h</td>
<td>—</td>
</tr>
</tbody>
</table>
5 Getting Started

5.1 TIDA-00363 Board

5.1.1 TIDA-00363 Board Picture (Final Revision)

Figure 38 and Figure 39 show the top and bottom views of the TIDA-00363 PCB, respectively. The important sections are highlighted with RED arrows and captions.

Figure 38. TIDA-00363 PCB—Top View (Showing Important Sections)

Figure 39. TIDA-00363 PCB—Bottom View (Showing Important Sections)
5.1.2 TIDA-00363 Board Preparation

Add a jumper at J7 on positions 2 through 3 to use the 15-V supply from the PGA411-Q1 internal booster. Also, if parallel mode is not used, it is recommended to place a jumper between Pin 1 and Pin 3 of Connector J2.

5.1.3 Connecting All Three Boards Together

The adapter board, the TIDA-00363 board, and LaunchPad are connected as shown in Figure 40 and Figure 41.

![Figure 40. Top View](image1)

![Figure 41. Side View](image2)
Follow these hardware setup steps to configure the F28069M LaunchPad:

1. Load the demo firmware into the flash. The binaries can be obtained from the TIDA-00363 product page. Note: To allow emulator flash access, all positions on SW1 should be ON.

2. Provide the following jumper and connectors. The locations of the jumper are shown in Figure 42:
   (a) USB cable connected to the PC on connector CON1
   (b) Configure SW1 for loading from flash, SW1-1: ON, SW1-2: ON, SW1-3: OFF
   (c) JP4 = Closed, JP5 = Closed, JP6 = Open, JP7 = Closed
   (d) To power the LaunchPad from USB port, close JP1 and JP2. Alternatively, JP1 and JP2 can be open to provide isolation between PC terminal and hardware; in this case, the 3.3-V DC power supply must be given externally on J9.
   (e) Supply the TIDA-0363 hardware with a 24-V DC supply.

3. Follow the virtual COM port settings as shown in Figure 43.

4. Power up the board.

Troubleshooting: If no connection gets established, the VCP driver of the USB virtual com port TI XDS100 Channel B needed to be enabled under Windows® 7 Device Manager. For more details, see the InstaSPIN-MOTION LaunchPad documentation.
5.2 User Guide for Terminal Interface

On power up, the terminal should display the starting message shown in Figure 44. It highlights that the user must ensure that Jumper J7 is set to positions 2 and 3 to use the internal PGA411 boost DC/DC to supply the internal exciter amplifier of the PGA411-Q1. It also shows the name and version of firmware. To continue, click on the "Enter" key.

![Figure 44. Start-up Message](image)

Figure 44. Start-up Message

Figure 45 shows the default menu for the evaluation. To select a menu option, click the corresponding alphabet key on the keyboard.

![Figure 45. Main Menu](image)

Figure 45. Main Menu

Section 5.2.1 through Section 5.2.11 shows the different configurations possible using the different keys.
5.2.1 Key "a"

If the "a" key is pressed on the keyboard, the measured angle is displayed in degrees as shown in Figure 46. The update rate for angle is 10 Hz.

![Figure 46. Angle Display in Degrees](image)

5.2.2 Key "b"

If the "b" key is pressed on the keyboard, the measured angle is displayed as an integer as shown in Figure 47. The update rate for angle is 10 Hz.

![Figure 47. Angle Display in Integer](image)

5.2.3 Key "p"

If the "p" key is pressed on the keyboard, the measured angle is displayed as an integer as shown in Figure 47. The update rate for angle is 10 Hz.

5.2.4 Key "h"

If the "h" key is pressed on the keyboard, the histogram of the angle is displayed for 16,000 samples. For the histogram, the GUI asks for the angle value (as shown in Figure 48) and then after the angle is set on the resolver, the histogram is displayed as shown in Figure 49.

![Figure 48. Start-up Requirement for Histogram Display](image)
5.2.5 Key "d"

If the "d" key is pressed on the keyboard, the default settings of the PGA411-Q1 internal registers are displayed as shown in Figure 50. Along with register settings, the settings for AMODE and BMODE0 pins are also displayed. See Section 4.3 for a list of the PGA411 default settings.
5.2.6 Key "g"

If the "g" key is pressed on the keyboard, the register settings are displayed as shown in Figure 51. These may or may not be the default register settings. The "g" key just gets whatever register settings available at that moment. Along with register settings, the settings for AMODE and BMODE0 pins are also displayed.

![Figure 51. Get Register (Key "g") Displays Register Settings](image_url)
5.2.7 Key "w"

If the "w" key is pressed on the keyboard, any of the available registers inside the PGA411-Q1 can be written. Figure 52 shows the message that appears after the "w" key is pressed. Once the register is modified using this function, the user can check back by using the "g" key (get register). Figure 53 shows such one example.

![Figure 52. Writing Internal Register of PGA411-Q1](image)

![Figure 53. Example Showing Register is Modified After Using Key "w"](image)
5.2.8 Key "m"

If the "m" key is pressed on the keyboard, the settings for the AMODE pin and BMODE0 pins can be modified as shown in Figure 54.

![Figure 54. AMODE and BMODE0 Pin Settings](image)

5.2.9 Key "j"

If the "j" key is pressed on the keyboard, the setting for exciter voltage (4 \( V_{\text{RMS}} \) or 7 \( V_{\text{RMS}} \)) as shown in Figure 55 and the setting for angle hysteresis as shown in Figure 56.

![Figure 55. Setting Exciter Voltage (4 \( V_{\text{RMS}} \) or 7 \( V_{\text{RMS}} \))](image)
5.2.10 Key "f"
If the "f" key is pressed on the keyboard, the FAULT pin indication is displayed as shown in Figure 57. The firmware continuously monitors the fault signal from the PGA411-Q1 and the fault indication bits in the read SPI frame. The faults are polled every ISR period and if the fault is preset an appropriate counter is incremented.

![Figure 57. FAULT Pin Indication](image)

5.2.11 Key "r"
If the "r" key is pressed on the keyboard, the FAULT is reset as shown in Figure 58.

![Figure 58. FAULT Reset](image)
6 Testing and Results

6.1 Power Supply Tests

6.1.1 24-V Input to 5-V Rail (5V_VCC)

The following tests were performed to characterize the DC/DC buck converter, which converts the 24-V to a 5-V VCC rail.

6.1.1.1 Switcher Efficiency

Figure 59 shows the efficiency graph for the TPS54140A at $V_{\text{IN}} = 24$-V DC and $V_{\text{OUT}} = 5$-V DC. The peak efficiency observed is 83.3%.

![Graph showing efficiency of TPS54140A at 24-V input and 5-V output with peak efficiency at 83.3%]

Figure 59. Efficiency of TPS54140A at $V_{\text{IN}} = 24$ V and $V_{\text{OUT}} = 5$ V
6.1.1.2 **Load and Line Regulation**

Figure 60 and Figure 61 show the output regulation of the TPS54140A with respect to output load current and input voltage, respectively.

**Figure 60.** Load Regulation (at \( V_{IN} = 24 \) V)

**Figure 61.** Line Regulation (at \( I_{OUT} = 0.5 \) A)
### 6.1.1.3 Output Voltage Ripple

Figure 62 shows the ripple on the 5-V output voltage. The ripple is 14.1 mV(p-p).

**Figure 62. Waveform Showing Output Voltage Ripple**
6.1.1.4 Output Voltage and Switching Waveforms

Figure 63 and Figure 64 show the DC output voltage and the switching waveform, respectively, for the TPS54140A.

Figure 63. Waveform Showing VCC (5 V)

Figure 64. Switching Waveforms for TPS54140A (at I_{out} = 0.5 A)
6.2 PGA411-Q1 Boost Supply Tests

6.2.1 Switcher Efficiency

Figure 65 shows the efficiency graph for internal boost converter of the PGA411-Q1 at $V_{IN} = 5$-V DC and $V_{OUT} = 15$-V DC. The peak efficiency observed is 88.5%.

![Efficiency Graph](image)

**Figure 65. Efficiency of Internal Boost Converter at $V_{IN} = 5$ V and $V_{OUT} = 15$ V**

**NOTE:** As per the PGA411-Q1 datasheet, the input supply to the boost (VCCSW) should range from 4.75 to 8.5 V. Typically, VCCSW can be supplied with the same 5-V rail as VCC and QVCC; however, in applications where high voltages and high currents are needed out of the boost, it is recommended to increase the voltage on VCCSW to achieve desired performance.
6.2.2 Output Voltage Ripple

Figure 66 shows the ripple on the 15-V output voltage. The ripple is 86 mV(p-p).

![Waveform Showing Output Voltage Ripple for Internal Boost Converter](image)

Figure 66. Waveform Showing Output Voltage Ripple for Internal Boost Converter
6.2.3 Output Voltage and Switching Waveforms

Figure 67 and Figure 68 show the DC output voltage and the switching waveform, respectively, for internal boost converter.

Figure 67. Waveform Showing VCC (5 V)

Figure 68. Switching Waveforms for Internal Boost Converter (at $I_{\text{OUT}} = 50 \text{ mA}$)
6.3 Measured Voltages and Currents

Table 21 shows the measured voltages and current consumptions on the TIDA-00363 board with the LTN R58 resolver connected.

Table 21. Measured Voltages and Currents

<table>
<thead>
<tr>
<th>DESIGNATOR</th>
<th>VOLTAGE (V)</th>
<th>MEASURED VOLTAGE (V)</th>
<th>CURRENT CONSUMPTION AT FEXC = 10 kHz (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>24.0</td>
<td>—</td>
<td>36.000</td>
</tr>
<tr>
<td>VCC</td>
<td>5.0</td>
<td>4.996</td>
<td>159.030</td>
</tr>
<tr>
<td>VIO</td>
<td>3.3</td>
<td>3.295</td>
<td>3.910</td>
</tr>
<tr>
<td>VEXT</td>
<td>15.0</td>
<td>14.952</td>
<td>34.227</td>
</tr>
</tbody>
</table>

6.4 Thermal Plot

Figure 69 shows thermal plot of the design at an ambient of 24°C. It is taken at an excitation frequency of 10 kHz with an LTN resolver connected to the board through the Sub-D9 connector. The thermal plot is taken 10 minutes after powering up the board. The maximum temperature on the board is 46.3°C at the PGA411-Q1.

- Excitation current (load current) = 36 mA\text{RMS}
- Excitation voltage = 7 V\text{RMS}
6.5 System Level Tests

6.5.1 Test Setup and Test Equipment
Resolver: LTN resolver (part number R58CURE151B04-021-07AX)
Reference encoder: HEIDENHAIN ROD-480

6.5.2 Output Signal Waveforms for PGA411-Q1
This section shows waveforms measured at different test points available on the TIDA-00363 board.

6.5.3 AOUT Signal
Figure 71 shows the AOUT signal measured on TP3. The resolver is rotated at a very low constant speed to measure the AOUT signal waveform.
6.5.4 Encoder Emulation Signals

Figure 72 and Figure 73 show the encoder emulation signals along with the AOUT signal. The resolver is rotated at a very low constant speed to measure these signal waveforms.

![Figure 72. Encoder Emulation Signals](image1)

![Figure 73. Encoder Emulation Signals (Zoomed)](image2)
6.5.5 OSIN and OCOS Signals

Figure 74 shows the OSIN and OCOS signals along with the AOUT signal taken at an angle of 135 degrees. The OSIN signal is measured on TP1 and the OCOS signal is measured on TP2.

![Figure 74. OSIN and OCOS Signals](image)

6.6 Static Angle Test

As explained in Section 5.2.4, the angle is tested for static accuracy and the angle distribution. Three angles are tested to get the histogram with and without enabling the angle hysteresis.

Figure 75 shows the register settings for the PGA411-Q1 for angle distribution test with the following conditions:

- Angle hysteresis = Disabled
- Excitation mode = 7 V\text{RMS}
- Excitation frequency = 10 kHz
- Number of samples taken = 16000

![Figure 75. Register Settings for Angle Distribution Test](image)
Figure 76 through Figure 78 show the angle distribution for the angles measured.

Figure 76. Angle Distribution for Angle = 0 Degrees

Figure 77. Angle Distribution for Angle = 45 Degrees

Figure 78. Angle Distribution for Angle = 90 Degrees
Figure 79 shows the register settings for the PGA411-Q1 for the angle distribution test with the following conditions:

- Angle hysteresis = Enabled (1 LSB)
- Excitation mode = 7 V\text{RMS}
- Excitation frequency = 10 kHz
- Number of samples taken = 16000

![PGA411 Register Data (Hex)](image)

**Figure 79. Register Settings for Angle Distribution Test**
Figure 80 through Figure 82 show the angle distribution for the angles measured.

6.6.1 Minimum Measured Angular Accuracy

The angular accuracy test is done using the test bench shown in Figure 70 and with two exciter voltage modes: $4\,V_{\text{RMS}}$ and $7\,V_{\text{RMS}}$. Figure 83 shows the accuracy graph. Regardless the mode used for excitation, the angle accuracy is within ±0.2 degrees.

NOTE: With a 12-bit resolution, 1 LSB equals 0.087 degrees (5.27 arc min).
To check the repeatability of the angle accuracy after the power supply, the design is tested before and after the power cycle. Figure 84 shows the accuracy graph. The angle accuracy is within ±0.2 degrees before and after the power cycling.

**Figure 84. Angle Error With 4-V\textsubscript{RMS} Excitation Mode (Before and After Power Cycle)**
The AFE circuit uses resistors as explained in Section 3.5.1. To create a gain error, this design is intentionally tested with the high tolerance (2.5%) gain set resistors on the SIN channel. Figure 85 shows the measured angle accuracy due to an incorrect gain setting resistors on the SIN channel. Therefore, set the gain resistors with a tolerance of 0.1%.

Figure 85. Angle Error With 4-V\(_{\text{RMS}}\) Excitation Mode (2.5% Gain Error on SIN Channel)
6.6.2 Dynamic Angle Test (Step Response)

Many drives applications have a dynamic change in the angle, and the RDC should be able to respond to these changes. The TIDA-00363 is tested for two small angle step responses. Figure 86 shows the step response for a 1-degree change and the angle settles to the required angle within 938 µs. Figure 87 shows the step response for a 5-degree change and the angle settles to the required angle within 2 ms.

Figure 86. Step Response for 1-Degree Angle Change

Figure 87. Step Response for 5-Degree Angle Change
6.6.3 System Fault Conditions Test

The TIDA-00363 is tested for several fault conditions as shown in Table 22. During the fault conditions, the status of the FAULT pin and exciter output signal is observed.

Table 22. FAULT Conditions Tested With TIDA-00363

<table>
<thead>
<tr>
<th>SR NO</th>
<th>FAULT CONDITION</th>
<th>STATUS OF FAULT PIN</th>
<th>STATUS OF EXCITER OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Resolver disconnected</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>2</td>
<td>Sine input disconnected</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>3</td>
<td>Cosine input disconnected</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>4</td>
<td>Exciter output disconnected</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>5</td>
<td>Exciter connected to GND</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>6</td>
<td>SINE connected to GND</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>7</td>
<td>COS connected to GND</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>8</td>
<td>SINE mutual short</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
<tr>
<td>9</td>
<td>COS mutual short</td>
<td>FAULT pin goes high</td>
<td>Exciter output turns off</td>
</tr>
</tbody>
</table>

6.7 EMC Test Results

The TIDA-00363 TI Design has been tested for IEC61000-4-2, 4-4, and 4-5 (ESD, EFT, and surge) with the test levels and performance criterion specified in the standard IEC 61800-3 "EMC immunity requirements and specific test methods applicable in adjustable speed, electrical power drive systems".

The design is compliant to these standards and exceeds the voltage requirements according to IEC 61800-3 EVM immunity requirements. A summary is shown in the following tables and more details in the following sections.

The performance (acceptance) criterion is defined in Table 23:

Table 23. Performance Criterion

<table>
<thead>
<tr>
<th>PERFORMANCE (ACCEPTANCE) CRITERION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The module must continue to operate as intended. No loss of function or performance even during the test</td>
</tr>
<tr>
<td>B</td>
<td>Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.</td>
</tr>
<tr>
<td>C</td>
<td>During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart, or power off, or power on.</td>
</tr>
</tbody>
</table>

The performance criterion A is often customer specific and the expected accuracy is depending system requirements.

Table 24. IEC618000-3 EMC Immunity Requirements for Second Environment and Measured

<table>
<thead>
<tr>
<th>IEC618000-3 EMC IMMUNITY REQUIREMENTS FOR SECOND ENVIRONMENT AND MEASURED</th>
<th>TIDA-00363 MEASUREMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORT</td>
<td>PHENOMENON</td>
</tr>
<tr>
<td>ENCLOSURE PORTS</td>
<td>ESD</td>
</tr>
<tr>
<td>PORTS FOR CONTROL LINES AND DC AUXILIARY SUPPLIES (&lt; 60 V)</td>
<td>Fast transient burst (EFT)</td>
</tr>
<tr>
<td></td>
<td>Surge 1.2/50 µs, 8/20 µs</td>
</tr>
</tbody>
</table>
6.7.1 Test Setup

Figure 88 shows the basic test setup for the TIDA-00363 design. The following equipment was used:

- Cable: HEIDENHAIN 20-m shielded cable, PUR M23 male/female (4 × 2 × 0.14 mm; 4 × 0.5 mm)
- Resolver: LTN resolver (part number R58CURE151B04-021-07AX)

To verify the angle signal integrity during and after the EMC test, the resolver initial angle position (standstill) was used as a reference during the EMC tests and the resolver was not turned. The angle was measured every 16 kHz and the result was compared to the initial reference angle position. The angle output is a 12-bit resolution, hence every time a bit changes (because of angle error during the EMC test), the corresponding error counter was increased by 1.

The firmware used was the Resolver_PGA411_F28069M_Example_Firmware v1_0.out, as provided with this TI Design. The firmware runs on the TMS320F28069M Piccolo MCU.

A picture of the specific test setup for ESD, EFT, and surge is shown in the corresponding following subsections.
6.7.2 IEC 61000-4-2 ESD Test Results

Figure 89 shows the ESD test setup for the TIDA-00363. The ESD strike was applied to the Sub-D9 female connector's shield. The shield was also connected to Earth and the LTN resolver was connected through a 20-m shielded twisted pair cable.

![Figure 89. IEC61000-4-2 ESD Test Setup for TIDA-00363](image)

Figure 90. Zoomed Photo Showing Where ESD Was Stroked on Board

![Figure 90. Zoomed Photo Showing Where ESD Was Stroked on Board](image)
Table 25 shows the complete ESD test results for contact discharge at voltage levels, which also exceed the requirements per IEC61800-3. This is marked accordingly.

Table 25. IEC-61000-4-2 ESD Test Results for TIDA-00363

<table>
<thead>
<tr>
<th>PHENOMENON</th>
<th>BASIC STANDARD</th>
<th>LEVEL</th>
<th>TIDA-00363 CONNECTOR</th>
<th>ANGLE BEFORE ESD TEST (DEGREE)</th>
<th>ANGLE AFTER ESD TEST (DEGREE)</th>
<th>ACHIEVED PERFORMANCE</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>±4-kV CD</td>
<td>Sub-D9</td>
<td>161.1914</td>
<td>161.1914</td>
<td>B</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td>±6-kV CD</td>
<td>Sub-D9</td>
<td>161.1035</td>
<td>161.1035</td>
<td>B</td>
<td>Not required per IEC61800-3</td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td>±8-kV CD</td>
<td>Sub-D9</td>
<td>161.1035</td>
<td>161.1035</td>
<td>B</td>
<td>Not required per IEC61800-3</td>
<td></td>
</tr>
</tbody>
</table>

6.7.3 IEC 61000-4-4 EFT Test Results

Figure 91 shows a picture of the EFT test setup for the TIDA-00363. During the EFT test, the Sub-D9 female connector was connected to a 20-m twisted pair shielded cable with the LTN resolver at the far end.

![Figure 91. IEC61000-4-4 EFT Test Setup for TIDA-00363](image)

Table 26 shows the complete EFT test results, which also exceed the requirements per IEC61800. This is marked accordingly.

Table 26. IEC-61000-4-4 EFT Test Results for TIDA-00363

<table>
<thead>
<tr>
<th>PHENOMENON</th>
<th>BASIC STANDARD</th>
<th>LEVEL</th>
<th>TIDA-00363 CONNECTOR</th>
<th>ANGLE BEFORE EFT TEST (DEGREE)</th>
<th>ANGLE AFTER EFT TEST (DEGREE)</th>
<th>ACHIEVED PERFORMANCE</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>EFT</td>
<td>±2-kV/5-kHz capacitive clamp</td>
<td>Sub-D9</td>
<td>161.1914</td>
<td>161.1914</td>
<td>B</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>EFT</td>
<td>±4-kV/5-kHz capacitive clamp</td>
<td>Sub-D9</td>
<td>161.1035</td>
<td>161.1035</td>
<td>B</td>
<td>Not required per IEC61800-3</td>
<td></td>
</tr>
</tbody>
</table>
6.7.4 IEC 61000-4-5 Surge Test Results

Figure 92 shows a picture of the surge test setup for the TIDA-00363. During the surge test, the Sub-D9 female connector was connected to a 20-m twisted pair shielded cable with the LTN resolver at the far end.

![Surge test setup diagram]

**Figure 92. IEC61000-4-5 Surge Test Setup for TIDA-00363**

Table 27 shows the complete EFT test results, which also exceed the requirements per IEC61800. This is marked accordingly.

<table>
<thead>
<tr>
<th>PHENOMENON</th>
<th>BASIC STANDARD</th>
<th>LEVEL</th>
<th>TIDA-00363 CONNECTOR</th>
<th>ANGLE BEFORE SURGE TEST (DEGREE)</th>
<th>ANGLE AFTER SURGE TEST (DEGREE)</th>
<th>ACHIEVED PERFORMANCE</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surge</td>
<td>IEC 61000-4-5</td>
<td>±1 kV/2 Ω (20-m shielded cable)</td>
<td>Sub-D9</td>
<td>161.1035</td>
<td>161.1035</td>
<td>B</td>
<td>—</td>
</tr>
<tr>
<td>Surge</td>
<td>IEC 61000-4-5</td>
<td>±2 kV/2 Ω (20-m shielded cable)</td>
<td>Sub-D9</td>
<td>161.1035</td>
<td>161.1035</td>
<td>B</td>
<td>Not required per IEC61800-3</td>
</tr>
</tbody>
</table>
7 Design Files

7.1 Schematics
To download the schematics for each board, see the design files at TIDA-00363.

7.2 Bill of Materials
To download the bill of materials for each board, see the design files at TIDA-00363.

7.3 PCB Layout Recommendations
Find specific layout guidelines for each individual TI part used in this TI Design in their respective datasheets. Figure 38 and Figure 39 show the top and bottom views of the TIDA-00363 PCB, respectively. The important sections are highlighted with red arrows and captions.

7.3.1 Layout for Power Management Circuit—TPS54140A
Layout is a critical portion of a good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 93 for a PCB layout example. Tie the GND pin directly to the power pad under the IC and the power pad. Connect the power pad to any internal PCB ground planes using multiple vias directly under the IC. Route the PH pin to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor must be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at a full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise, so the RT resistor must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however, this layout has been shown to produce good results and is meant as a guideline.

Figure 93. Layout for TPS54140A
7.3.2 Layout for Power Management Circuit—TPS79933

Figure 94 shows the layout for the TPS79933. The important components for the TPS79933 are highlighted. To improve AC performance (such as PSRR, output noise, and transient response), it is important to design the board with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition:

1. Do place at least one 2.2-μF ceramic capacitor as close as possible to the OUT pin of the regulator.
2. Do not place the output capacitor more than 10 mm away from the regulator.
3. Do connect the bypass capacitor directly to the GND pin of the device.

![Figure 94. Layout for TPS79933](image)

7.3.3 Star Ground Topology

The PGA411-Q1 has three ground pins: PGND (power ground), DGND (digital ground), and QGND (quiet ground). PGND and DGND pins are connected through the PGA411-Q1 itself. The TIDA-00363 implements STAR ground topology and all three grounds are connected to each other as shown in Figure 95. R41 is added for further flexibility and decoupling of the quiet ground from the power and digital ground.

![Figure 95. Star Ground Topology](image)
7.3.4 PCB Layer Stack

The PCB has four layers. The top and bottom layers are mainly assigned to signals. The mid layer 1 is assigned to the ground plane and mid layer 2 is assigned to the supply planes. Figure 96 shows the placement of R41, which connects QGND with PGND (and DGND).

Figure 96. Placement of R41 on PCB (Only Top and Bottom Layer Shown)

Figure 97 shows the star ground for the PCB: (A) shows the QGND plane and (B) shows the PGND plane.

Figure 97. Star Ground on PCB (A) QGND Plane (B) PGND Plane
7.3.5 Ground and Power Planes:

While Figure 97 highlights the ground planes with all layers enabled, Figure 98 shows the ground plane only on the mid layer 1 (referred to as the ground layer) on the TIDA-00363 board.

Figure 99 shows the mid layer 2 (referred to as the supply layer) for the power planes: 5V_VCC plane, 3V3_VIO plane, QVCC_5V_FE Plane, and VEXT Plane (15-V plane for the TIDA-00363).
Figure 99. Power Planes and Cutouts

Note the cut-outs shown in Figure 98 and Figure 99. These cut-outs are placed below the following components:

- Components related to the boost circuit of the PGA411-Q1
- Inductor of the TPS54140A-based buck converter
7.3.6 Layout of Boost Circuit for PGA411-Q1

Figure 100 shows the boost circuit, and Figure 101 shows the layout and placement of boost circuit for the PGA411-Q1. The following are the most important points to be highlighted:

1. The placement of components L1 and D6 should form a smallest possible switching current loop.
2. C32 is input capacitor, which placed on the bottom layer and very close to the IC.
3. D5 is DNP and was used only for test and debug. C18 and C23 are output caps. They close the loop very tightly.

Figure 100. Boost Section for PGA411-Q1

Figure 101. Layout of Boost Circuit for PGA411-Q1
7.3.7 Layout for Front-End Circuit for PGA411-Q1

Figure 17 and Figure 18 show the AFE with the gain setting resistors, filters, and ESD protection for the resolver's differential SIN and COS signals, respectively.

Figure 102 shows the placement and layout of both the circuits.

Figure 102. Placement of Protection Circuit for AFE
7.3.8 Decoupling for PGA411-Q1

The PGA411-Q1 has five supply pins as shown in Figure 103.

1. The VDD regulator receives a 5-V input supply voltage from the VCC pin and generates a stable 1.8-V supply for internal digital logic circuits. The VDD pin requires an external filtering capacitor. A 10-µF capacitor is connected to VDD pin for filtering.

2. VIO_3.3V is the digital supply voltage for I/O pins of the PGA411-Q1.

3. C5 and C6 are used as decoupling caps for VCC pin.

4. VEXT pin has a decoupling cap of 0.1 µF (C49).

5. The QVCC generation and decoupling for QVCC is explained in Section 7.3.9.

Figure 104 shows the placement of decoupling caps on the PCB.

![Figure 103. Decoupling of Supply Pins for PGA411-Q1](image1)

![Figure 104. Highlighted Decoupling Components](image2)
7.3.9 Generation of QVCC for PGA411-Q1

The AFE is referenced to the quiet ground pin QGND and powered by the quiet voltage supply QVCC pin. Quiet VCC (QVCC) is generated by providing more filtering to 5V_VCC. As shown in Figure 105, a ferrite bead (FB1) with two capacitors C33 (10 µF) and C34 (0.1 µF) form a filter. QVCC_5V is connected to Pin 39 of the PGA411-Q1. The QVCC_5V_FE is further filtered using an RC filter (R43 and C37) to provide to the input circuitry, which connects the PGA411-Q1 to the resolver.

Figure 105. QVCC Generation

Figure 106. Placement and Layout for QVCC Generation Circuit
7.4 Layout Prints
To download the layout prints for each board, see the design files at TIDA-00363.

7.5 Altium Project
To download the Altium project files for each board, see the design files at TIDA-00363.

7.6 Gerber Files
To download the Gerber files for each board, see the design files at TIDA-00363.

7.7 Assembly Drawings
To download the assembly drawings for each board, see the design files at TIDA-00363.

8 Software Files
To download the firmware for this reference design, see the link at TIDA-00363.

9 Related Documentation
1. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)
2. Texas Instruments, TINA-TI Simulation Software (http://www.ti.com/tina-ti)
3. LTN Servotechnik GmbH, LTN Resolver Part Number R58CURE151B04-021-07AX (http://www.ltn.de/en/products/resolvers/)
4. Texas Instruments, Design considerations for resolver-to-digital converters in electric vehicles, Technical Brief (SLYT661)
5. Texas Instruments, Troubleshooting Guide for PGA411-Q1, Application Report (SLAA687)
6. IEC 61800-3 ed2.0 (2004-08), Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods, [IEC 61800-3 ed2.0 (2004-08)]
7. IEC 61800-3-am1 ed2.0 (2011-11), Amendment 1 - Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods, [IEC 61800-3-am1 ed2.0 (2011-11)]

9.1 Trademarks
All trademarks are the property of their respective owners.

10 About the Authors
SANJAY PITHADIA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Sanjay has been with TI since 2008 and has been involved in designing products related to Energy, Smart Grid, and Industrial Motor Drives. Sanjay brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Sanjay earned his bachelor of technology in electronics engineering at VJTI, Mumbai.

NELSON ALEXANDER is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Nelson has been with TI since 2011 and has been involved in designing products related to smart grid and embedded systems based on microcontrollers. Nelson earned his bachelor of technology in electrical engineering at MSRIT, Bangalore.

MARTIN STAEBLER is a system architect in the Industrial Systems-Motor Drive team at Texas Instruments, responsible for specifying reference designs for industrial drives.
### Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>Changes from Original (August 2016) to A Revision</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed from preview draft</td>
<td>1</td>
</tr>
</tbody>
</table>

---

---
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include, without limitation, TI's standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated