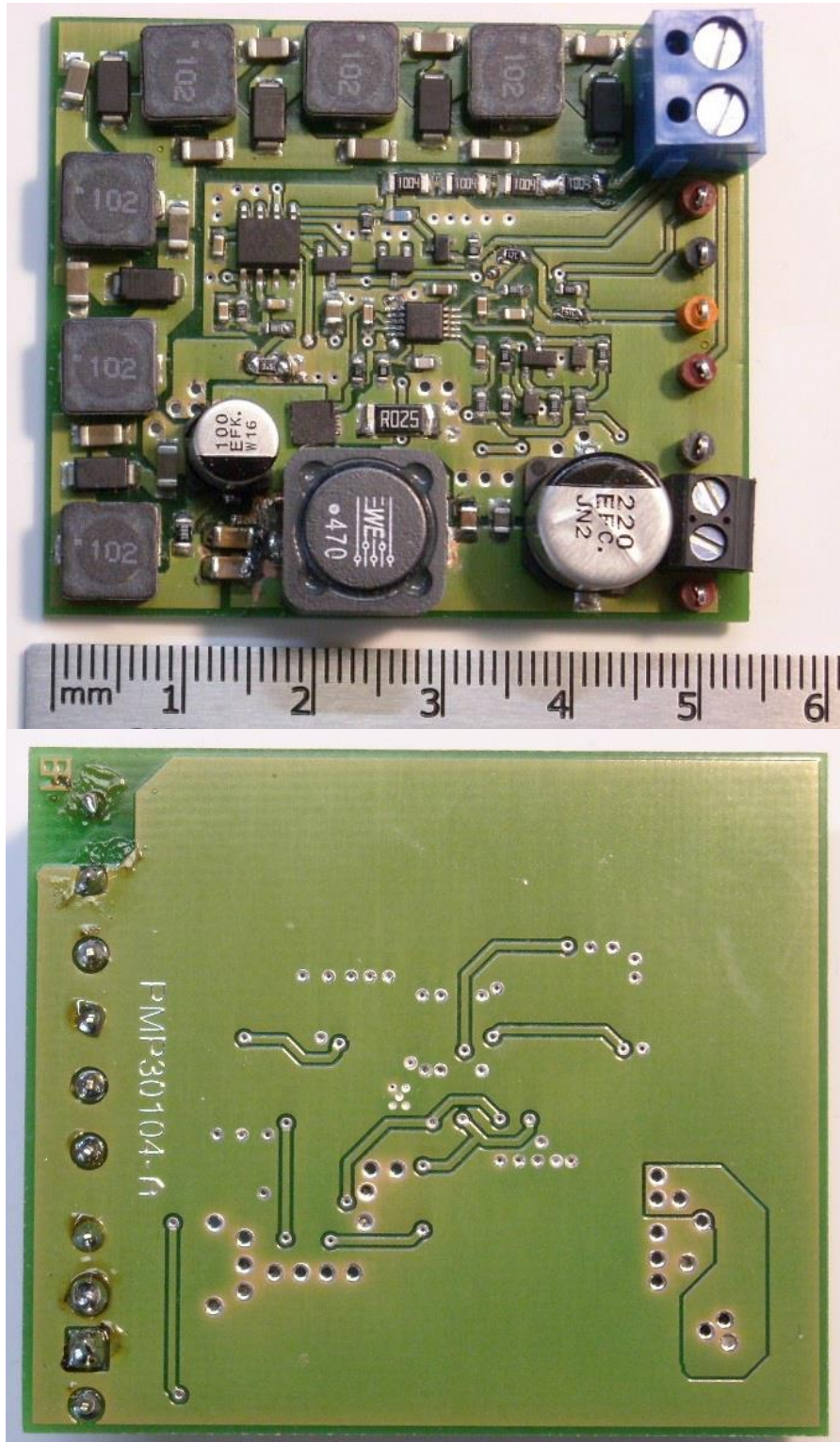


1 Photo of the prototype (54.61mm x 46.61mm, height 13mm).

The Reference design PMP30104 Revision B has been built on PMP30104 Revision A PCB.



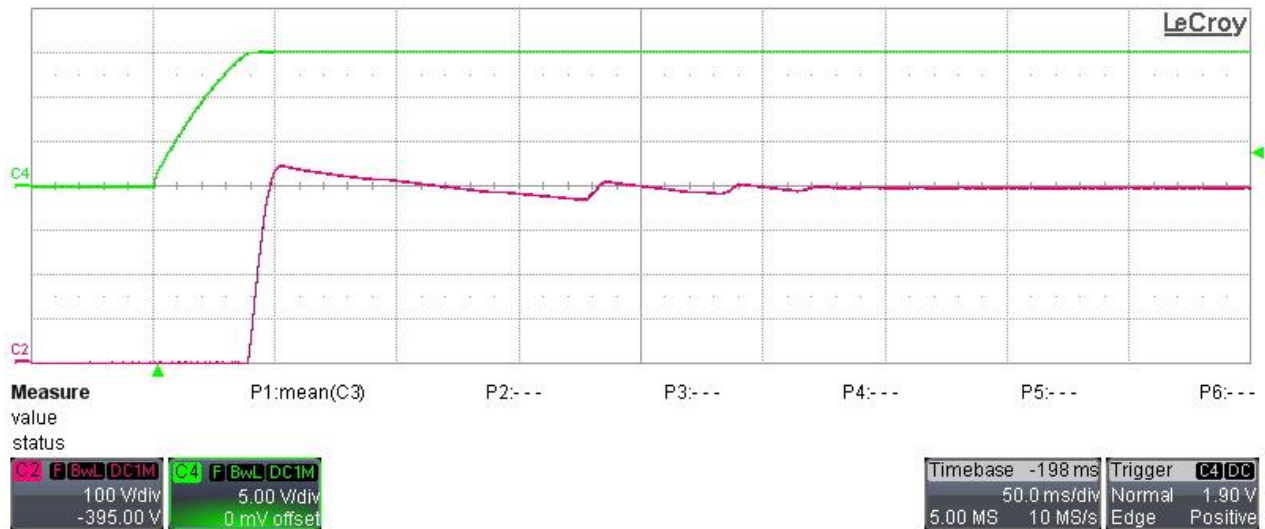
2 Startup

The input and output voltage behavior in different load conditions is shown in the images below.

Ch.2: Output voltage (100V/div, 50ms/div, 20MHz BWL)

Ch.4: Input voltage (5V/div, 20MHz BWL)

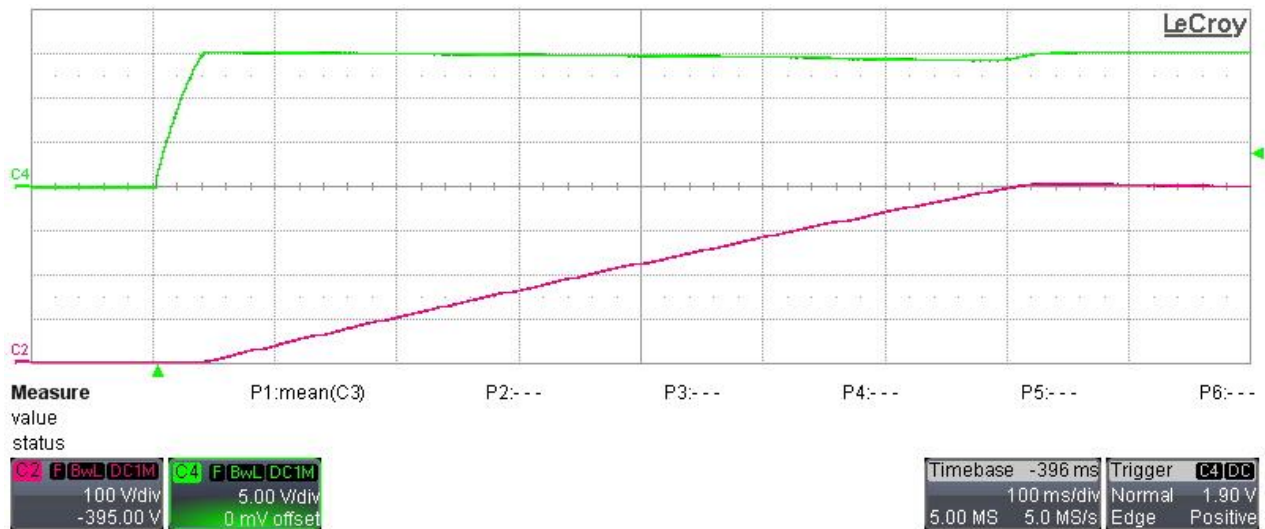
Vout set to 400V, output connector left open (no load, no capacitor), Vin = 15V.



Ch.2: Output voltage (100V/div, 100ms/div, 20MHz BWL)

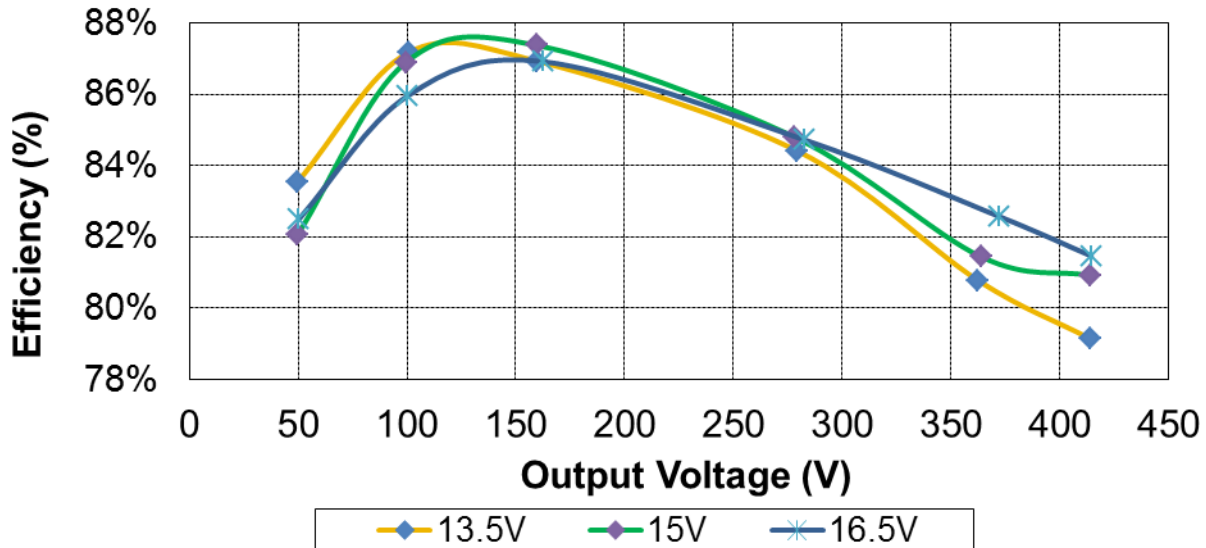
Ch.4: Input voltage (5V/div, 20MHz BWL)

Vout set to 400V, 130uF capacitor connected to Vout, output unloaded, Vin = 15V.



3 Efficiency

The efficiency data, versus input and output voltage are shown in the tables and graph below. The load (variable resistor) has been varied in order to get different Vout (since the converter is a constant current generator, set to deliver 420V (Q3 ON)). The input voltage has been set respectively to 15V \pm 10%.



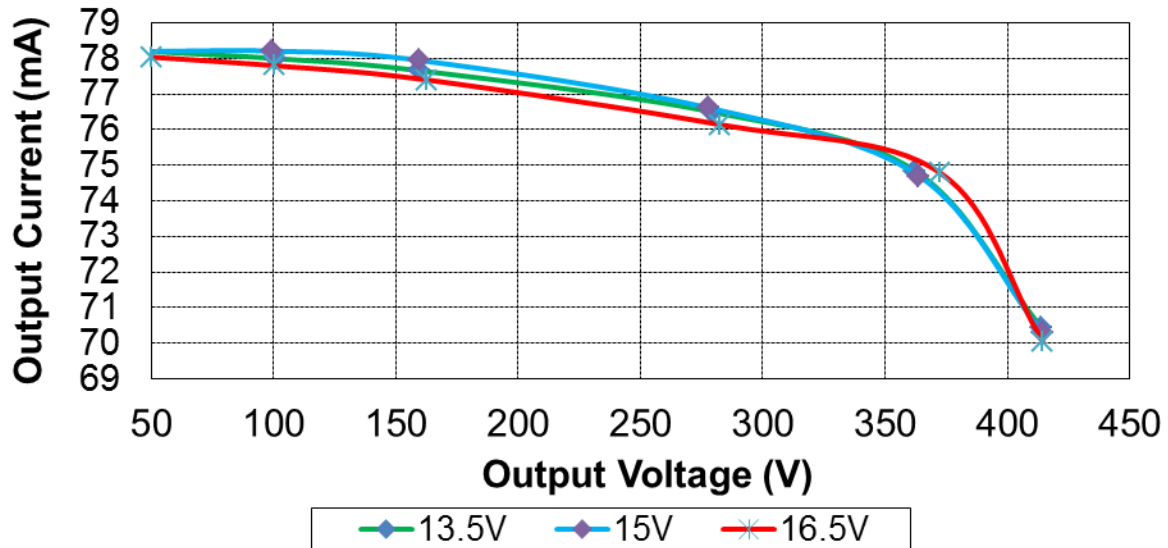
Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
13.64	0.341	4.65	49.69	78.20	3.89	83.5%
13.55	0.666	9.02	100.8	78.00	7.86	87.2%
13.48	1.057	14.25	159.5	77.66	12.39	86.9%
13.55	1.868	25.31	279.3	76.50	21.37	84.4%
13.53	2.480	33.55	362.2	74.84	27.11	80.8%
13.65	2.698	36.83	413.9	70.42	29.15	79.1%
13.53	0.0188	0.254	418.8	0	0	0.0%

Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
15.00	0.316	4.74	49.74	78.20	3.89	82.1%
14.95	0.600	8.97	99.6	78.21	7.79	86.9%
15.01	0.948	14.23	159.5	77.95	12.43	87.4%
15.03	1.671	25.12	278.0	76.61	21.30	84.8%
14.93	2.235	33.37	363.8	74.70	27.18	81.4%
14.92	2.411	35.97	414.1	70.29	29.11	80.9%
15.57	0.0191	0.297	420.2	0	0	0.0%

Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
16.75	0.283	4.74	50.10	78.04	3.91	82.5%
16.55	0.548	9.07	100.2	77.80	7.80	86.0%
16.67	0.869	14.48	162.6	77.40	12.59	86.9%
16.53	1.537	25.41	282.7	76.14	21.52	84.7%
16.59	2.033	33.73	372.3	74.80	27.85	82.6%
16.51	2.158	35.63	414.4	70.04	29.02	81.5%
16.50	0.0179	0.295	420.4	0	0	0.0%

4 Output Current

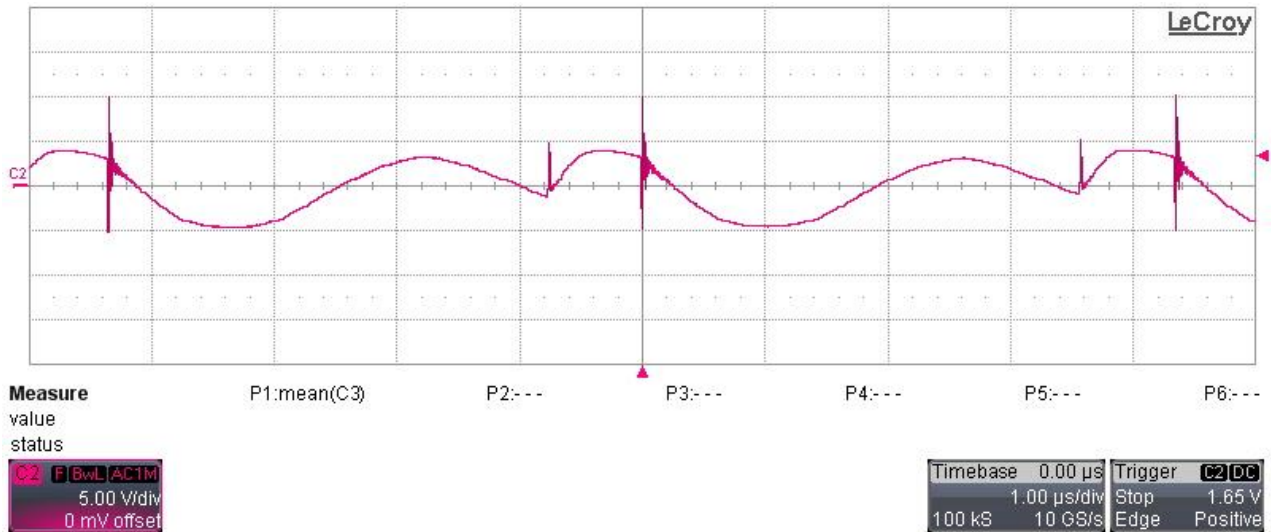
The output current variation versus output voltage, for different input voltages, is plotted below.



5 Output Ripple Voltage

The output ripple voltage has been measured by supplying the converter at 15V while running in constant current limit and set to deliver 420V.

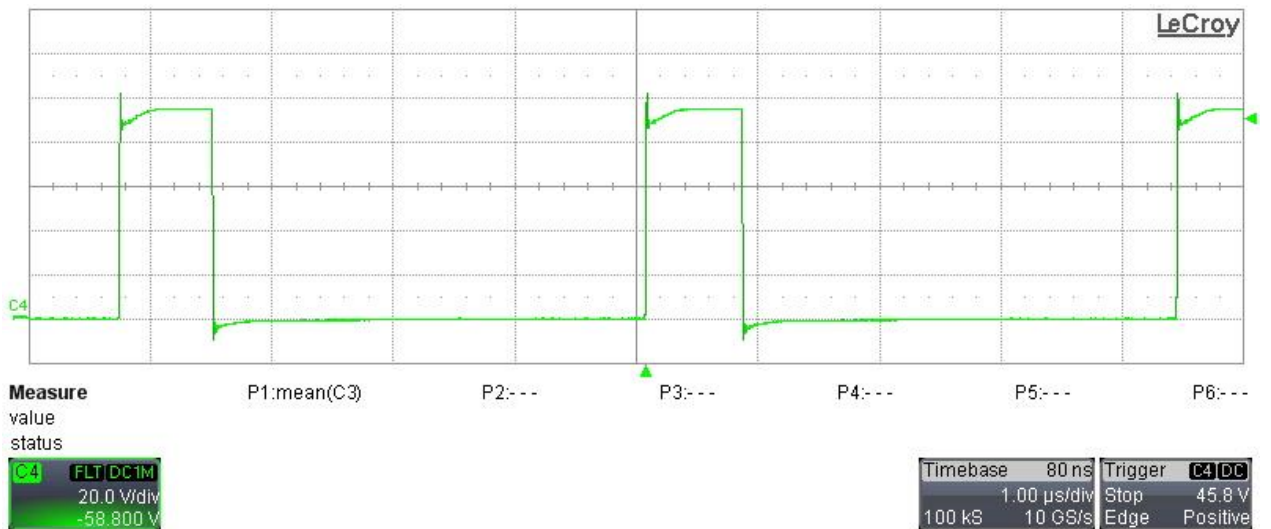
Ch.2: Output ripple voltage (5V/div, AC coupling, 1usec/div, 20MHz BWL)



6 Switch node

The image below shows the drain of Q2 taken at $V_{in} = 16.5V$ and $V_{out} = 420V$, while delivering 78mA.

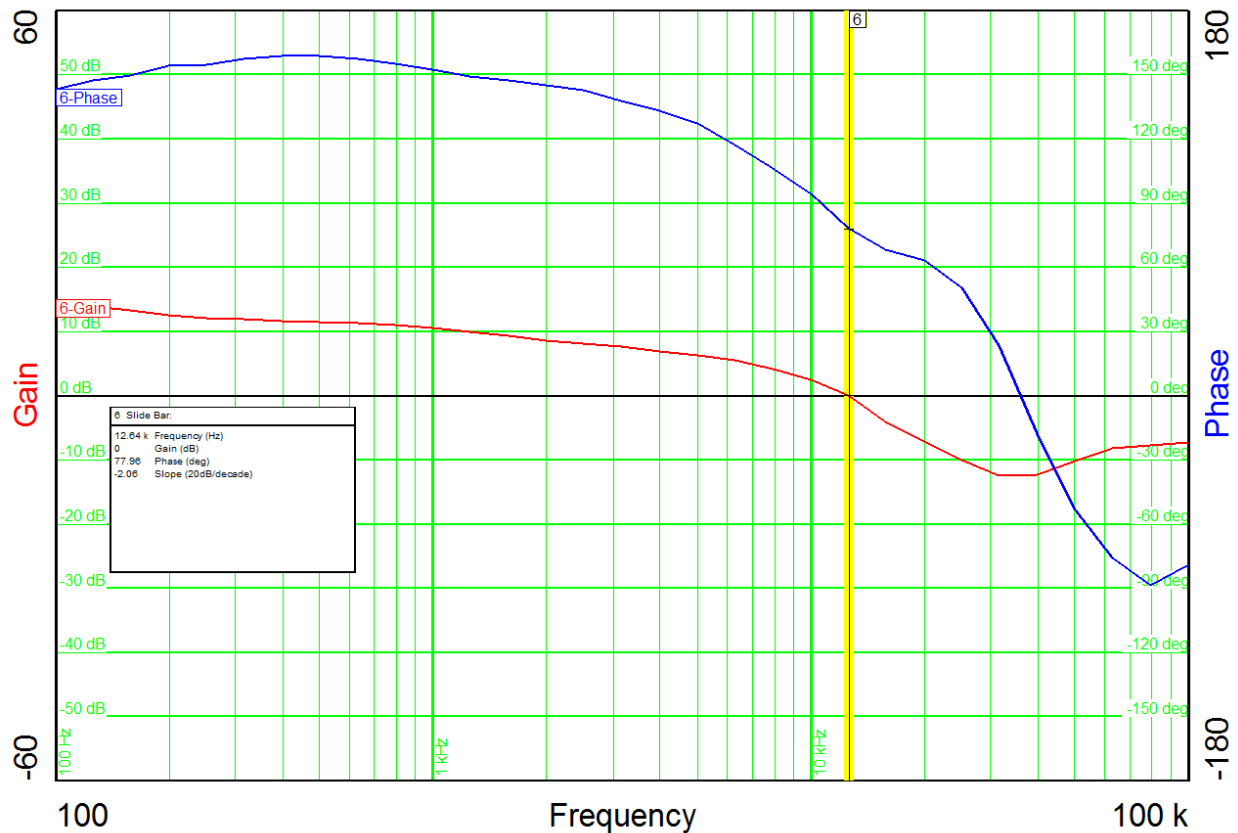
Ch.4: Q2-Drain voltage (20V/div, 1us/div, no BWL)



7 Feedback Loop Analysis

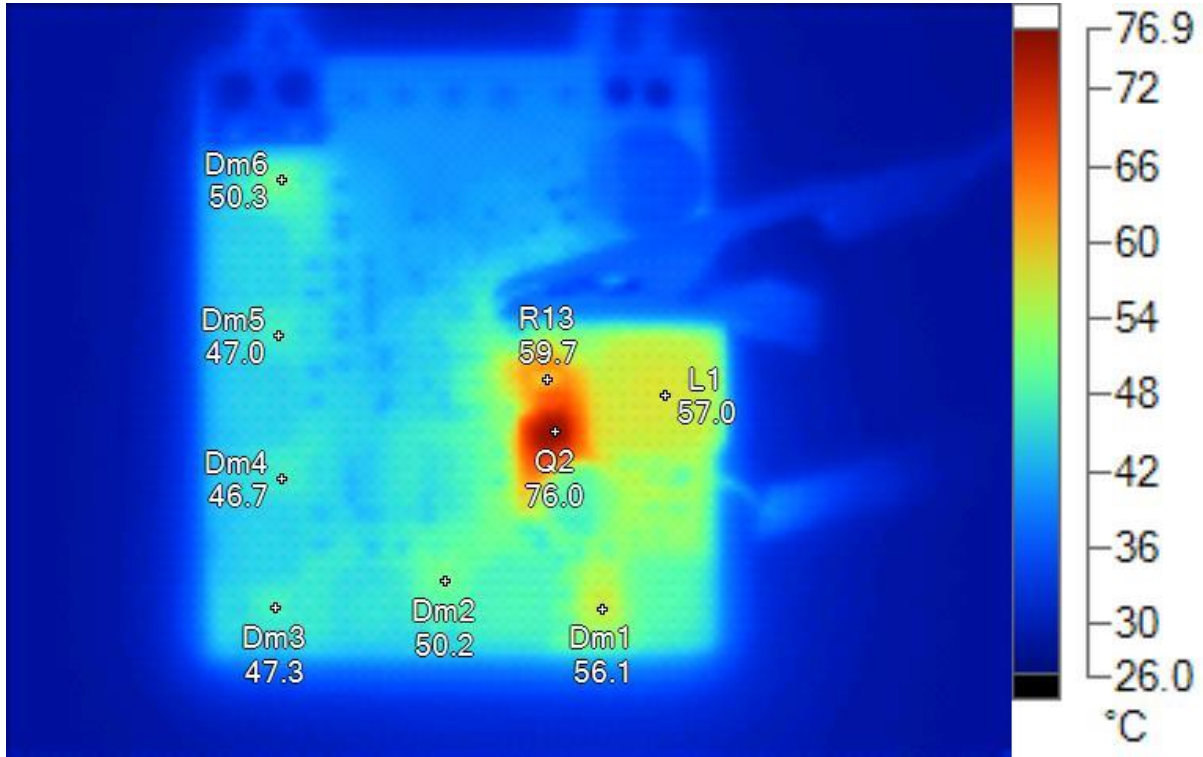
The image below shows the open loop gain and phase margin of the constant current loop. The board has been supplied at $V_{in} = 15V$ and the load was a resistor + an electrolytic capacitor (130uF). The resistor has been varied to obtain 350V on output terminals. Here are the results:

Crossover frequency: 12.64 KHz
 Phase margin: 77.96 deg.
 Gain margin: 12.45 dB



8 Thermal Analysis

During the thermal analysis, the converter has been placed horizontally on the bench in still air conditions, while supplied 13.5V (worst case) and delivering 390V @ 80mA for two minutes.



Main Image Markers

Name	Temperature	Emissivity	Background
Q2	76.0°C	0.95	23.0°C
Dm1	56.1°C	0.95	23.0°C
L1	57.0°C	0.95	23.0°C
Dm6	50.3°C	0.95	23.0°C
Dm5	47.0°C	0.95	23.0°C
Dm4	46.7°C	0.95	23.0°C
Dm3	47.3°C	0.95	23.0°C
Dm2	50.2°C	0.95	23.0°C
R13	59.7°C	0.95	23.0°C

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated