**Description**

The TIDA-01366 (also known as PMP9799) demonstrates a complete power solution for Altera’s MAX® 10 FPGA. This simple solution uses just three DC/DC converters to power the MAX 10 cost-effectively. This TI Design supports numerous industrial applications and any application that requires a small, high efficiency, high temperature power supply.

**Features**

- Supports Dual-Supply Power Option of MAX 10 to Enable Full FPGA Functionality
- Requires Just Three DC/DCs for a Cost-Effective and Simple Power Solution
- Total Solution Size < 300 mm² for Space-Constrained Applications
- 92% Efficiency at Half of Rated Load and 89% Efficiency at Full Rated Load for Low Temperature Rise and High Reliability
- Supports Instant-On Feature for Fastest Startup of MAX 10
- 125°C Rated Devices and Passives for High Temperature Applications with a Temperature Warning Flag at 120°C

**Resources**

- TIDA-01366 Design Folder
- TPS62097 Product Folder
- TPS62480 Product Folder
- TPS22925 Product Folder

**Applications**

- Motor Drives
- Test and Measurement
- Factory Automation and Control
- Electronic Point of Sale
- Medical

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System Overview

1  System Overview

1.1  System Description

Altera's MAX® 10 Field-Programmable Gate Array (FPGA) is used in a variety of industrial applications that require a lower power, smaller, and configurable processing device. The TIDA-01366 provides a tested and documented power solution when using the MAX 10 as a dual-supply device. The power architecture follows what is shown in Reference 2 when using the built-in analog-to-digital converter (ADC) feature. A 1.2-V rail is required for the core, a 2.5-V rail for the ADC, and possibly a third rail is required for the input/output (I/O) rails. 1.5 V is chosen for the I/O rail to support DDR3 memory. A load switch is included as an optional feature to support Instant-On.

The TIDA-01366 achieves high efficiency by using efficient, integrated DC/DC converters and no low dropout (LDO) linear regulators. High efficiency results in a low self-temperature rise and higher reliability. All components are rated to 125°C to support high ambient temperature industrial environments. Furthermore, a temperature warning flag (Thermal Good feature in the TPS62480) is implemented to alert the system host of high temperatures. The three DC/DC converters and their passive components occupy less than 300 mm² of printed circuit board (PCB) space. At less than 100 mm² per rail, this enables space-constrained systems with little PCB space.
## 1.2 Key System Specifications

### Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>2.7 to 5.5 V</td>
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<tr>
<td>OUTPUTS PROVIDED</td>
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</tr>
<tr>
<td><strong>VCC (JP2 shorted)</strong></td>
<td></td>
<td></td>
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<tr>
<td>Voltage setpoint</td>
<td>1.2 V</td>
<td>Section 4.1</td>
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<tr>
<td>Ripple</td>
<td>&lt; 20 mV</td>
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<tr>
<td>Transient response</td>
<td>&lt; 5% (50% load step)</td>
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<tr>
<td>Load regulation</td>
<td>&lt; 1.2%</td>
<td></td>
</tr>
<tr>
<td>Line regulation</td>
<td>&lt; 0.4%</td>
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<tr>
<td>VCCIO</td>
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<tr>
<td>Voltage setpoint</td>
<td>1.5 V</td>
<td>Section 4.2</td>
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<tr>
<td>Ripple</td>
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<tr>
<td>Transient response</td>
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<tr>
<td>Load regulation</td>
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<td></td>
</tr>
<tr>
<td>Line regulation</td>
<td>&lt; 0.4%</td>
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<tr>
<td>VCCA</td>
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<td></td>
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<tr>
<td>Voltage setpoint</td>
<td>2.5 V</td>
<td>Section 4.3</td>
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<td>Ripple</td>
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<tr>
<td>Transient response</td>
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<tr>
<td>Load regulation</td>
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<tr>
<td>Line regulation</td>
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<td>VCCD_PLL</td>
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<td>Voltage setpoint</td>
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<td>Section 4.4</td>
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<td>VCCA_ADC</td>
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<td>Voltage setpoint</td>
<td>2.5 V</td>
<td>Section 4.5</td>
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<tr>
<td>Transient response</td>
<td>&lt; 2% (50% load step)</td>
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<tr>
<td>VCCINT</td>
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<td></td>
</tr>
<tr>
<td>Voltage setpoint</td>
<td>1.2 V</td>
<td>Section 4.6</td>
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<tr>
<td>Transient response</td>
<td>&lt; 3% (50% load step)</td>
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<td>Efficiency (each regulator at half of its rated load, JP2 shorted)</td>
<td>92%</td>
<td>Section 4.1, Section 4.2, Section 4.3</td>
</tr>
<tr>
<td>Efficiency (each regulator at its full rated load, JP2 shorted)</td>
<td>89%</td>
<td>Section 4.1, Section 4.2, Section 4.3</td>
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<td>Sequencing order (JP2 open)</td>
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<td>Section 4.7</td>
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<tr>
<td>Sequencing order (JP2 shorted)</td>
<td>VCCIO, VCCA, VCC</td>
<td>—</td>
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</table>
1.3 Block Diagram

Figure 1. Block Diagram

1.4 Highlighted Products

1.4.1 TPS62097

The TPS62097 is a 2-A, high efficiency step-down converter optimized for a very accurate output voltage and small solution size. Its forced pulse width modulation (PWM) mode and 1% output voltage accuracy provide an accurate DC output voltage. Its iDCS-Control topology enables a very fast transient response to regulate the output voltage during heavy load changes, while its high switching frequency enables the use of a small inductor and output capacitor.

1.4.2 TPS62480

The TPS62480 is a 6-A, dual-phase, high efficiency step-down converter optimized for a very accurate output voltage and small solution size. Its forced pulse width modulation (PWM) mode and 1% output voltage accuracy provide an accurate DC output voltage. A dual-phase architecture is used to reduce the inductor size and the \( I^2R \) losses by halving the total output current for each phase. Its high switching frequency enables the use of small inductors and output capacitors.

1.4.3 TPS22925

The TPS22925 is a 3-A load switch that is used for the VCC rail when the MAX 10's Instant-On feature is required. This load switch has a very low on-resistance \( (R_{on}) \) which results in both high efficiency and improved load regulation. If Instant-On is not required, the load switch is omitted and VCC connected directly to the TPS62480's 1.2-V output voltage.
2 System Design Theory

An FPGA's power requirements are a function of the specific FPGA functionality used in a given application. In most cases, the current drawn by each rail is not known precisely during the design phase. Only gross estimates are available when the power supply is designed. For this reason, the TIDA-01366 uses DC/DC converters that are high enough power to support the majority of MAX 10 applications, while still supplying a small solution size and high efficiency. A 2-A converter is used for the I/O rail, as well as the VCCA (2.5-V analog) rail. A 6-A converter is used for the 1.2-V core rail. A 3-A load switch supports a high current core rail when Instant-On is required. The I/O rail converter's output voltage is adjustable for other memory solutions besides DDR3.

Simple sequencing is integrated into the DC/DC converters. Though no specific sequencing is required for the MAX 10 (except for Instant-On support), sequencing is a good design practice to reduce inrush current drawn from the input source, as well as to provide a controlled system startup. The TIDA-01366 starts VCCIO first, then VCCA, and then the 1.2-V converter (VCC rail). If Instant-On is required, JP2 should be left open and a load switch powers the VCC rail after all other rails are in regulation. When Instant-On is used, the entire startup time is about 8 ms. This time is fully adjustable, faster or slower, on each DC/DC converter.

3 Getting Started Hardware

To test this TI Design, simply apply an input voltage (typically 5 V) to the J1 input connector. Then, connect a jumper between ON and EN on JP1. Install or omit a jumper on JP2, as required for Instant-On support. Sequencing is automatically handled by the onboard DC/DC converters.

4 Testing and Results

This section includes the relevant test results to power the MAX 10 FPGA. Unless otherwise noted, all testing was conducted with 5 V\textsubscript{IN} and at room temperature.
4.1 VCC

Figure 2. VCC Efficiency (5 V_{IN}, JP2 Shorted, Measured at J33)

Figure 3. VCC Load Regulation (5 V_{IN}, JP2 Shorted, Measured at TP35/TP36)

Figure 4. VCC Line Regulation (6-A Load, JP2 Shorted, Measured at J33)

Figure 5. VCC Transient Response (5 V_{IN}, 3- to 6-A Load Step, JP2 Shorted, Measured at J33)

Figure 6. VCC Ripple (5 V_{IN}, 6-A Load, JP2 Shorted, Measured at C45)
4.2 VCCIO

**Figure 7.** VCCIO Efficiency (5 V$_{IN}$)

**Figure 8.** VCCIO Load Regulation (5 V$_{IN}$)

**Figure 9.** VCCIO Line Regulation (2-A Load)

**Figure 10.** VCCIO Transient Response (5 V$_{IN}$, 0- to 2-A Load Step)

**Figure 11.** VCCIO Ripple (5 V$_{IN}$, 2-A Load)
4.3 VCCA

**Figure 12. VCCA Efficiency (5 V\textsubscript{IN})**

**Figure 13. VCCA Load Regulation (5 V\textsubscript{IN})**

**Figure 14. VCCA Line Regulation (2-A Load)**

**Figure 15. VCCA Transient Response (5 V\textsubscript{IN}, 0- to 1-A Load Step)**

**Figure 16. VCCA Ripple (5 V\textsubscript{IN}, 2-A Load)**
4.4 VCCD_PLL

Figure 17. VCCD_PLL Transient Response (5 V_{\text{IN}}, 0- to 1-A Load Step)

4.5 VCCA_ADC

Figure 18. VCCA_ADC Transient Response (5 V_{\text{IN}}, 0- to 1-A Load Step)
4.6 VCCINT

Figure 19. VCCINT Transient Response (5 V<sub>IN</sub>, 0- to 1-A Load Step)

4.7 System Startup

Figure 20. Startup on EN (5 V<sub>IN</sub>, No Load, JP2 Open)
5 Design Files

5.1 Schematics
To download the schematics, see the design files at TIDA-01366.

5.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-01366.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-01366.

5.4 Gerber Files
To download the Gerber files, see the design files at TIDA-01366.

5.5 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-01366.

6 Related Documentation
1. Altera, MAX 10 Power Management User Guide
2. Altera, MAX® 10 FPGA Device Family Pin Connection Guidelines PCG-01018-1.6
3. Texas Instruments, 2-A High Efficiency Step-Down Converter with iDCS-Control, Forced PWM Mode and Selective Switching Frequency, TPS62097 Datasheet (SLVSCD6)
4. Texas Instruments, 2.4-V to 5.5-V, 6-A, 2-Phase Step-Down Converter, TPS62480 Datasheet (SLVSCL9)
5. Texas Instruments, 3.6-V, 3-A, 9-mΩ On-Resistance Load Switch, TPS22925 Datasheet (SLVS840)
6. Texas Instruments, High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions, Technical Brief (SLYT531)

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