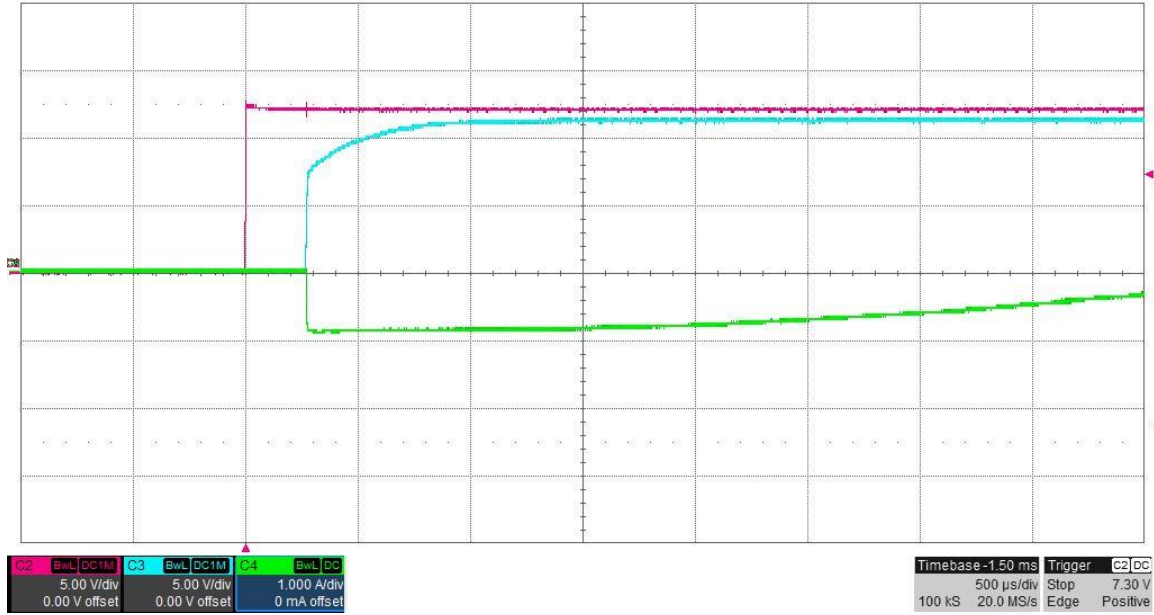


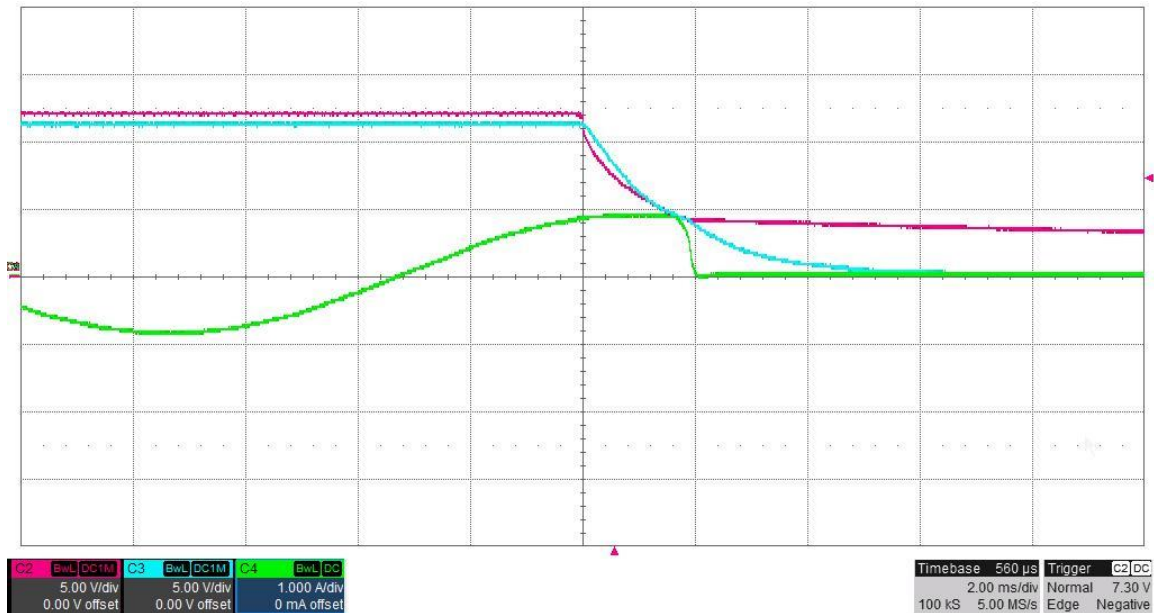
## 1 Turn-on delay

The photo below shows the FET gate-to-source voltage (Blue) and the 24Vac current (Green), after a 12V bias (Red) is applied on the primary. (5V/DIV, 1A/DIV, 500uS/DIV)



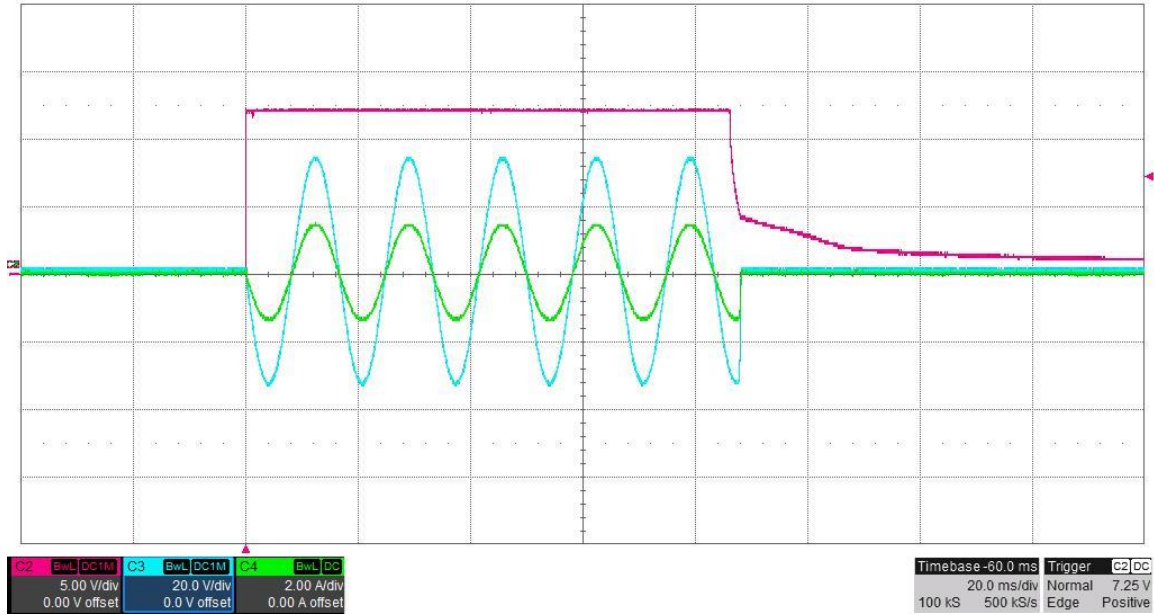
## 2 Turn-off delay

The photo below shows the FET gate-to-source voltage (Blue) and the 24Vac current (Green), after the 12V bias (Red) is removed. (5V/DIV, 1A/DIV, 2mS/DIV)

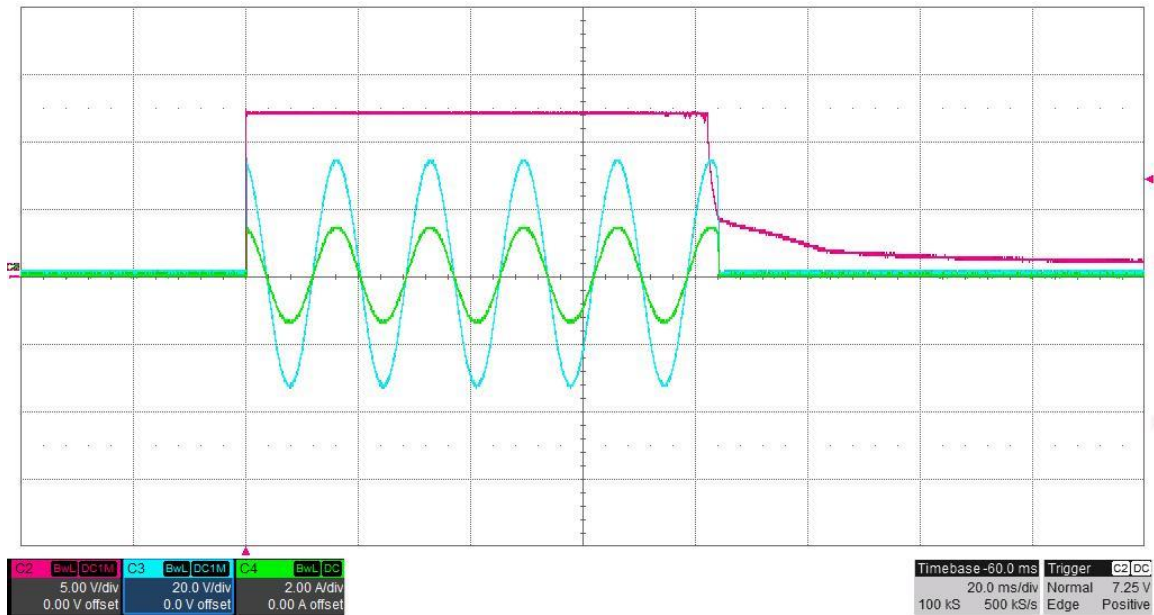


## 3 Switching

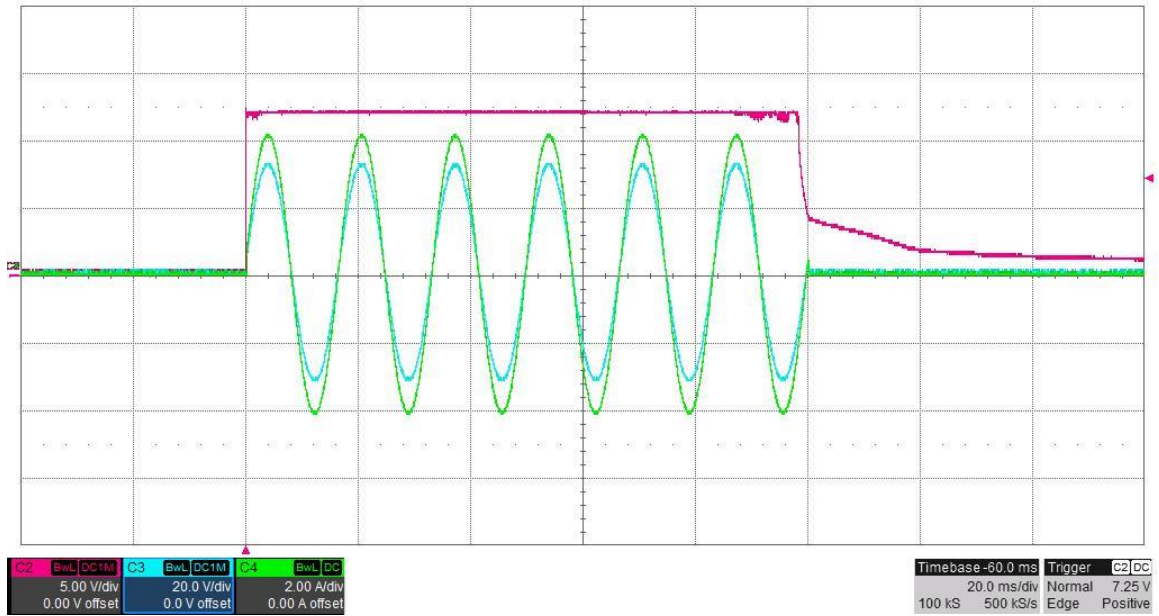
The photo below shows switching of the 24Vac by applying/removing the 12Vdc primary bias (Red) voltage. The load voltage (Blue) was set to 24Vac and the load current (Green) was 1Arms. (12V bias is 5V/DIV, 24Vac voltage is 20V/DIV, 2A/DIV, 20mS/DIV)



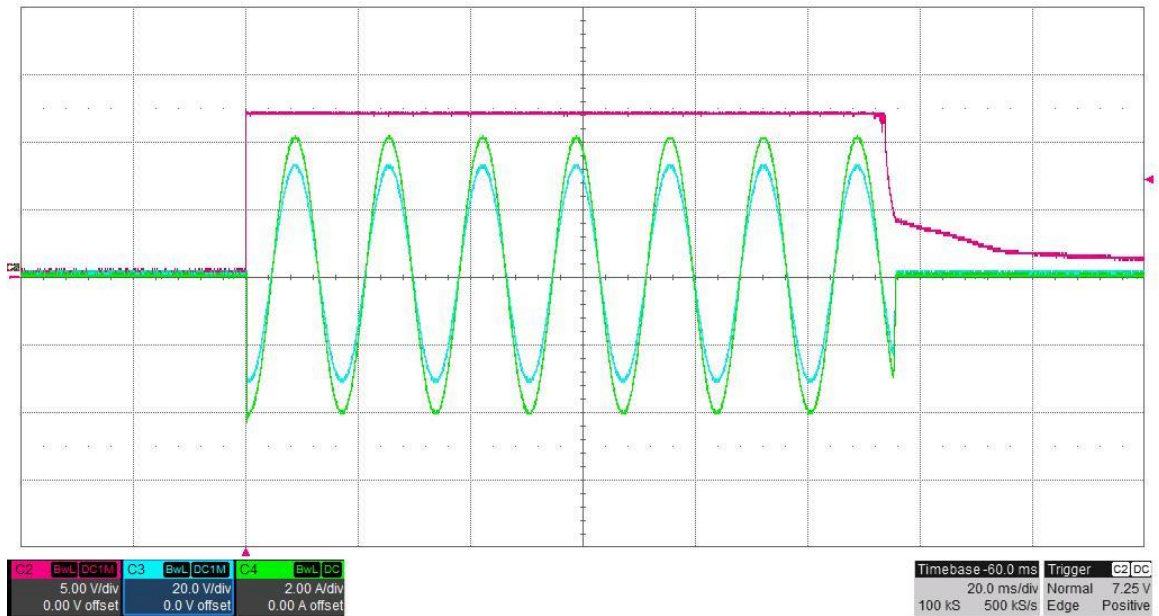
The photo below shows switching of the 24Vac by applying/removing the 12Vdc primary bias (Red) voltage. The load voltage (Blue) was set to 24Vac and the load current (Green) was 1Arms. (12V bias is 5V/DIV, 24Vac voltage is 20V/DIV, 2A/DIV, 20mS/DIV)



The photo below shows switching of the 24Vac by applying/removing the 12Vdc primary bias (Red) voltage. The load voltage (Blue) was set to 24Vac and the load current (Green) was 4.1A<sub>pk</sub> (~3Arms). (12V bias is 5V/DIV, 24Vac voltage is 20V/DIV, 2A/DIV, 20mS/DIV)

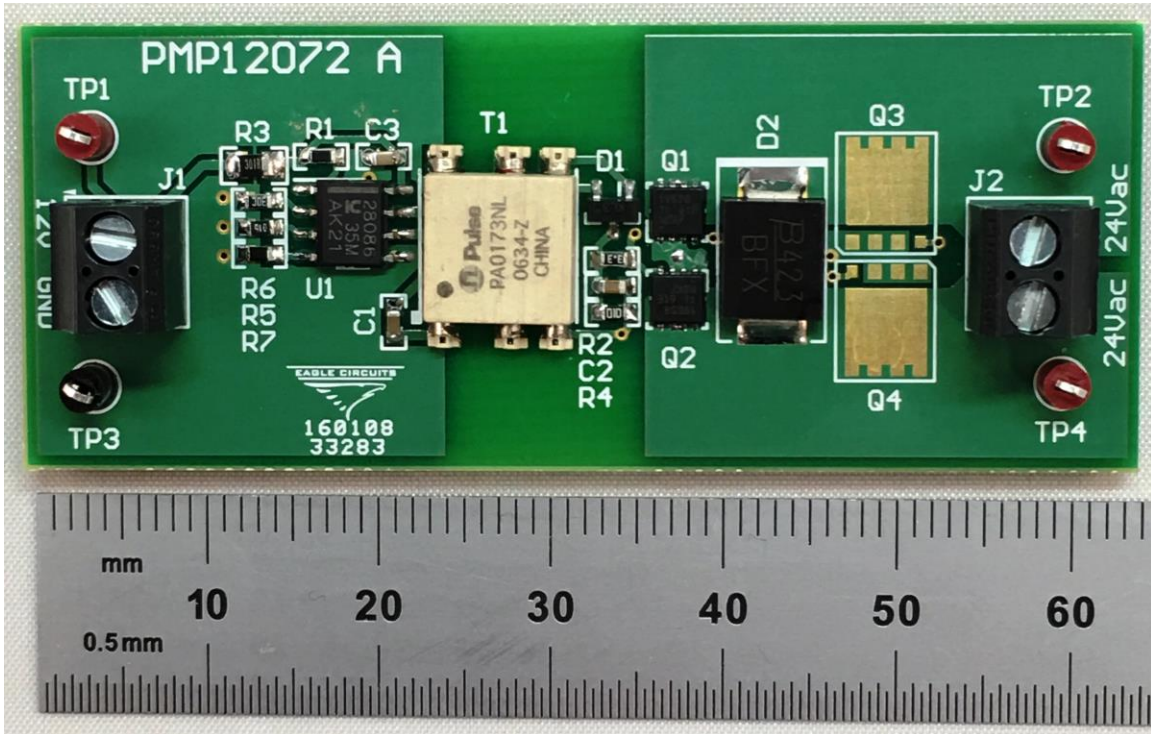


The photo below shows switching of the 24Vac by applying/removing the 12Vdc primary bias (Red) voltage. The load voltage (Blue) was set to 24Vac and the load current (Green) was 4.1A<sub>pk</sub> (~3Arms). (12V bias is 5V/DIV, 24Vac voltage is 20V/DIV, 2A/DIV, 20mS/DIV)



## 4 Photo

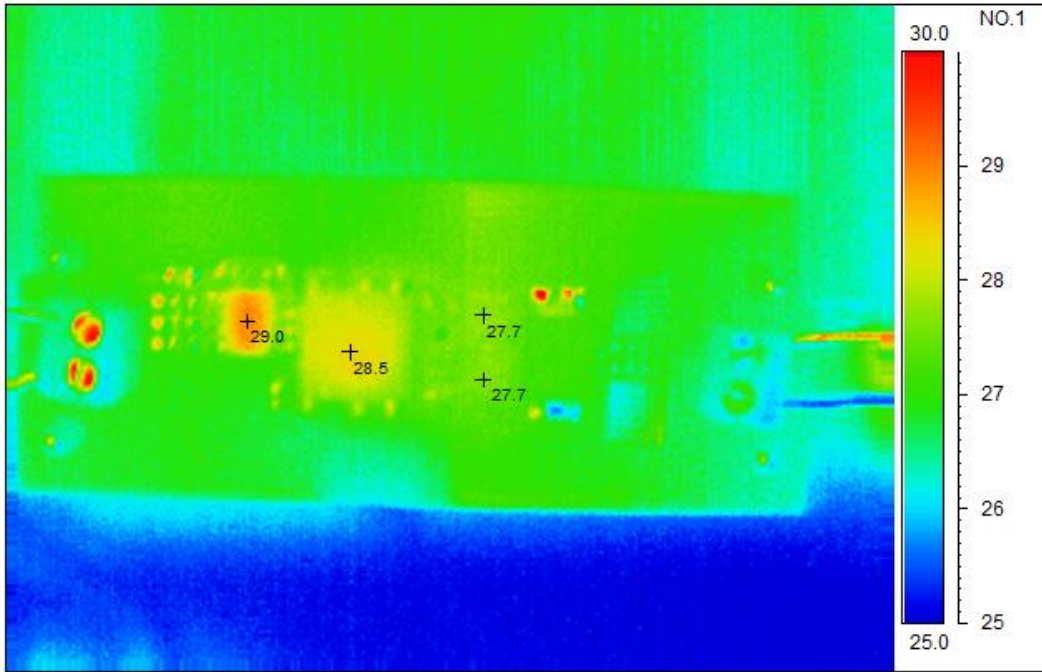
The photo below shows the PMP12072 REVA assembly.



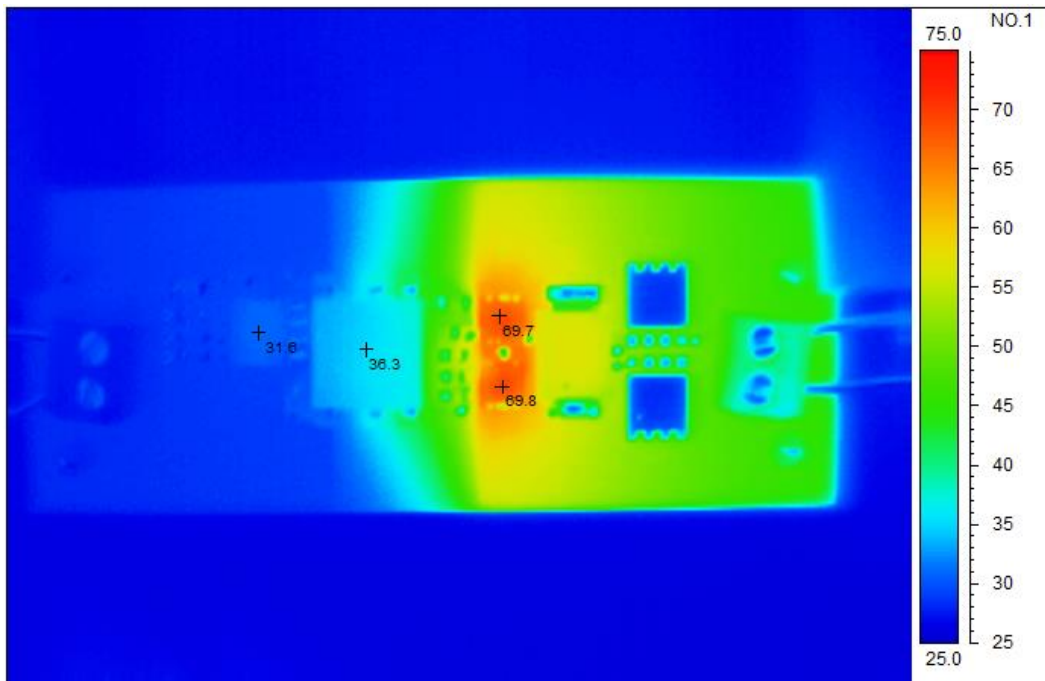


## 5 Thermal Image

A thermal image is shown below while conducting 24Vac @ 1Arms. The primary is powered from a 12V bias. The circuit is at room temp with no airflow.



A thermal image is shown below while conducting 24Vac @ 3Arms. The primary is powered from a 12V bias. The circuit is at room temp with no airflow.



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