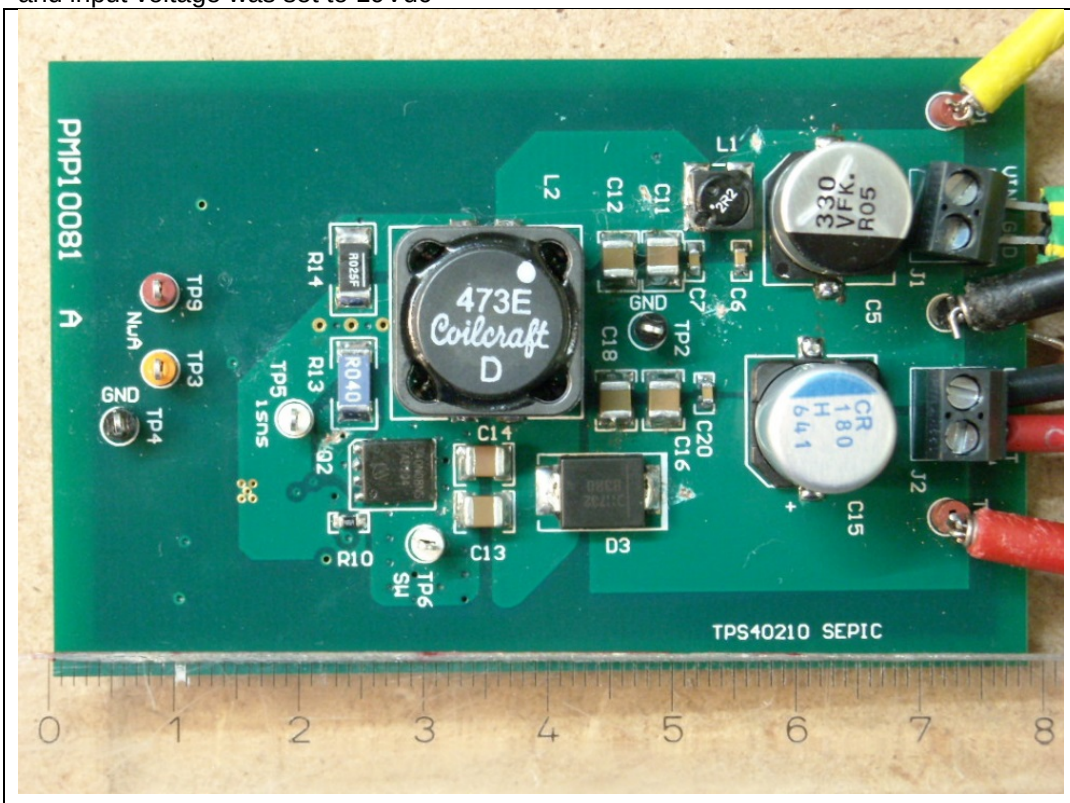
PMP30157RevB Test Results

Topology: SEPIC with added feature for battery charging (TLC272)
Device: TPS40210
The circuit switches on at 14.8V and switches off at 13.28V input voltage.
Unless otherwise indicated, resistive load was applied, load current was adjusted to 0.45A and input voltage was set to 19Vdc



1 Startup

The startup waveform is shown in the Figure 1.

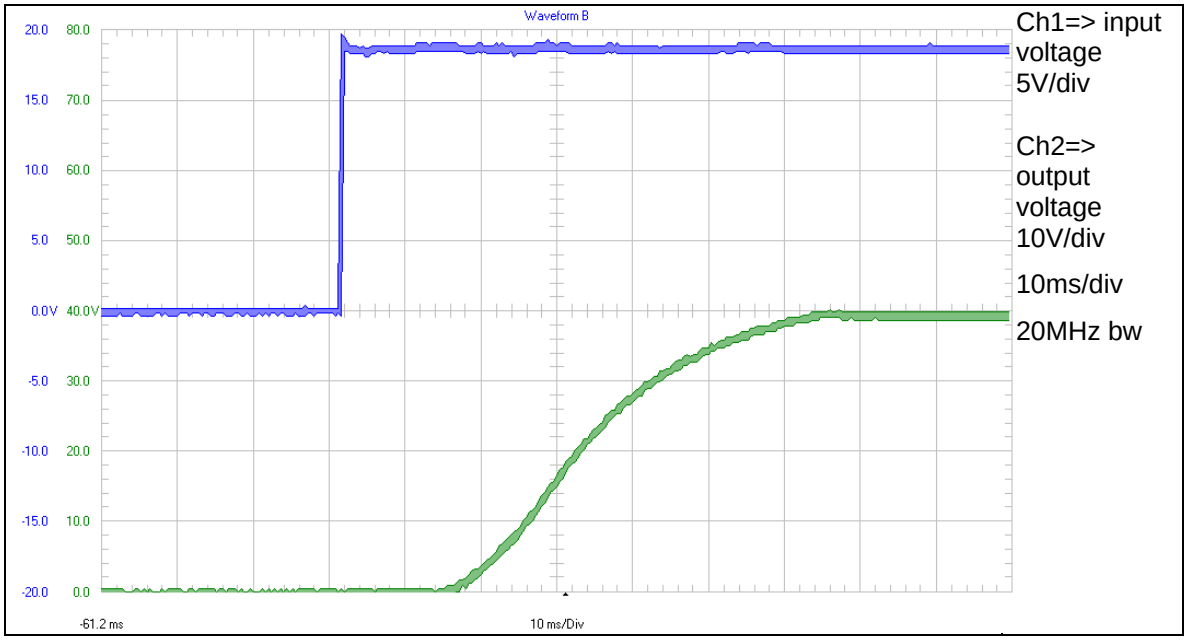


Figure 1

2 Shutdown

The shutdown waveform is shown in the Figure 2. The power supply was disconnected**.**

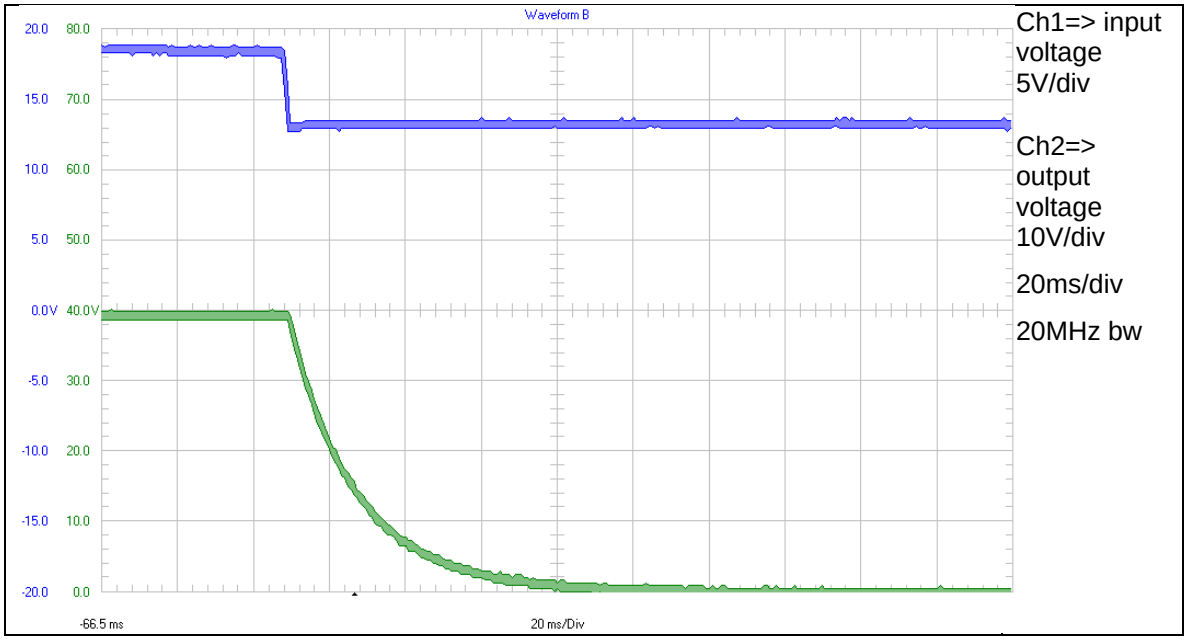


Figure 2

3 Efficiency

The efficiency is shown in the Figure 3 below, current limit set around 480mA.

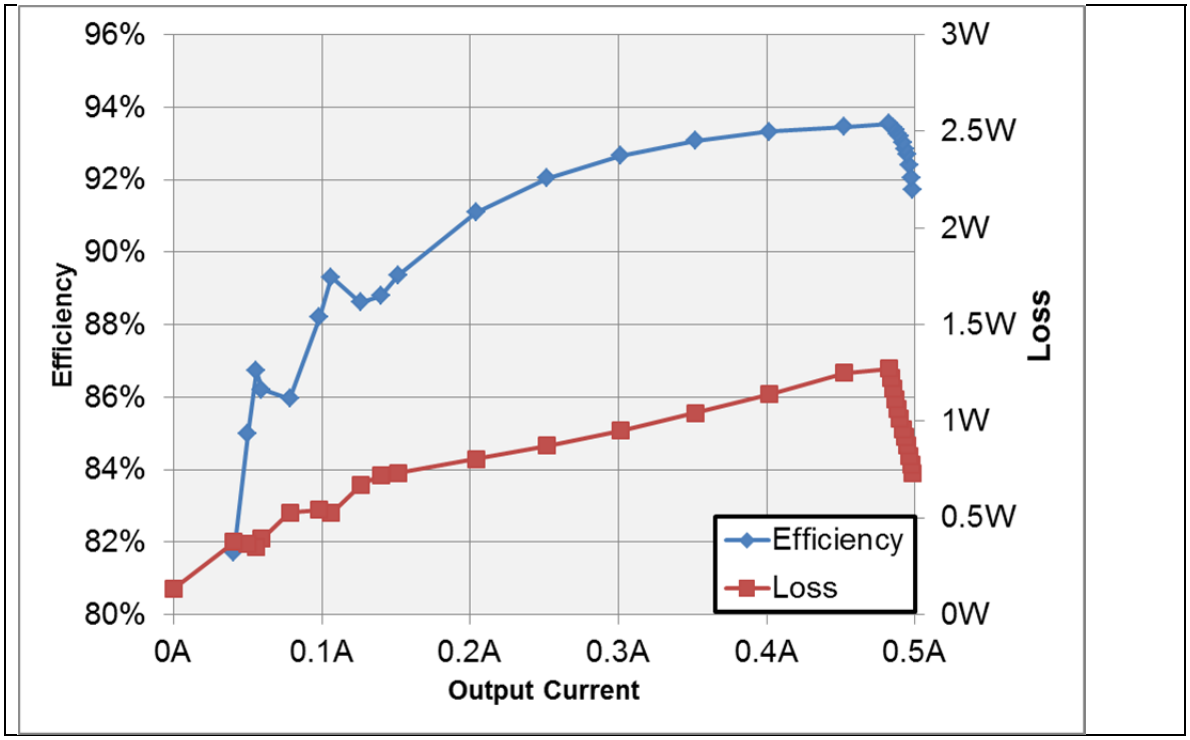


Figure 3

Another view of the efficiency and loss is shown in Figure 4

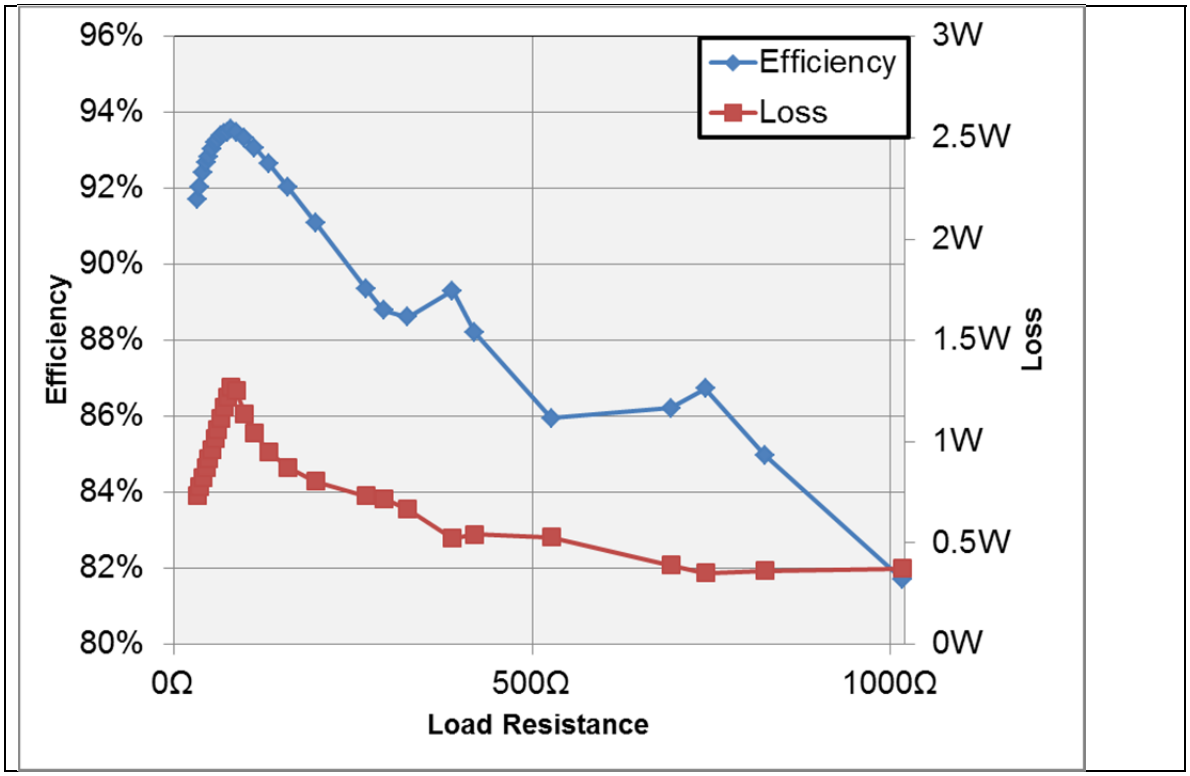


Figure 4

4 Load Regulation

The load regulation of the output is shown in the Figure 5 below, CV loader behavior.

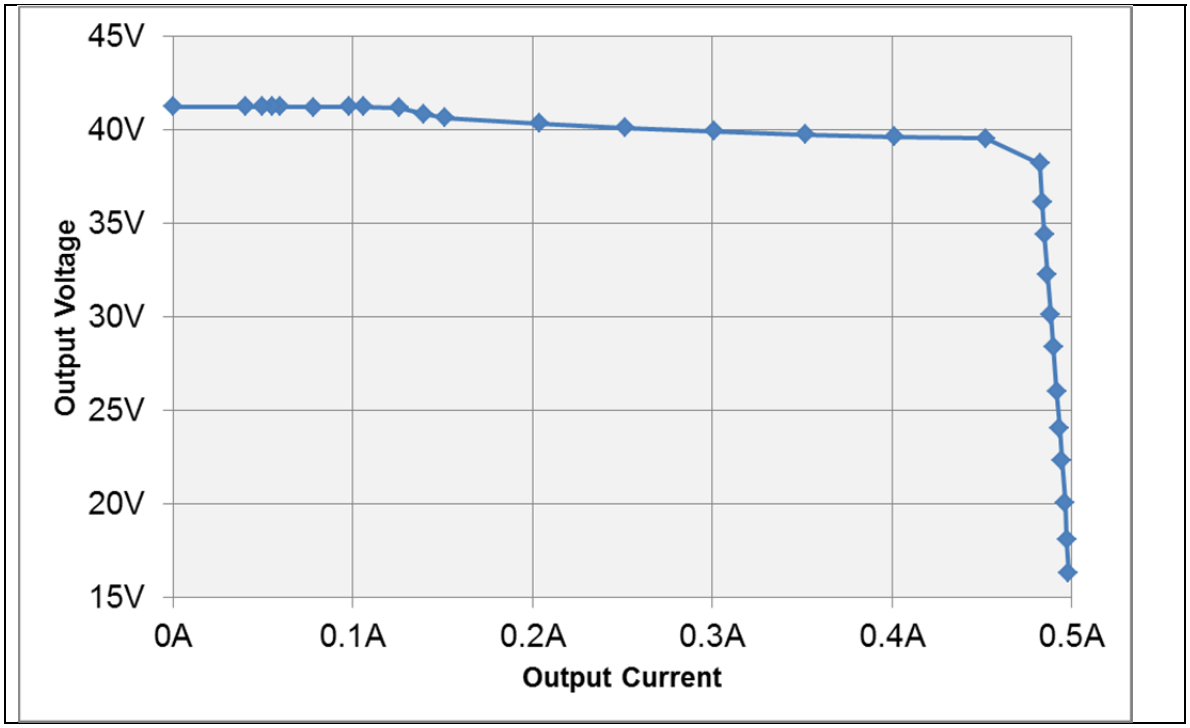


Figure 5

Another view for the load regulation is shown in Figure 6, CV loader behavior.

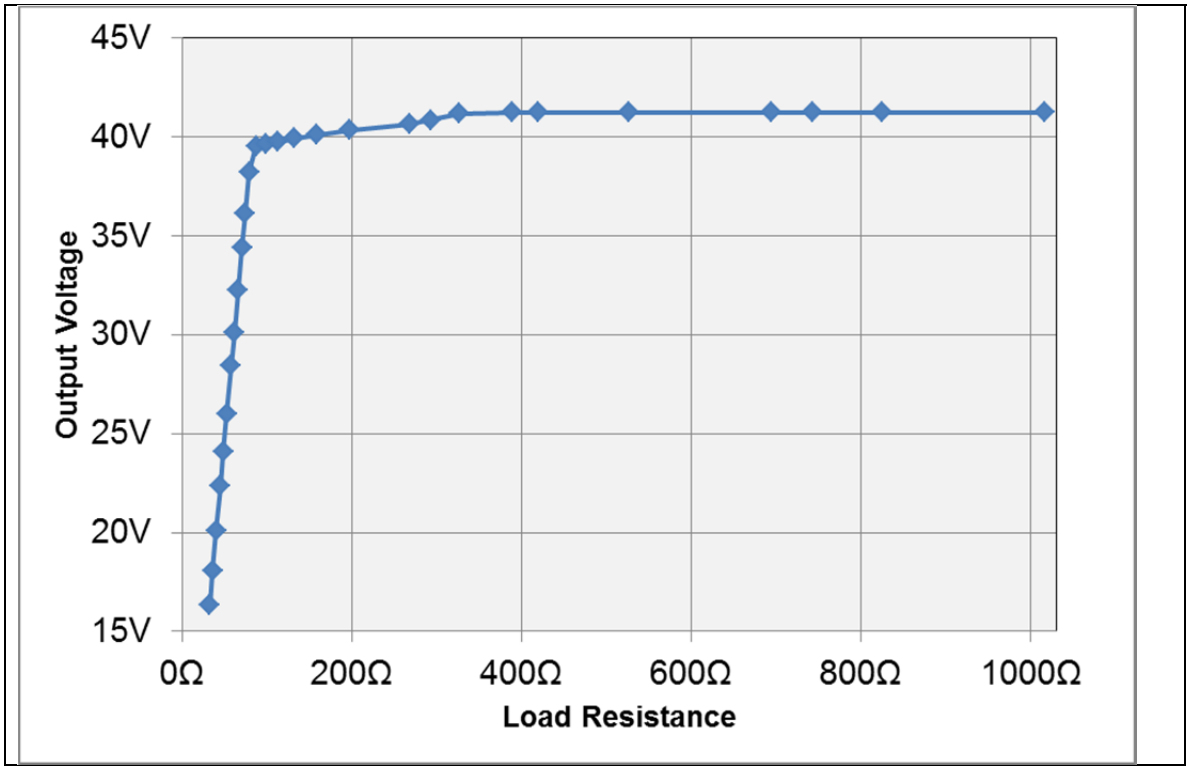


Figure 6

5 Output Ripple Voltage

The output ripple voltage is shown in Figure 7.

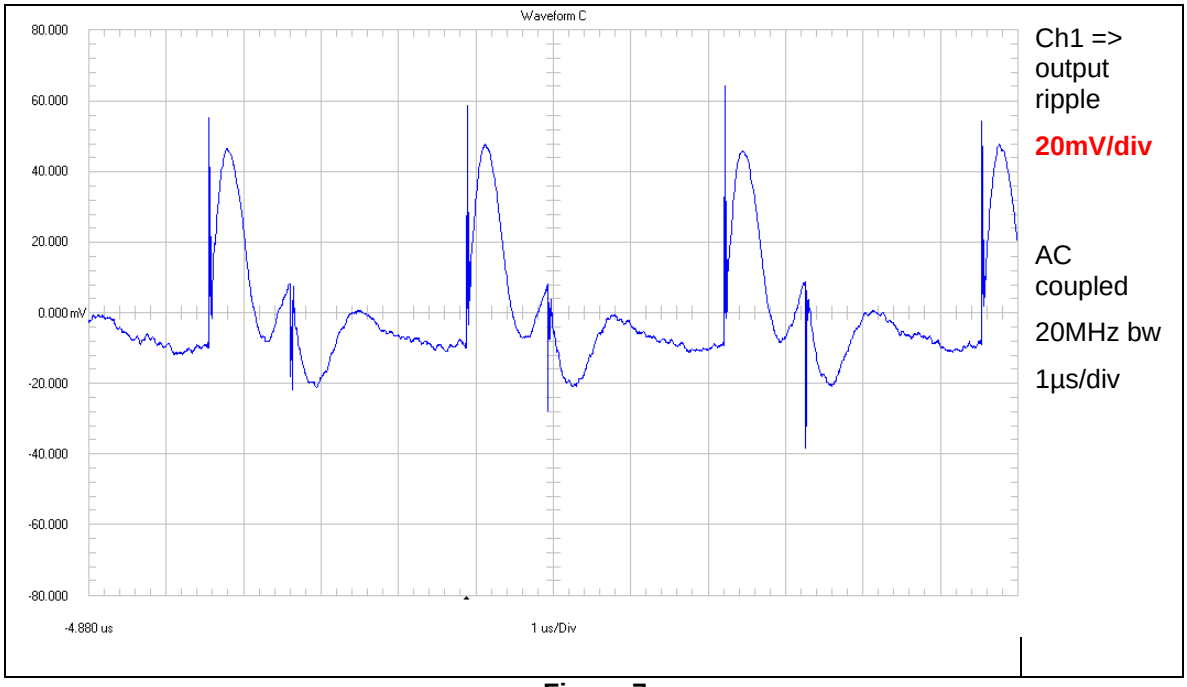


Figure 7

6 Input Ripple Voltage

The input ripple voltage is shown in Figure 8. The measurement was done one the bottom side of the board at 450mA load – input filter prevents from reflected ripple = conducted emissions.

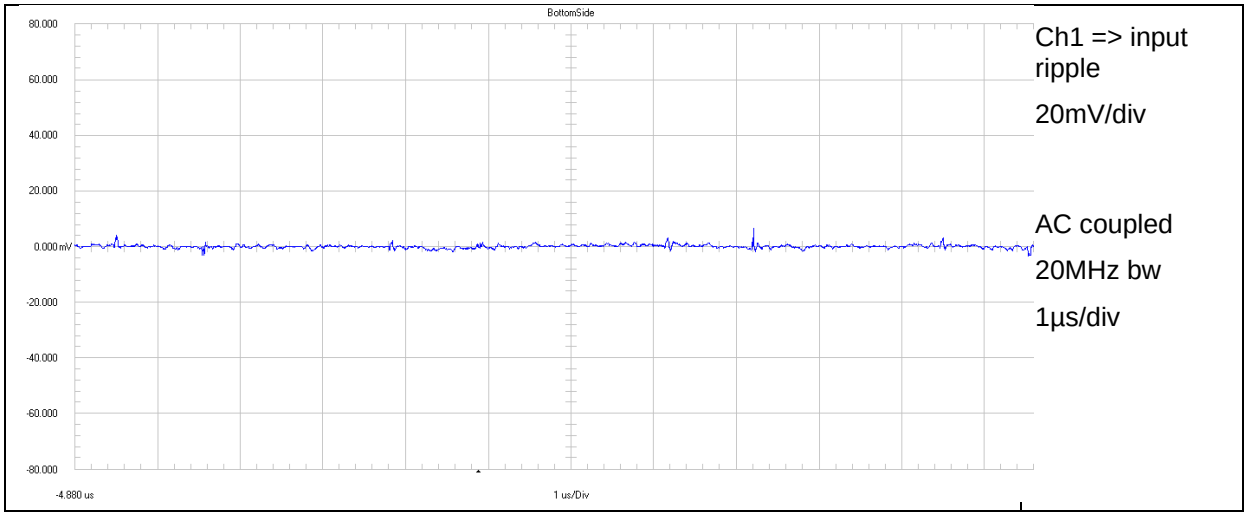
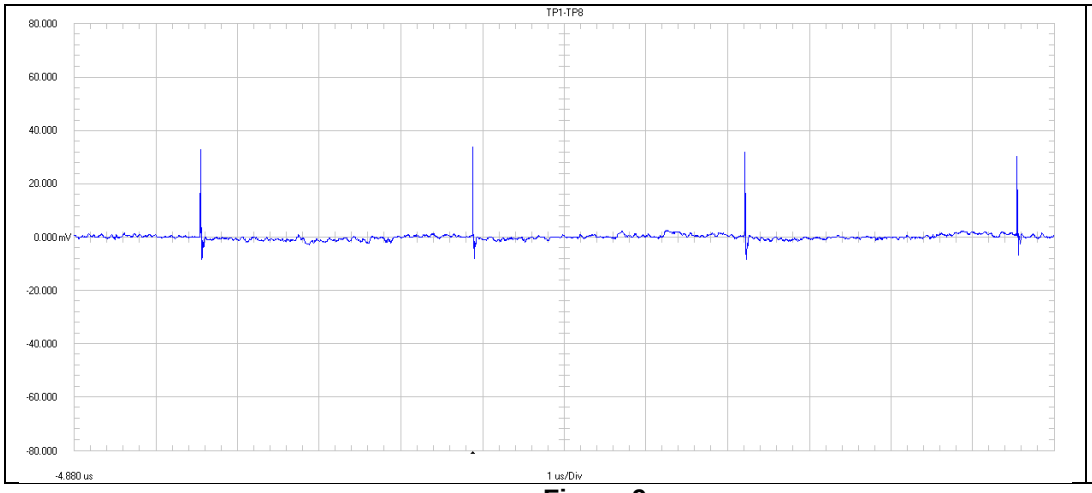


Figure 8

In Figure 9 the measurement was done directly on the testpoints TP1 and TP8



Ch1 => input ripple

20mV/div

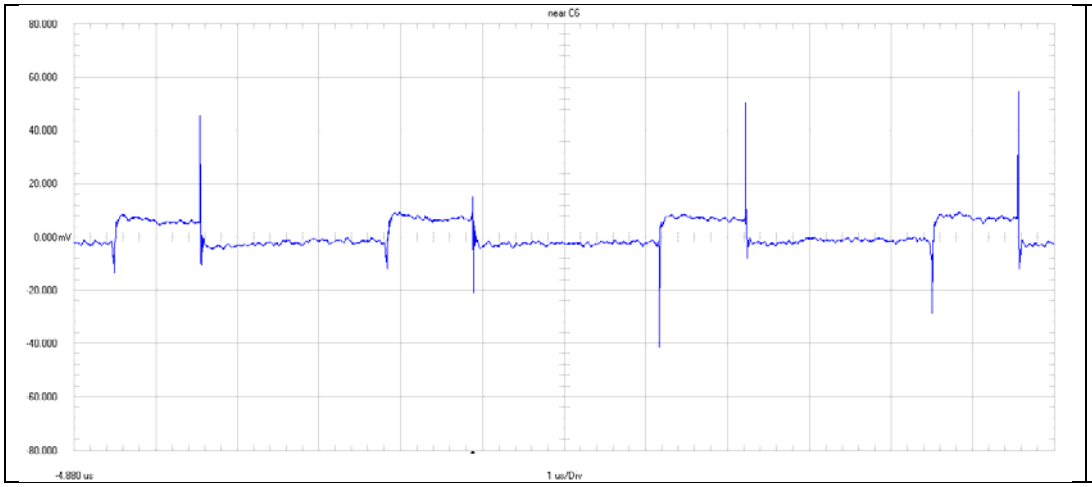
AC coupled

20MHz bw

1µs/div

Figure 9

In Figure 10 the measurement was done near C6



Ch1 => input ripple

20mV/div

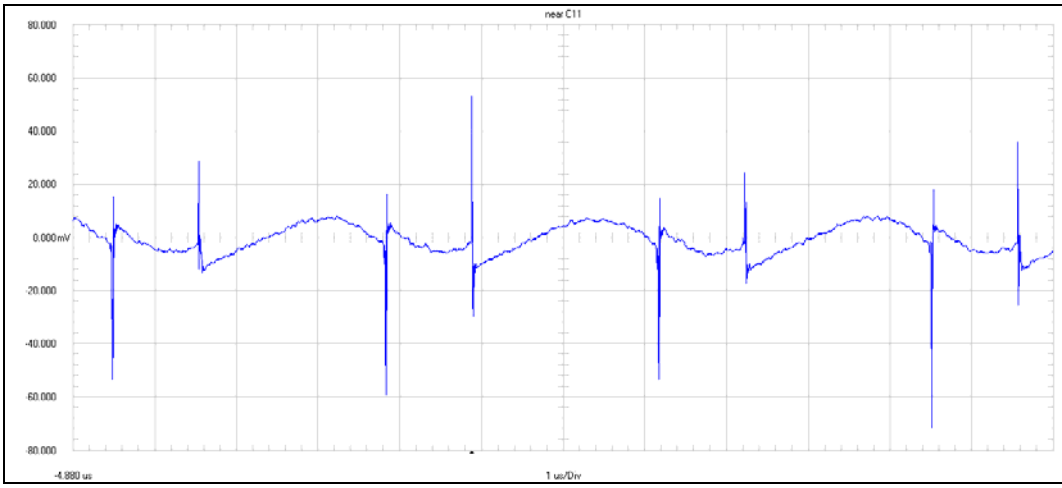
AC coupled

20MHz bw

1µs/div

Figure 10

In Figure 11 the measurement was done near C11 ("powerstage VIN")



Ch1 => input ripple

20mV/div

AC coupled

20MHz bw

1µs/div

Figure 11

8 Control Loop Frequency Response

Figure 12 shows the loop response. Diode D5 was removed, so only voltage loop was measured. Output current was set to 500mA – voltage loop needs to be slower than current loop.

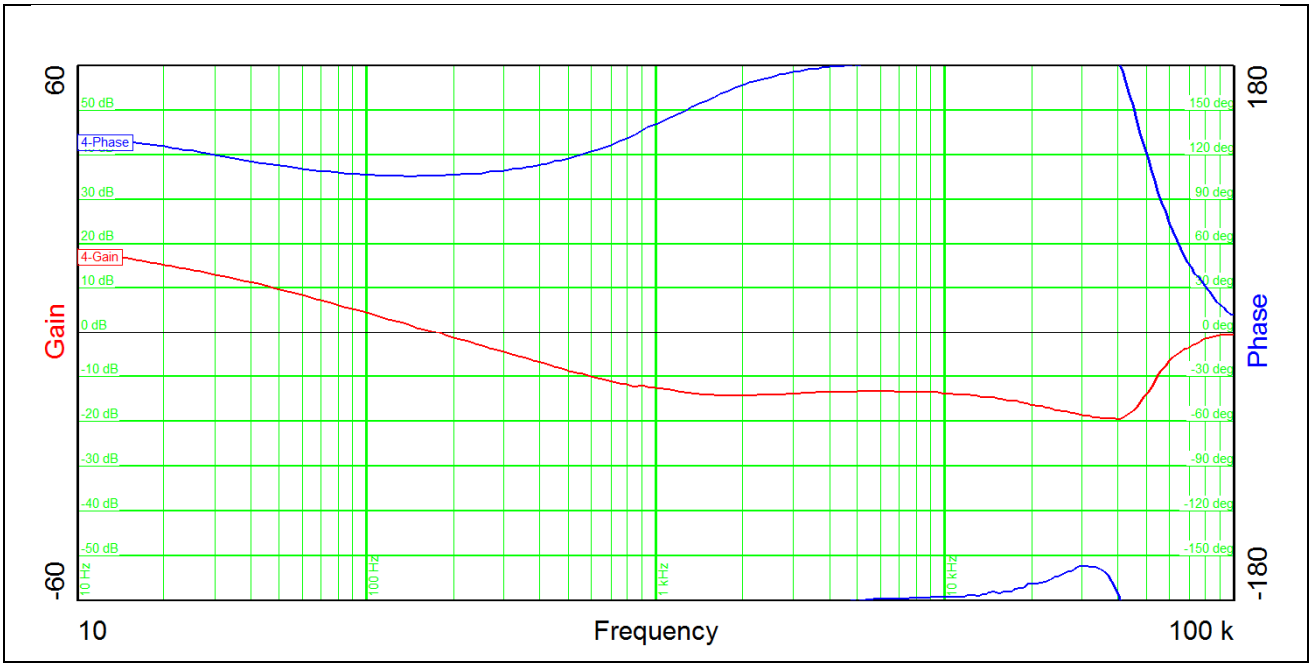


Figure 12

Vin	19
Bandwidth (kHz)	173
Phase margin	105.6°
slope (20dB/decade)	0.95

Table 1

9 Miscellaneous Waveforms

9.1 Switchnode (drain-source)

The waveform of the voltage on switchnode (drain to source) is shown in Figure 13.

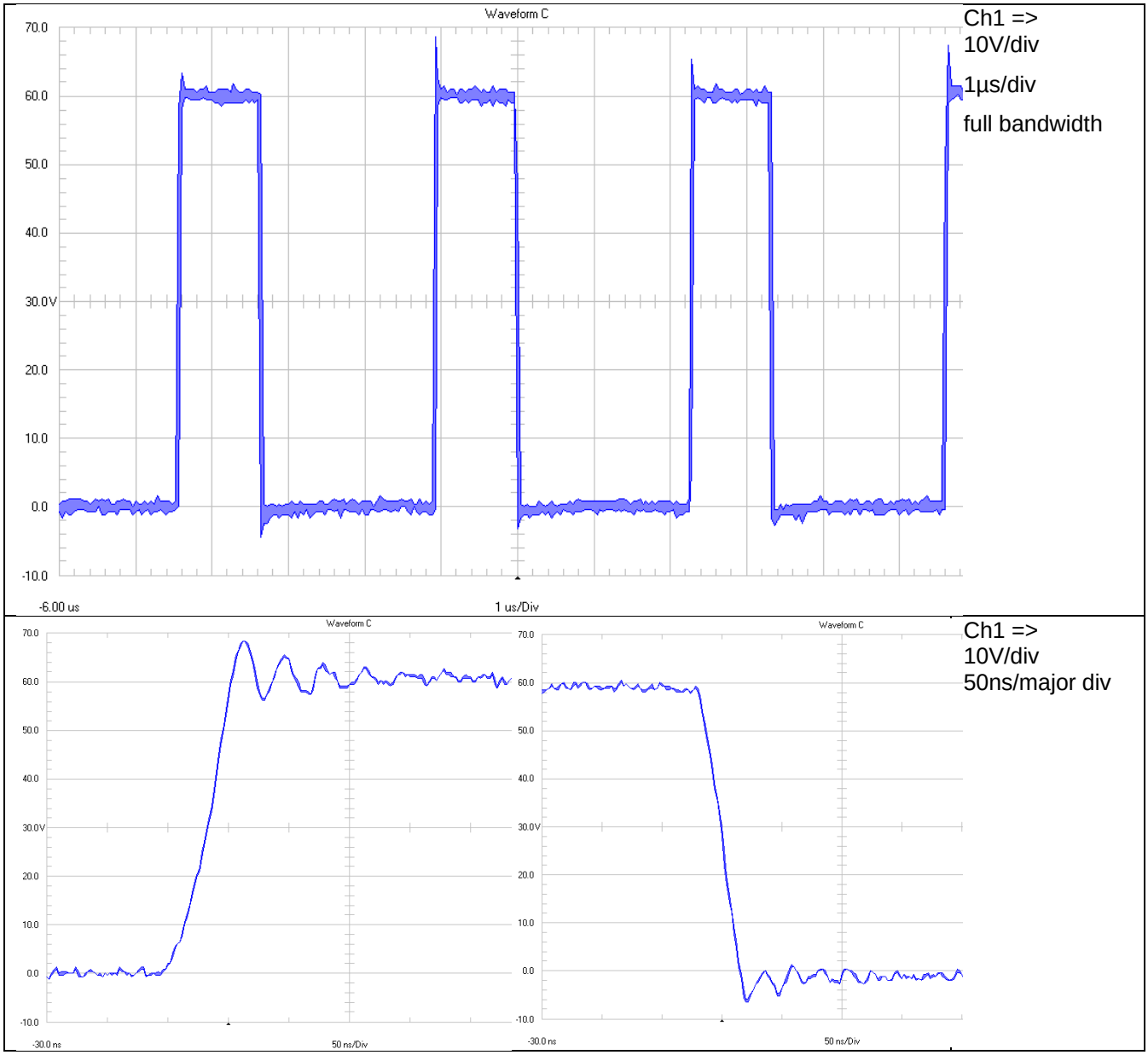


Figure 13

9.2 Gate to Source

The waveform of the voltage on the gate to source is shown in Figure 14

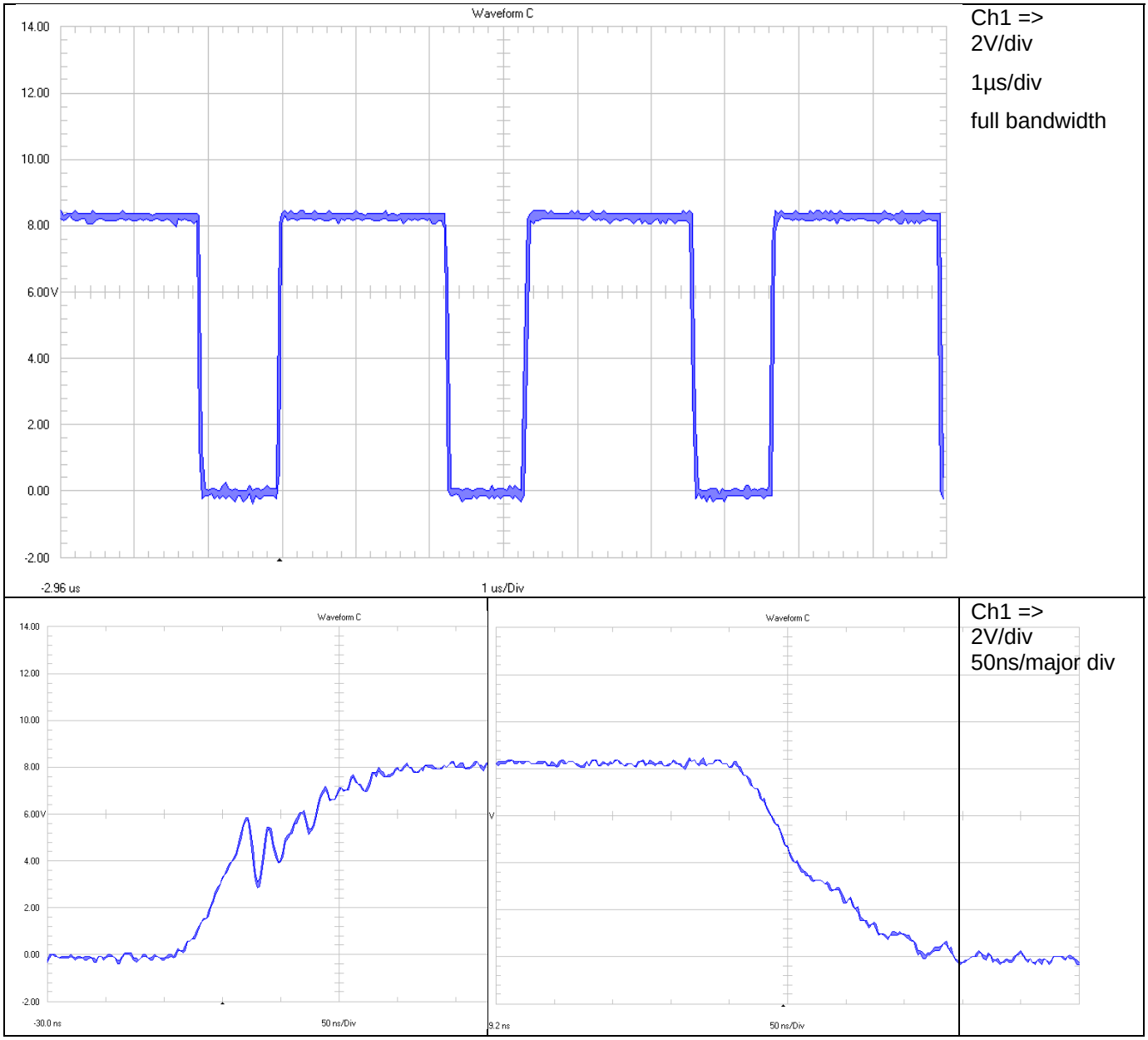


Figure 14

9.3 Voltage D3 (referenced to VOUT)

The waveform of the voltage is shown in Figure 15.

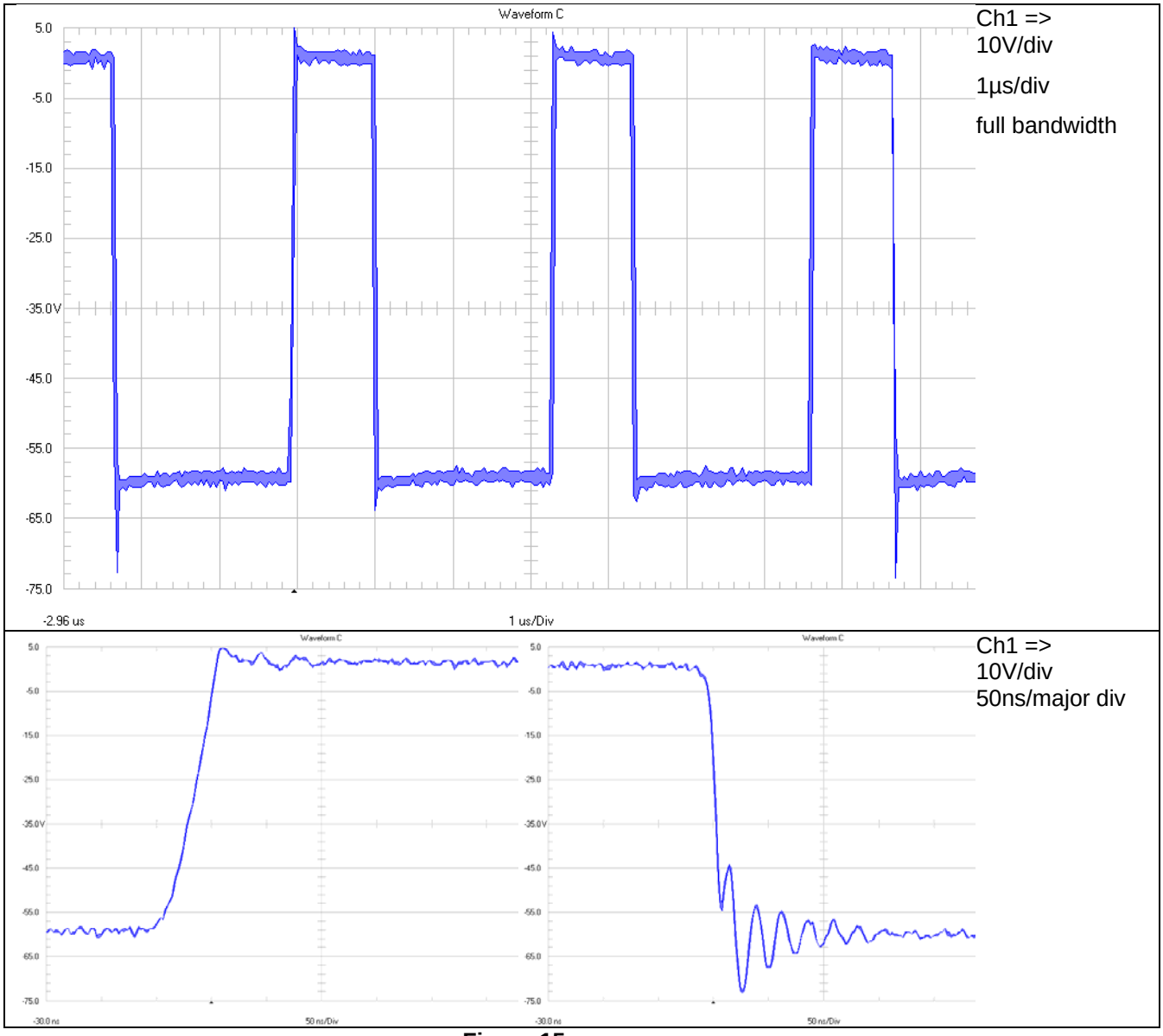


Figure 15

10 Thermal Image

Figure 16 shows the thermal image.

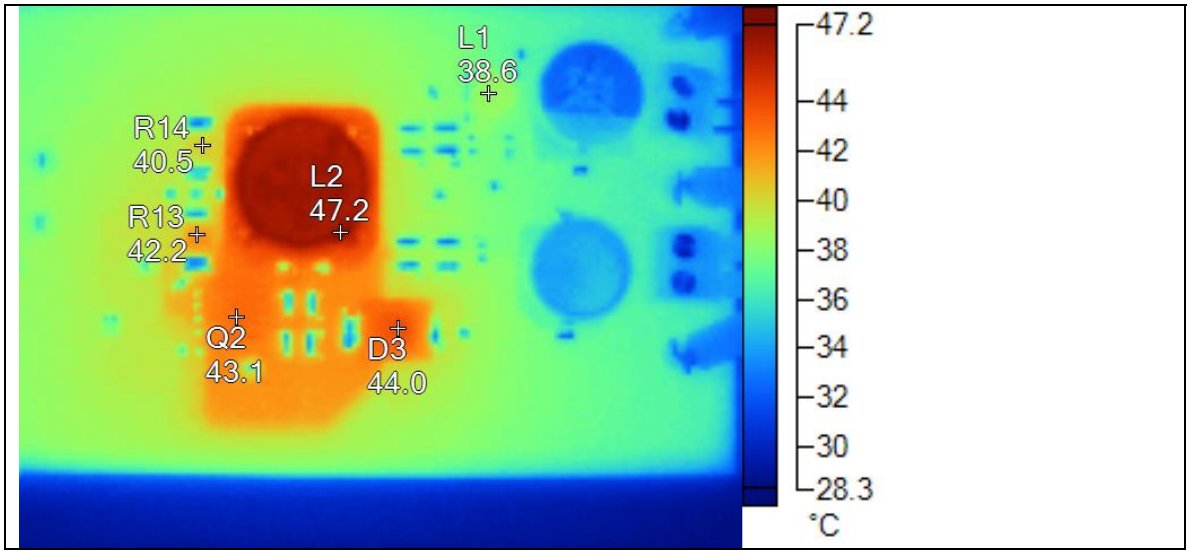


Figure 16

Name	Temperature
L2	47.2°C
D3	44.0°C
Q2	43.1°C
R13	42.2°C
R14	40.5°C
L1	38.6°C

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