TI Designs: TIDA-01411
Type-2 PoE PSE, 6-kV Lightning Surge Reference Design

Description

This reference design provides a solution for lightning surge protection for Power over Ethernet (PoE) power-sourcing equipment (PSE) systems based on TI PSE controller TPS23861. The use cases for implementing such protection typically depends on the environment in which the PSE is intended to operate and the inherent isolation properties of the PSE. Lighting surge protection is an important design consideration for a system and useful in industrial applications such as network video recorders (NVRs), digital video recorders (DVRs), and in telecom applications such as Ethernet switches, gateways, and so forth.

Resources

TIDA-01411	Design Folder
TPS23861	Product Folder
LM5019	Product Folder
ISO7221	Product Folder
ISO1541	Product Folder

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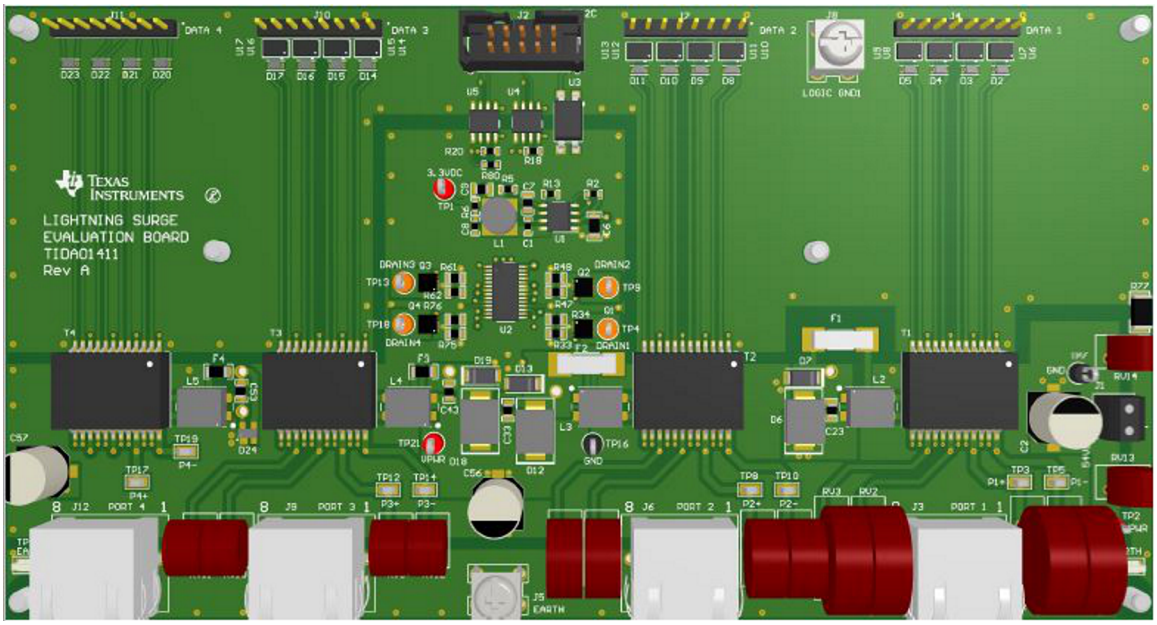
Features

- Passes UNH-IOL PoE Conformance and Interoperability and SIFOs Type-1 and Type-2 Test Suites
- Full Autonomous Mode Eliminates Requirement for Digital Interface
- Auto Detection and Classification; Auto Turnon and Disconnect of PD
- Passes 6-kV Common Mode and 4-kV Deferential Mode Lightning Surge Tests
- Four Levels of Lightning Surge Level Design

Applications

- Surveillance NVR and DVRs
- Small Home and Office Routers
- Ethernet Switches
- PoE Pass-Through Systems
- Residential Gateways
- Small Cells (Pico, Micro, Femto Base Stations)



1 System Description

As integrated circuits (ICs) continue to scale, they become more susceptible to damage from voltage transients. One of the most dangerous types of voltage transients is lightning surge, which can cause arcing or component degradation and lead to device failure. Designing effective protection circuitry is difficult due to the variability of both the magnitude and path of the surges. This reference design shows practical methods for designing protection circuitry for various lightning surge situations.

This reference design showcases robust lightning surge protection for POE PSE systems based on the TI TPS23861 PSE controller. This protection is realized through a variety of methods including: transient voltage suppressors (TVS), Bob Smith terminations, varistors, and grounding. Proper selection and implementation of these components aids in both the suppression and diversion of lightning surges to prevent component failure. A series of surge tests were performed to measure the success of the design. The stated goal during testing was to retain proper device functionality after applying up to 6 kV of common and differential voltage surges to the device.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
DC power supply	54 V
PD classification	Class 4
Surge waveform for common mode	±1 kV, 2 kV, 4 kV, and 6 kV; 1.2/50 µs, 10/700 µs
Surge waveform for differential mode	±1 kV, 2 kV, 4 kV; 1.2/50 µs

2 System Overview

2.1 Block Diagram

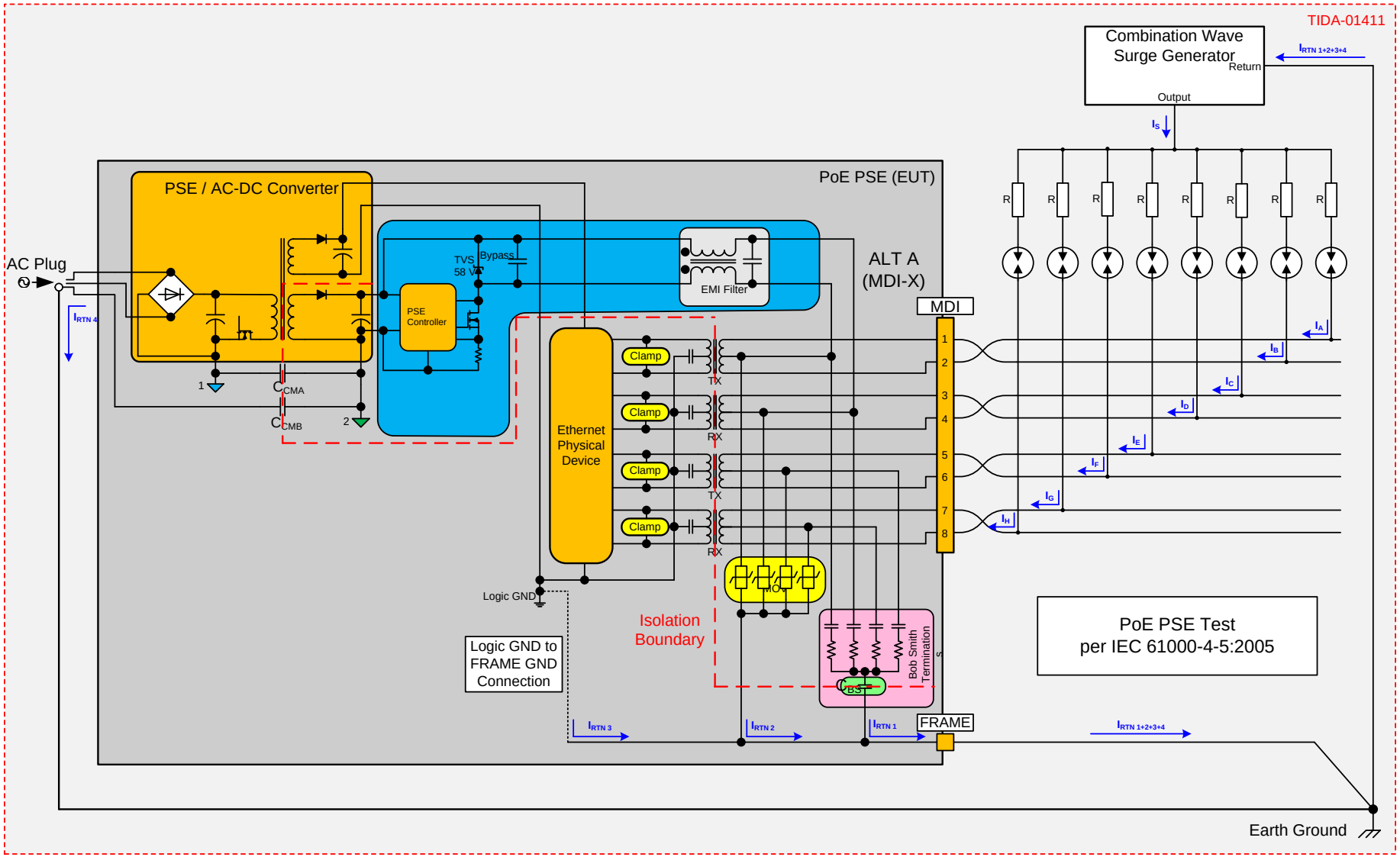


Figure 1. Examples of Surge Current Paths Through Earthed PSE Application

Most (if not all) PSE applications include a dedicated connection to earth ground, as the previous Figure 1 shows. Along with acting as a safety ground, this earth-ground connection can serve as a reference ground for internal PSE circuitry, such as Bob Smith cable terminations and the primary-side of an isolated AC/DC converter. These internal earth-ground connections can create paths for common-mode surge currents to flow from the generator, through the PSE, and back to the return of the generator (see Figure 1).

Referring to Figure 1, the surge current from the generator, I_S, divides into the eight-wire input of the PSE, as current paths I_A through I_H indicate. After entering the PSE, the surge current seeks any paths to earth ground to return to the generator. Two possible return paths are $I_{RTN\ 1}$, through the Bob Smith termination circuit block, $I_{RTN\ 4}$, and through the isolated AC/DC converter circuit block. The main conduits for these return paths are the highlighted C_{BS} capacitor in the Bob Smith termination block and the typically-used C_{CMB} common-mode noise capacitor in the AC/DC converter block, each of which crosses the isolation boundary. These two return paths plus $I_{RTN\ 2}$ and $I_{RTN\ 3}$ combine as $I_{RTN\ 1+2+3+4}$, which then returns back to the generator.

The currents indicate a positive surge from the surge generator, despite the fact that the PSE will be subjected to five positive and five negative surges, according to the IEC 61000-4-5 test procedure. Note that the surge current paths within each circuit block can vary depending on the surge polarity. For example, during a positive surge, some surge current flows through the port TVS to the positive rail of the 48-V power supply; conversely, during a negative surge, some surge current flows through the body diode of the port MOSFET.

The PSE controller block includes an electromagnetic interference (EMI) filter, which is normally required to meet conducted emissions requirements. This filter typically employs ferrite beads or a common-mode choke, which can help to reduce the amount of surge current that flows back to the converter. The shown PSE controller block also includes a 58-V TVS, which is typically placed across the port to protect against hot-plug transients and electrostatic discharge (ESD) events. This TVS device also contributes to the protection of the PSE controller during a lightning surge.

Although this reference design primarily focuses on lightning surge protection for the front end and power sections of the PSE, note that surge protection devices (SPD) may be required on the secondary-side data lines, as shown by the clamp blocks highlighted in Figure 1. Several manufacturers, such as Bourns® and Littelfuse®, offer devices to protect the data lines. To maintain signal integrity, the type of device selected normally depends on the capacitance associated with the device and the data rate of the PoE system. Consult the data sheet of the manufacturer for proper selection of these devices.

The requirements for SPDs in a PSE application normally depends on the required surge test level and the inherent isolation properties of the PSE. The IEEE 802.3 standard specifies that the PSE must provide electrical isolation that withstands an electrical strength test of 1500 V_{RMS}, 2250-V DC, or the 1500 V_{PK} 10/700-µs impulse test defined in the IEC 60950-1 standard. If the surge test level is below the inherent withstand strength of the PSE, then additional SPDs may not be required. Alternatively, if the PSE is to encounter surge test levels that exceed the withstand strength of the PSE, then the design will most likely require additional SPDs at the front end of the PSE to either clamp the surge voltage below the withstand rating of the PSE or crowbar the surge to earth ground.

2.2 Highlighted Products

2.2.1 TPS23861

The TPS23861 is an easy-to-use, flexible, IEEE802.3at PSE solution. As shipped, the device automatically manages four 802.3at ports without the requirement of any external control.

The TPS23861 automatically detects powered devices (PDs) that have a valid signature, determines power requirements according to classification, and applies power. Two-event classification is supported for type-2 PDs. The TPS23861 supports DC disconnection and the external field-effect-transistor (FET) architecture allows designers to balance size, efficiency, and solution cost requirements.

The unique pin-out enables two-layer printed-circuit board (PCB) designs through logical grouping and clear upper- and lower-differentiation of I^2C and power pins. This configuration delivers best-in-class thermal performance, Kelvin accuracy, and low-build cost.

In addition to automatic operation, the TPS23861 supports semi-auto mode through I^2C control for precision monitoring and intelligent power management.

Compliance with the 400-ms TPON specification is ensured whether in semi-automatic or automatic mode.

The key features are as follows:

- IEEE 802.3at quad-port PSE controller
- Auto detect, classification
- Automatic mode available as shipped
- Optional I^2C control and monitoring
- TSSOP 28 package 9.8 mm × 6.6 mm

2.2.2 ISO7221BD

The ISO7221B is a dual-channel digital isolator. This device has a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V_{PK} per V_{DE}. When used with isolated power supplies, this device blocks high voltage, isolates grounds, and prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

2.2.3 ISO1541D

The ISO1541 device is a low-power, bidirectional isolator which is compatible with I^2C interfaces. This device has logic input and output buffers which are separated by Texas Instrument's Capacitive Isolation technology using an SiO2 barrier. When used with isolated power supplies, this device blocks high voltages, isolates grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology offers function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1541 device enables the designer to implement a complete, isolated I^2C interface within a small form factor.

2.2.4 LM5019

The LM5019 is a 100-V, 100-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant-on-time (COT) control scheme employed in the LM5019 requires no loop compensation, provides excellent transient response, and enables very-low step-down ratios. A high-voltage start-up regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows users to independently program the input undervoltage threshold and hysteresis. Other protection features include thermal shutdown and bias supply undervoltage lockout.

2.3 Design Considerations

2.3.1 Overall Guidelines

Many guidelines apply to voltage transient protection for electronic systems. The following is a list of some practical rules along with circuits design strategies:

- The source of transient voltage can be differential-, common-mode type, or both.
- The main categories of protection techniques against transient voltages are shielding and grounding, filtering, isolation, and nonlinear devices.
- A well-designed circuit protection interface is usually the result of a good combination of blocking and diverting techniques.
- The selected voltage suppressor must have the speed and robustness (short-circuit current and waveform) required for the application. Shunt (line-to-earth GND) capacitors that may take direct transient hits must be rated for high voltage (≥ 2 kV). These capacitors must also have the following characteristics: low equivalent series resistance (ESR) at high frequency and low parasitic inductance.
- The protection circuit must not interfere with the normal behavior of the circuitry under protection.

- The protection circuit must be able to prevent any voltage transient from causing erratic behavior (repetitive or not) throughout the complete system—electrical fast transient (EFT) is one example. Use common-mode chokes when necessary.

2.3.2 Basic Circuit Layout Rules

The basic rules of the circuit layout design are:

- Define a low-impedance path that diverts any transient current or voltage away from sensitive components. Do not allow ESD to find a way to earth GND by itself.
- Have a good, solid, and low-impedance earth ground connection onboard.
- Keep the transient current density and the current path impedances as low as possible by using multipoint grounds where the current is designed to flow, and single-point grounds where it is not.
- The loop within which the fast-rising currents must circulate should be a small area. For fast transients, use local ceramic capacitors whenever necessary, particularly when using clamping diodes on a power-supply rail.
- Create physical separation between high-voltage/current transients area, in close proximity to I/O connectors, and the sensitive circuitry. The high-current suppressors must be located in that I/O area, as well as the switches, LEDs, and displays
- Put all the connectors on one edge of the circuit, if possible. Place sensitive circuitry at the center of the PCB, if possible.
- Route each protected signal from the suppressor to the sensitive circuitry in parallel with its individual return signal to prevent any inadvertent transformer effect.
- Use a surface-mount package for suppressors. Use a four-terminal connection type to mitigate the parasitic inductance effect (see Figure 2 and Figure 3).
- Mitigate parasitic capacitances that are bypassing blocking series elements. However, having parasitic inductance in series with blocking elements is not a problem.

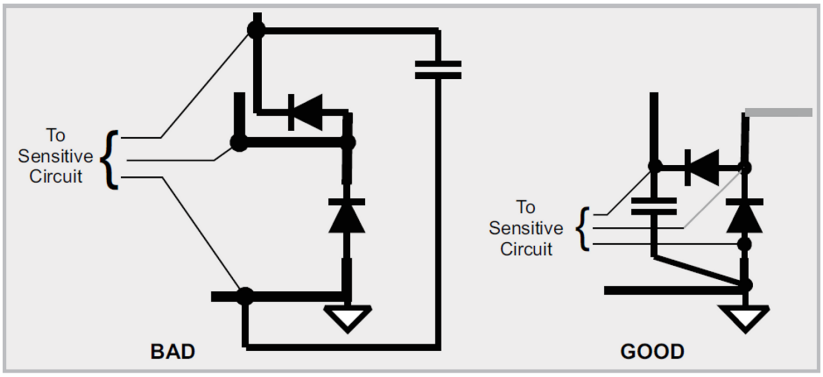


Figure 2. Interconnection to Clamping Devices

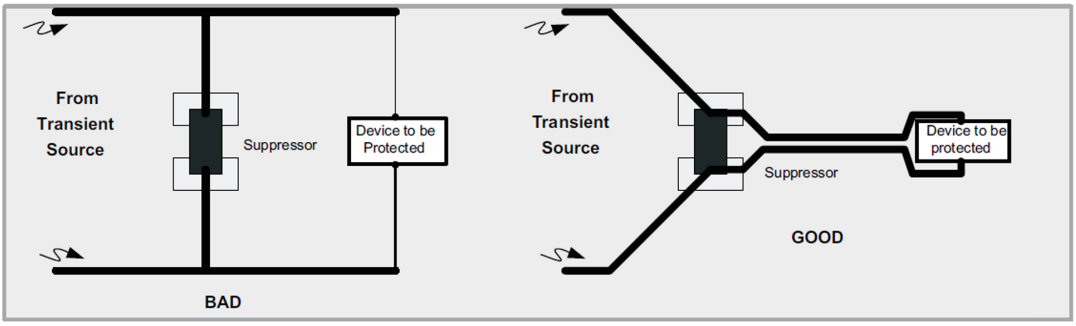


Figure 3. Interconnection of Transient Voltage Suppressor on PCB Diagram

2.3.2.1 PCB Layout Considerations for TPS23861

- KSENSA is shared between SEN1 and SEN2, while KSENSB is shared between SEN3 and SEN4. To optimize the accuracy of the measurement, the designer must carefully perform the PCB layout to minimize impact of PCB trace resistance. Refer to Figure 4 as an example.

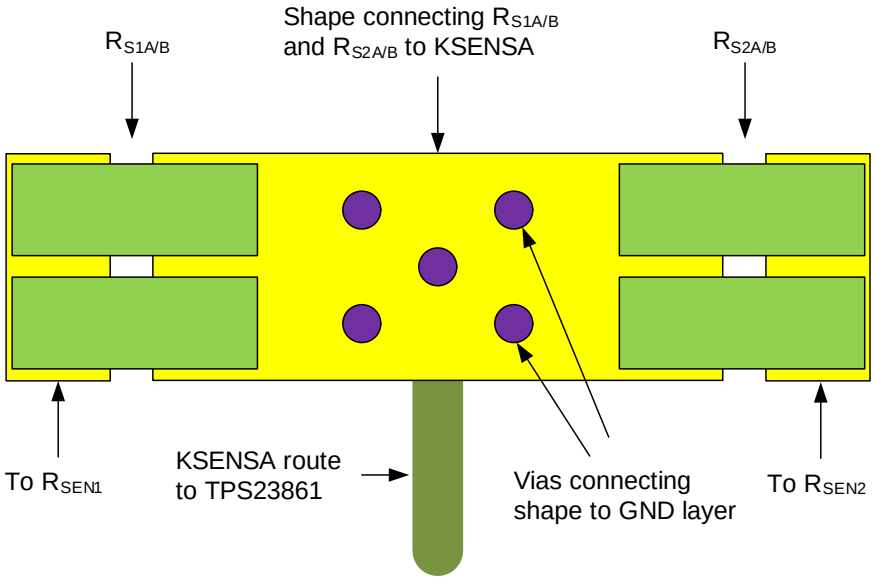


Figure 4. Kelvin Sense Layout Example

- Power pin bypass capacitors
  - C_{VPWR}: Place close to pin 28 (VPWR) and connect with low inductance traces and vias according to Figure 5.
  - C_{VDD}: Place close to pin 1 (VDD) and connect with low inductance traces and vias according to Figure 5.

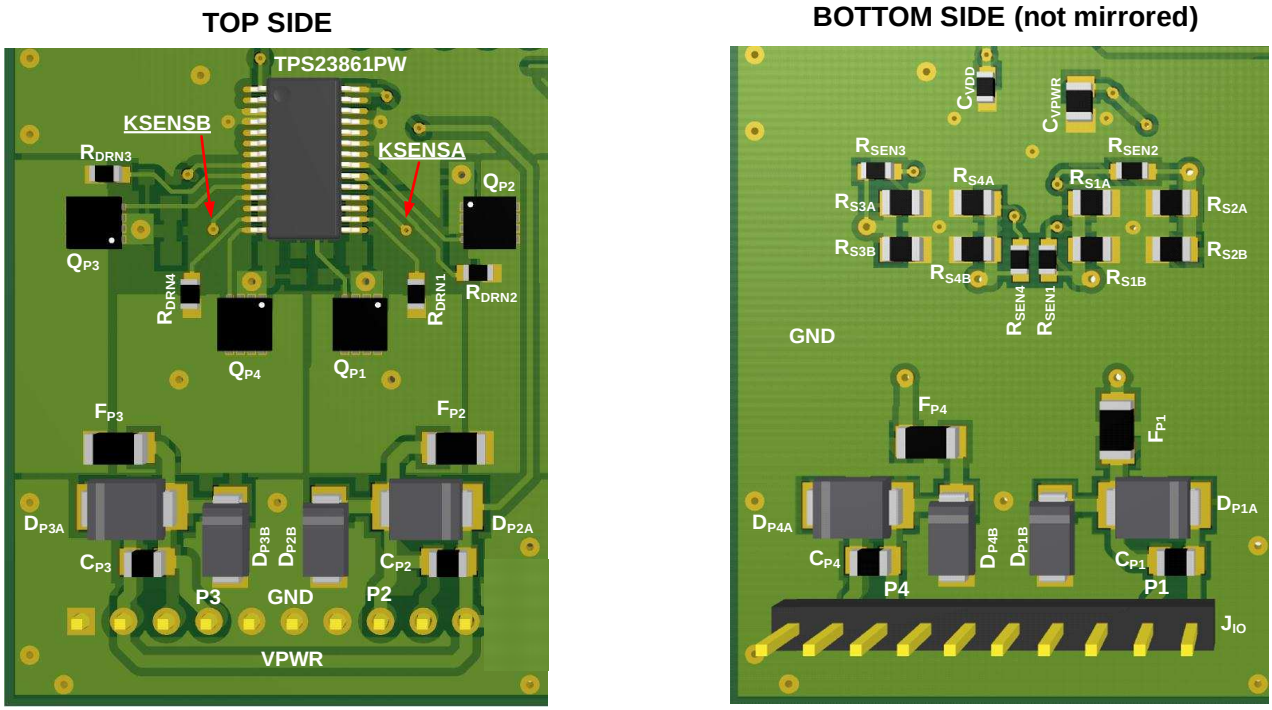


Figure 5. Four-Port Layout Example

- Per-port components
  - R_{SnA} / R_{SnB}: Place according to Figure 4 in a manner that facilitates a clean Kelvin connection with KSENSEA/B.
  - Q_{Pn}: Place Q_{Pn} around the TPS23861 as shown in Figure 5. Provide sufficient copper from Q_{Pn-D} to F_{Pn}.
  - R_{DRNn}: Place R_{DRNn} near to Q_{Pn-D}. Connect to DRAINn pins as shown in Figure 5.
  - R_{SENn}: Place R_{SENn} near to Q_{Pn-S}. Connect to S_{ENn} pins as shown in Figure 5.
  - F_{Pn}, C_{Pn}, D_{PnA}, D_{PnB}: Place this circuit group near the RJ45 port connector (or port power interface if using a daughterboard type of interface as shown in Figure 5). Connect this circuit group to Q_{Pn-D} / GND (TPS23861-AGND) using low inductance traces.

2.4 Choosing SPDs for High-Voltage Surge PSE Applications

This section expands on the PSE example introduced in Section 2.1 by relating the actual requirement and selection of SPDs to the various test levels associated with the IEC 61000-4-5:2005 symmetrical lines test.

The SPD block is shown to be metal oxide varistors (MOVs) that are used to clamp the surge voltage to earth ground, which creates an added current path, $I_{RTN\ 2}$, to return the surge current back to the generator when the MOVs are activated. Each MOV would have to be capable of handling the combined currents of two lines. The actual necessity for the MOVs depends on the test-level requirement and the withstand strength of the PSE.

This section also discusses a four-port PSE application with each port defined to meet a different surge level. Table 2 shows the high-level requirement summary.

Table 2. Requirements for Four Port Design

PORT	INSTALLATION CLASS	TEST LEVELS				WAVEFORM (OCV-SCC)	
		UNSYMMETRICALLY-OPERATED CIRCUITS/LINES		SYMMETRICALLY-OPERATED CIRCUITS/LINES			
		COUPLING MODE		COUPLING MODE			
		LINE-TO-LINE	ALL LINES TO GROUND	LINE-TO-LINE	ALL LINES TO GROUND		
4	2	—	1000	—	1000	10/700 µs - 5/320 µs	1.2/50 µs - 8/20 µs
3	3	—	2000	—	2000		
2	4[1]	2000	4000	—	4000		
1	5++	—	6000	—	6000		

(1) The line-line can be implemented as a line-GND test for an unbalanced circuit or line.

The MOVs may not be required for test levels up to 1000 V because the IEEE 802.3 standard specifies that the PSE must have a withstand strength of at least 1500 V_{PK} for the 10/700-µs impulse test. This is the case for port 4 (Table 2) . Use the guidance provided in *Electrical Transient Immunity for Power-Over-Ethernet* for this case. If the PSE port has been designed with a withstand rating per the 1500-V_{RMS} or 2250-V DC rating specified in the IEEE 802.3 standard then the MOVs may not be required for the 2000-V test level. This design example uses MOVs for port 3. The MOVs are a definite requirement to meet test levels that exceed the withstand strength of the PSE, which includes the 4000-V test level in most cases and the 6000-V level always. MOVs are also used for port 1 and port 2 to show the design and selection procedure.

Although the MOVs may not be required to meet some of the lower test levels, implementing them for all conditions can reduce the stress on sensitive components within the AC/DC converter and add to the overall robustness of the PSE. Consider the intended operating environment of the PSE should to assess the potential risk of damage and downtime of the PSE equipment against the added cost of the protection.

When selecting the proper MOV, be sure to consider the allowable operating voltage, maximum clamping voltage, and surge current ratings. The repetitive surge capability (lifetime rating) of the MOV is equally important because it must survive ten repetitions (five positive and five negative) during the test. In general, the package size of the MOV is directly proportional to its energy handling and surge capability. While MOVs are available in a variety of package styles, this reference design focuses on the use of radial-leaded disc-type devices, which are available in various diameters ranging from 5 mm to 20 mm.

As the test results later verify, the chosen MOVs provide a significantly-higher lifetime rating than ten pulses, which is proven by performing surge testing well beyond the normal product surge lifetime.

The general safety section of the IEEE 802.3 standard specifies that the PoE equipment must conform to the safety requirements of the IEC 60950-1 standard. Section 6.1.2 of this IEC standard states the following regarding SPDs that are connected from telecommunications networks to earth:

6.1.2 Separation of the telecommunication network to earth

6.1.2.1 Requirements

Except as specified in 6.1.2.2, there shall be insulation between circuitry intended to be connected to a telecommunications network and any parts or circuitry that will be earthed in some applications, either within the EUT or via other equipment.

Surge suppressors that bridge the insulation must have a minimum rated operating voltage Uop (for example, the sparkover voltage of a gas discharge tube) of Uop = Upeak + ΔUsp + ΔUsa where Upeak is one of the following values: for equipment intended to be installed in an area where the nominal voltage of the AC mains exceeds 130 V: 360 V for all other equipment: 180 V ΔUsp … shall be taken as 10% of the rated operating voltage of the component.

ΔUsa … shall be taken as 10% of the rated operating voltage of the component.

Therefore, based on standard principle, the MOV used for the earthed PSE must have an allowable operating voltage of at least 216 V_{RMS} when installed in an area where the nominal AC mains is less than 130 V and at least 432 V_{RMS} when installed in an area where the nominal AC mains is greater than 130 V. This reference design assumes that the PSE is installed in an area where the nominal AC mains are less than 130 V, which requires an MOV with an allowable operating voltage of at least 230 V_{RMS} (standard value).

Note that the IEC 60950-1 standard allows the removal of insulation-bridging surge suppressors during the steady-state electrical strength test of an SELV circuit. Additionally, the IEEE 802.3 standard specifies that the PSE of the PoE system must not introduce non-SELV power into the PoE wiring plant, which implies that the PSE is considered to be an SELV circuit.

For this example, use the current levels for the two-line differential mode (DM), four-wire CDN shown in Table 3. The Littelfuse UltraMOV® Varistor Series was chosen based on availability and because of the detailed repetitive surge capability curves within the device data sheet. The standard value for the 230-V_{RMS} rating was chosen (VxxE230P, where xx = disc diameter). The selection process continues by using the repetitive surge curves provided for each MOV size. The repetitive surge curves indicate the maximum current versus the pulse-width rating of the MOV based on the number of expected surge pulses.

Table 3. Maximum Configuration—Two Center-Tap Currents: 10/700 and 1.2/50 Waveforms

VPOC (V)	4-LINE CMIPCT-PSC (A)	1-LINE DMIPCT-PSC (A)	2-LINE DMIPCT-PSC (A)	8-LINE CMIPCT-PSC (A)	1-LINE DMIPCT-PSC (A)	2-LINE DMIPCT-PSC (A)
500	6.25	3.13	6.25	3.76	1.88	3.76
1000	12.50	6.25	12.50	7.52	3.76	7.52
1500	18.75	9.38	18.75	11.28	5.64	11.28
2000	25.00	12.50	25.00	15.04	7.52	15.04
4000	50.00	25.00	50.00	30.08	15.04	30.08
6000	75.00	37.50	75.00	37.50	18.75	37.50

For the IEC 61000-4-5:2005 test, the MOV must be able to survive ten surge pulses with each current surge having an equivalent rectangular pulse width of 320 µs, which is based on the 320-µs time to half value associated with the 10/700-µs to 5/320-µs combination wave.

The Littlefuse V14E230P, V10E230P, and V07E230P were selected for port 1 (75 A), port 2 (50 A), and port 3 (25 A), respectively. For port 1, use a 320-µs impulse duration and 75-A surge current (see Figure 6) to obtain approximately 600 repetitions. This configuration provides additional lifetime margin for extended testing and higher current levels such as the values in Table 3. If the V10E230P MOV is used at a 320-µs impulse duration and 75-A surge current, the number of repetitions drops to approximately 30.

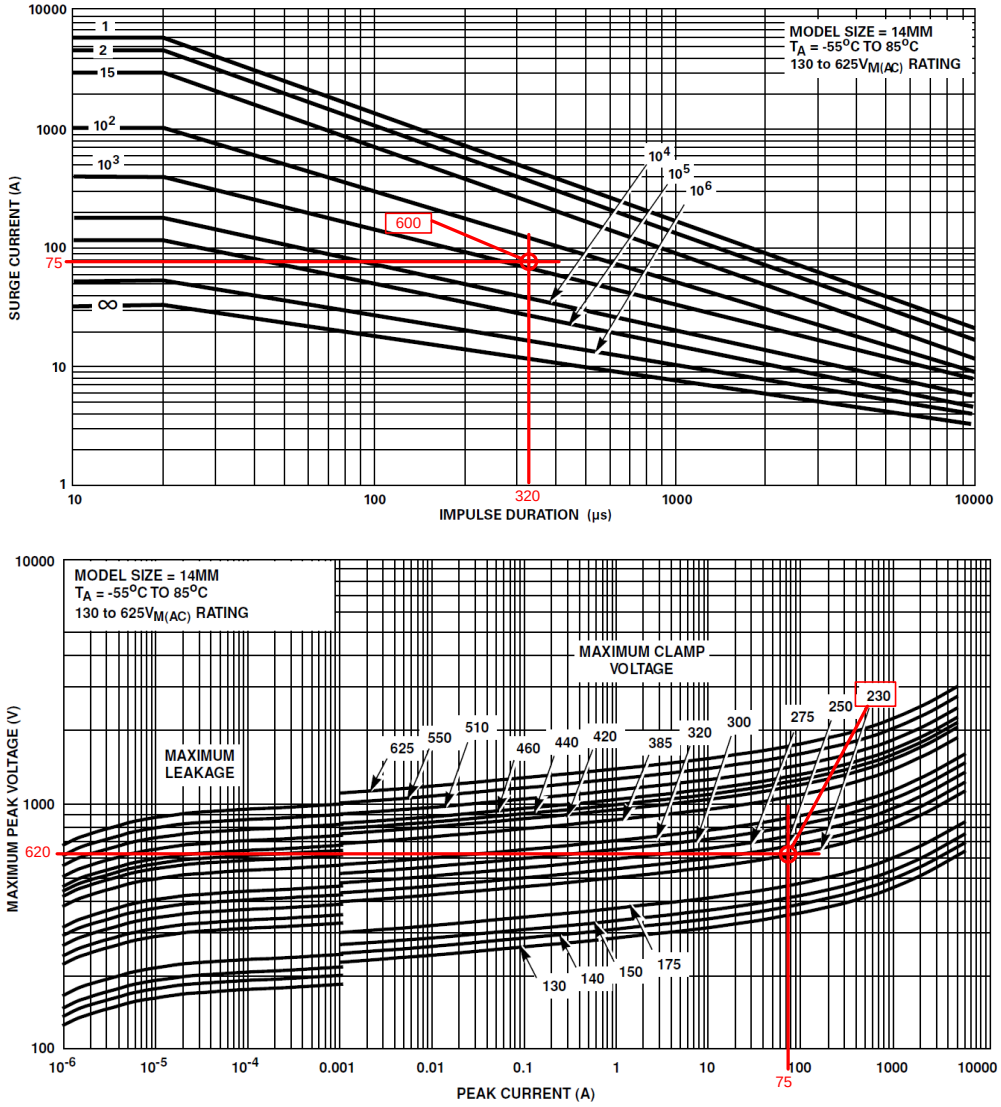


Figure 6. Using MOV Repetitive Surge Capability and Maximum Clamping Voltage Curves

To finish the design for port 2 and port 3, see the Littelfuse data sheet for V10E230P and V07E230P. For port 2, at a 320-µs impulse duration and 50-A surge current, there are approximately 100 repetitions. For port 3 (25 A), there are 300 repetitions. The surge voltage at port 2 (50 A) and port 3 (25 A) is 640 V and 630 V, respectively.

If the current waveform of the 1.2/50-µs to 8/20-µs combination wave generator sets the PSE surge requirement, the MOV surge current requirement is reduced by approximately ten times. This requirement can reduce the amount of PCB area and the cost associated with the larger MOVs.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This section covers an overview of the TIDA-01411 design board and all the test connections required to evaluate the reference board.

3.1.1 Hardware

To evaluate the lighting surge for PSE devices, the designer must first set up the complete system solution.

ITEM	COMMENTS	PART NUMBER
Lighting surge evaluation board	Four-port IEEE 802.3at compliant PSE TPS23861	PR2189E1
PD controller	Must be IEEE 802.3at compliant	TPS2378EVM-105
USB TO GPIO	Connect USB port of PC to JTAG port of PSE board	—
Two CAT5 Ethernet cables	Both < 100 m in length	—
Power supply	Supply 54 V to PSE	—
CDN-UTP	Coupling and decoupling network for test	EMC PARTNER
Transient 2000	SURGE generator	EMC PARTNER
PC with USB port	Control PSE through GUI	—

3.1.2 Software

The Texas Instruments PI Commander graphical user interface (GUI) can be used with this reference design to provide real-time feedback on port telemetry and also control advanced PSE settings. Download PI Commander (PI Commander - TPS23861- setup.exe) from the TPS23861 product page: Software Section. For more information on how to connect and communicate with the TIDA-01411 design, see the section regarding TPS23891EVM-612 PI Commander GUI Setup in *TPS23861EVM-612 Auto-Mode Evaluation Module for TPS23861* .

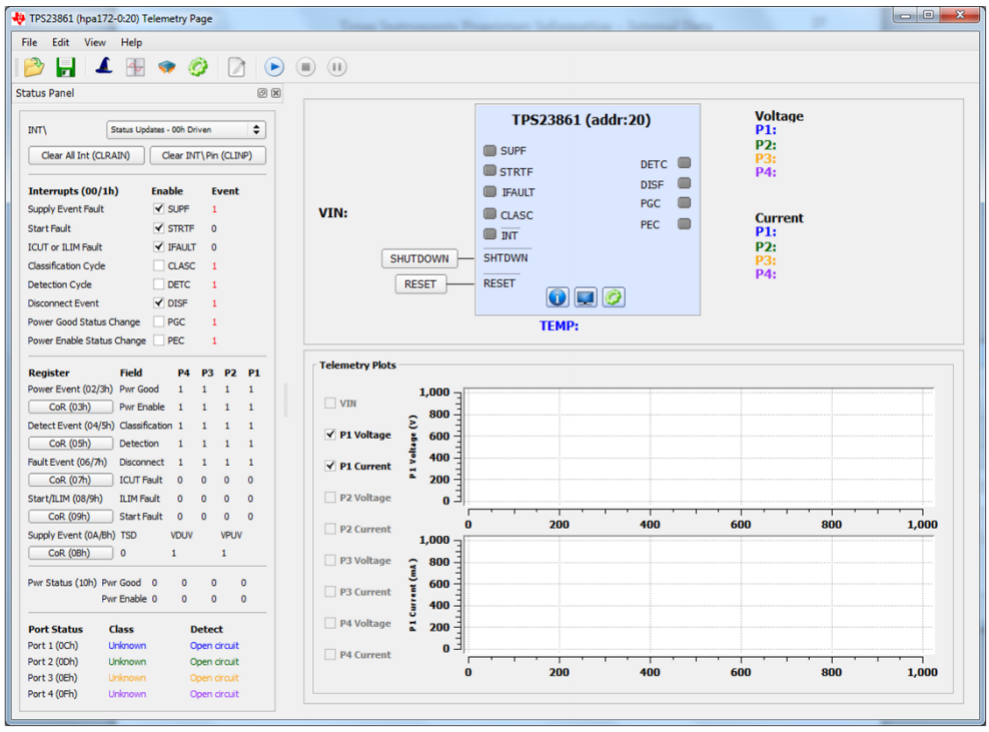


Figure 7. TPS23861EVM GUI

3.2 Testing and Results

3.2.1 Test Setup

Figure 8 shows a photo of the entire test system. The first step is to connect the USB-to-GPIO from the JTAG port of the PSE evaluation board to the USB port of the computer. Then connect the 54-V power supply and make sure that it is OFF before testing. Next, use a CAT5 Ethernet wire to connect from the PSE port to the coupling side of CDN-UTP and connect the PD to the decoupling side of CDN-UTP. The following step is to connect the surge generator output of the Transient 2000 to the CDN and apply surge to each line. After these steps, the user can begin lighting surge testing with a power on and configuration of the PSE.

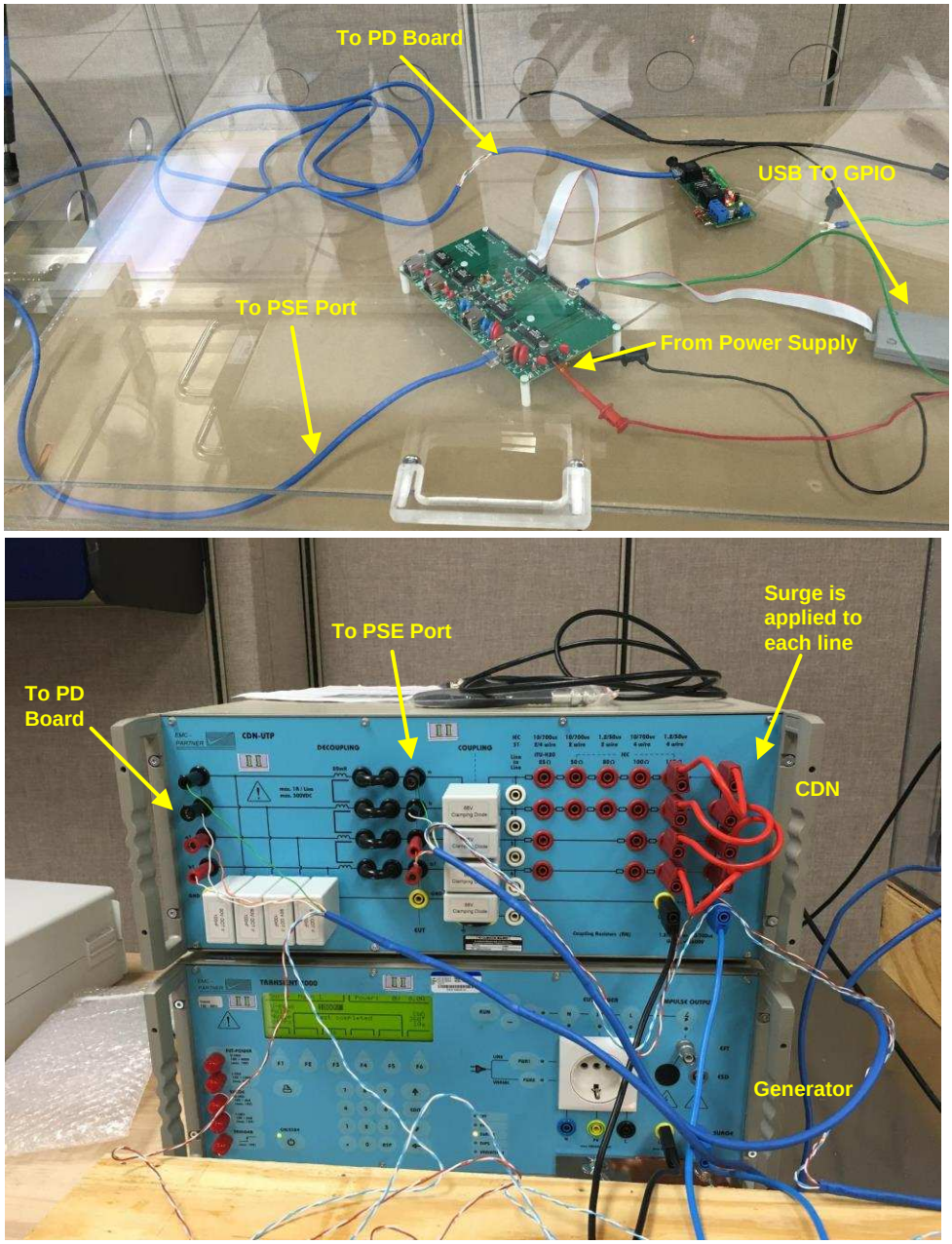


Figure 8. PSE Surge Test Setup

3.2.2 Test Results

3.2.2.1 Common Mode

Table 4. Common Mode: 1.2/50-µs Waveform Test Results

PORT	DETECTION STATUS	CLASS STATUS	SURGE WAVEFORM	PORT ON
1[(1)]	Open circuit	Unknown	±6 kV 1.2/50 µs	Pass
2	Resistance valid	Class 4	±4 kV 1.2/50 µs	Pass
3	Resistance valid	Class 4	±2 kV 1.2/50 µs	Pass
4	Resistance valid	Class 4	±1 kV 1.2/50 µs	Pass

(1) Surges applied to pair 1 and 2 followed by pair 3 and 6 using the surge generator in series with a 42-Ω resistor. Port tested is in forced ON state with DC disconnect disabled.

Table 5. Common Mode: 10/700-µs Waveform Test Results

PORT	DETECTION STATUS	CLASS STATUS	SURGE WAVEFORM	PORT ON
1[(1)]	Open circuit	unknown	±6 kV 10/700 µs	Pass
2[(1)]	Open circuit	unknown	±4 kV 10/700 µs	Pass
3[(1)]	Open circuit	unknown	±2 kV 10/700 µs	Pass
4[(1)]	Open circuit	unknown	±1 kV 10/700 µs	Pass

(1) Surges applied to pair 1 and 2 followed by pair 3 and 6 using the surge generator in series with a 40-Ω resistor. Port tested is in forced ON state with DC disconnect disabled.

3.2.2.2 Differential Mode (Single-Wire Differential)

Table 6. Single-Wire Differential Mode: 1.2/50-µs Waveform Test Results

PORT	DETECTION STATUS	CLASS STATUS	SURGE WAVEFORM	PORT ON
1[(1)]	Resistance valid	Class 4	±4 kV 1.2/50 µs	Pass
2	Resistance valid	Class 4	±4 kV 1.2/50 µs	Pass
3	Resistance valid	Class 4	±2 kV 1.2/50 µs	Pass
4	Resistance valid	Class 4	±1 kV 1.2/50 µs	Pass

(1) The surge generator used during testing had a ±4-kV maximum capability.

3.2.2.3 Differential Mode (Single-Pair Differential)

Table 7. Single-Pair Differential Mode: 1.2/50-µs Waveform Test Results

PORT	DETECTION STATUS	CLASS STATUS	SURGE WAVEFORM	PORT ON
1[(1)]	Resistance valid	Class 4	±4 kV 1.2/50 µs	Pass
2	Resistance valid	Class 4	±4 kV 1.2/50 µs	Pass
3	Resistance valid	Class 4	±2 kV 1.2/50 µs	Pass
4	Resistance valid	Class 4	±1 kV 1.2/50 µs	Pass

(1) The surge generator used during testing had a ±4-kV maximum capability.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01411.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01411.

4.3 PCB Layout Recommendations

- PCB spacings
  - More than 80 mils from earth (and logic) ground (> 4 kV based on 20 V/mil)
  - More than 30 mils from Ethernet cable side nets (> 600 V)
  - More than 20 mils from 54-V DC (VPWR) and port DRAINx nets
- Grounding
  - System frame or earth ground-current shunting path for RJ45 housings
  - PoE or 54-V DC power ground from DC power supply
  - Logic or digital ground may be connected to earth ground through resistors

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01411.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01411.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01411.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01411.

5 Software Files

To download the software files, see the design files at TIDA-01411.

6 Related Documentation

1. Texas Instruments, *Lightning Surge Considerations for PoE Power Sourcing Equipment Devices*
2. Texas Instruments, *Electrical Transient Immunity for Power-Over-Ethernet*
3. Texas Instruments, *TPS23861EVM-612: Auto-Mode Evaluation Module for TPS23861*
4. Texas Instruments, *TPS2378 EVM User's Guide*

6.1 Trademarks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to A Revision	Page
• Changed title from *Type-2 PoE PSE, 60-kV Lightning Surge Reference Design* to *Type-2 PoE PSE, 6-kV Lightning Surge Reference Design*	1

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