TI Designs: TIDA-01425

Automotive Stand-Alone Gateway Reference Design With Ethernet and CAN

Description

This reference design targets automotive gateways with a focus on increasing bandwidth and processing power in gateway applications. The design implements Ethernet physical layer transceivers (PHYs) for increased bandwidth along with an automotive processor for greater processing capabilities allowing automotive gateways to pass more data at higher speeds. Furthermore, the design offers a starting point for a full automotive gateway design with a full power tree, CAN PHYs, and components selected with automotive requirements and emission specifications in mind to simplify the design process.

Resources

Design Folder

TIDA-01425

Product Folders

DRA710	DP83848Q-Q1	TCAN1042-Q1
TPS51200-Q1	TPS22965-Q1	LM53625-Q1
TPS61240-Q1	CDCE913-Q1	LM74610-Q1
LP87332D-Q1	LP873220-Q1	DP83TC811R-Q1

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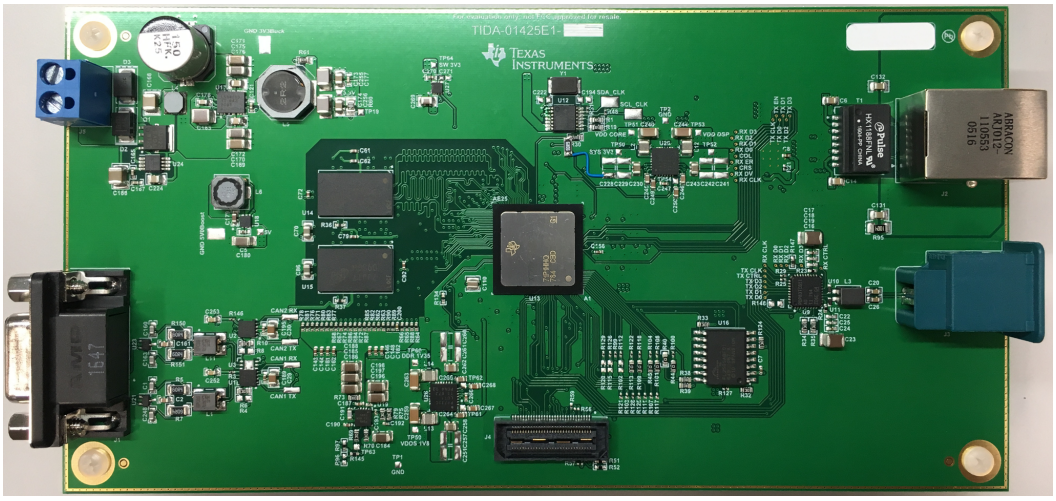
Features

- Processor-Based System
- IEEE 802.3bw 100BASE-T1 Ethernet PHY
- IEEE 802.u 100BASE-TX Ethernet PHY
- CAN PHY
- Designed to Operate Through Cold Crank, Jump Start, and Load Dump
- Reverse Battery Protection
- Reduced EMI Power Stages

Applications

- Automotive Gateways
- Multi-Function BCM With Gateway



1 System Description

The TIDA-01425 is a reference design for automotive gateways focused on increasing bandwidth and processing power in gateway applications. The design implements Ethernet PHYs for increased bandwidth along with an automotive processor for greater processing capabilities. Furthermore, the design offers an excellent starting point for a full automotive gateway design. All components were selected based on automotive requirements and emission specifications in mind. The TIDA-01425 implements four total PHYs: two ethernet PHYs and two controller area network (CAN) PHYs. A 100BASE-T1 PHY allows for Ethernet communication over a single twisted-pair cable, which lowers the wiring weight within the vehicle while also boosting overall bandwidth (100 Mb/s). Along with the single 100BASE-T1 PHY, a 100BASE-TX PHY is utilized to allow for diagnostic readings from the various electronic systems of a vehicle. In addition to the Ethernet PHYs, two CAN PHYs allow for communication to CAN buses within the automobile. Finally, the automotive processor allows for faster processing speeds to keep up with the increased bandwidth and also offers software scalability. Furthermore, through software, the processor can improve overall vehicle security.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Operational input voltage from the automotive battery	4.1	12	24	V
V_{IN} survivability	Input voltage system can survive but not operate	–42	—	42	V
I_{IN}	Operational input current	0.144 (24 V_{IN})	0.286	0.744 (4.1 V_{IN})	A
Temperature	Operating temperature	–40°C	—	105°C	°C
F_{SW} buck	Buck converter switching frequency	1.85	2.1	2.35	MHz
F_{SW} boost	Boost converter switching frequency	3.5	—	3.8	MHz
Ethernet speeds	Ethernet communication speed	—	—	100	MB/s
CAN speeds	CAN communication speed	—	—	1	MB/s

2 System Overview

2.1 Block Diagram

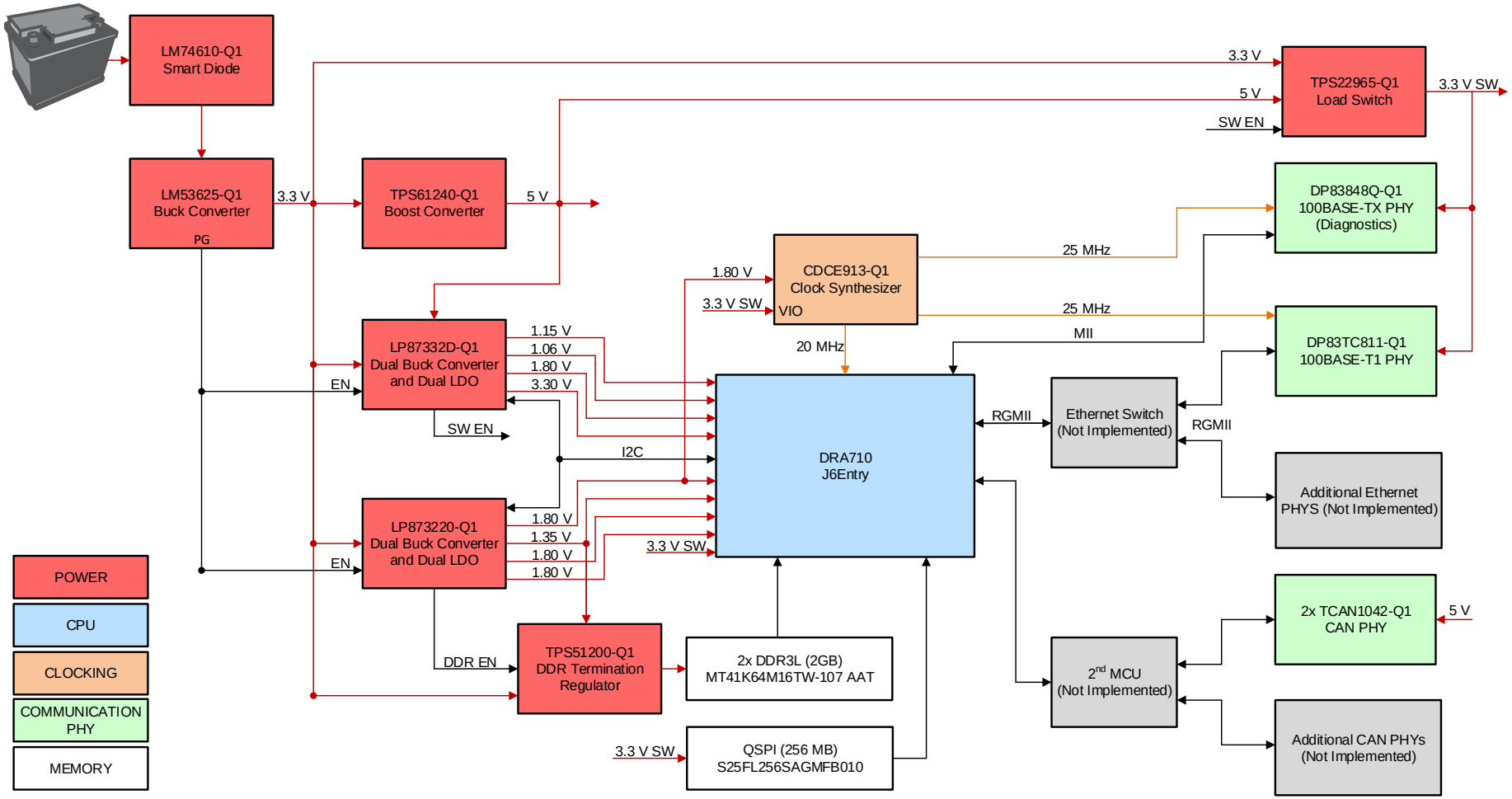


Figure 1. TIDA-01425 Block Diagram

2.2 Highlighted Products

2.2.1 DRA710 J6Entry Automotive Processor

The DRA71x J6Entry processor family is a scalable processor family designed for automotive applications. The DRA710 specifically includes an internal gigabit Ethernet (GMAC) switch with two external ports, dual controller area network (DCAN) modules with CAN 2.0B protocol, up to 512KB of on-chip L3 RAM, DDR3/DDR4 memory interface supporting up to 2GB across single chip select, speeds up to DDR-1333 (667 MHz), a general-purpose memory controller (GPMC), an enhanced direct-memory-access (EDMA) controller and sixteen 32-bit general-purpose timers. The processor also contains a 32-MPU watchdog timer, six high-speed inter-integrated circuit (I^2C) ports, an HDQ/1-Wire Interface, ten configurable UART/IrDA/CIR modules, four multichannel serial peripheral interfaces (MCSPIs), a quad-SPI (QSPI), a SuperSpeed USB 3.0 dual-role device, a high-speed USB 2.0 dual-role device, a high-speed USB 2.0 on-the-go, PCI-express 3.0 subsystems with two 5-Gbps lanes (one two-lane Gen2-compliant port or two one-lane Gen2-compliant ports), up to 186 general-purpose IO (GPIO) pins, on-chip debug with CTools technology, as well as power, reset, and clock management. This processor is capable of operating over extreme temperatures ranging from –40°C to 125°C. This processor family also contains devices that include two M4 cores and a c66x digital signal processing (DSP) core.

Figure 2 shows the functional block diagram of the DRA71x device.

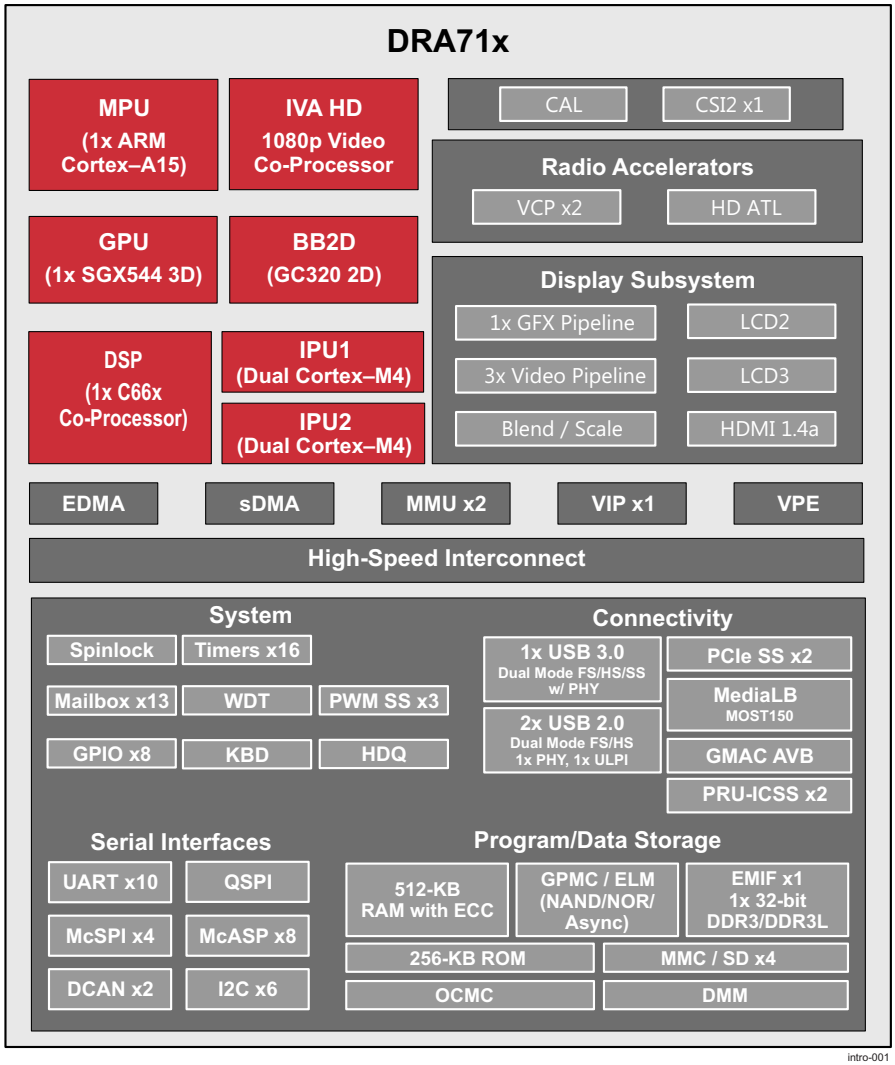


Figure 2. DRA71x Functional Block Diagram

2.2.2 DP83TC811R-Q1 Automotive Single-Port 100BASE-T1 Ethernet PHYTER™

The DP83TC811R-Q1 is a single-port automotive Ethernet PHY which is compliant to the IEEE802.3bw standard and can operate at 100 Mb/s over 15 m of unshielded twisted-pair cable. The DP83TC811R-Q1 also has a best-in-class transmit and receive latency of less than 150 ns and supports audio video bridging/time sensitive network (AVB/TSN) systems with 1588 start-of-frame (SFD) detection.

Figure 3 shows the DP83TC811R-Q1 functional block diagram.

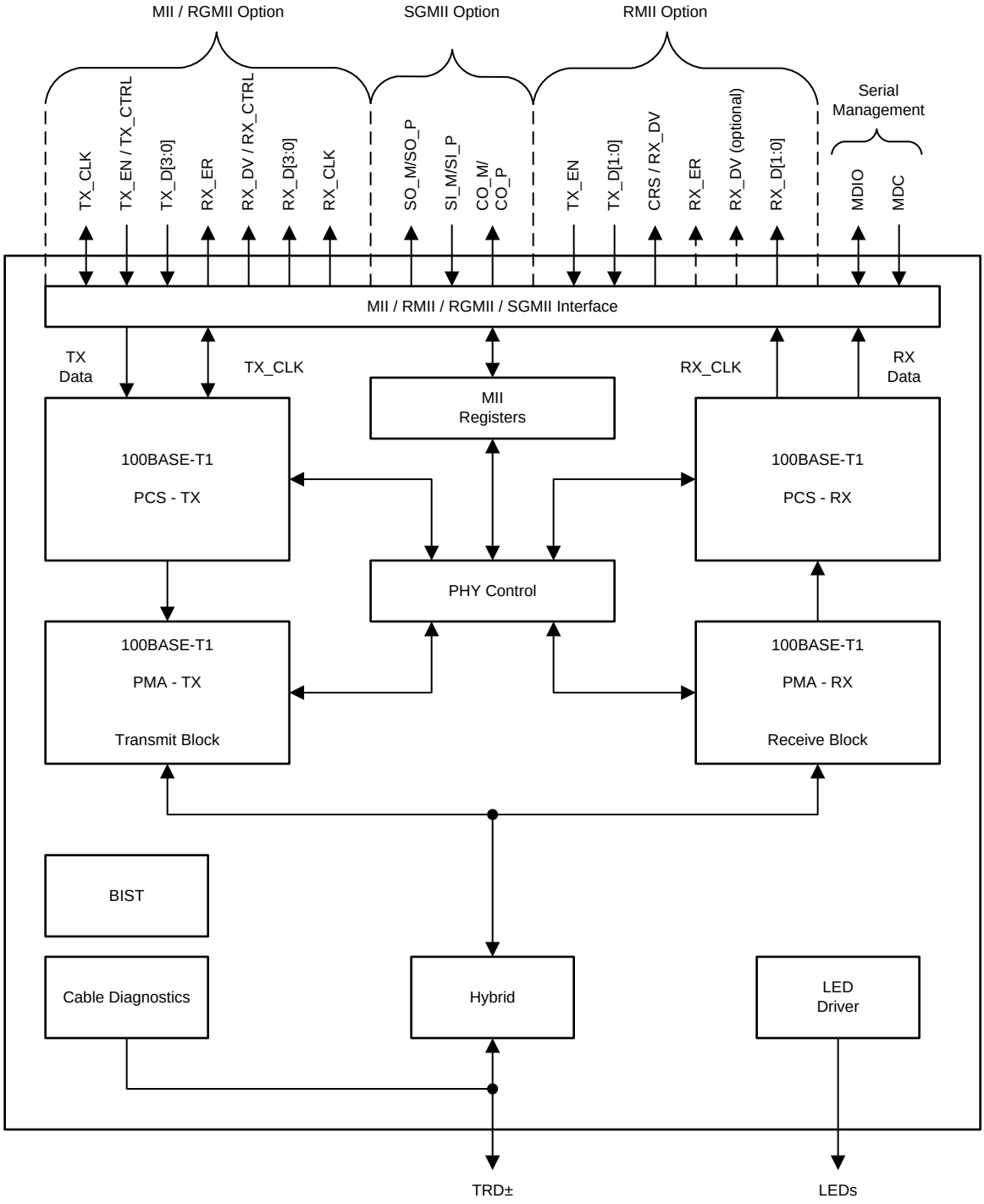


Figure 3. DP83TC811RH-Q1 Functional Block Diagram

The DP83TC811R-Q1 supplies all physical layer functions required to transmit and receive data over single twisted-pair cables at 100 Mb/s. Therefore, the IEEE 802.3bw standard can be used within the vehicle, reducing cost and cable weight. The DP83TC811R has a low power consumption of around 150 mW in active mode and a flexible interface that can communicate through MII, RMII, RGMII, or SGMII to a media access controller (MAC). Furthermore, the device can operate in extreme temperatures from –40°C to 125°C.

2.2.3 DP83848Q-Q1 Automotive Single-Port 10/100 Mbps Ethernet PHYTER™

The DP83848Q-Q1 is a highly-reliable, feature rich, robust device that meets IEEE 802.3u specifications over an extended temperature range of –40°C to 105°C.

Figure 4 shows the DP83848Q-1 functional block diagram.

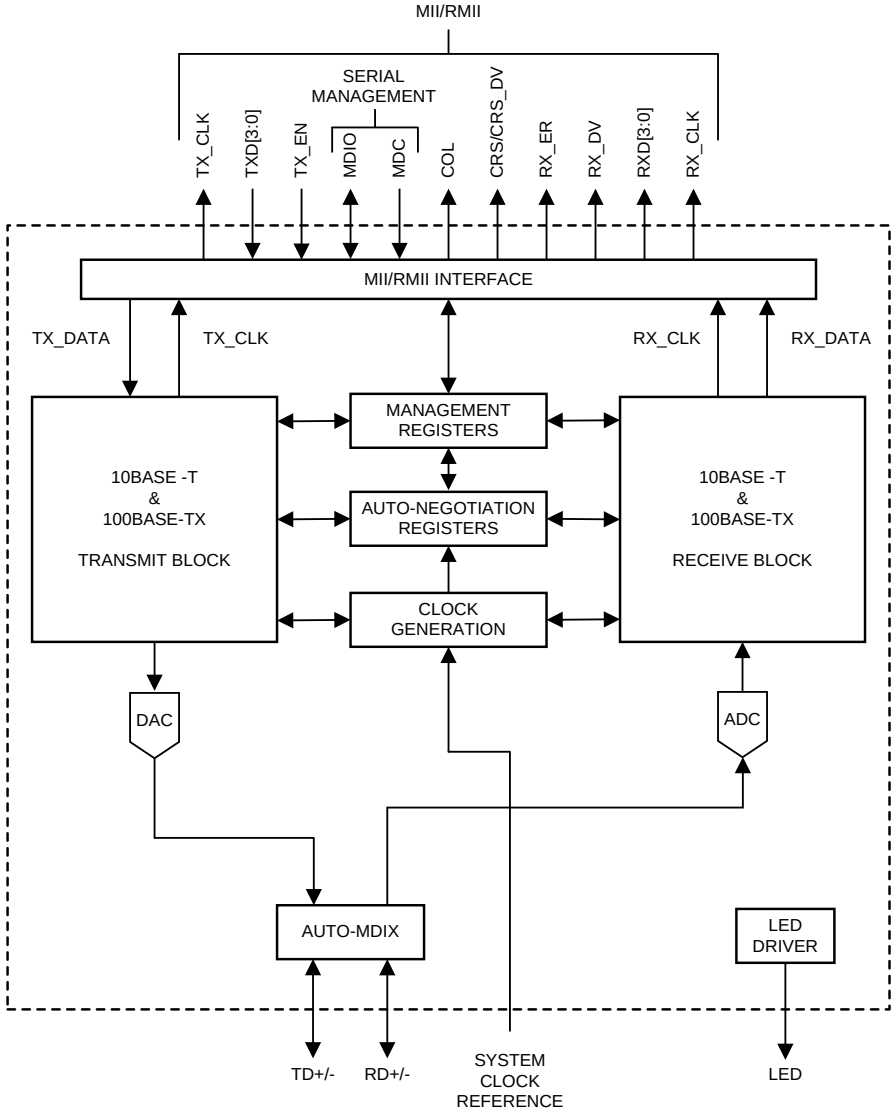


Figure 4. DP83848Q-1 Functional Block Diagram

The DP83848Q-Q1 is AEC-Q100 grade-2 qualified and has a low power consumption of less than 270 mW. In addition, the PHY offers communication speeds of 10 Mb/s and 100 Mb/s along with MII and RMII MAC interface options. The DP83848Q-Q1 also has deterministic-, low-transmit-, and receive latency. The device allows for the use of 100BASE-TX Ethernet, which is typically used in automotive systems for reading diagnostics data from a vehicle using the onboard diagnostics (OBD) connector.

2.2.4 TCAN1042-Q1 Automotive Fault-Protected CAN Transceiver

The TCAN1042-Q1 is a family of automotive CAN transceivers that meet the ISO11898-2 high-speed CAN physical-layer standard. In addition, the devices come with the option of CAN FD for up to 2-Mb/s communication speeds, IO level shifting, or both.

Figure 5 shows the TCAN1042-Q1 functional block diagram.

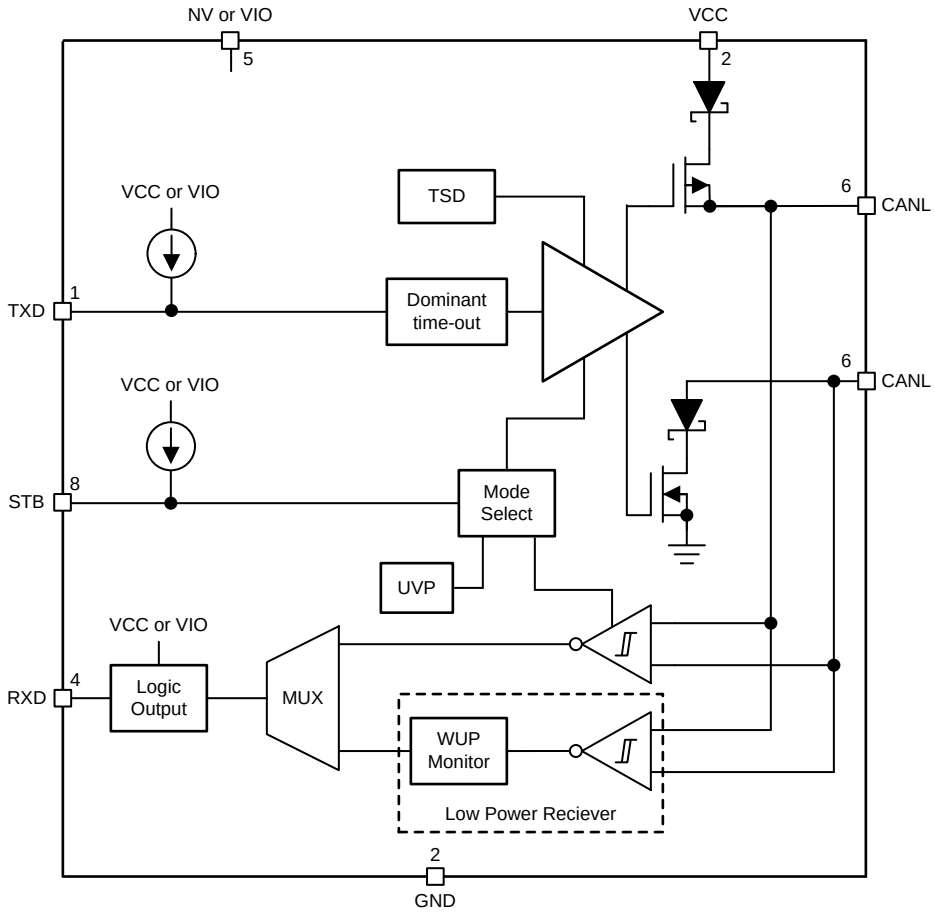


Figure 5. TCAN1042-Q1 Functional Block Diagram

All TCAN1042-Q1 integrated circuits are AEC-Q100 qualified and have low-power standby modes with remote wake request. Furthermore, the devices include protection features to enhance device and network robustness.

2.2.5 CDCE913-Q1 Programmable 1-PLL VCXO Clock Synthesizer

The CDCE913-Q1 is a modular, PLL-based programmable clock synthesizer. The device offers flexible and programmable options, such as output clock frequencies, input signals, and control pins so that the user can configure the device for their specific design.

Figure 6 shows the CDCEx913-Q1 functional block diagram.

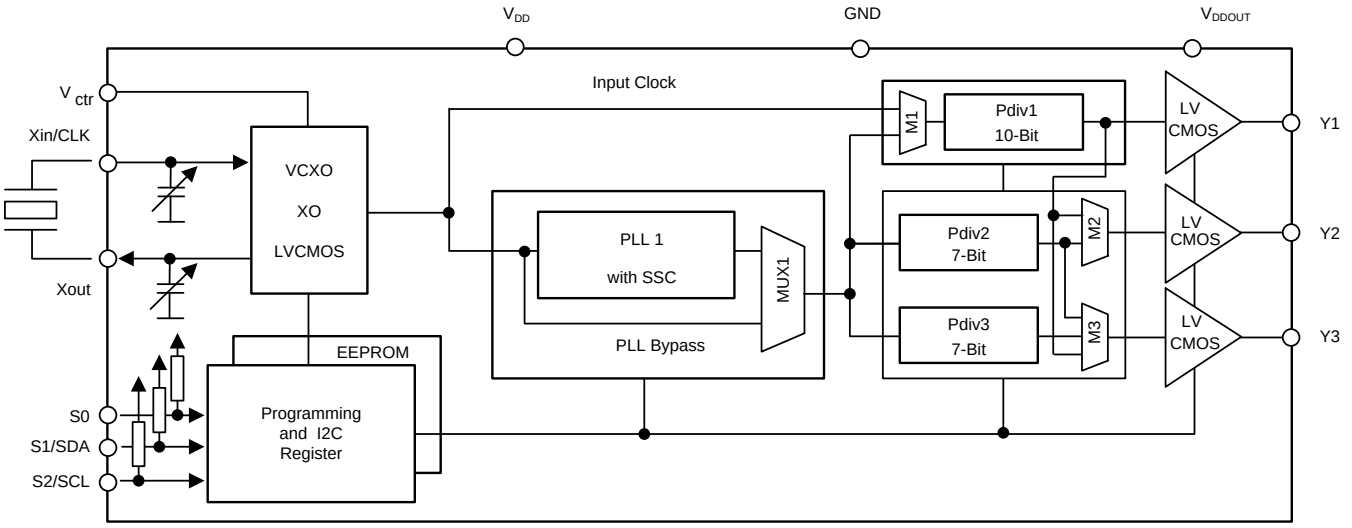


Figure 6. CDCEx913-Q1 Functional Block Diagram

The CDCE913-Q1 generates up to three output clocks from a single input frequency reducing board space and cost. Additionally, the device utilizes a low-noise PLL core that offers output frequencies of up to 230 MHz and an input crystal range from 8 MHz to 32 MHz. The device is AEC-Q100 qualified and can operate from –40°C to 125°C.

2.2.6 LM53625-Q1 2.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter

The LM53625-Q1 synchronous buck regulator is optimized for automotive applications, providing an output voltage of 5 V, 3.3 V, or an adjustable output.

Figure 7 shows the LM53625-Q1 functional block diagram.

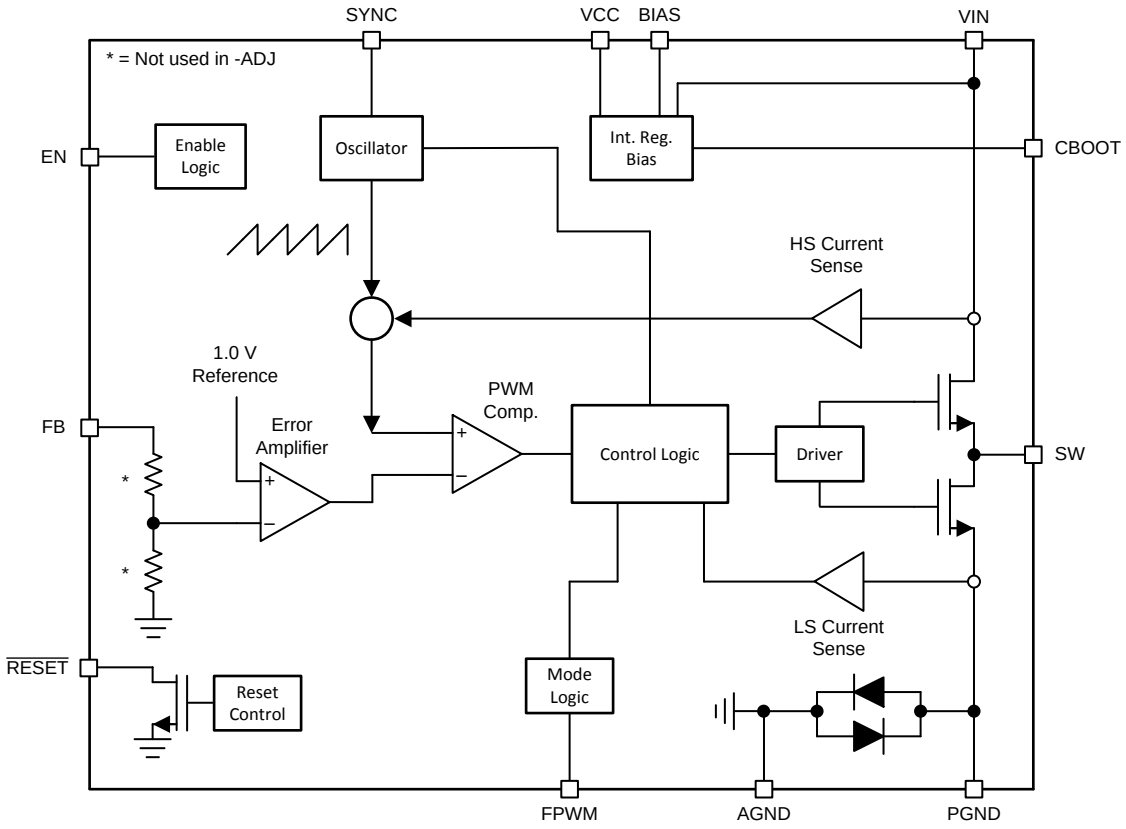


Figure 7. LM53625-Q1 Functional Block Diagram

Innovative architecture allows the LM53625-Q1 to regulate a 3.3-V output from an input voltage of only 3.55 V. Also, the device has a wide operational input voltage range and can operate at a max of 36 V. The LM53625-Q1 comes in the automotive-qualified Hotrod QFN package that reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering electromagnetic interference (EMI). The buck regulator can operate at extended temperatures from –40°C to 125°C.

2.2.7 LP873220-Q1 and LP87332D-Q1 Dual High-Current Buck Converters and Dual Linear Regulators

The LP873220-Q1 and LP87332-Q1 devices are designed to meet the power management requirements of the latest processors and platforms in automotive applications. Each device contains two step-down DC-DC converters along with two linear regulators and two general purpose digital-outputs. One-time programming ensures that the devices meet the required power-up and power-down sequencing for the supported processors and also establishes the GPO pins as required.

Figure 8 shows the LP8732x-Q1 block diagram.

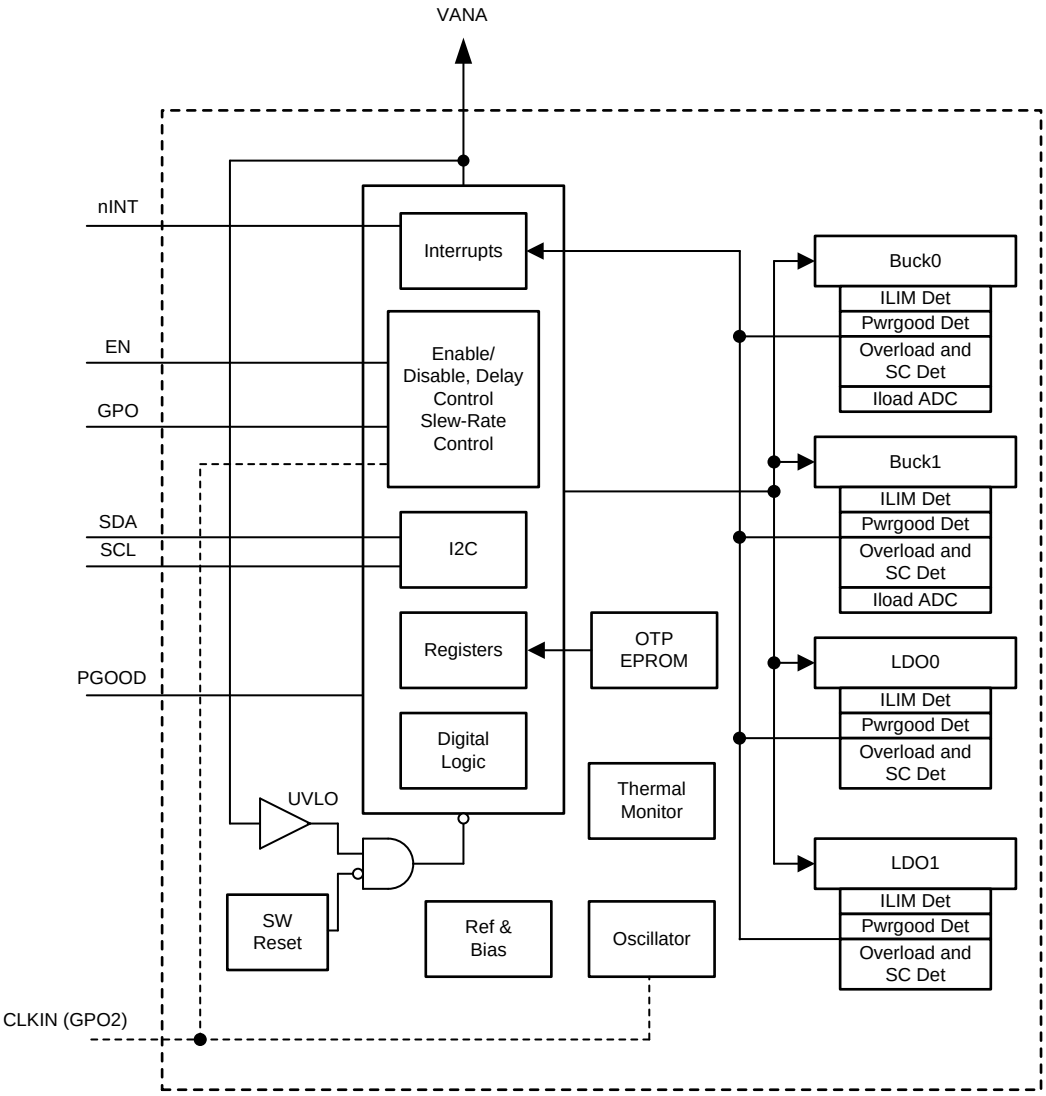


Figure 8. LP8732x-Q1 Block Diagram

The LP873220-Q1 and LP87332D-Q1 are controlled through enable signals and an I^2C interface. The DC-DC converters have automatic pulse width modulation (PWM) and pulse frequency modulation (PFM) operation allowing high efficiency over a wide output-current range. Remote voltage sensing is an option to help improve the accuracy of these output voltages. The switching clock can also be forced to PWM mode and synchronized to an external clock to minimize EMI of the system. Both devices support load-current measurement without the addition of external current-sense resistors. The LP873220-Q1 and LP87332D-Q1 devices support programmable start-up and shutdown delays along with sequences

including GPO signals synchronized to the enable signal. Both devices are AEC-Q100 qualified capable of operating from –40°C to 125°C with input voltage ranges of 2.8 V to 5.5 V. The DC-DC converters operate at 2 MHz with spread-spectrum mode and phase interleaving to help reduce EMI. The difference between the LP873220-Q1 and LP87332D-Q1 is that the LP873220-Q1 DC-DC converter has a maximum output current of 2 A, where the LP87332D-Q1 has a maximum current output of 3 A for the buck regulators.

2.2.8 LM74610-Q1 Smart Diode Controller

The LM74610-Q1 is a controller device that drives an N-Channel MOSFET in a reverse polarity protection circuit. The device drives the MOSFET to emulate an ideal diode rectifier when connected in series with a power source.

Figure 9 shows the LM74610-Q1 functional block diagram.

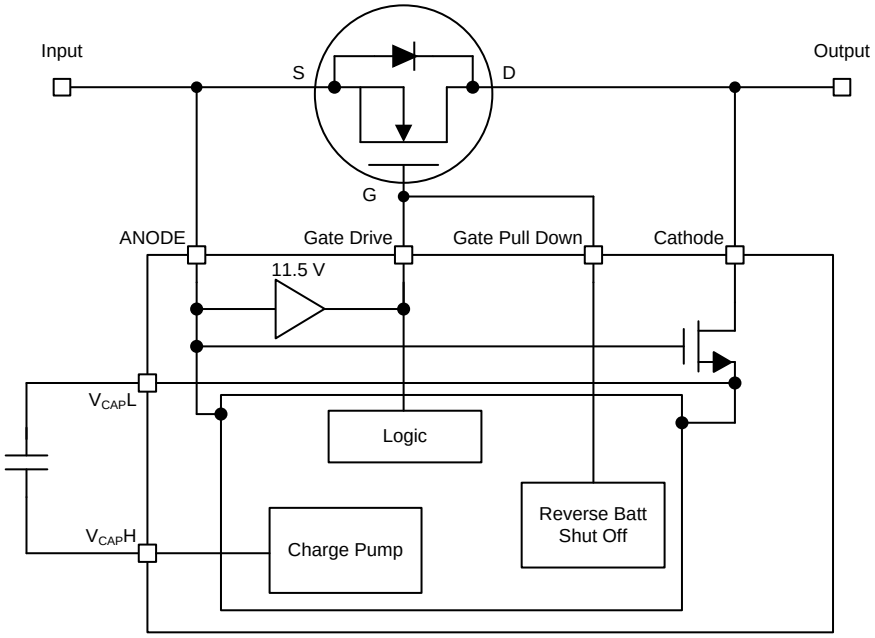


Figure 9. LM74610-Q1 Functional Block Diagram

A unique advantage of the LM74610-Q1 smart diode controller is that there is no reference to ground and therefore zero quiescent current (I_q). The LM74610-Q1 provides a fast-response internal comparator to discharge the MOSFET gate in the event of reverse polarity. Also, due to a lower voltage drop across the MOSFET versus a diode, the total voltage input to the first stage power supply can go much lower. The smart diode is AEC-Q100 qualified, meets CISPR25 EMI specifications, and can operate from –40°C to 125°C.

2.2.9 TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter

The TPS61240-Q1 is a high-efficiency, synchronous step-up DC-DC converter that provides best-in-class line and load transient performance. The device supports currents up to 450 mA at a fixed output voltage of 5 V. Additionally, the device has an input voltage range of 2.3 V to 5.5 V and operates at a 3.5-MHz switching frequency in typical load conditions. The TPS61240-Q1 is AEC-Q100 qualified and can operate from –40°C to 105°C.

Figure 10 shows the TPS61240-Q1 functional block diagram.

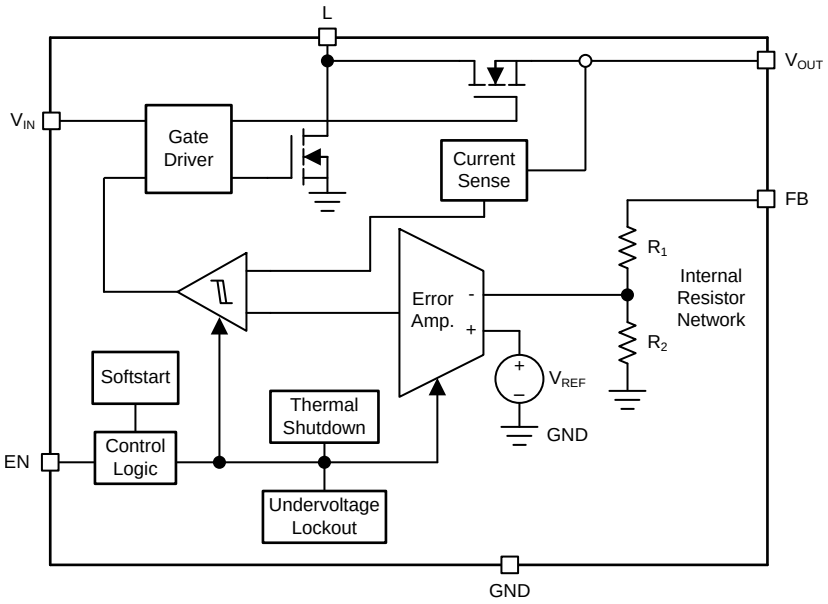


Figure 10. TPS61240-Q1 Functional Block Diagram

2.2.10 TPS51200-Q1 Sink and Source DDR Termination Regulator

The TPS51200-Q1 is a sink and source double-data-rate (DDR) termination regulator specifically designed for low input voltage, low cost, low noise, and systems where space is a key consideration. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, and low-power DDR3 and DDR4 VTT bus termination. In addition, the device is AEC-Q100 qualified with an operational temperature of –40°C to 125°C.

Figure 11 shows the TPS51200-Q1 functional block diagram.

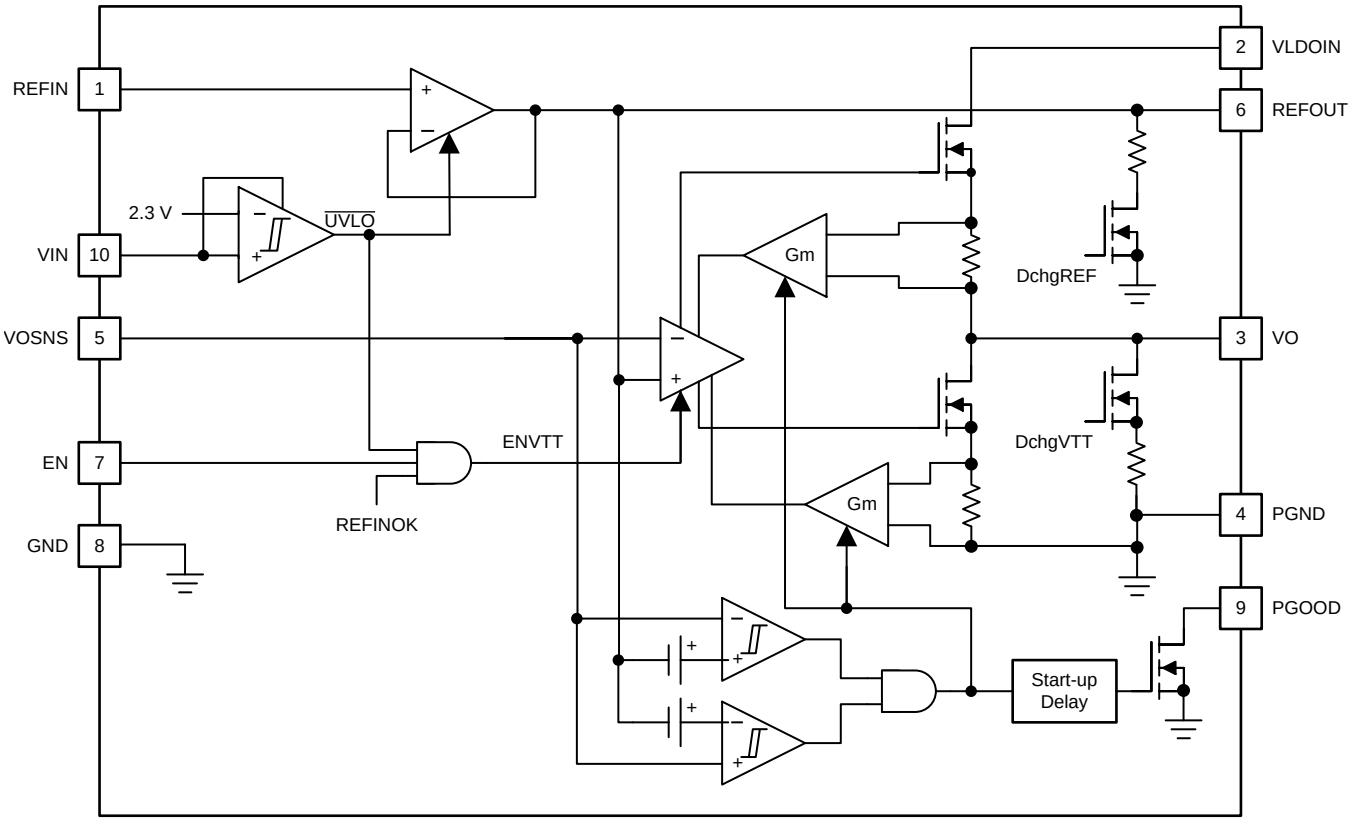


Figure 11. TPS51200-Q1 Functional Block Diagram

2.2.11 TPS22965-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch

The TPS22965-Q1 is a small, ultra-low-R_{on}, single-channel load switch with controlled turnon.

Figure 12 shows the TPS22965-Q1 functional block diagram.

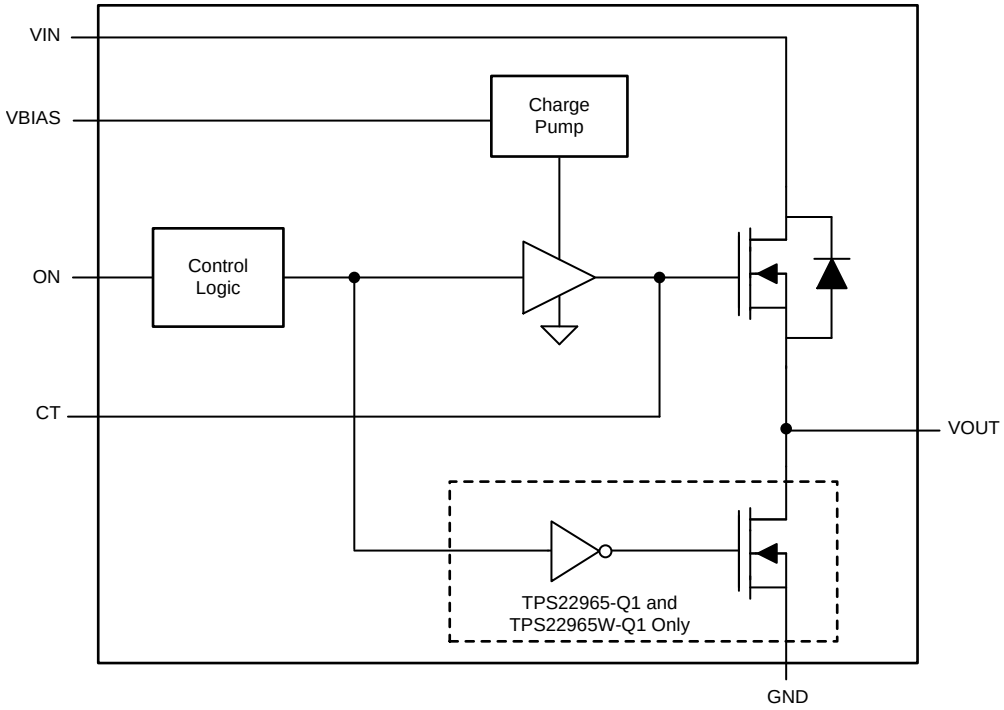


Figure 12. TPS22965-Q1 Functional Block Diagram

The TPS22965-Q1 device can operate over an input range of 0.8 V to 5.5 V and can support up to 4 A of continuous current. Furthermore, the IC offers a configurable VOUT rise time to limit inrush current. The TPS22965-Q1 is AEC-Q100 qualified and can operate from –40°C to 125°C or –40°C to 105°C depending on the desired package.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 System Design Theory Introduction

The TIDA-01425 is designed to demonstrate the performance of the J6Entry processor along with the various CAN and Ethernet PHYs in an automotive gateway application. The subsystem is designed to use both the CAN and Ethernet PHYs to receive and send data at 1 Mb/s and 100 Mb/s, respectively. Therefore, if a CAN PHY receives data then the processor has the capability of transmitting the exact same data from any PHY, whether Ethernet or CAN, without any errors. The same process works for data received through the Ethernet PHYs.

The TIDA-01425 reference design is designed to operate off a typical automotive battery and withstand or operate through automotive situations such as cold crank, load dump, jump start, and reverse battery. Furthermore, various components are utilized to help meet these conditions and reduce EMI. All components within the design are automotive Q-100 qualified. To ensure good performance, a well designed printed-circuit board (PCB) layout is crucial to functionality along with software to validate the processor communications to and from the Ethernet and CAN PHYs.

3.2 Communications

3.2.1 DRA710 J6Entry Processor

The J6Entry processor has been chosen due to the inclusion of Ethernet and the greater processing power and memory requirements entailed. As a member of a scalable family, the DRA710 J6Entry processor is an excellent starting point for stand-alone and integrated gateways. Both Linux and TI Real-Time Operating System (RTOS) drivers are available to speed up software development.

The J6Entry DRA710 processor has an internal gigabit Ethernet switch with three ports: one for the processor and two for external Ethernet PHYs. These Ethernet ports are capable of MII, RMII, GMII, and RGMII communication and are used in this design to interface with the DP83TC811R-Q1 and DP83848Q-Q1 Ethernet PHYs. The processor also has two CAN ports with CAN 2.0B protocol, which are used to interface with the two TCAN1042-Q1 PHYs. QSPI flash memory is used to allow a faster boot time, and 2GB of DDR are included with speeds up to DDR-1333 (667 MHz). Cypress S25FL256S SPI flash memory is used for the QSPI memory. The S25FL256S memory is 32MB and is automotive AEC-Q100 grade-1 qualified. For the DDR3L, Micron MT41K64M16TW-107 AAT:J devices were selected. The Micron MT41K64MTW-107 AAT:J are 1-Gb devices and are automotive AEC-Q100 qualified. Lastly, the processor runs off of a 20-MHz system clock, which is supplied from the CDCE913-Q1 device.

3.2.2 Ethernet

The DP83TC811R-Q1 100BASE-T1 compliant Ethernet PHY has been chosen to support IEEE 802.3bw Ethernet communications. The PHY is powered by 3.3 V and the configurable IO voltage is set to 3.3 V. Figure 13 shows the DP83TC811R-Q1 schematic.

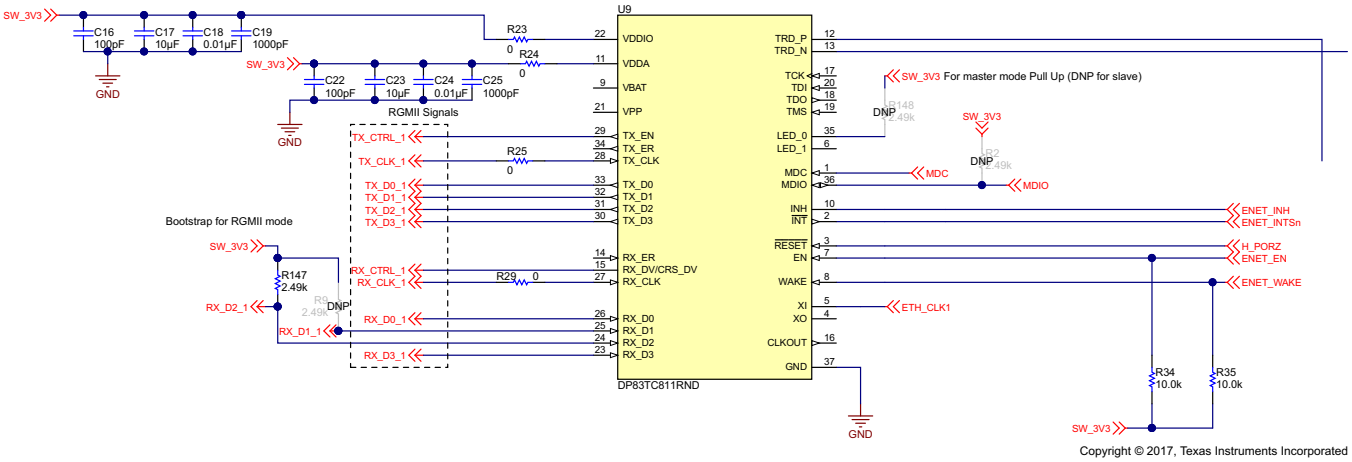


Figure 13. DP83TC811R-Q1 100BASE-T1 Ethernet PHY Schematic

The 3.3 V is supplied from the LM53625-Q1 through the load switch (TPS22965-Q1). RGMII MAC interface is used for communication to the J6Entry processor at 100 Mb/s. The 25-MHz reference clock for the RGMII interface is provided by the CDCE913-Q1 clock synthesizer. Resistors R9, R147, and R148 are boot-strap resistors; Resistor R9 allows for RGMII TX and RX shift mode (if desired, not populated on this design), R147 for setting the device into RGMII mode, and R148 for establishing master mode if it is desired (not populated). Figure 14 shows the DP83TC811R-Q1 with the TE MATEnet jack schematic.

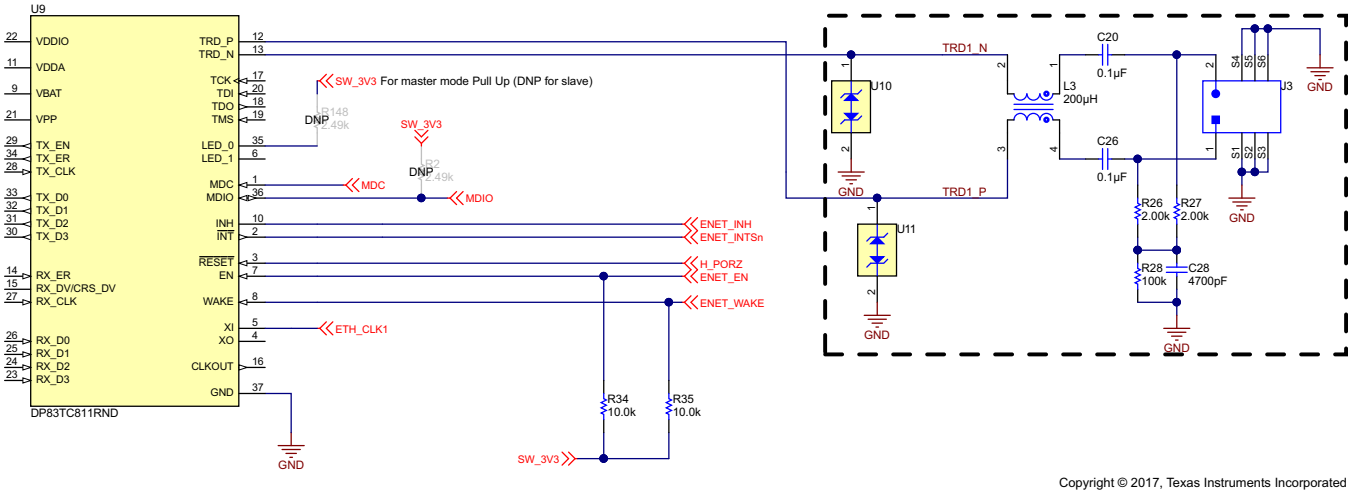


Figure 14. DP83TC811R-Q1 Connector Schematic

The media dependent interface (MDI) pins of the device connect to the TE MATEnet jack J3. U10 and U11 provide electrostatic discharge (ESD) protection and the common-mode chock L3 adds common-mode noise filtering. The common-mode choke L3 is selected based on the data sheet recommendation and because it meets the IEEE standards for a 100BASE-T1 choke. The common-mode choke must meet the specifications listed in the following Table 2.

Table 2. CMC Electrical Specifications

These specifications are based off the IEEE 802.3bw common-mode choke standards. Capacitors C20 and C26 are used for AC coupling and the components R26, R27, R28, and C28 provide termination to match impedances and improve signal integrity.

The DP83848Q-Q1 100BASE-TX compliant Ethernet PHY setup is very similar to the DP83TC811R-Q1. The device is powered by 3.3 V and the IO voltage is also set to 3.3 V. Figure 15 shows the schematic.

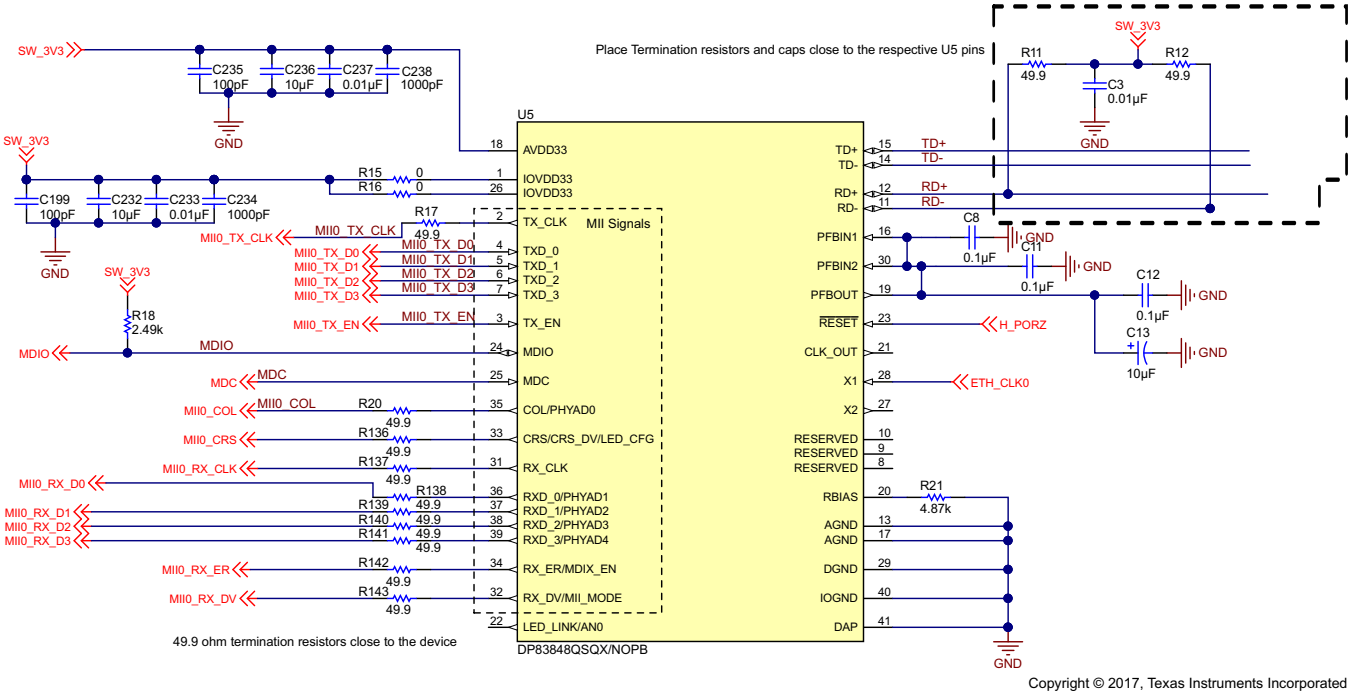


Figure 15. DP83848-Q1 100BASE-TX Ethernet PHY Schematic

The DP83848Q-Q1 PHY uses MII communication to the MAC. This type of communication is selected because the PHY can only communicate either MII or RMII to the MAC; RMII is not necessary for this design. The PHY receives a 25-MHz input clock from the CDCE913-Q1. 50-Ω termination resistors are connected to the MII pins for impedance matching to help reduce noise. Figure 16 shows the RJ45 connector schematic.

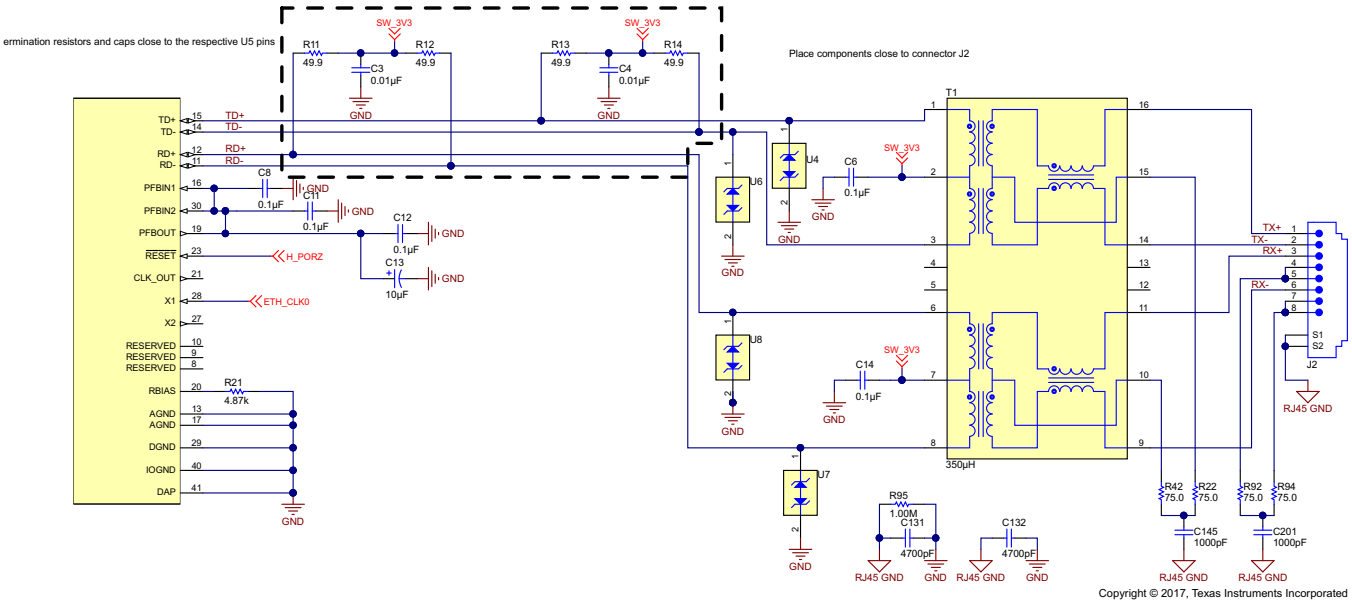


Figure 16. DP83848-Q1 Connector Schematic

Termination resistors R11, R12, R13, and R14 are recommended on the MDI lines (TX+, TX–, RX+, and RX–) for impedance matching along with bypass capacitors C3 and C4. U8, U7, U6, and U4 provide ESD protection. T1 is a transformer and common-mode choke device. The transformer DC isolates the MDI signals to the PHY from the MDI signals on the cable. The center taps on pins 2 and 7 bias the incoming signals to the proper voltage level for the PHY. "Bob Smith" termination through 75-Ω resistors and 1000-pF caps help to reduce noise from common-mode current flows and reduce susceptibility to additional noise from unused wire pairs on the jack. J2 is a shielded RJ-45 jack to help improve EMI performance. R95, C131, and C132 connect the RJ-45 chassis ground to the system ground. The capacitors C131 and C132 help filter any high-frequency signals from the chassis ground to the system ground. R95 is a bleeder resistor that discharges the capacitors C131 and C132 to keep the chassis ground from floating at a higher potential.

3.2.3 CAN PHYs

The TCAN1042-Q1 CAN PHYs are selected because the gateway must communicate to various CAN busses within a vehicle. The devices are a great fit for a gateway because they are AEC-Q100 qualified and they meet the ISO 11898-2 physical layer standards. The PHYs are powered by 5 V from the TPS61240-Q1 device. IO voltage for the devices are set to 3.3 V. This voltage is provided by the LM53625-Q1 device but is switched on or off by the load switch (TPS22965-Q1) similar to the Ethernet PHYs. Figure 17 shows the TCAN1042-Q1 schematic.

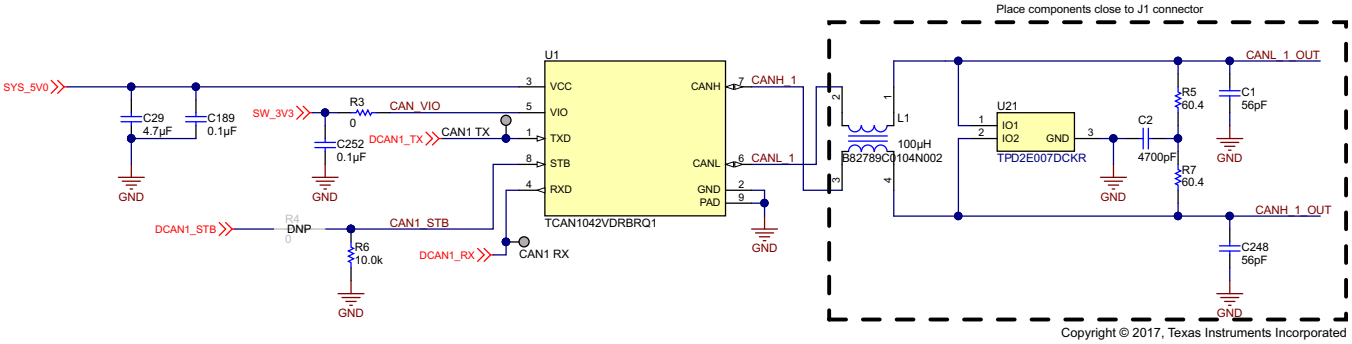


Figure 17. TCAN1042-Q1 CAN PHY Schematic

The standby pin (pin 8) is not used in this design but the option is available by placing a 0-Ω resistor on the board. The L1 common-mode chock provides common-mode noise filtering and C1 and C248 provide filtering, too. U21 provides ESD protection with R5, R7, and C2 improving impedance matching. A D-Sub 9 connecter is chosen to simplify connecting to the CAN PHYs.

3.2.4 Clock

The CDCE913-Q1 clock synthesizer is required to provide a reference clock for the DRA710 processor and the two Ethernet PHYs. The device has the capability of outputting three independent clocks from a single crystal. This feature saves board space and cost by reducing the amount of crystals required. Figure 18 shows the CDCE913-Q1 schematic.

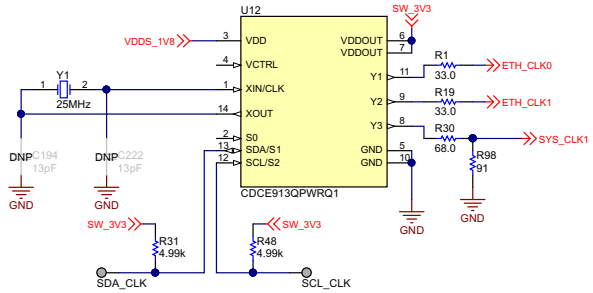


Figure 18. CDCE913-Q1 Clock Synthesizer Schematic

The CDCE913-Q1 is powered from the 1.8-V rail of the power management integrated circuit (PMIC). A 25-MHz crystal is selected to simplify the programing of the devices because of the demand for 25 MHz from both Ethernet PHYs. The clock synthesizer provides one 20-MHz clock signal and two 25-MHz clock signals to the DRA710 processor, DP83TC811R-Q1 Ethernet PHY, and the DP83848Q-Q1 Ethernet PHY, respectively. The device is preprogrammed using the CDCE949 family EEPROM programming board to create the 20-MHz clock for the J6Entry processor and the 25-MHz clocks for the Ethernet PHYs. The output clock supply voltage pin VDDOUT is tied to 3.3 V off the switched 3.3-V rail. One important task is to make sure the slew rate established by the load switch is fast enough to meet the J6Entry power-on sequence; because, if not, the clock outputs may not reach the full 3.3 V and are therefore not detectable by the processor during power-on sequencing. The 20-MHz clock (SYS_CLK1) must be at the 3.3-V output after all voltage rails have been powered ON. A voltage divider is also required on the J6Entry 20-MHz clock because the processor requires a 1.8-V clock and not 3.3 V like the DP83848Q-Q1 Ethernet PHY. The voltage divider resistors are selected so that, looking into the driver, the impedance would be about 50 Ω (47.64 Ω in this case). The CDCE913-Q1 driver impedance is approximately 32 Ω; therefore, using a 68-Ω series resistor gives about 100 Ω parallel with 91 Ω. Instead of using 100 Ω for the shunt resistor to make a perfect 50-Ω impedance, 91 Ω is selected to keep the voltage divider closer to 1.8 V. If a 68-Ω series and 100-Ω shunt resistive divider are used instead, the voltage is about 1.96 V instead of 1.88 V using the 91-Ω shunt resistor. The clock outputs Y1 and Y2 have 33-Ω termination resistors to match impedances and reduce reflections. I^2C pads are on the board just in case the CDCE913-Q1 preprogramming requires adjustment. Any desired adjustments require an external MCU.

3.3 Power

The system power is separated into two stages with protection devices and filtering before the first stage. The first power stage for the TIDA-01425 is a wide-voltage input buck LM53625-Q1 that provides 3.3 V to the system. Overall, the system operational input voltage minimum is reduced by using a wide V_{IN} 3.3-V output buck, which allows the system to operate in low-voltage supply situations such as cold crank. After the buck there are several different power supplies including the TPS61240-Q1 boost converter, the LP873220-Q1 PMIC, the LP87332D-Q1 PMIC, and the TPS51200-Q1 DDR termination regulator. A load switch is also necessary to prevent any components that communicate to the processor from powering on before the processor is initialized. The TPS61240-Q1 boost provides 5 V for the CAN PHYs in the system, both the LP873220-Q1 and LP87332D-Q1 provide all necessary power rails to the processor, and the TPS51200-Q1 supplies the DDR termination voltage and voltage reference for the processor.

3.3.1 Protection

Two transient-voltage-suppression (TVS) diodes and the LM74610-Q1 are used in the design enabling the system to survive reverse battery connection and transient spikes. Figure 19 shows the system protection.

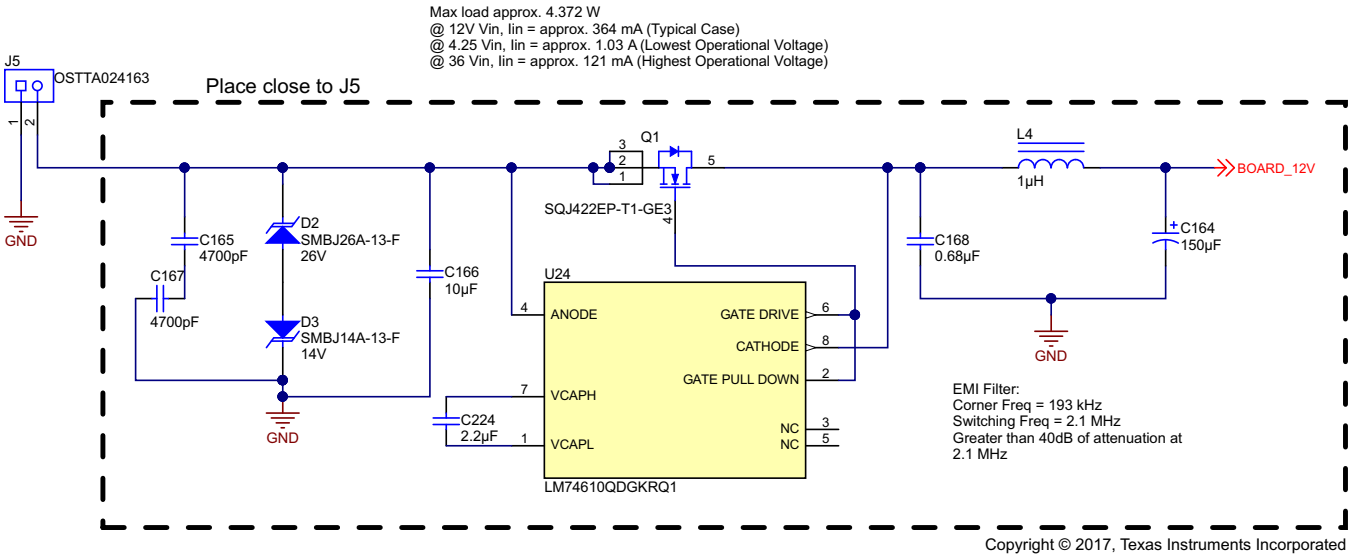


Figure 19. LM74610-Q1 Smart Diode Schematic

Diodes D2 and D3 are TVS diodes which are designed to clamp any unexpected voltage spikes that may occur during operation. The TVS diodes act similar to Zener diodes, reaching an avalanche at a specific breakdown voltage. D2 begins to clamp around 26 V or just over a double battery condition (jump start). D2 clamps load dump voltages with the diode fully clamped around 34 V, which is just under the max operational voltage of the LM53625-Q1 device at 36 V. D3 clamps all negative voltages greater than the battery voltage. Transients larger than 14 V are blocked from the system, which prevents any shorts during a reverse-battery condition. Both diodes have a max peak pulse power dissipation of 600 W. Table 3 shows these parameters.

Table 3. TVS Diode Specifications

DIODE PART NUMBER	REVERSE STANDOFF VOLTAGE	BREAKDOWN VOLTAGE MIN	BREAKDOWN VOLTAGE MAX	MAX CLAMPING VOLTAGE
D2: SMBJ26A	26.0 V	28.9 V	33.2 V	42.1 V
D3: SMBJ14A	14.0 V	15.6 V	17.9 V	23.2 V

The LM74610-Q1 along with the MOSFET SQJ422EP are used to emulate an ideal diode with the LM74610-Q1 providing fast response in the case of reverse polarity. Another benefit of the smart diode is that the drop across the MOSFET is much smaller than the drop across a diode. This benefit allows the wide V_{IN} buck to operate much closer to its minimum input voltage (and thus lower the operating voltage of the entire system) which is very helpful in situations such as cold crank where the battery voltage can drop down to as low as 3.5 V. The SQJ412EP MOSFET is selected based on the LM74610-Q1 data sheet. Table 4 shows some of the key parameters.

Table 4. Smart Diode FET Specifications

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
I_D	Drain-to-source current	—	—	75	A
V_{DS}	Drain-to-source voltage	—	—	40	V
$V_{GS(th)}$	Gate-to-source voltage	1.5	2.0	2.5	V
$R_{DS(on)}$	Drain-to-source on resistance at V_{GS} = 4.5 V	—	4.3	—	mΩ

The I_D current must be able to support the max load of approximately 1.2 A and have a V_{GS} of less than 3 V. A small $R_{DS(on)}$ is desired to reduce the amount of voltage drop across the MOSFET.

3.3.2 Input Filter

EMI is an important factor in designing automotive systems or subsystems. An EMI filter has been designed to help attenuate any noise from the first power stage switch mode power supply to help reduce the amount of EMI from the TIDA-01425 reference design. Figure 20 shows the filter.

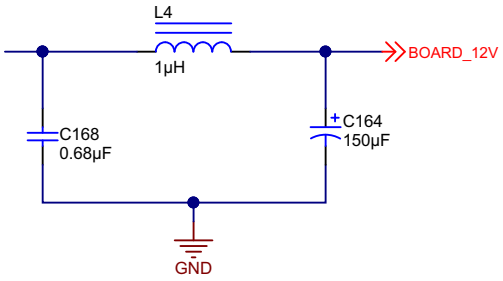


Figure 20. EMI Filter Schematic

The filter actually works from right to left filtering the battery from noise generated by the system. The filter is designed to have an attenuation of 40 dB at 2.1 MHz; 2.1 MHz is the switching frequency of the first stage buck (LM53625-Q1). Equation 1 is used to find the value of capacitor C168:

$$2\pi f = \frac{1}{\sqrt{LC}} \tag{1}$$

where,

- C = C168.

The inductor is selected as 1 uH to save board space and to ensure that a common inductor value is used. The corner frequency is 210 kHz based off the desired 40-dB attenuation. The calculated value of C168 is 0.574 µF, so a 0.68-µF capacitor is selected. Using a larger 0.68-µF capacitor allows for even greater than 40-dB attenuation while still using a realistic value. Capacitor C167 is selected based off of Equation 2 and Equation 3, where C164 = C_d and C_{in} is the equivalent capacitance on the input of the LM53625-Q1 or 29.4 µF.

$$C_d \geq 4C_{in} \tag{2}$$

$$ESR_d \approx \sqrt{\frac{L_f}{C_{in}}} \tag{3}$$

From Equation 2, C_d must be greater than 117 µF or about 120 µF. Using Equation 3 is necessary to decide the amount of equivalent series resistance (ESR) required from capacitor C164. The ESR of this capacitor is important to reduce the peak output impedance of the filter at the cutoff frequency. The calculated ESR is 0.1844 Ω. Based on the results of these two equation, capacitor C164 is selected with a value of 150 µF and an ESR of 0.18 Ω. The final filter has a corner frequency of 193 kHz, which improves the attenuation to approximately 41.47 dB at the switching frequency (2.1 MHz).

3.3.3 First Power Stage

The first power stage allows for the system to operate at a low battery voltage input of an estimated 4.27 V by stepping the voltage down from VBATT (12 V to 14 V typical) to 3.3 V. The LM53625-Q1 device is connected to the battery voltage directly after the circuit protection and EMI filter. The system is estimated to operate at about 4.372 W based off the J6Entry power estimator spreadsheet and all the specified, maximum operational power ratings of the other components. With the LM53625-Q1 device operating at an output voltage of 3.3 V, the system draws about 1.325 A from the buck, which is much less than its max output current of 2.5 A. Also, based off the estimated power, the resulting maximum current from the battery is approximately 1.023 A with the assumption of 100% efficiency on the buck. Figure 21 shows the LM53625-Q1 schematic.

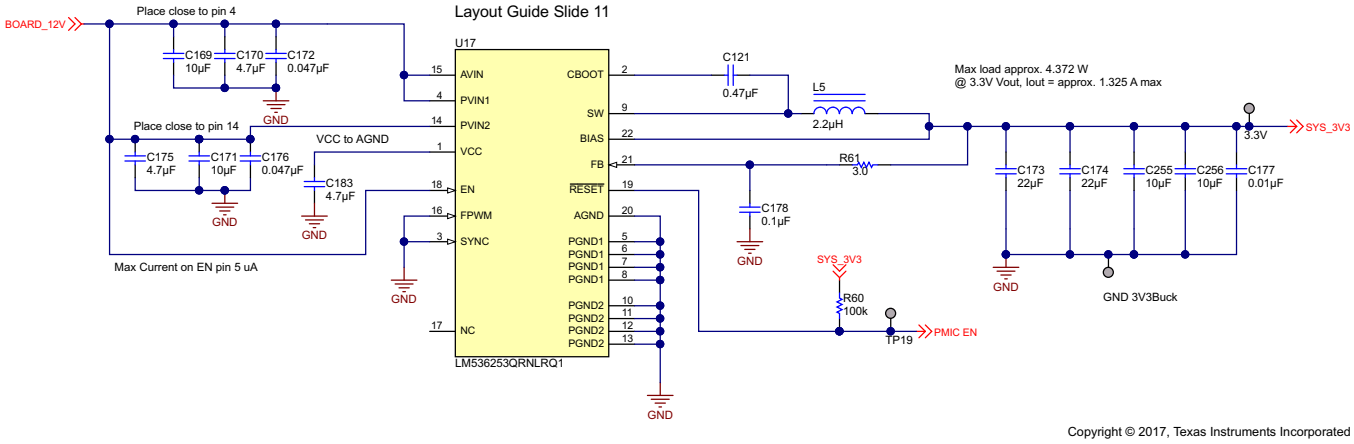


Figure 21. LM53625-Q1 3.3-V Buck Schematic

All components for the LM53625-Q1 have been selected based off data sheet recommendations, including the output capacitance and inductor. The total output capacitance is split between four capacitors to optimize the layout. An important aspect of this design is the use of the RESET pin (power good) to act as an enable for the system. When the RESET pin is high (output voltage is 95% of the expected voltage), the PMICs that power the processor are enabled and power-up sequencing for the processor begins. If the output of the LM53625-Q1 drops below 95% of the output voltage then the RESET pin falls to a logical low and the processor is reset. Furthermore, the RESET pin goes low if the output voltage reaches 107% of the expected level and goes high when the level drops back to or below 106%. One important thing to note is that, in a typical automotive gateway, another MCU is present to enable the PMICs, thus replacing the power good signal from the first power stage. For this design, there is no other controller to enable the system.

3.3.4 Second Power Stage

The second power stage includes the TPS61240-Q1 boost converter, the LP87332D-Q1 and LP873220-Q1 PMICs, the TPS22965-Q1 load switch, and the TPS51200-Q1 DDR termination regulator. The TPS61240 provides the necessary 5 V to the system for both the PMICs, load switch, and CAN PHYs. The LP87332D-Q1, LP873220-Q1, and the TPS22965-Q1 devices are necessary to provide the proper sequencing and voltages to the J6Entry processor. The load switch is required to switch the 3.3 V from the first-stage power supply (LM53625-Q1) in sequence with the PMICs. This sequence of operation helps prevent any devices powered by the 3.3 V from powering on unexpectedly for short bursts of time and also properly sequences when the 3.3 V is switched to the J6Entry VDDSHVx rails. Finally, the TPS51200-Q1 device is used to provide the proper termination voltage and reference voltage for the DDR3L memory and the J6Entry processor.

3.3.4.1 5-V Rail TPS61240-Q1

The TPS61240-Q1 boost IC is implemented to provide the 5-V rail in the design. The 5-V output from the boost is connected to power the CAN PHYs, LP87332D-Q1 PMIC low-dropout linear-regulator (LDO) rails, and the load switch. This setup may seem like a lot of devices are on the 5-V rail and thus draw a lot of power; however, the devices do not dissipate more than an estimated 105 mW. The CAN PHYs typically dissipate 52 mW each (104 mW total with both CAN PHYs). The LP87332D-Q1 requires a voltage greater than 3.3 V for each of the LDO outputs on the device (LDOs are 3.3-V outputs). In this design, the LDO outputs from the LP87332D-Q1 are not to be used (little to no current drawn) but the voltages are still necessary for the J6Entry processor. One important factor to note is that if the LDOs are used, a different 5-V power supply may be required based on the power estimation of the LDO rails. Lastly, the TPS22965-Q1 requires the 5-V rail to bias the charge pump within the device, which does not draw more than a few mA of current. The TPS61240-Q1 device can provide up to 2.25 W of power (450-mA max output current) and therefore provides the necessary power requirements for the 5-V rail in this application. Figure 22 shows the TPS61240-Q1 schematic. All discrete components for the device have been selected based off data sheet recommendations.

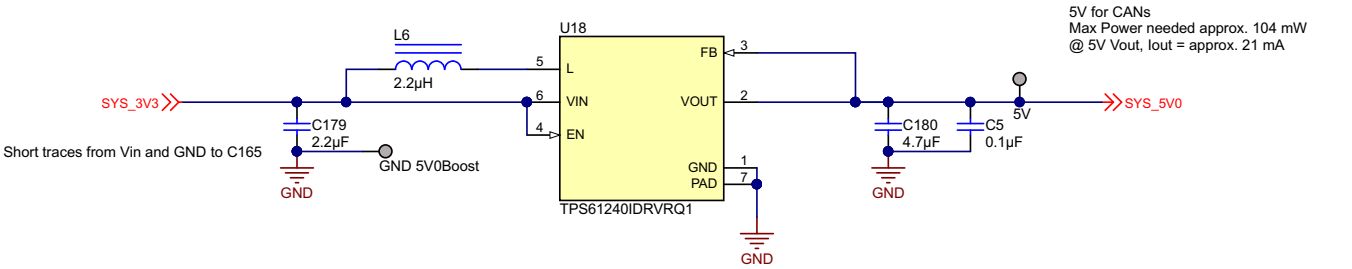


Figure 22. TPS61240-Q1 5-V Boost Schematic

3.3.4.2 PMICs LP873220-Q1 and LP87332D-Q1

The LP873220-Q1 and LP87332D-Q1 PMICs are critical in the design to power the J6Entry processor. The two-PMIC solution meets all of the J6Entry power-up and power-down sequencing requirements and also provides all eight voltage rails. Also, the J6Entry processor requires tight voltage ranges and low noise on some of its voltage rails to power on and operate correctly. Both LP87332D-Q1 and LP873220-Q1 utilize adaptive voltage scaling (AVS) on their outputs to meet the voltage rail requirements of the J6Entry and also save the total power consumption of the system. These devices are preprogrammed to power up and power down each voltage rail in the proper order. When powered on, the J6Entry can adjust the power level by communicating I^2C to the PMICs. One important thing to note is that a discrete power solution can cost more time and money to implement. Table 5 and Table 6 show the voltage domain power-on sequence and power-down sequence as named in the schematics that follow.

Table 5. J6Entry Power-On Sequence

ORDER	VOLTAGE DOMAIN J6ENTRY	VOLTAGE SOURCE	SOURCE VOLTAGE	SOURCE MAX CURRENT
1st	VDDS and VDDSHV11	LP873220 SMPS 0	1.8 V	1.5 A
2nd	VDA PLL	LP873220 LDO 0	1.8 V	300 mA
3rd	VDD DDR	LP873220 SMPS 1	1.35 V	2 A
4th	VDD CORE AVS	LP87332D SMPS 0	1.15 V	3 A
5th	VDD DSP AVS	LP87332D SMPS 1	1.06 V	3 A
6th	VDA PHY	LP873220 LDO 1	1.8 V	300 mA
7th	VDDSHVx (excluding VDDSHV11)	LP87332D open-collector enable for load switch (TPS22965-Q1)	3.3 V (from LM53625 switched through load switch)	2.5 A
8th	VDA USB	LP87332D LDO 1	3.3 V	300 mA
9th	VDDSHV8	LP87332D LDO 0 (not used)	1.8 V	Not used

Table 6. J6Entry Power-Down Sequence

ORDER	VOLTAGE DOMAIN J6ENTRY	VOLTAGE SOURCE
1st	VDDSHV8	LP87332D LDO 0 (not used)
2nd	VDA USB	LP87332D LDO 1
3rd	VDDSHVx (excluding VDDSHV11)	LP87332D open-collector enable for load switch (TPS22965-Q1)
4th	VDA PHY	LP873220 LDO 1
5th	VDD DSP AVS	LP87332D SMPS 1
6th	VDD CORE AVS	LP87332D SMPS 0
7th	VDD DDR	LP873220 SMPS 1
8th	VDA PLL	LP873220 LDO 0
9th	VDDS and VDDSHV11	LP873220 SMPS 0

Meeting these sequencing requirements is important for the processor to operate correctly. Note that the max current for each rail will not be met in this application. For more information on the voltage domains and the full sequencing requirements, see *DRA71x Infotainment Applications Processor* (SPRS960)[1].

The LP873220-Q1 provides power for the first three and sixth voltage rails, which are the VDDS (and VDDSHV11), VDA PLL, VDD DDR, and VDA PHY rails, respectively. Figure 23 shows the schematic for the LP873220-Q1.

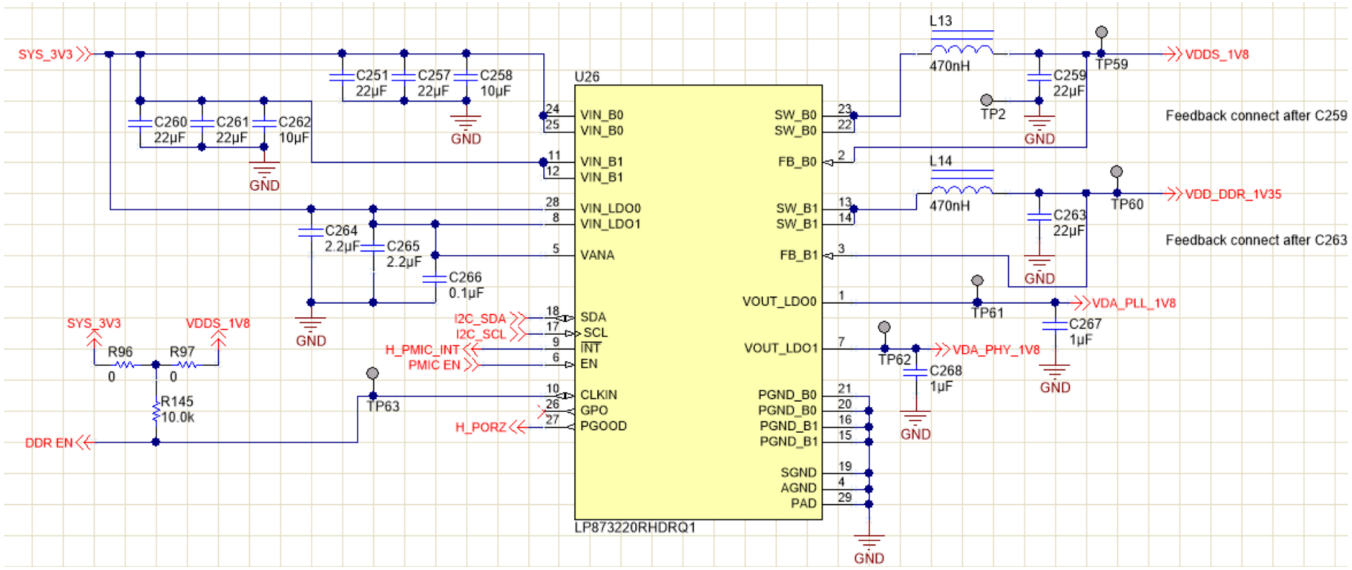


Figure 23. LP873220-Q1 Schematic

The PMIC has several digital IOs: INT, EN, DDR EN, and PORz are the four IOs necessary for operation. Every input and output is preprogramed to the device and therefore the name on the schematic, such as CLKIN, is not necessarily the function of the pin in this design. For more information on the possible configurations of the LP873220-Q1 digital IO pins, see *LP873220-Q1 Dual High-Current Buck Converters and Dual Linear Regulators* (SNVSAT3)[8]. The PMIC interrupt and PGOOD outputs connect to the processor and are both open-drain outputs (pullup resistors on the LP87332D-Q1 schematic). The INT pin is driven low if a fault or internal interrupt has occurred and returns to a high state when the interrupt has been cleared. The PGOOD output ties to the PGOOD output of the LP87332D-Q1 device and is connected to the power-on reset (PORz) pin of the processor. Therefore, if the power from any of the PMICs bucks are insufficient, the J6Entry will be reset. The EN pin is tied to the power good of the first-stage power supply LM53625-Q1 RESET (power good) output as well as the LP87332D-Q1 EN input pin. This RESET pin enables both PMICs when the LM53625-Q1 output is in the correct operating percentage of 3.3 V (see Section 3.3.3) and thus begins power-on sequencing. Lastly, the DDR EN output enables the

TPS51200-Q1 DDR termination regulator to power the DDR3L memory in the proper sequence that the processor requires. The option to pull the DDR EN output to 1.8 V or 3.3 V has been created just in case the 1.8 V is not quite enough voltage for the TPS51200-Q1 EN pin because it has a 1.7-V high-level input voltage threshold. Discrete components have been selected based off the LP873220-Q1 data sheet recommendations.

The LP87332D-Q1 PMIC is used to power the processor VDD CORE, VDD DSP, VDA USB and VDDSHV8 rails. The VDD CORE and VDD DSP are the most important rails of the processor and require the most power; because of this, the LP87332D-Q1 buck outputs are used because they can provide a maximum current of 3 A. The LP873220-Q1 buck outputs can only provide 2 A maximum. Figure 24 shows the LP87332D-Q1 schematic.

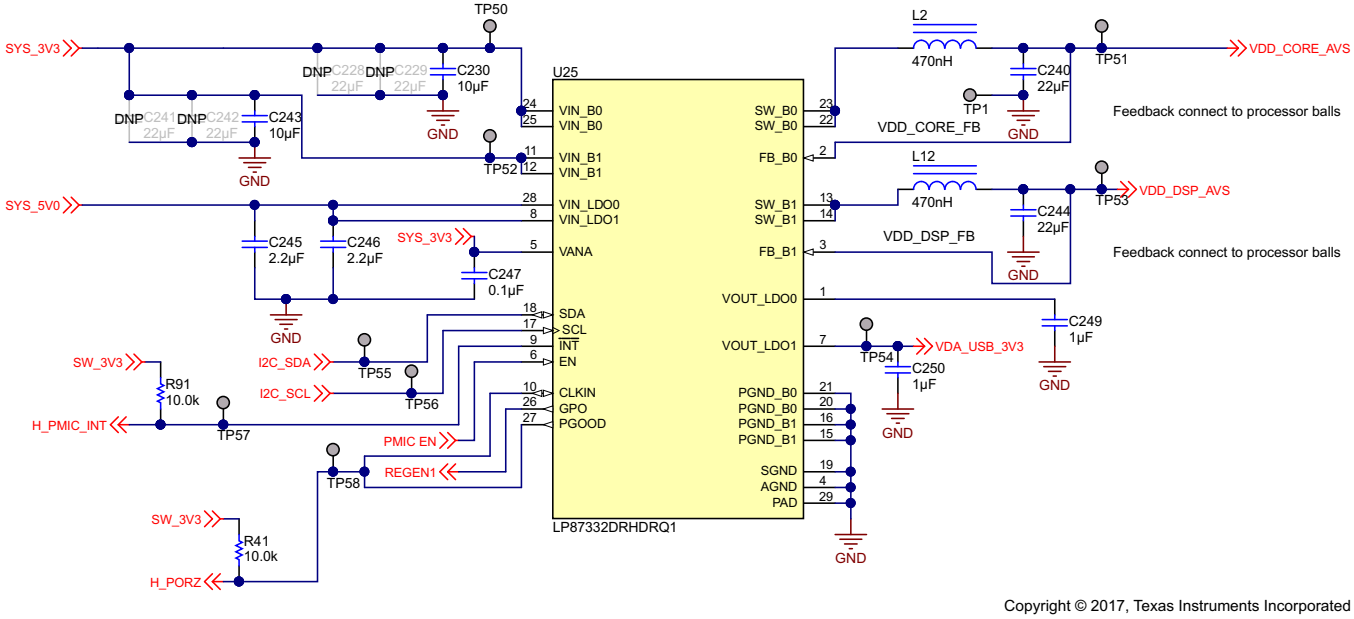


Figure 24. LP87332D-Q1 Schematic

The feedback for each buck rail must be connected close to the processor balls. This close connection allows for better regulation of the output voltages on the bucks, which is required due to the VDD CORE and VDD DSP voltage requirements shown in Table 7. The voltages for these rails are preliminary so the design can be modified in software to comply with future recommendations. The nominal voltage should be the target for VDD CORE and VDD DSP rails.

Table 7. J6Entry Voltage Domains Operating Points

DOMAIN	CONDITION	MIN	NOM	MAX
VDD CORE	BOOT (before AVS is enabled)	1.11 V	1.15 V	1.2 V
	After AVS is enabled	1.108 V	1.15 V	1.2 V
VDD DSP	BOOT (before AVS is enabled)	1.11 V	1.15 V	1.2 V
	After AVS is enabled	1.023 V	1.06 V	1.2 V

The LP87332D-Q1 schematic is almost the exact same as the LP873220-Q1 schematic except for a few differences. The LDO inputs for the LP87332D-Q1 require 5 V instead of 3.3 V (like the LP873220-Q1 LDOs) because they output 3.3 V. Also, instead of a DDR EN output, the LP87332D-Q1 has an EN for the TPS22965-Q1 load switch (REGEN1). This enable is required to ensure that the J6Entry rails that require 3.3 V are powered on in the correct sequence and also prevents any other devices such as the Ethernet PHYs from powering on before the processor CORE rails are ready. Figure 25 shows the TPS22965-Q1 load switch schematic.

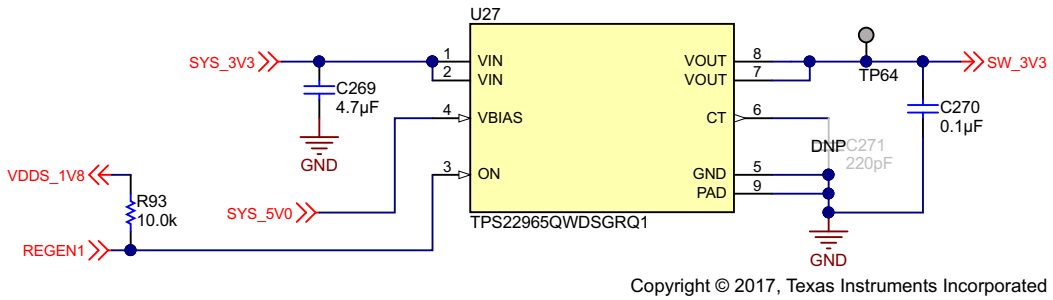


Figure 25. TPS22965-Q1 Load Switch

The TPS22965-Q1 has an adjustable slew rate based on the capacitance connected to pin 6 (CT pin) and GND. For this design, no capacitor is used because no slew is actually required. For capacitor values and there corresponding slew rates, see *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch* (SLVSCI3) [12]. The processor sequencing can be affected if too large of a skew rate is added to the 3.3-V switched rail. Lastly, 5 V is required for the VBIAS pin because of the load switch requirement which specfiies that V_{IN} is less than or equal to VBIAS.

3.3.4.3 TPS51200-Q1

The TPS51200-Q1 DDR termination regulator is necessary to provide a regulated 1.35 V and 0.675 V for DDR3L termination. Figure 26 shows the TPS51200-Q1 schematic.

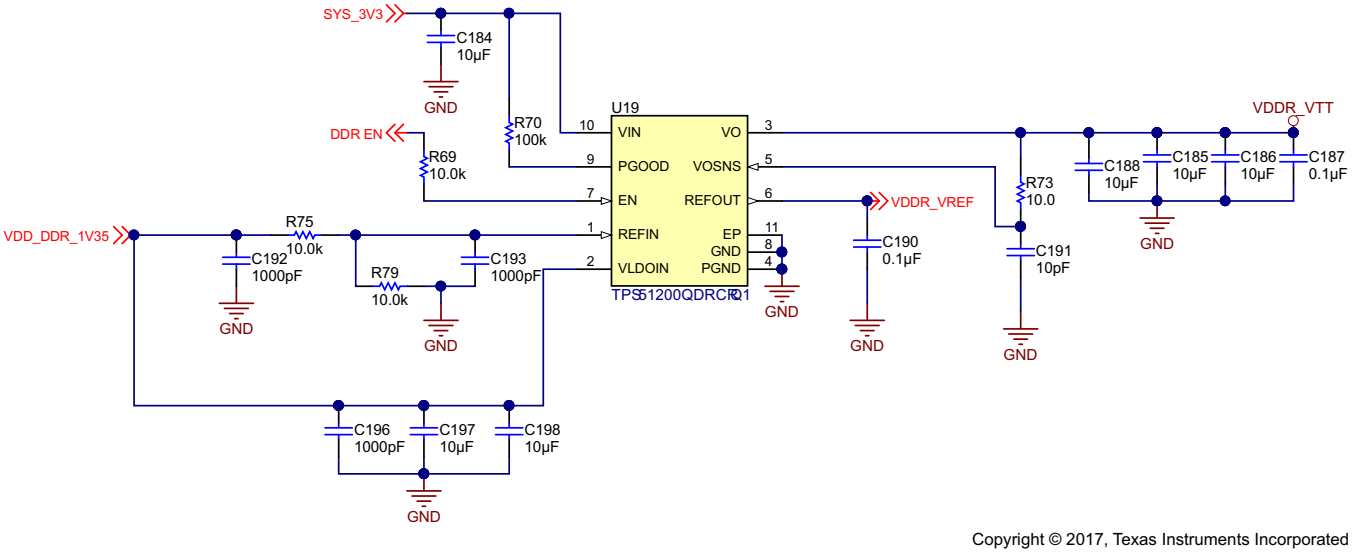


Figure 26. TPS51200-Q1 Schematic

The TPS51200-Q1 is powered by 3.3 V from the LM53625-Q1 device and is enabled by the LP873220-Q1 PMIC (DDR EN). The 1.35 V from the LP873220-Q1 device is divided in half using the 10k-Ω resistors R75 and R79 to obtain 0.675 V for the REFOUT voltage, which connects to the processor and also the termination resistors of the DDR3L memory. The 1.35 V at the input of the VLDOIN is also regulated to output 1.35 V for the termination resistors as well and provide the VDD voltage for the DDR3L memory. All components have been selected based on data sheet recommendations.

3.4 Software

The software application for the board was developed after verifying all the hardware. To verify the hardware, each communication PHY was programmed individually and put into loopback test modes to ensure that the PHYs were established correctly in hardware. Each test sent data from the processor to the PHY and back to the processor to make sure the PHYs could receive data form the processor as well as send data to the processor. The loopback tests were also run on a J6Eco EVM to verify that the software was operating correctly. After all PHYs were verified, the application was created to send data from a PC to the board through 100BASE-TX and have the same data loop through each CAN PHY and back to the PC (see Figure 27).

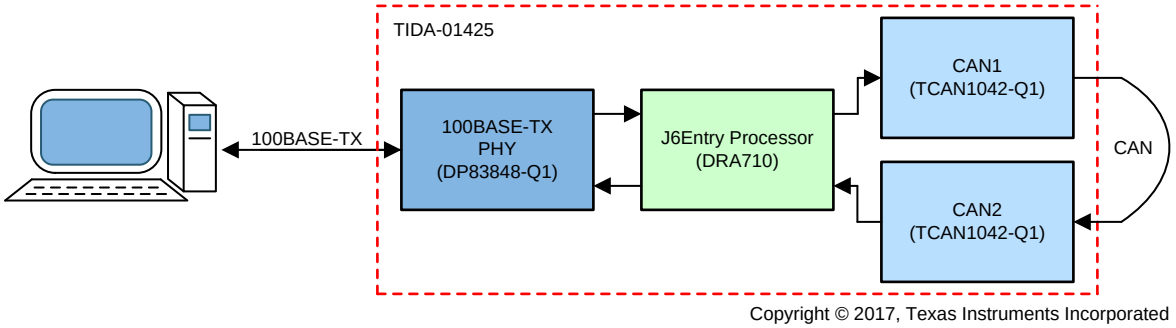


Figure 27. 100BASE-TX/CAN Loopback Block Diagram

This application is similar to an end user's application of a gateway communication through an OBD port to the system. Figure 28 shows the application flow chart.

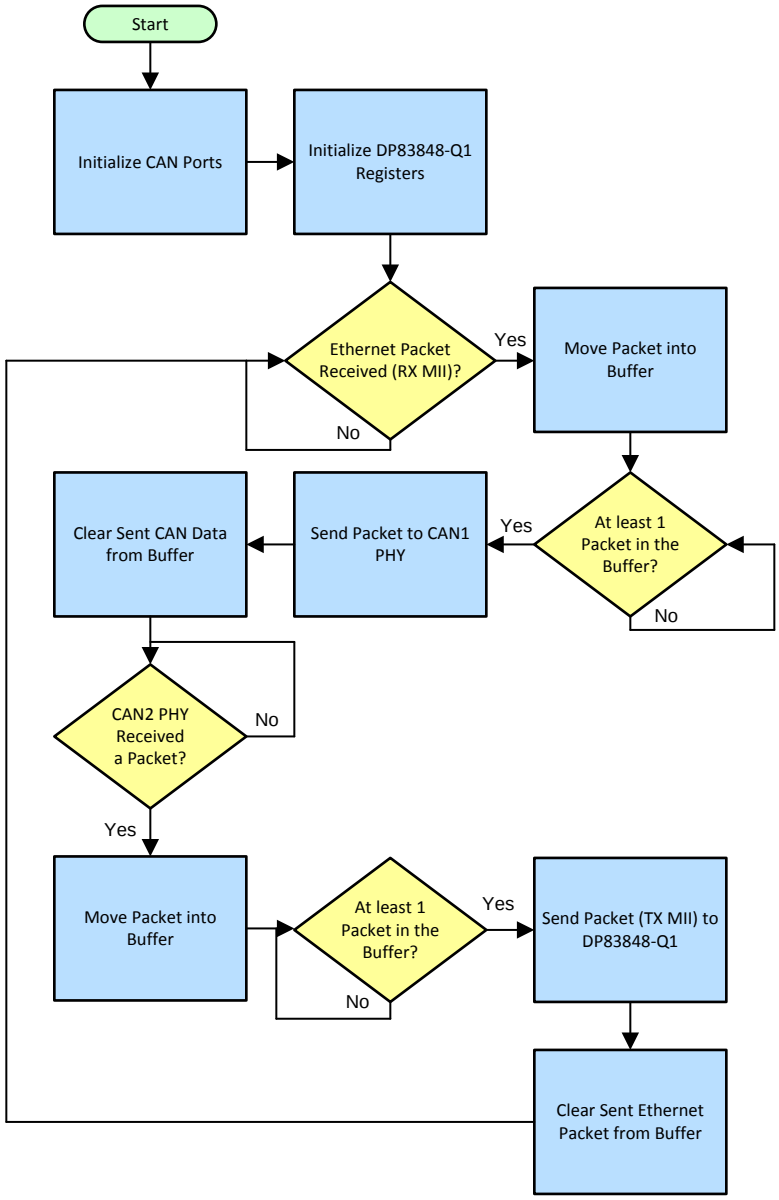


Figure 28. 100BASE-TX/CAN Loopback Flow Chart

First, the CAN port for the J6Entry must be configured correctly. Then the DP83848-Q1 registers are written to configure the PHY for 100BASE-TX communications using the MDIO bus. After the PHY has been configured, it waits to establish a link with another PHY. When the link has been established and data is transferred, the processor receives data on the MII lines (RX lines specifically). A buffer must be created for two reasons: First, 100BASE-TX protocol is much faster than CAN protocol. Data is received at 100 Mb/s through Ethernet and must be sent out at 1 Mb/s on the CAN bus. Second, Ethernet packets are much larger than CAN packets. The CAN driver that the J6Entry DRA710 utilizes can only send 8 bytes of data per packet at a time. Therefore, a buffer has been created to store data received from Ethernet until previous data can be transmitted on the CAN bus. When enough data is stored in the buffer, the data is sent to the first TCAN1042-Q1 PHY. Data is sent from the first CAN PHY to the second and received back at the processor. The same buffer is again used for the same reasons when sending data from the CAN to 100BASE-TX Ethernet, as previously discussed. Data can be continuously sent from a PC to the board with data constantly passing through each stage as shown in the previous Figure 28.

3.5 Testing and Results

The ultimate goal of the TIDA-01425 preprogramed software is to verify the various hardware components with one another in a gateway functionality, specifically the DRA710 J6Entry processor, DP83TC811R-Q1 100BASE-T1 PHY, DP83848-Q1 100BASE-TX PHY, and the two TCAN1042-Q1 CAN PHYs. After the hardware was verified, a gateway application was created to send data from a computer to the 100BASE-TX Ethernet PHY through both CAN PHYs and back to the computer. After the application was verified, further testing on system power was conducted by varying the input voltage from the minimum operating voltage to double battery voltage.

3.5.1 Test Setup

The TIDA-01425 board was powered with a 12-V supply with the PHYs connected as shown in Figure 29. A standard Ethernet cable was used to connect the PC to the gateway. The CAN nodes were connected together using the DE-9 connector on the board.

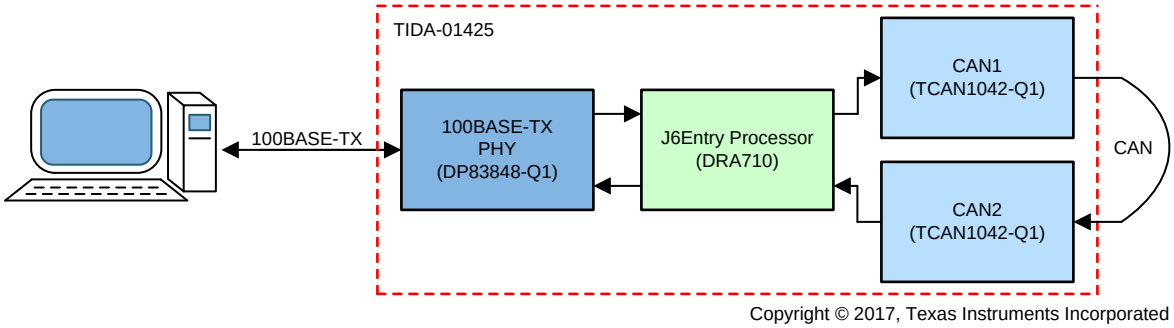


Figure 29. 100BASE-TX/CAN Loopback Block Diagram

Packets were continuously sent from the PC to the TIDA-01425 reference design through 100BASE-TX Ethernet using an application provided by the NDK driver. The application sends packets from a host PC to a designated IP address, waits to receive them back, and checks that the received packets are the same as the ones that were sent. The packets are received by the gateway design through 100BASE-TX, sent out through CAN1 to CAN2, and then sent back to the PC through 100BASE-TX Ethernet. All tests were run with the setup shown in Figure 30.

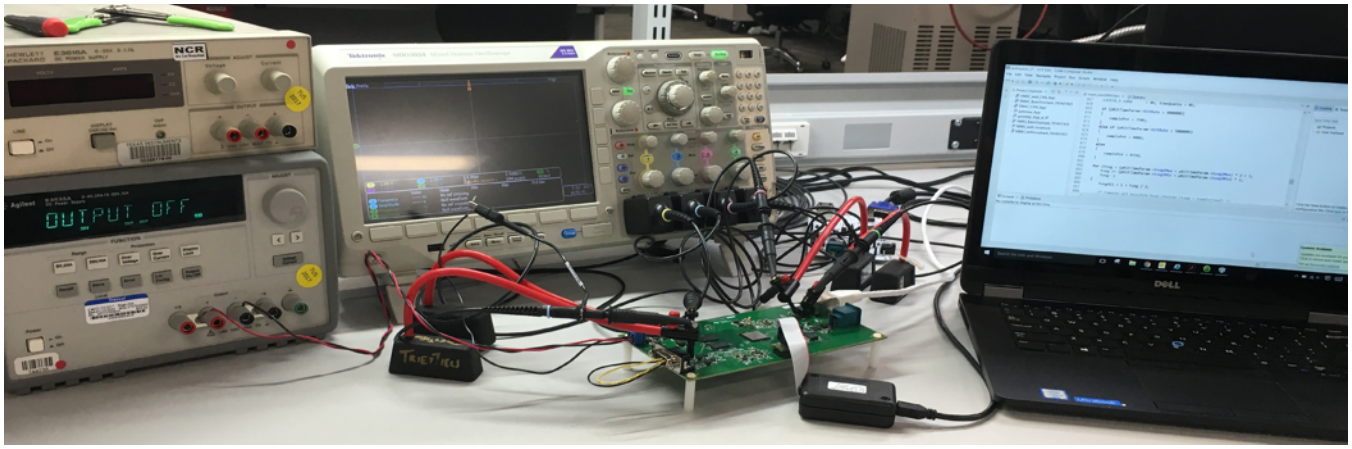


Figure 30. 100BASE-TX/CAN Loopback Test Setup

For the communications test, various data lines were probed to verify communications were up and running. The media dependent interface of the 100BASE-TX PHY was probed along with the CAN bus (see Figure 31).

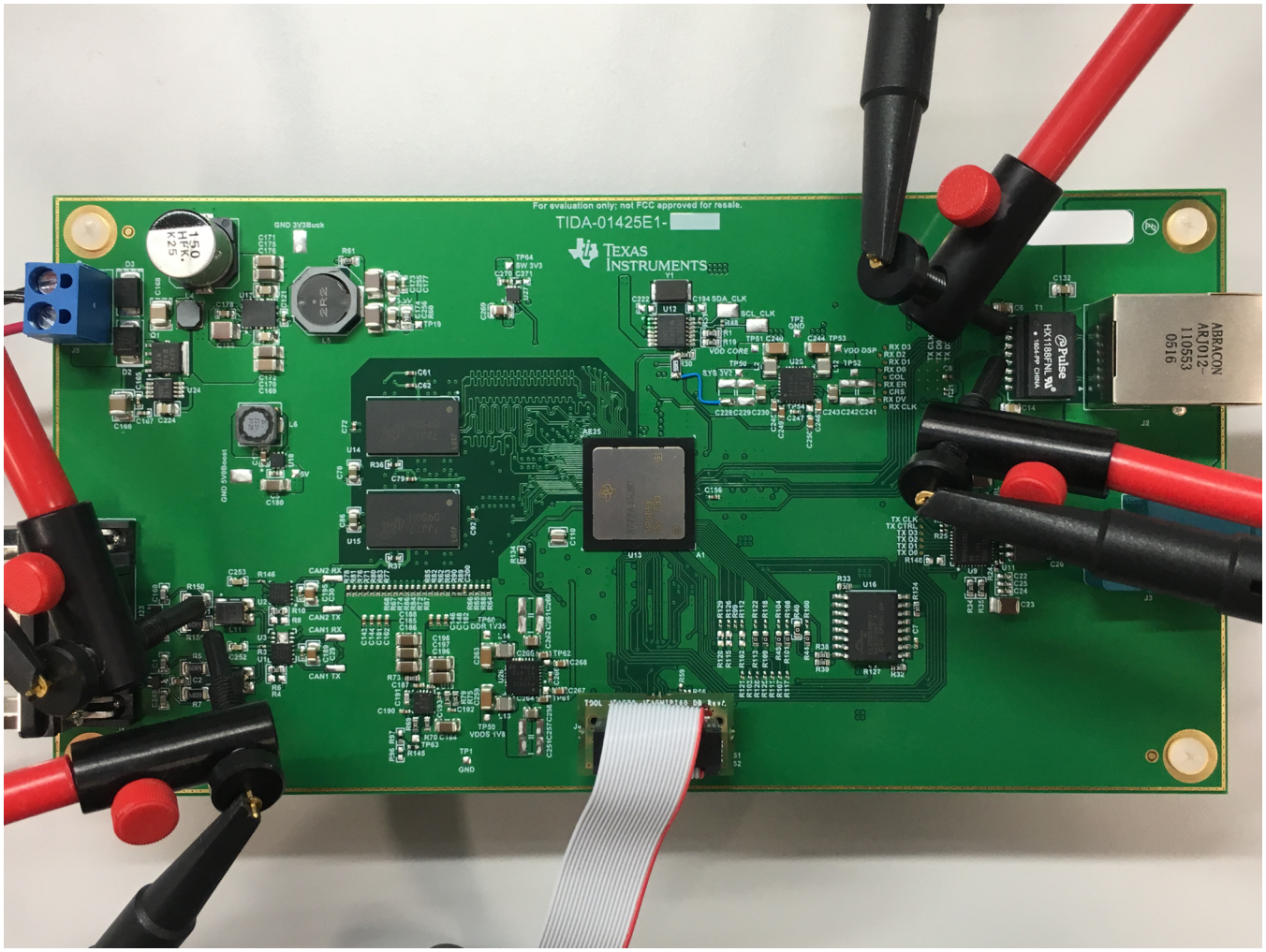


Figure 31. 100BASE-TX/CAN Loopback Probe Setup

Notice the small blue wire. This wire ties the shunt resistor to ground and is not required in the updated layout. The system has also been tested at various input voltages and reverse battery protection using a Fluke® multimeter. The different voltage rails of the TIDA-01425 reference design were measured to see how they change along with how the system power changed depending on the input voltage.

3.5.2 Test Results

There are several ways to verify that the packets are sent from the computer to the board and back to the computer. First, the oscilloscope is set to probe both the Ethernet MDI lines and the CAN bus. Second, the computer terminal (command prompt) displays when packets are sent and received correctly using an application in the NDK driver. Finally, if packets are being sent continuously and the CAN PHYs become disconnected or the Ethernet cable is disconnected, all communication is stopped and is visibly shown on both the oscilloscope and the computer terminal (command prompt) window. Figure 32 shows the 100BASE-TX Ethernet MDI data, Figure 33 shows the CAN Bus data line, and Figure 34 and Figure 35 show both the CAN and 100BASE-TX data. Figure 36 shows the command prompt window, which shows that packets have been sent as well as received.

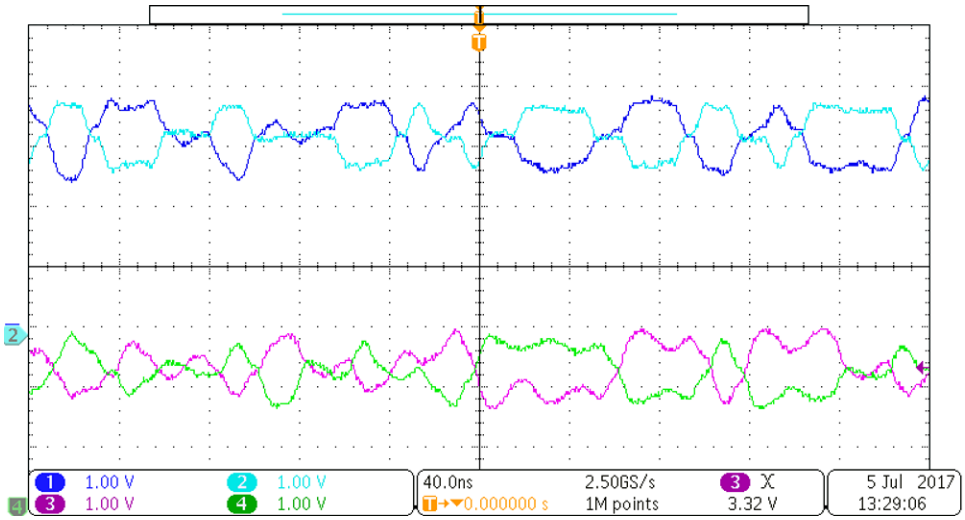


Figure 32. 100BASE-TX MDI Data

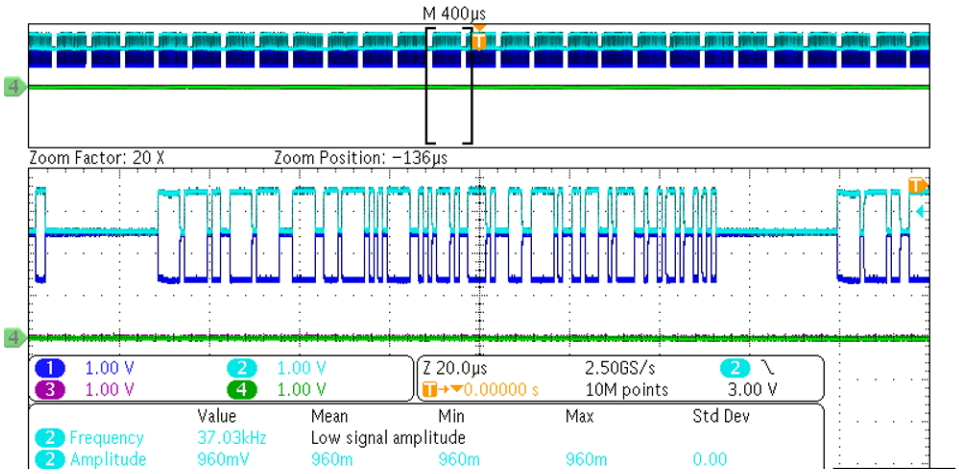


Figure 33. CAN Bus Data

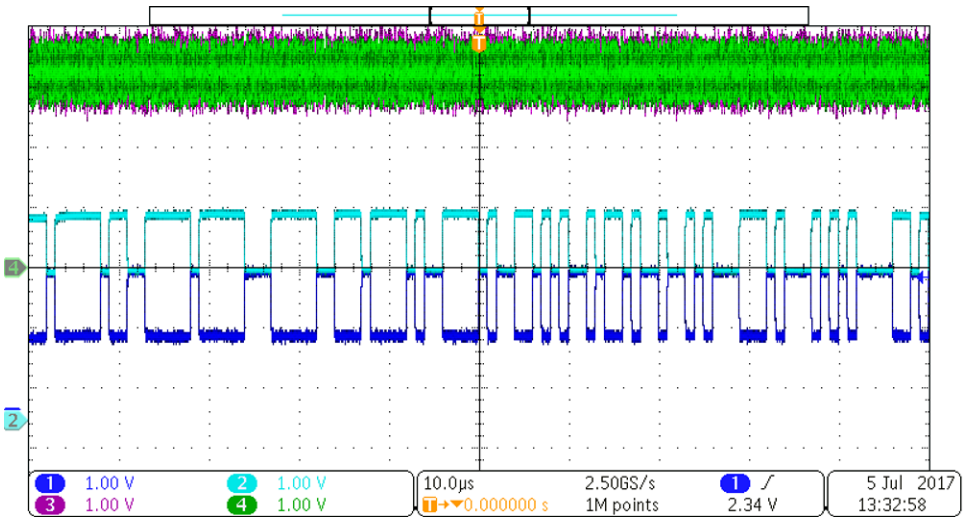


Figure 34. 100BASE-TX and CAN Bus Zoomed-in on CAN Data

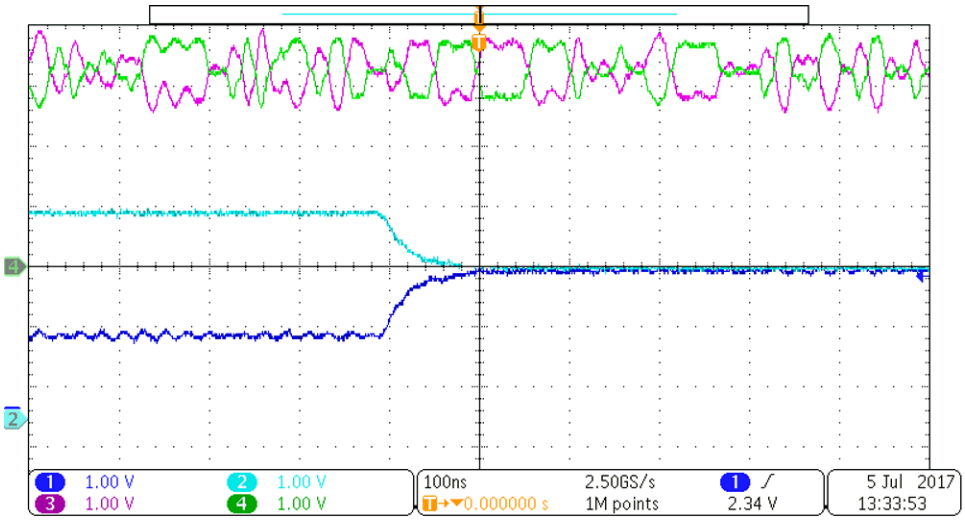


Figure 35. 100BASE-TX and CAN Bus Zoomed-in on Ethernet Data

```
C:\ti\ndk_2_25_01_11\packages\ti\ndk\winapps>echoc 192.168.1.4 1
1 Sending 6500 bytes ... receive ... verify ... passed
2 Sending 6500 bytes ... receive ... verify ... passed
3 Sending 6500 bytes ... receive ... verify ... passed
4 Sending 6500 bytes ... receive ... verify ... passed - 26000 bytes/s
5 Sending 6500 bytes ... receive ... verify ... passed - 32500 bytes/s
6 Sending 6500 bytes ... receive ... verify ... passed - 39000 bytes/s
7 Sending 6500 bytes ... receive ... verify ... passed - 45500 bytes/s
8 Sending 6500 bytes ... receive ... verify ... passed - 52000 bytes/s
9 Sending 6500 bytes ... receive ... verify ... passed - 58500 bytes/s
10 Sending 6500 bytes ... receive ... verify ... passed - 32500 bytes/s
11 Sending 6500 bytes ... receive ... verify ... passed - 35750 bytes/s
12 Sending 6500 bytes ... receive ... verify ... passed - 39000 bytes/s
13 Sending 6500 bytes ... receive ... verify ... passed - 42250 bytes/s
14 Sending 6500 bytes ... receive ... verify ... passed - 45500 bytes/s
15 Sending 6500 bytes ... receive ... verify ... passed - 48750 bytes/s
16 Sending 6500 bytes ... receive ... verify ... passed - 52000 bytes/s
17 Sending 6500 bytes ... receive ... verify ... passed - 36833 bytes/s
18 Sending 6500 bytes ... receive ... verify ... passed - 39000 bytes/s
19 Sending 6500 bytes ... receive ... verify ... passed - 41166 bytes/s
20 Sending 6500 bytes ... receive ... verify ... passed - 43333 bytes/s
21 Sending 6500 bytes ... receive ... verify ... passed - 45500 bytes/s
22 Sending 6500 bytes ... receive ... verify ... passed - 47666 bytes/s
23 Sending 6500 bytes ... receive ... verify ... passed - 49833 bytes/s
24 Sending 6500 bytes ... receive ... verify ... passed - 39000 bytes/s
25 Sending 6500 bytes ... receive ... verify ... passed - 40625 bytes/s
26 Sending 6500 bytes ... receive ... verify ... passed - 42250 bytes/s
27 Sending 6500 bytes ... receive ... verify ... passed - 43875 bytes/s
28 Sending 6500 bytes ... receive ... verify ... passed - 45500 bytes/s
```

Figure 36. 100BASE-TX/CAN Test Terminal

The previous figures show that communication from a PC to the TIDA-01425 gateway is achievable through 100BASE-TX Ethernet and CAN sending data in both directions. This application verifies that data can be shared through 100BASE-TX to CAN and vice versa.

The full operational input voltage was swept from 4.1 V to 24 V at 2-V intervals to look at the system power. The goal was to see how much power the TIDA-01425 dissipates depending on the input voltage (see Figure 37).

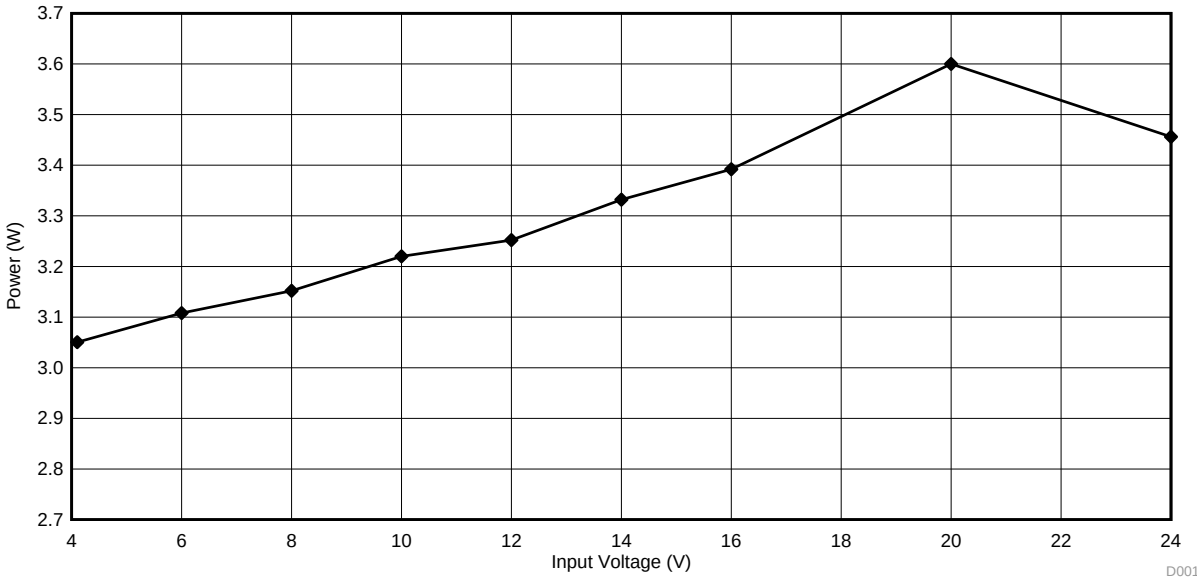


Figure 37. Power versus Input Voltage

The power dissipated by the design linearly increases as the voltage input increases. The TIDA-01425 continues to transmit and receive data at 4.1 V and 24 V. Figure 38 shows all the voltage rails on the TIDA-01425 from V_{IN} minimum, V_{IN} typical, and V_{IN} double battery.

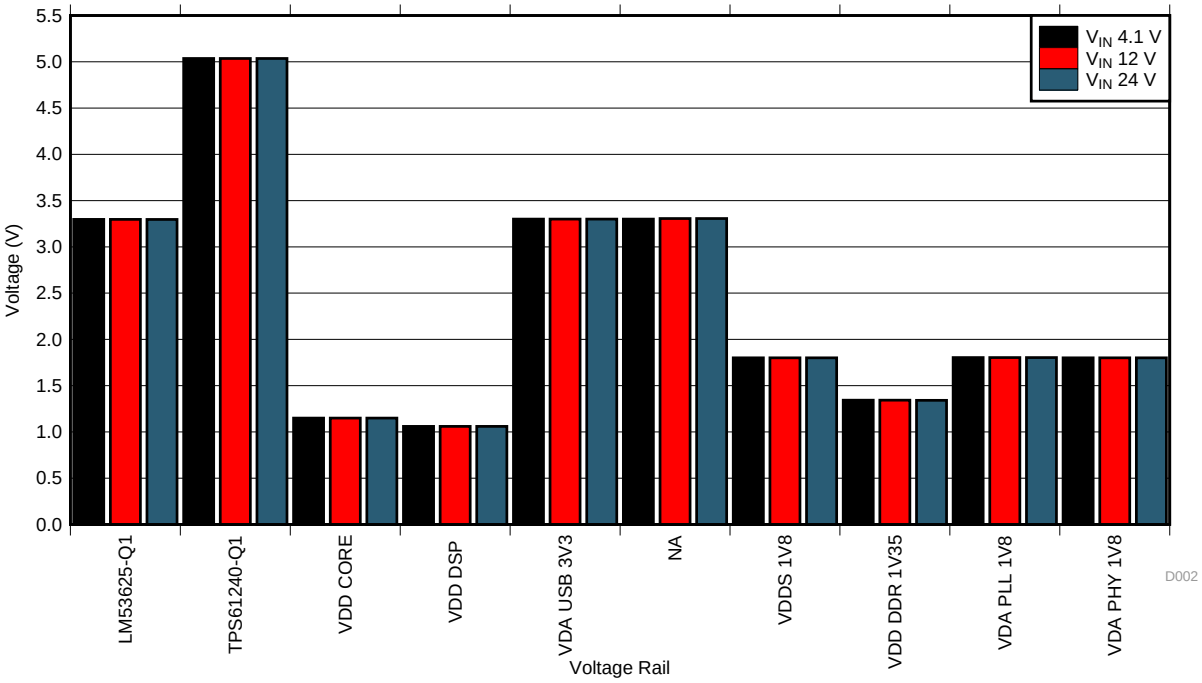


Figure 38. TIDA-01425 Voltage Rails versus Input Voltage

All voltage rails stay very stable throughout the whole operating voltage range. The processor can not be brought up when the voltage input drops to below 4.1 V due to the first-stage buck converter (LM53625-Q1) not reaching a stable 3.3 V. The power good signal is therefore staying low to keep the PMICs from being enabled.

4 Design Files

4.1 Schematics

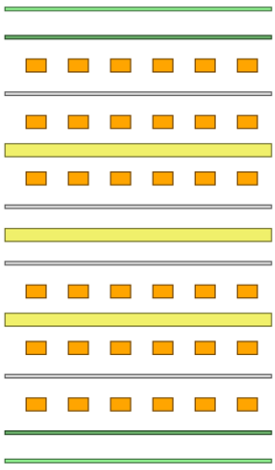
To download the schematics, see the design files at TIDA-01425.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01425.

4.3 PCB Layout Recommendations

The PCB design includes many considerations from the power, EMI, Ethernet communications, CAN communications, and the processor itself. All differential pairs in the layout have a differential impedance of 100 Ω and all single-ended traces have an impedance of 50 Ω. Figure 39 shows the board stackup.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/...	Surface Mat...	0.5	Solder Resist	3.5			0
Layer 1 - Top...	Signal	Copper	1.2				Top	
Dielectric 1	Dielectric	Prepreg	3.4	370H (1080...	4.2			
Layer 2 - GND	Signal	Copper	1.2				Not Allowed	
Dielectric 2	Dielectric	Core	4.1	370H (1-211...	4.2			
Layer 3 - Sig...	Signal	Copper	0.6				Not Allowed	
Dielectric 3	Dielectric	Prepreg	5.7	370H (1080)	4.2			
Dielectric 4	Dielectric	Core	28	370H (4-762...	4.2			
Dielectric 5	Dielectric	Prepreg	5.7	370H (1080)	4.2			
Layer 4 - Sig...	Signal	Copper	0.6				Not Allowed	
Dielectric 6	Dielectric	Core	4.1	370H (1-211...	4.2			
Layer 5 - PWR	Signal	Copper	1.2				Not Allowed	
Dielectric 7	Dielectric	Prepreg	3.4	370H (1080...	4.2			
Layer 6 - Bot...	Signal	Copper	1.2				Bottom	
Bottom Solder	Solder Mask/...	Surface Mat...	0.5	Solder Resist	3.5			0
Bottom Over...	Overlay							

Figure 39. PCB Stack-Up

The majority of signal traces and buses are routed on the top, third, and bottom layer. Layer 2 provides a good reference GND for the top and third layer and layer 5 provides a decent reference for the bottom layer signals. The DDR3L routing uses both the second and fifth layers for references with a section cut out of the fifth layer to specifically be used for the DDR3L routing reference plane. Important traces such as clocks and communication busses were kept as short as possible with a good reference plane above or below them. The two main rails of the processor, VDD_CORE and VDD_DSP, have large planes on multiple layers all the way to the balls to reduce inductance. One important thing to note is that the processor and discrete component layout and placement are based on a reference design that was optimized to meet the recommended system-on-chip (SoC) power integrity (PI) parameters of IR drop, decoupling capacitor loop inductance and target impedance versus frequency on a six-layer board. Also, the DDR3L component placement and routing of matched data-byte groups along with address and control signals were tested. TI highly recommends to use this layout when designing a six-layer PCB for the J6Entry because the layout has been verified as robust for proper J6Entry operation. For power, the majority of planes are kept on the inner layers, layer 4 and 5, to reduce the noise emitted from the supplies. Also, all unused copper on the board is connected as ground to provide a large ground for the board.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01425.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01425.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01425.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01425.

5 Software Files

To download the software files, see the design files at TIDA-01425.

6 Related Documentation

1. Texas Instruments, *DRA71x Infotainment Applications Processor*, J6Entry DRA710 Data Sheet (SPRS960)
2. Texas Instruments, *DP83TC811R-Q1 Low Power Auto PHYTHER 100BASE-T1 Automotive Ethernet Physical Layer Transceiver*, DP83TC811R-Q1 Data Sheet (SNLS579)
3. Texas Instruments, *DP83848Q-Q1 PHYTHER Extended-Temperature, Single-Port 10/100-Mbps Ethernet Physical Layer Transceiver*, DP83848Q-Q1 Data Sheet (SNLS341)
4. Texas Instruments, *TCAN1042-Q1 Automotive Fault Protected CAN Transceiver with CAN FD*, TCAN1042-Q1 Data Sheet (SLLSES9)
5. Texas Instruments, *CDCEx913-Q1 Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs*, CDCE913-Q1 Data Sheet (SCAS918)
6. Texas Instruments, *LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter*, LM53625-Q1 Data Sheet (SNVSAA7)
7. Texas Instruments, *TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter*, TPS61240-Q1 Data Sheet (SLVSAO4)
8. Texas Instruments, *LP873220-Q1 Dual High-Current Buck Converters and Dual Linear Regulators*, LP873220-Q1 Data Sheet (SNVSAU7)
9. Texas Instruments, *LP87332D-Q1 Dual High-Current Buck Converters and Dual Linear Regulators*, LP87332D-Q1 Data Sheet (SNVSAT1)
10. Texas Instruments, *TPS51200-Q1 Sink and Source DDR Termination Regulator*, TPS51200-Q1 Data Sheet (SLUS984)
11. Texas Instruments, *LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller*, LM74610-Q1 Data Sheet (SNOSCZ1)
12. Texas Instruments, *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*, TPS22965-Q1 Data Sheet (SLVSCI3)
13. Texas Instruments, *DRA72x (SR2.0, SR1.0) and DRA71x (SR2.0) SoC for Automotive Infotainment*, DRA710 Technical Reference Manual (SPRUHP2)
14. Cypress Semiconductor Corporation, *128 Mbit (16 Mbyte)/256 Mbit (32 Mbyte) 3.0-V SPI Flash Memory*, S25FLS256S Data Sheet (001-98283 Rev. *N) (http://www.cypress.com/file/177966/download)
15. Micron Technology, *Automotive DDR3L SDRAM*, MT41K64M16TW-107 Data Sheet (09005aef85e0b6f6) (https://www.micron.com/parts/dram/ddr3-sdram/mt41k64m16tw-107-aat)

6.1 Trademarks

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7 Terminology

AVB/TSN— Audio video bridging/time sensitive network

Automotive gateway— An automotive module that routes data from one control domain to another such as the infotainment domain to the body domain. Data includes real-time control, diagnostics, calibration, audio, and video data. Typically a gateway contains multiple communication interfaces such as CAN, LIN, and Ethernet.

AVS— Adaptive voltage scaling

CIR— Channel independent reporting

DDR— Double-data-rate

EMI— Electromagnetic interference

ESD— Electrostatic discharge

ESR— Equivalent series resistance

IrDA— Infrared Data Association

LDO— Low-dropout linear regulator

MAC— Media access controller

OBD— Onboard diagnostics

PHY— Physical layer transceiver (a device that performs physical layer functions)

PLL— Phase-locked loop

PORz— Power-on reset

PI— Power integrity

PMIC— Power management integrated circuit

PCB— Printed-circuit board

PFM— Pulse frequency modulation

PWM— Pulse width modulation

RTOS— Real-Time Operating System

SFD— Start-of-frame

SoC— System-on-chip

TVS— Transient-voltage-suppression

UART— Universal asynchronous receiver and transmitter

8 About the Author

DONOVAN PORTER is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Donovan specializes in gateway modules, helping create end equipment block diagrams and reference designs for automotive customers. Donovan earned his bachelors of science in electrical engineering from Texas Tech University in Lubbock, Texas.

HEATHER LOTHAMER is an Applications Engineer at Texas Instruments. In her previous role on the Automotive Systems Engineering team, she specialized in gateway modules, helping to create reference designs and their associated software. She now supports the J6 family of devices as a member of the Automotive Processor Applications team. She earned her bachelors of science in computer engineering from Rose-Hulman Institute of Technology in Terre Haute, Indiana.

Revision History B

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2017) to B Revision	Page
• Updated DP83TC811-Q1 to DP83TC811R-Q1 in *Resources* and throughout document	1

Revision History A

Changes from Original (August 2017) to A Revision	Page
• Added IEEE 802.u 100BASE-TX Ethernet PHY to *Features*	1
• Updated content in *System Description*	2
• Deleted section *Design Considerations*	4
• Added content to Section 2.2.1	4
• Added Section 2.2.2	5
• Updated content in Section 3.1	15
• Updated content in Section 3.2.1	15
• Updated content in Section 3.2.2	16
• Updated content in Section 3.2.4	19
• Updated content in Section 3.5	29

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