TI Designs: TIDA-01430

Cost- and Space-Optimized, Channel Isolated (Reinforced) AC/DC Voltage, Current DAQ Reference Design

Description

This reference design highlights an architecture that is optimized for size and cost for achieving channel-to-channel isolation when measuring AC/DC voltage and current signals. Accuracy of ±0.3% is achieved using an ultra-low-power (<1 mW at 1 MSPS) 12-bit ADC and an ARM® core MCU. Space savings and component count reduction is achieved using a digital isolator with integrated power converter that isolates channels and ADC and MCU.

Resources

TIDA-01430	Design Folder
ADS7043	Product Folder
ADS7044	Product Folder
MSP-EXP432P401R	Tool Folder
ISOW7841	Product Folder
TLV316	Product Folder
TLV2316	Product Folder
REF1930	Product Folder
LP5907	Product Folder
TLV431	Product Folder

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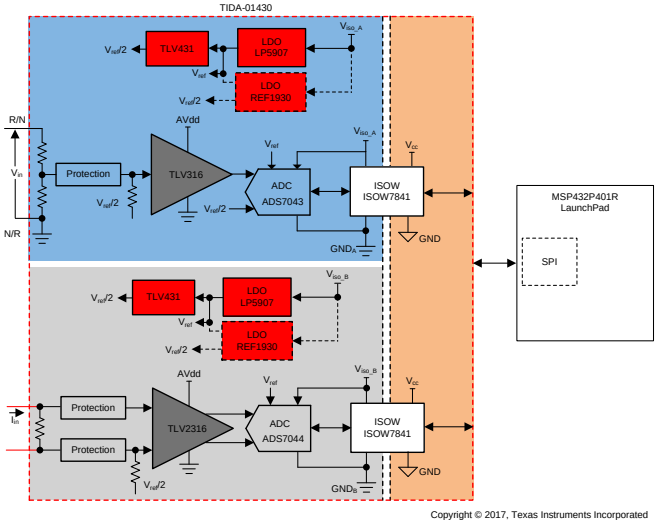
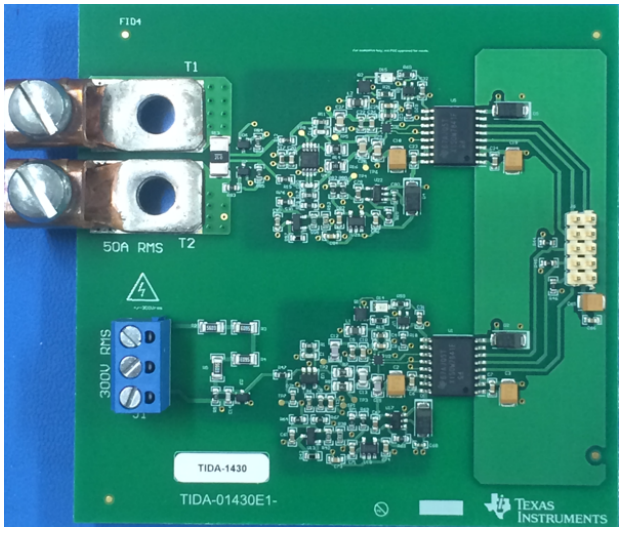
Features

- Channel-to-Channel Isolation Using Digital Isolator With Integrated Power Converter (ISOW7841)
- AC/DC Voltage and Current Measurement Accuracy:
  - AC Voltage: < ±0.25% for 5 to 300 V
  - AC Current: < ±0.3% for 0.5 to 50 A
- Ultra-Low-Power (<1 mW) Data Acquisition Using ADS7043 or ADS7044 and TLVx316
- Space Savings Achieved Using REF1930 (Integrated REF, REF/2) and ISOW7841 (Integrated Digital Isolator, Power Converter)
- Low Power Consumption and Simplified Multi-SPI Achieved Using MSP432P401R, an ARM Cortex® M4F Based MCU

Applications

- Circuit Breakers
- Protection Relay
- Terminal Units
- Storage and End Equipment Monitoring





1 System Description

Applications in grid infrastructure cover protection, control, and monitoring of systems such as generators, transformers, distribution lines, substations, bus bars, and so on. End equipment such as protection relays, circuit breakers, terminal units, and power quality analyzers measure multiple voltages and currents. While high voltage levels require primary-to-secondary isolation, some of these applications require isolation between channels due to different reference potential. The type of the current and voltage sensors used drive the architectural choice for providing this isolation.

This reference design achieves channel-to-channel isolation when measuring voltage and current signals from the transducers.

- A resistor potential divider is used for sensing voltages as the sensors are linear and have smaller profile.
- A shunt resistor is used for measuring currents.
- A digital isolator is used to provide isolation between the primary and secondary side while the integrated power converter provides channel-to-channel isolation.
- Overall system power is minimized using proper selection of AFE components and MCU.

1.1 Circuit Breaker

A circuit breaker monitors the flow of current and voltage and trips during the event of fault. This design has an architecture that can be used for measuring voltages or currents within 0.3% when individual channel isolation is important. True RMS is also computed for each channel for it to be used in an electronic trip unit (ETU). Group isolation architecture is covered under the TIDA-00661 reference design.

1.2 Protection Relay

In some of the protection relays, the secondary CTs are getting replaced with shunt resistors. In this case, channel-to-channel isolation can be achieved using the architecture shown in this reference design. While previous designs such as the TIDA-00080, TIDA-00555, and TIDA-00738 use a transformer driver to isolate power from channel to channel, this reference design demonstrates doing the same using the ISOW7841 with an integrated power converter to minimize the overall design footprint.

1.3 Storage and End Equipment Monitoring

Individual voltages and currents from various equipment can be monitored using this reference design as it provides isolation between channels in a single board with simplified architecture.

1.4 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Number of channels	One voltage and one current	Isolation between two channels
Input voltage range	300-V AC RMS ±400-V DC	5- to 300-V AC
Type of voltage measurement	Potential divider	Section 2.3.1
Voltage measurement accuracy	±0.25%	SPI to host Section 3.2
Input current range	50-A AC RMS ±70-A DC	0.5- to 50-A AC
Current measurement sensor type	Shunt	Section 2.3.1
Current measurement accuracy	±0.3% (0.5 to 50 A), ±0.3% (1 to 50 A)	SPI to host Section 3.2
ADC	12-bit SAR ADC	Pseudo (voltage) and fully (current) differential
Power supply for ADC	AV_{CC} = 3 V	Section 2.3.3
Isolation type	Digital isolator with integrated isolated power up to a 75-mA output current	Section 2.3.5
Isolation approach	Channel-to-channel isolation	Reinforced isolation Section 2.2.1
Sampling frequency	64 samples per cycle (50 or 60 Hz)	16× oversampling Section 3.1.2
RMS calculation	True RMS with 64 samples per cycle	—

2 System Overview

2.1 Block Diagram

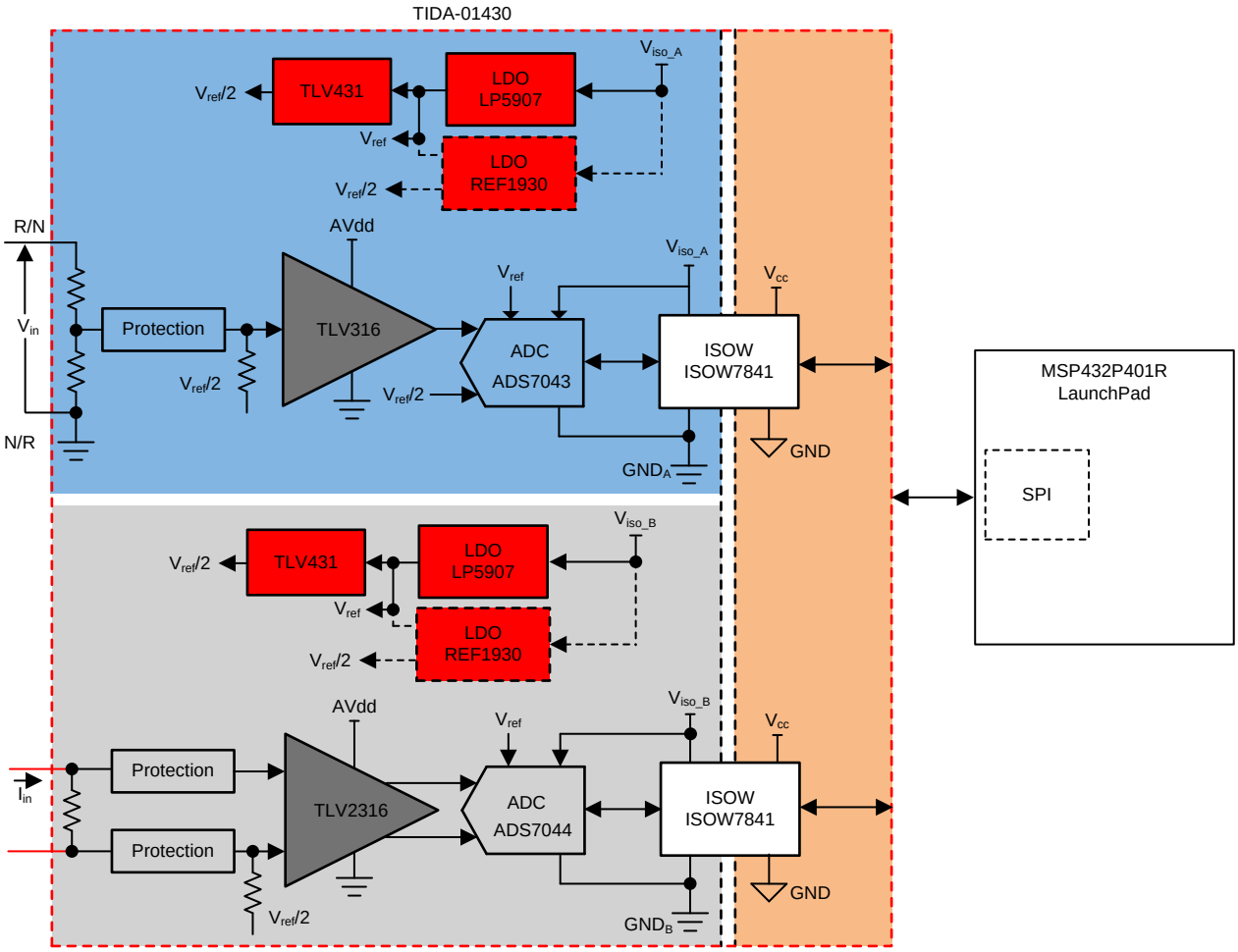


Figure 1. TIDA-01430 Block Diagram

2.2 Highlighted Products

2.2.1 ISOW7841: Digital Isolator With Integrated DC-DC Converter

The ISOW7841 is a high-performance, quad-channel, reinforced digital isolator with an integrated high-efficiency power converter. The integrated DC-DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore, this device eliminates the need for a separate isolated power supply in space-constrained isolated designs.

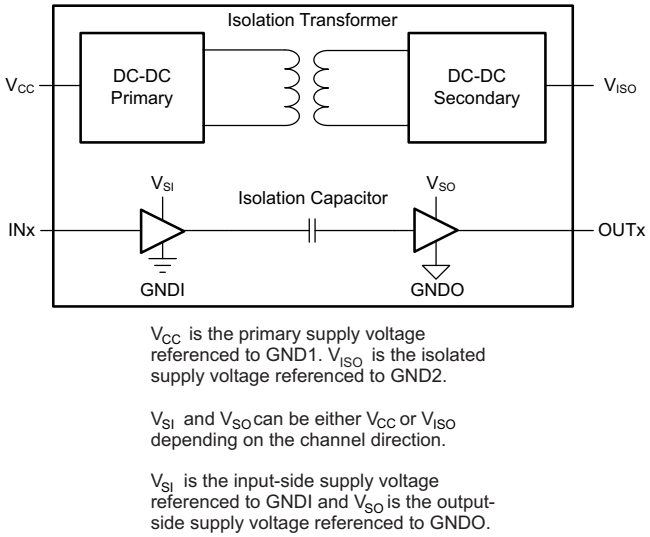


Figure 2. Functional Block Diagram of ISOW7841

The ISOW7841 device provides high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital I/Os. The signal isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier, whereas power isolation uses on-chip transformers separated by thin film polymer as insulating material.

Key features of this device include:

- Integrated high-efficiency DC-DC converter with on-chip transformer:
  - 3- to 5.5-V wide input supply range
  - Regulated 5-V or 3.3-V output
  - Up to 0.65-W output power
  - 5 to 5 V; 5 to 3.3 V: Available load current ≥ 130 mA
  - 3.3 to 3.3 V: Available load current ≥ 75 mA
- Soft-start to limit inrush current
- Overload and short-circuit protection
- Thermal shutdown
- Signaling rate up to 100 Mbps
- Low propagation delay: 13 ns typ (5-V supply)
- High CMTI: ±100 kV/μs minimum
- Robust electromagnetic compatibility (EMC)
- System-level ESD, EFT, and surge immunity
- Low emissions
- 5000-V_{RMS} isolation for 1 minute per UL 1577

2.2.2 ADS704x: Ultra-Low-Power, 12-Bit, 1-MSPS SAR ADC

The ADS704x is a 1-MSPS, analog-to-digital converter (ADC). The device supports a wide analog input voltage range (±0.825 to ±1.8 V) and includes a capacitor-based, successive-approximation register (SAR) ADC with an inherent sample-and-hold circuit. The SPI-compatible serial interface is controlled by the CS and SCLK signals. The input signal is sampled with the CS falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 to 3.6 V), enabling direct interface to a variety of host controllers.

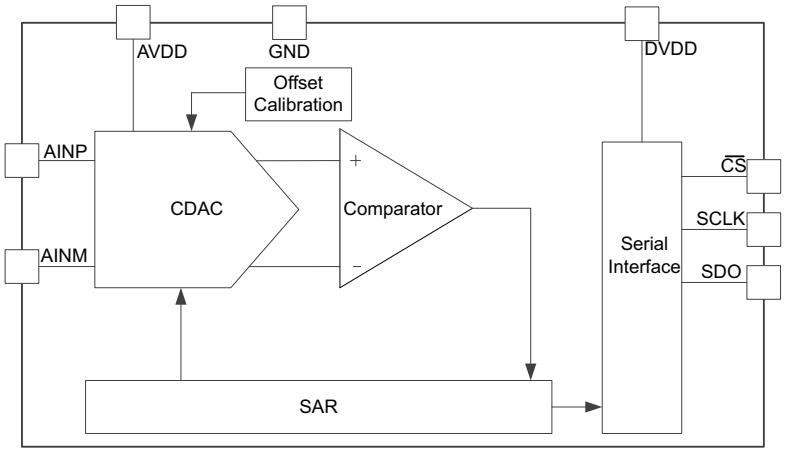


Figure 3. Functional Diagram of ADS704x

Key features of this device include:

- Industry's first SAR ADC with nanowatt power consumption
- ADS7044:
  - 261 μW at 1 MSPS with 1.8-V AVDD
  - 900 μW at 1 MSPS with 3-V AVDD
  - 90 μW at 100 kSPS with 3-V AVDD
  - Less than 1 μW at 1 kSPS with 3-V AVDD
- ADS7043:
  - 243 μW at 1 MSPS with 1.8-V AVDD
  - 780 μW at 1 MSPS with 3-V AVDD
  - 78 μW at 100 kSPS with 3-V AVDD
  - Less than 1 μW at 1 kSPS with 3-V AVDD
- Industry's smallest SAR ADC: X2QFN-8 package with 2.25-mm^2 footprint
- 1-MSPS throughput with zero data latency
- Wide operating range:
  - AVDD: 1.65 to 3.6 V
  - DVDD: 1.65 to 3.6 V (independent of AVDD)
  - Temperature range: –40°C to 125°C
- Excellent performance:
  - 12-bit resolution with NMC applications
  - ±1-LSB (max) DNL and INL
  - 71-dB SNR with 3-V AVDD
  - –85-dB THD with 3-V AVDD
- Unipolar, differential input range (ADS7044): –AVDD to AVDD
- Unipolar, pseudo-differential input range (ADS7043): (–AVDD / 2) to (AVDD / 2)

- Integrated offset calibration
- SPI-compatible serial interface: 16 MHz

2.2.3 TLV316: Rail-to-Rail Input/Output, Low Voltage Operational Amplifier

The TLV316 (single), and TLV2316 (dual) devices comprise a family of general-purpose, low-power operational amplifiers. Features such as rail-to-rail input and output swings, low quiescent current (400 μA/ch typical) combined with a wide bandwidth of 10 MHz, and very-low noise (12 nV/√Hz at 1 kHz) make this family attractive for applications that require a good balance between cost and performance. These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

Key features of this device include:

- Unity-gain bandwidth: 10 MHz
- Low I_Q: 400 μA/ch: Excellent power-to-bandwidth ratio and stable I_Q over temperature and supply range
- Wide supply range: 1.8 to 5.5 V
- Low noise: 12 nV/√Hz at 1 kHz
- Low input bias current: ±10 pA
- Offset voltage: ±0.75 mV
- Unity-gain stable
- Internal RFI and EMI filter
- Extended temperature range: –40°C to 125°C

2.2.4 REF1930: Low-Drift, Low-Power, Dual-Output Voltage Reference

Applications with only a positive supply voltage often require an additional stable voltage in the middle of the ADC input range to bias input bipolar signals. The REF1930 provides a reference voltage (V_{REF}) for the ADC and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals.

The REF1930 offers excellent temperature drift (25 ppm/°C, max) and initial accuracy (0.1%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 μA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. An extremely low dropout voltage of only 10 mV allows operation from very low input voltages, which can be very useful in battery-operated systems. Both the V_{REF} and V_{BIAS} voltages have the same excellent specifications and can sink and source current equally well. Very good long-term stability and low noise levels make these devices ideally-suited for high-precision industrial applications.

Key features of this device include:

- Two outputs, V_{REF} and V_{REF} / 2, for convenient use in single-supply systems
- Excellent temperature drift performance: 25 ppm/°C (max) from –40°C to 125°C
- High initial accuracy: ±0.1% (max)
- V_{REF} and V_{BIAS} tracking over temperature: 7 ppm/°C (max) from –40°C to 125°C
- Low dropout voltage: 10 mV
- High output current: ±20 mA
- Low quiescent current: 360 μA
- Line regulation: 3 ppm/V
- Load regulation: 8 ppm/mA

2.2.5 TLV431: Low-Voltage Adjustable Precision Shunt Regulator

The TLV431 device is a low-voltage, three-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

Key features of this device include:

- Low-voltage operation, V_{REF} = 1.24 V
- Adjustable output voltage, V_O = V_{REF} to 6 V
- Reference voltage tolerances at 25°C: 1% for TLV431A
- Typical temperature drift: 11 mV (–40°C to 125°C)
- Low operational cathode current: 80 μA (typ)

2.2.6 LP5907: 250-mA Ultra-Low-Noise LDO

The LP5907 is a low-noise LDO capable of supplying a 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1-μF input and a 1-μF output ceramic capacitor (no separate noise bypass capacitor is required). This device is available with fixed output voltages from 1.2 to 4.5 V in 25-mV steps.

2.3 System Design Theory

2.3.1 Voltage and Current Sensing

This reference design demonstrates measurement of one voltage and one current channel with isolation between these two channels. Isolation is also provided between the current and voltage channels with respect to the host processor using a digital isolator. Hence, the non-isolated method of a potential divider and shunt are used to measure the voltage and current, respectively.

The voltage divider circuit is used to step down the input voltage to match the input voltage range of the signal conditioning system. Multiple resistors are used to divide the input to increase reliability and withstand the rated voltage continuously. The overall gain of the resistor divider is selected based on the maximum input voltage and differential output voltage to the TLV316.

- Maximum input voltage = 300-V AC RMS = ±424-V peak
- Maximum differential input voltage to TLV316 = 3 V

The gain of the resistor divider is selected as 1/300 in this reference design, allowing margins on the input voltage rails of the TLV316. To reduce loading, impedance for the measurement circuit is selected at > 2 MΩ.

Shunt is used to measure the current in this reference design. The value of the shunt and power rating are equally important to minimize the power dissipation in the board mounted shunt. Selecting a shunt value depends on the maximum input current and maximum voltage drop across the shunt.

Find more details for the design of resistor divider and shunt in the TIDA-00555[2] and TIDA-00738[3] reference designs.

2.3.2 Analog Signal Conditioning

Figure 4 shows voltage measurement and signal conditioning for the voltage channels using a resistor divider followed by a level shifting to provide DC offset to the AC input voltage. In this reference design, AV_{CC} of 3 V is demonstrated and offset voltage is set to half of AV_{CC}, which is 1.5 V. The resistor divider is selected to limit the maximum voltage across R9 to be 3 V. The TLV316 is selected to drive the input analog signal going to the SAR ADC. The unity gain stage is implemented along with the DC level shifting of the input signal.

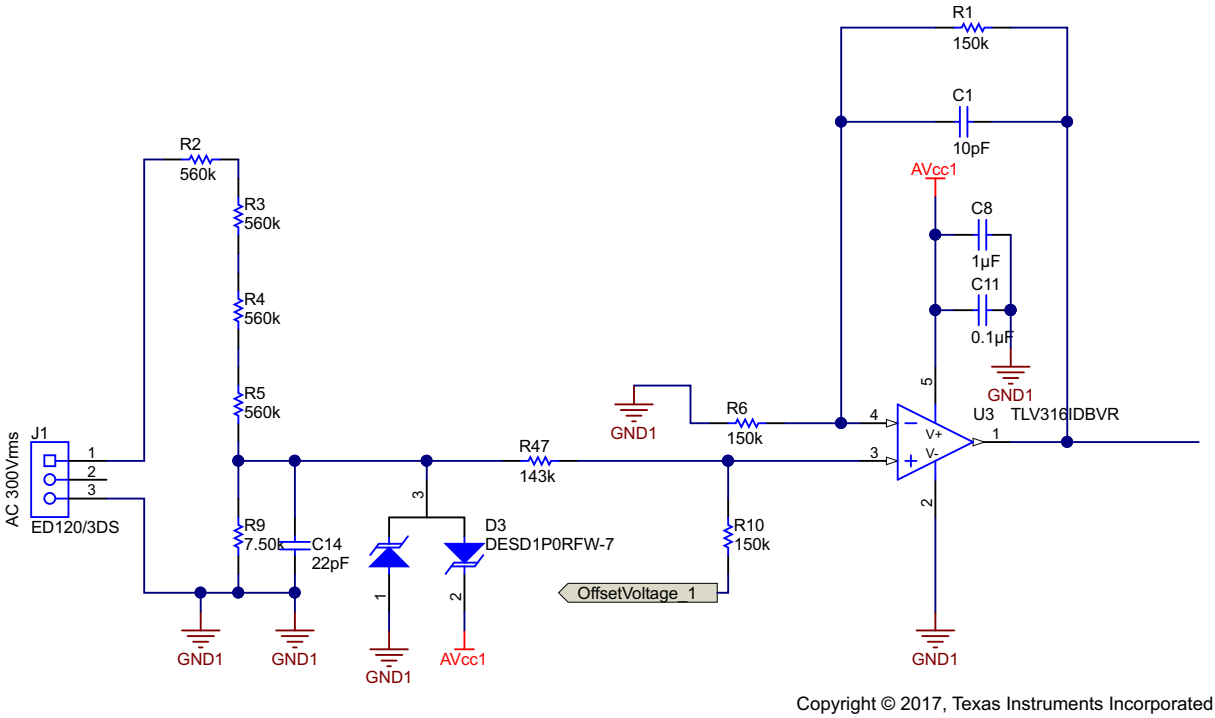


Figure 4. Voltage Sensing and Signal Conditioning

Analog signal conditioning for current measurement is shown in Figure 5. A differential amplifier configuration using the TLV2316 is realized to amplify the differential voltage drop across the shunt resistance. A gain of 20 has been selected. Protection is provided at both the terminals of differential input to limit the voltage levels. Voltage input to the fully differential ADC, ADS7044, needs to be offset by $AV_{DD}/2$. Hence, V_{OFFSET} of 1.5 V is provided to both the inputs of ADC as shown in Figure 5.

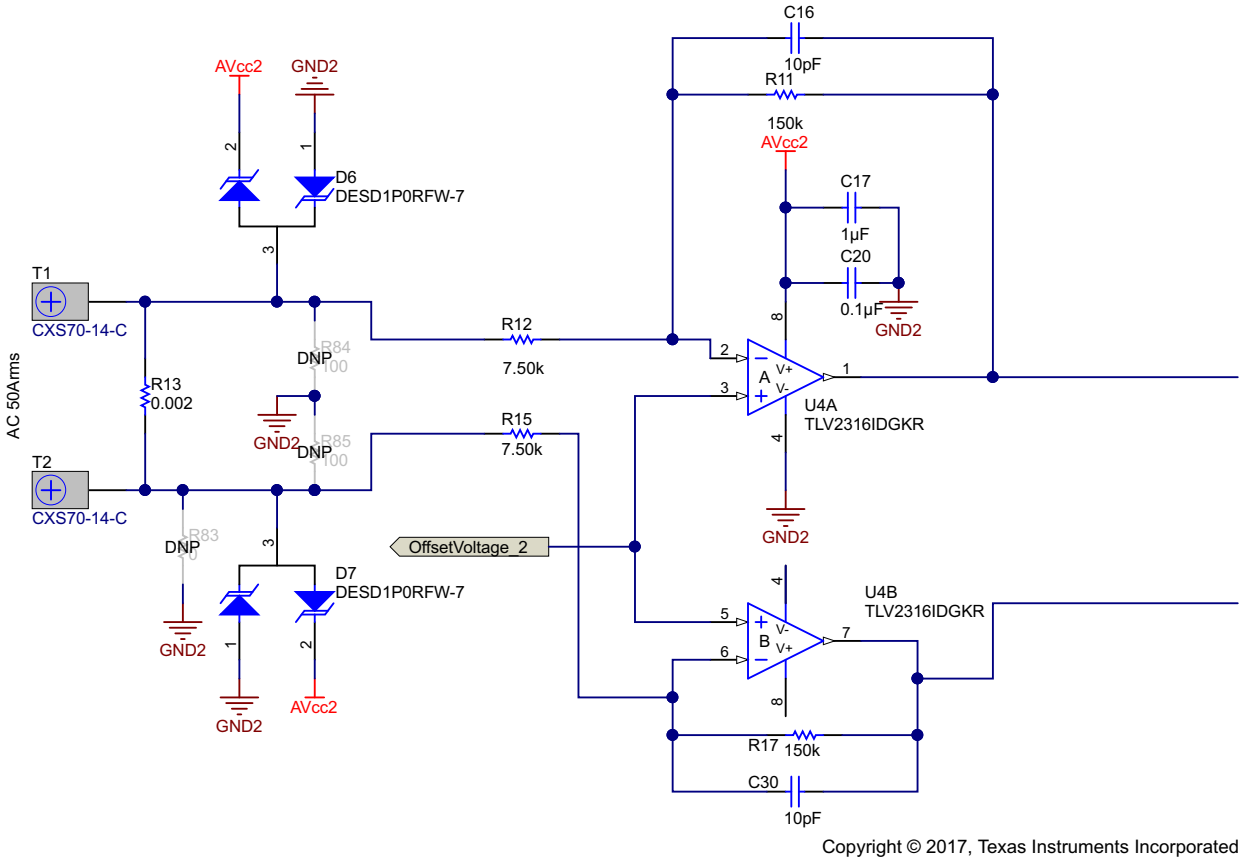


Figure 5. Sensing and Signal Conditioning for Current Using Shunt

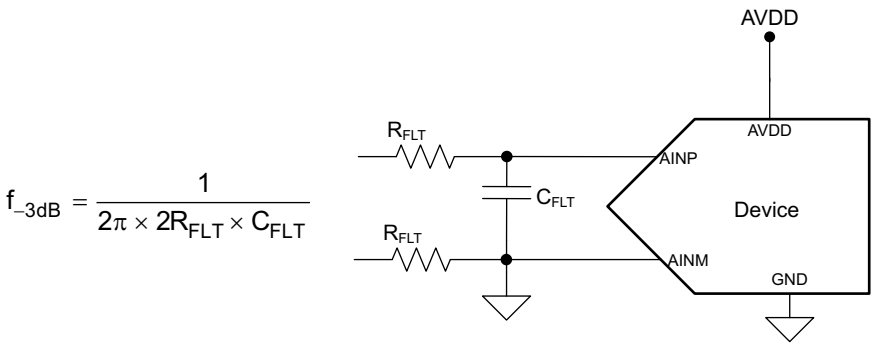


Figure 6. Antialiasing Filter for ADC

Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. To avoid this, an antialiasing filter is used at the input of both the ADCs. A low-pass RC filter is used whose 3-dB cutoff frequency is selected to be less than half the sampling frequency.

2.3.3 Voltage Reference

The isolated voltage obtained from ISOW has ripple voltage, which needs to be filtered before feeding this to the reference of the ADC. This reference design provides three options for obtaining the AV_{DD} and V_{OFFSET} voltage required for the ADC and signal conditioning.

- Option 1: Passive filters can be used to reduce the voltage ripple. Using combination of R and C, the filter can be tuned to obtain the required performance. This option can obtain an AV_{DD} of 3.3 V and V_{OFFSET} of 1.65 using the TLV431.
- Option 2: In this configuration, an LDO is used to derive stable voltage of 3 V from 3.3 V for AV_{DD}. For offset voltage, 1.5 V is derived from the 3-V supply using the TLV431 as shown in Figure 7.
- Option 3: Instead of two active components, only one is used to obtain both AV_{DD} and $AV_{DD}/2$ using the REF1930. This gives both the voltages for the required performance at smaller footprint.

Deciding between these three options can be configured by changing the corresponding components as mentioned in Table 4.

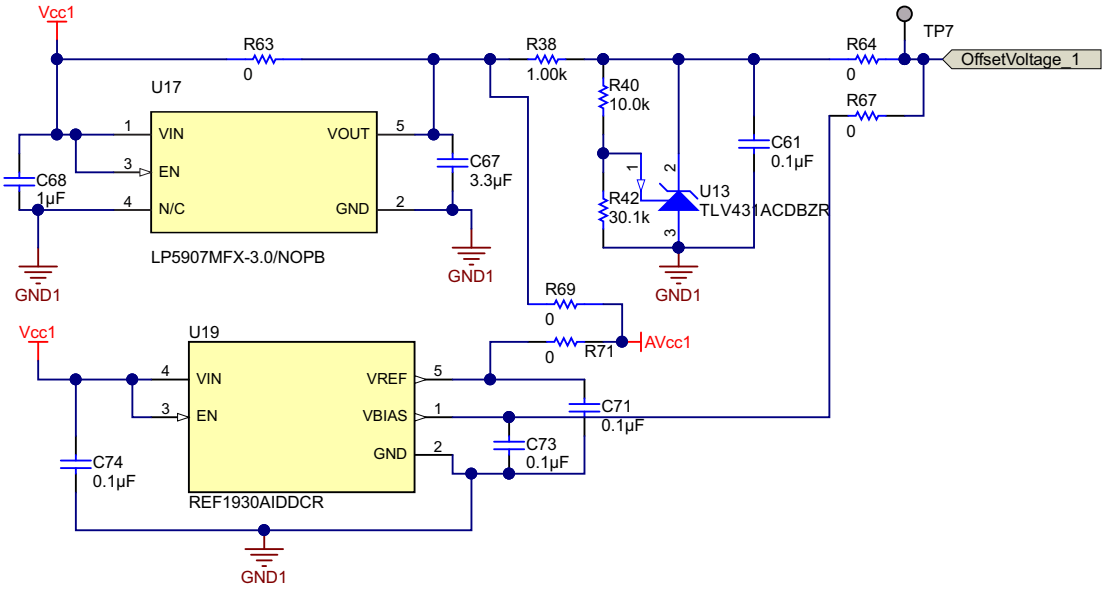


Figure 7. Voltage Reference for ADC and Analog Signal Conditioning

2.3.4 ADC

For voltage measurement, the pseudo-differential ADC ADS7043 is used in this reference design. The negative analog input terminal (AINM) of this ADC is tied to $AV_{DD}/2$, and the positive analog input (AINP) can swing between 0 to AV_{DD}. Hence, the analog input signal from a potential divider needs to be offset by $AV_{DD}/2$ as described in Section 2.3.2.

The ADS7044 is used for current measurement, which is fully differential ADC. Both positive and negative analog input (AINP and AINM) can swing between 0 and AV_{DD} with the full-scale differential input span of $2 \times AV_{DD}$.

NOTE: For higher resolution, use the ADS7057 (14Bit, 2.5-MSPS), ADS7062 (16 bits, 1MSPS, single-ended ADC), and ADS7064 (16 bits, 1MSPS, differential) devices.

The ADS704x includes a feature to calibrate its internal offset. The device initiates offset calibration on the first CS falling edge after power-up. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage. The device includes an internal offset calibration register (OCR) that stores the offset calibration result, which is not accessible to the user. OCR is updated by providing 16 SCLKs during the first serial transfer frame after power-up. It is also possible to recalibrate during normal operation by following procedures given in the ADS7043 datasheet.

2.3.5 Digital Isolator

In this reference design, analog voltage, and current signals after signal conditioning are converted to a digital signal. A digital isolator is used to provide isolation between the analog signal and the host processor, which is MSP432P401R in this reference design. ISOW also provides isolation between two measuring channels.

There are two approaches for providing digital isolation. The first method consists of using a digital isolator, isolation transformer, and transformer driver. The second approach is adopted in this reference design where ISOW is used for digital isolation, which also has integrated isolated power. This solution provides reduced component count and size, simplifying the system design with improved reliability. Find more details on the advantages of ISOW in Section 2.2.7 of the TIDA-00847 design guide.

Figure 8 shows the interface between the ADC and ISOW. The ADS704x has a serial (SPI) interface with two inputs (chip select and SCLK) and one output (SDO). The ISOW7841 provides three ports in one direction and one in the opposite direction.

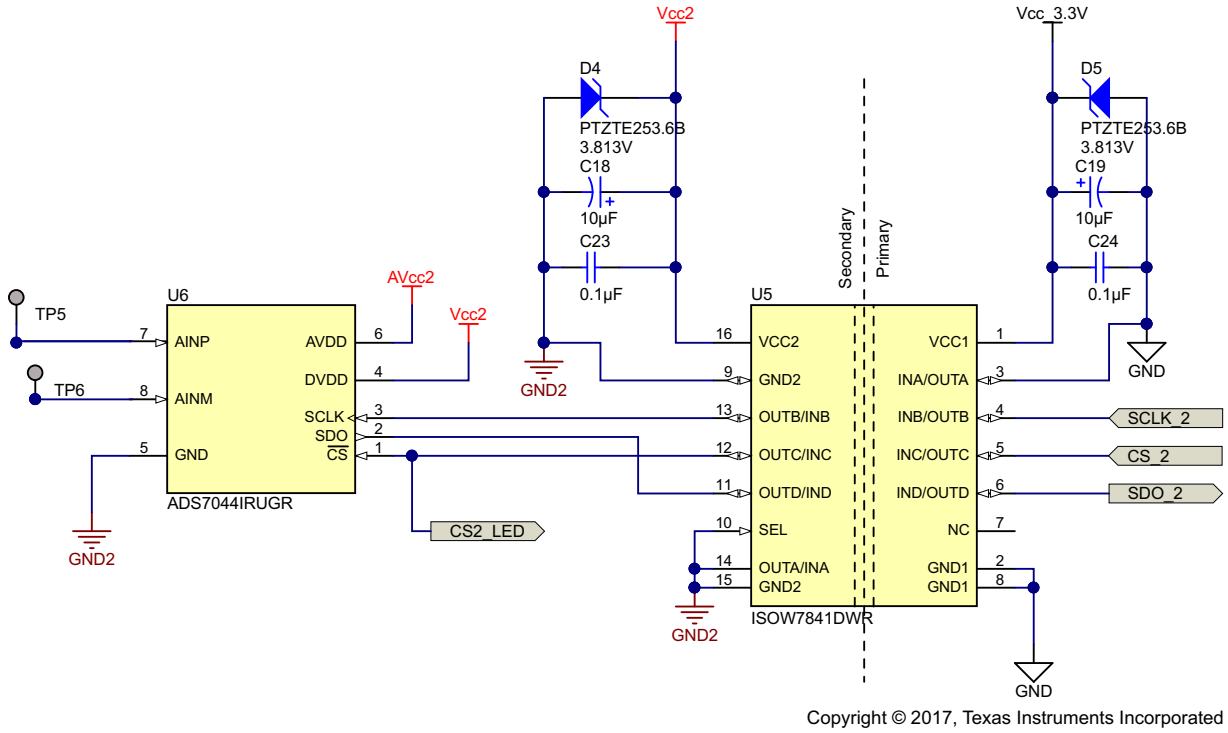


Figure 8. Interfacing Between ADC and ISOW

2.3.6 Interfacing With MSP432P401R

In this reference design, the MSP432P401R LaunchPad™ (MSP-EXP432P401R) is used as a host to provide the serial interface for the ADCs. ARM Cortex-M4F is used to compute the true RMS value of voltage and current for validating the accuracy.

Figure 9 shows the timing diagram for the serial interface of the selected ADCs. A minimum of 14 SCLKs are provided by the host processor to convert and transfer the data from the ADC.

NOTE: The ADS7044 provides a digital output in 2's complement format whereas the ADS7043 gives an unsigned format with 0x800 as the mid code. Take care of these differences in the MSP432P401R after data acquisition.

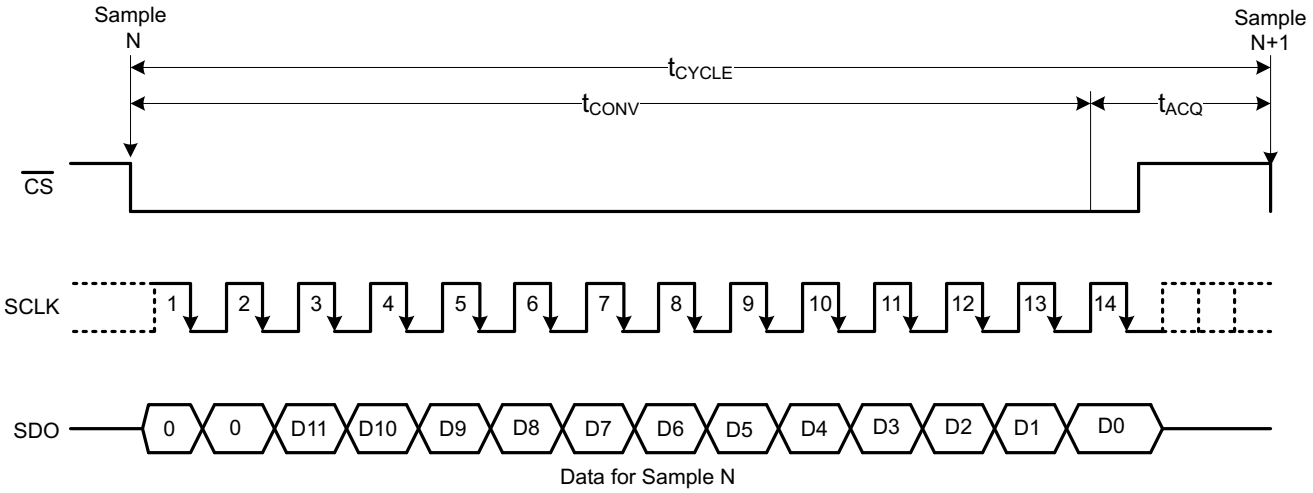


Figure 9. Serial Interface Timing Diagram

Interface between multiple ADCs and the MSP432P401R through the ISOW can be performed in two approaches as shown in Figure 10 and Figure 11. In Figure 10, multiple SPI ports of the MSP432P401R are used with a common CS for all the ADCs. In this configuration, data from multiple channels can be converter and transferred simultaneously using a single CS for all the ADCs. The MSP432P401R can handle only four SPI channels simultaneously. If the user wants to interface more than four channels, then a second approach can be used.

Figure 11 shows the second approach where a single SPI port is used for interfacing all the ADCs with a separate CS for different channels. This approach limits the data throughput of the converter depending on the number of channels connected in parallel.

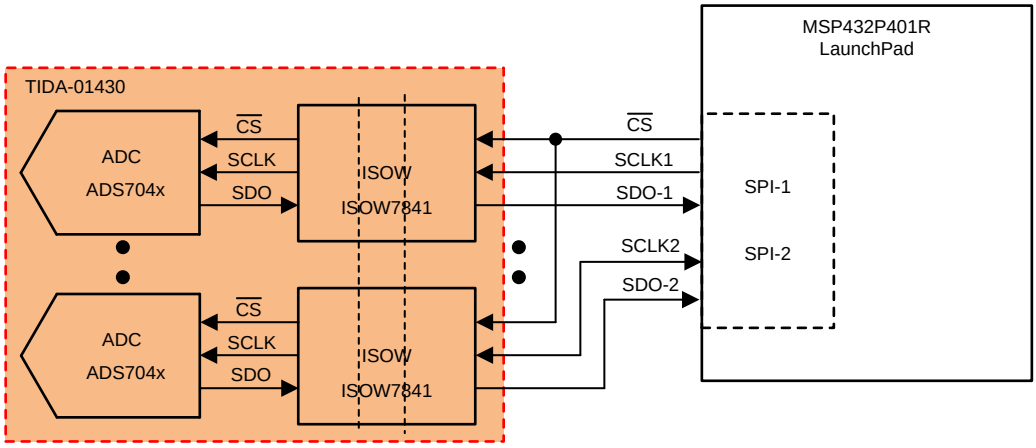


Figure 10. SPI Configuration Using Multiple Ports

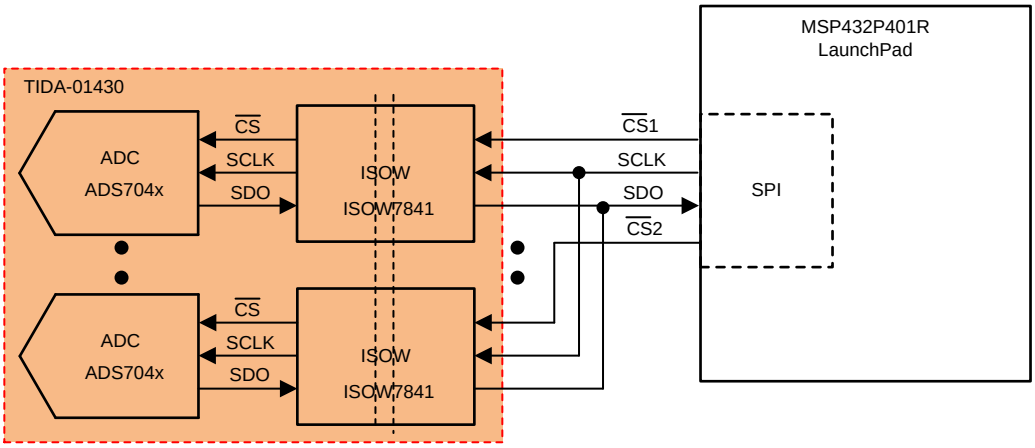


Figure 11. SPI Configuration Using Single SPI Port With individual CS

3 Hardware, Software, Testing Requirements, and Test Results

This section provides information on connecting this reference design for functional and performance testing.

3.1 Required Hardware and Software

3.1.1 Hardware

Table 2 provides details of the input and output connectors for the TIDA-01430.

Table 2. Connector Details for TIDA-01430

DESCRIPTION	CONNECTOR	PIN
Input voltage	J1	1(+), 2(–)
Input current	T1	—
	T2	—
Chip select for current channel (CS2)	J6	1
Serial output for current channel (SDO2)		2
CLK for current channel (SCLK2)		3
VCC (3.3 V)		4
Serial output for voltage channel (SDO1)		5
VCC (3.3 V)		6
Chip Select for voltage channel (CS1)		7
GND		8
CLK for voltage channel (SCLK1)		9
GND		10

CAUTION

HIGH VOLTAGE: Input voltage can vary between 0 to 300 V_{RMS}. Ensure the voltage source is switched off while connecting it to the board, and do not touch the input terminal during testing.

This reference design provides multiple test points for probing the voltages at different stages for debugging purposes. Different available test points are listed out in Table 3.

Table 3. Test Points on TIDA-01430

TEST POINTS	DESCRIPTION
TP1	Analog voltage reference for voltage channel
TP2	AINP for voltage channel
TP3	AINM for voltage channel
TP4	Analog voltage reference for current channel
TP5	AINP for current channel
TP6	AINM for current channel
TP7	Offset voltage for voltage channel
TP8	Offset voltage for current channel

Table 4 provides mounting of components for obtaining three different configurations for deriving analog voltage references.

Table 4. Different Options for Configuring Voltage Reference

??	PASSIVE FILTERS	LP5907 and TLV431	REF1930
R63, R75	—	Not fitted	Not fitted
R64, R76	—	—	Not fitted
R67, R78	Not fitted	Not fitted	—
R69, R80	—	—	Not fitted
R71, R82	Not fitted	Not fitted	—
U13 , U15	—	—	Not fitted
U17, U22	Not fitted	—	Not fitted
U19, U24	Not fitted	Not fitted	—

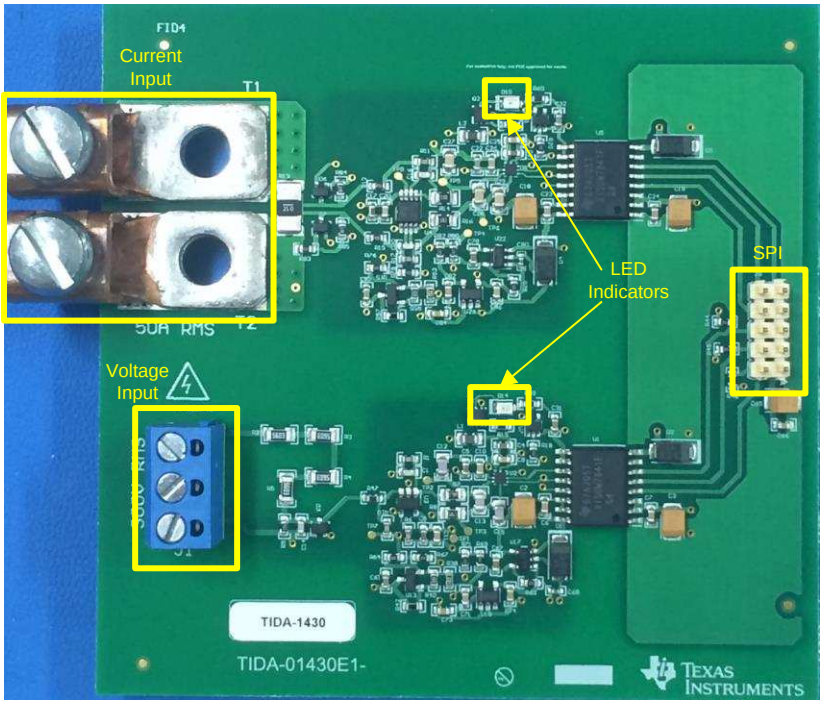


Figure 12. Diagram of Board Showing Connectors

3.1.2 Software

Table 5 shows the interface between this reference design and MSP432P401R LaunchPad. In this reference design, two different SPI ports are used for voltage and current data acquisition for demonstration.

Table 5. Pin Configurations Between TIDA-01430 and MSP-EXP432P401R

FUNCTION	PIN ON TIDA-01430	PIN ON MSP-EXP432P401R
SCLK1	J6-9	UCB0CLK (P1.5)
CS1	J6-7	P5.6 (Timer/PWM)
SDO1	J6-5	UCB0SOMI (P1.7)
SDI1 (Dummy)	—	UCB0SIMO (P1.6)
SCLK2	J6-3	UCB1CLK (P6.3)
CS2	J6-1	P5.7 (Timer/PWM)
SDO2	J6-2	UCB1SOMI (P6.5)
SDI2 (Dummy)	—	UCB1SIMO (P6.4)

Initializations:

- DCO is set to 48 MHz to use the full extent for computation of true RMS.
- SMCLK is set to 12 MHz, which is used as a source for SPI (SCLK).
- PWM with a fixed frequency (equal to sampling frequency) and fixed duty ratio is configured for CS. The timer interrupt generated by this is used to trigger the SPI transfer.
- Two SPI ports, UCB0 and UCB1, are configured in master mode, 8-bit transfer and MSB first.
- DMA is configured to collect 1024 samples from the each of the SPI ports. DMA is configured in Ping Pong mode to collect data in alternate buffers. Once DMA collects 1024 samples, the DMA interrupt is called, which switches between the ping-pong buffer and also informs the CPU for processing the collected data.
- After receiving the 1024 samples, the CPU does the post processing of data.
- 16 samples of 12 bit are added together to obtain a single 16-bit data value, which represents the average value of 16 samples.
- 1024 samples in one cycle is averaged to obtain 64 samples in one cycle.
- 64 samples are used for computing RMS value using the ARM DSP library.
- This procedure is repeated continuously to calculate the RMS value for each cycle.

3.2 Testing and Results

3.2.1 Functional Tests

A 3.3-V supply is provided at the SPI port using either an external source or from the MSP432P401R LaunchPad. Voltage at different stages are measured and are listed in Table 6.

Table 6. Functional Tests for Voltage Reference

DESCRIPTION	VOLTAGE (V)	RIPPLE (mV)
V_{IN}: Input supply voltage	3.3096	23.000
Vcc1: Isolated supply voltage from ISOW	3.3293	18.260
Vcc2: Isolated supply voltage from ISOW	3.3237	17.743
AVcc1: Analog voltage reference	2.9995	0.045
AVcc2: Analog voltage reference	2.9994	0.084
Offset voltage 1	1.4997	0.122
Offset voltage 2	1.4997	0.155

Input voltage at connector J1 is shorted to obtain DC performance of the voltage measurement channel. Figure 13 shows the histogram for the digital output obtained at the MSP432P401R through serial interface. DC offset is observed due to variation in the offset voltage.

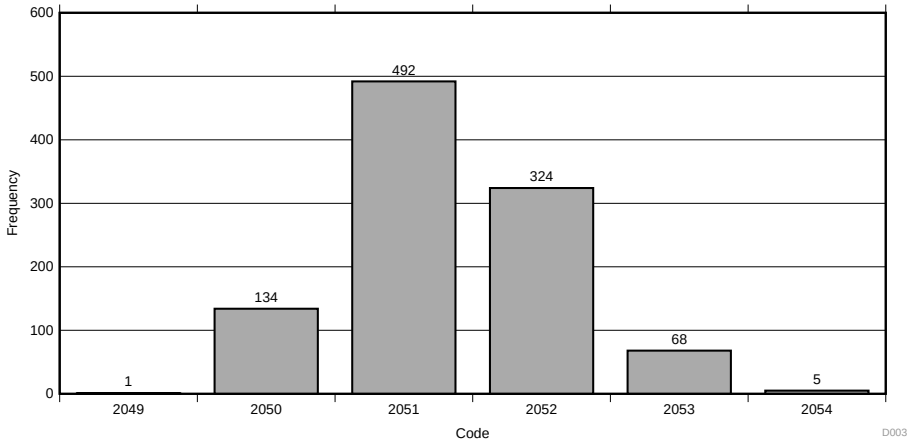


Figure 13. DC Voltage Histogram

Similarly, DC performance for the current measurement channel is obtained for zero current and DC histogram is obtained as shown in Figure 14. For zero current, ADC is supposed to read 0x000. Due to deviation in DC offset voltage, a small negative value is observed at the input of ADC, which results in shifting of midcode value. As a result, midcode has been observed to be 0xFFB instead of 0x000.

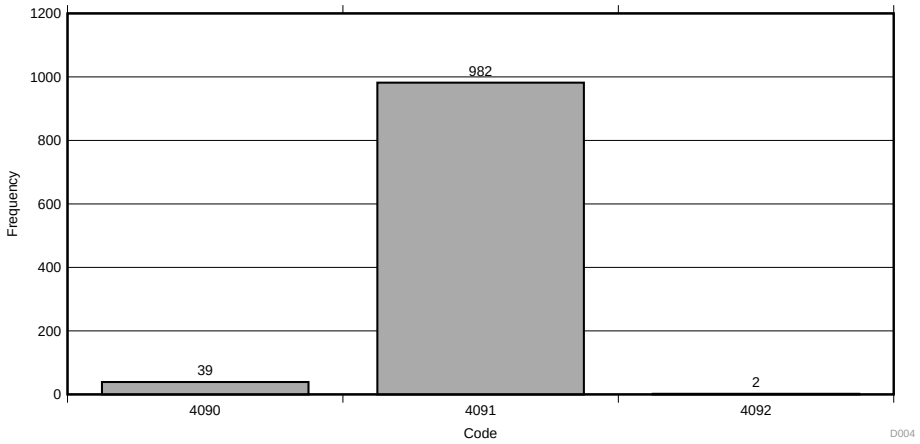


Figure 14. DC Current Histogram

3.2.2 Performance Tests

For testing the board for performance, a variable voltage and current source is connected at the input. The design board is connected to the MSP432P401R LaunchPad. Frequency of the input voltage and current is set to 50 Hz. Every line cycle, 1024 samples are collected through SPI from both the ADCs. These samples are averaged (16:1) to get 16-bit, 64 samples per cycle. RMS values are calculated for both voltage and current channels every cycle. For the voltage measurement channel, input AC voltage is varied from 5 up to 300 V. Applied voltage, measured voltage, and % error are listed in Table 7. The accuracy of the voltage measurement is also plotted in Figure 15.

Table 7. Voltage Measurement Data for AC Signal

VOLTAGE (V_{RMS})	APPLIED VOLTAGE	MEASURED VOLTAGE	ERROR
5	5.0030	4.999	0.0807%
10	10.0021	9.980	0.2249%
25	25.0008	25.018	–0.0687%
50	50.0007	49.971	0.0597%
75	75.0024	74.911	0.1213%
100	100.0040	99.976	0.0277%
125	125.0050	124.739	0.2125%
150	150.0040	150.080	–0.0508%
200	200.0060	199.536	0.2349%
250	250.0030	249.743	0.1041%
300	300.0020	300.050	–0.0158%

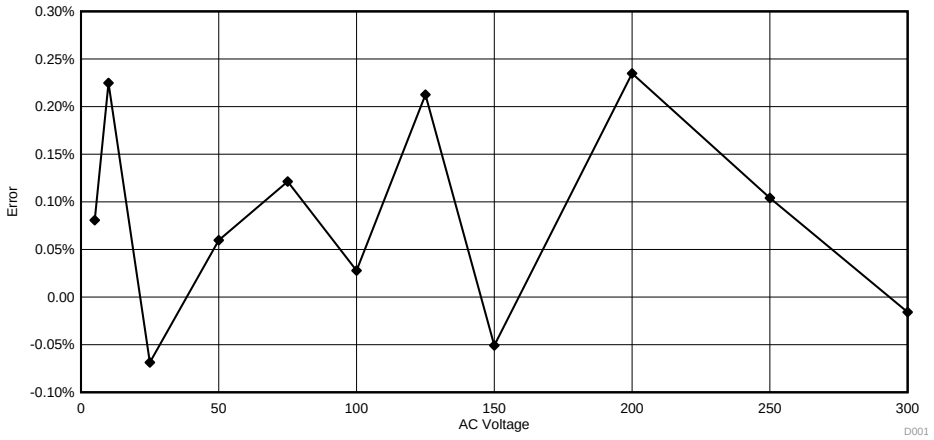


Figure 15. Voltage Measurement Accuracy

Accuracy for current measurement channels is also obtained similar to voltage. Table 8 and Figure 16 present AC performance of the current channel.

Table 8. AC Current Measurement Accuracy

CURRENT (A_{RMS})	APPLIED CURRENT	MEASURED CURRENT	ERROR
0.5	0.50000	0.499	0.1800%
1.0	1.00050	1.001	–0.0088%
2.5	2.50062	2.500	0.0335%
5.0	5.00076	5.000	0.0126%
10.0	10.00060	10.002	–0.0103%
20.0	20.00630	20.028	–0.1077%
35.0	35.00590	35.052	–0.1317%
50.0	50.00840	50.148	–0.2800%

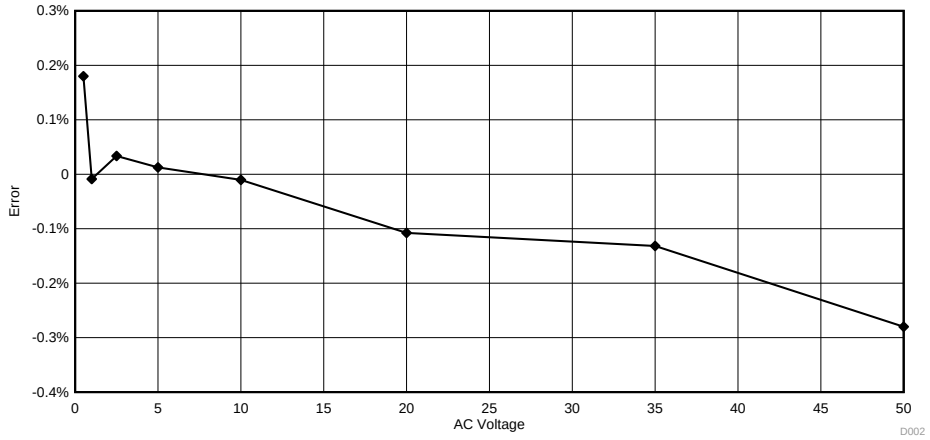


Figure 16. AC Current Measurement Accuracy

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01430.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01430.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01430.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01430.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01430.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01430.

5 Software Files

To download the software files, see the design files at TIDA-01430.

6 Related Documentation

1. Texas Instruments *Shunt-Based AC/DC Current and Voltage Sensing for Smart Grid Applications with Reinforced Isolation*, TIDA-00080 Design Guide (TIDU429)
2. Texas Instruments *Isolated Current and Voltage Measurement Using Fully Differential Isolation Amplifier Reference Design*, TIDA-00555 Design Guide (TIDUA58)
3. Texas Instruments *Extended Current and Voltage Measurement Using Shunts for Protection Relays Reference Design*, TIDA-00738 Design Guide (TIDUB79)
4. Texas Instruments *High-Resolution, Fast Start-Up, Delta-Sigma ADC-Based AFE for Air Circuit Breaker (ACB) Reference Design*, TIDA-00661 Design Guide (TIDUB80)
5. Texas Instruments *Size and Cost-Optimized Binary Module Reference Design Using Digital Isolator With Integrated Power*, TIDA-00847 Design Guide (TIDUCX3)

6.1 Trademarks

7 Terminology

ADC— Analog-to-digital converter

AFE— Analog front end

FRAM— Ferroelectric random access memory

LPF— Low-pass filter

LPM— Low power mode

MCU— Microcontroller unit

PD— Potential divider

RMS— Root mean square

SAR— Successive-approximation register

SPI— Serial peripheral interface

8 About the Authors

PRASANNA RAJAGOPAL is a systems engineer at Texas Instruments Dallas where he is responsible for developing reference design solutions for Grid Infrastructure in Industrial Systems. Prasanna brings to this role his expertise in power electronics, mixed signal systems. Prasanna earned his PhD from IISc, Bangalore, India.

KALLIKUPPA MUNIYAPPA SREENIVASA is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his bachelor of engineering (BE) in electronics and communication engineering (BE-E&C) from VTU, Mysore, India.

AMIT KUMBASI is a systems manager at Texas Instruments Dallas where he is responsible for developing subsystem solutions for Grid Infrastructure within Industrial Systems. Amit brings to this role his expertise with defining products, business development, and board level design using precision analog and mixed signal devices. He holds a master's in ECE (Texas Tech) and an MBA (University of Arizona).

9 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments**. If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
    1. Keep work area clean and orderly.
    2. Qualified observer(s) must be present anytime circuits are energized.
    3. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
    4. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
    5. Use stable and nonconductive work surface.
    6. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
    1. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
    2. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
    3. After EVM readiness is complete, energize the EVM as intended.

   WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.
3. Personal Safety
    1. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision	Page
• Updated Table 1 *Key System Specifications*: Changed parameter "Movements per hour assumed for lifetime calculation" to "Isolation type"	4

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265