TI Designs: TIDA-01445
Automotive High-Voltage Interlock Reference Design

Description

This reference design is a low BOM design that has good coverage of automotive interlock connection diagnosis. In hybrid or electric vehicles (HEV/EVs), battery management systems, traction inverters, DC-DC converters, onboard chargers, and other subsystems that operate at high voltages need to have interlock. Interlock is a current and voltage loop mechanism used to detect tampering or opening of the high-voltage equipment or service disconnect switch. This design covers generating and monitoring mechanism of high voltage interlock system.

Resources

TIDA-01445	Design Folder
TPS2H000-Q1	Product Folder
INA225-Q1	Product Folder
TPS7B6950-Q1	Product Folder
TPS7A1601-Q1	Product Folder
LM2903-Q1	Product Folder

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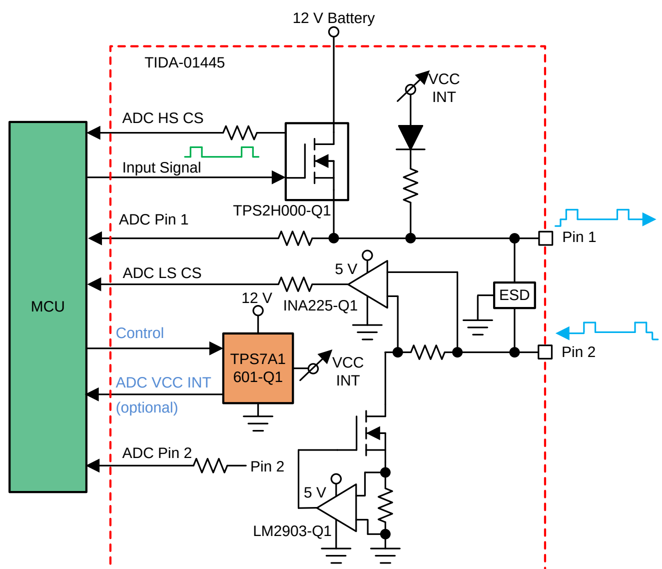
Features

- Unidirectional Interlock System
- Tristate Operation With Unidirectional System
- >97% Accurate Low-Side Current Sense at ≥ 5 mA
- >97% Accurate High-Side Current Sense at ≥ 5 mA
- Wide Coverage of Interlock Loop Fault Diagnosis
- Scalable Solution for Multiple Operation Modes
- Protection for Automotive Output Line Faults

Applications

- HEV/EV Onboard Charger
- Battery Management Systems
- HEV/EV Inverter
- HEV/EV DC-DC Converter



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1 System Description

Interlock is implemented in various applications such as heavy machinery factory installations, high-voltage smart grids, and relevant applications where there are heavy electrical installations or setups. Interlock is used to avoid damage to a person and equipment when the system is under use. Interlock supporting devices are categorized based on application and mechanism required for the system. It consists of electronic and mechanical components to detect tampering of high voltage system and prevent any failures.

To reduce the CO_2 emissions, most of the commercial and passenger vehicles are moving towards hybrid and electric vehicles (HEV/EVs). HEV/EVs have a high-voltage battery (> 60 V) to power the wheels. Automotive original equipment manufacturers (OEMs) need to create a guard zone to restrict the access to high-voltage operating environment. There is a need for interlock system to implement the guard zone for HEV/EVs. Every HEV/EV must have a disconnect switch within the reach of the driver or service personnel. This safety disconnect switch is linked with the interlock system of the vehicle, which disengages the high-voltage components.

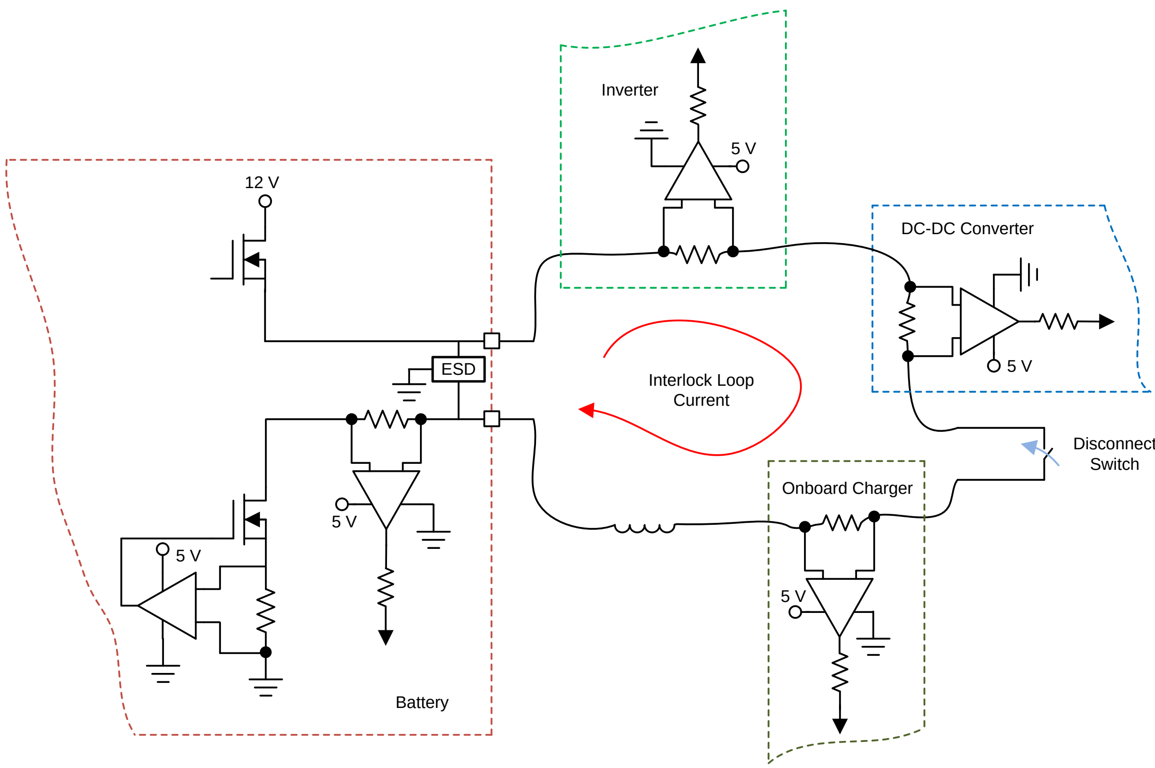


Figure 1. Typical Interlock System

As shown in Figure 1, the battery, traction inverter, DC-DC converters, and onboard charger all operate at a high voltage and need to have an interlock loop. Based on the safety architecture design of OEMs and component manufacturers, there can be a centralized and individual interlock system. A centralized interlock system has a common interlock loop shared with all high-voltage components. An individual or internal interlock mechanism helps ensure the assembly of each subsystem and proper assembly of complete component. A centralized interlock supports assembly of HEV/EV components and avoids any malfunctions during or post assembly stage. The state of an interlock loop plays an important role in the functioning of each high-voltage component. It is an important parameter in the boot sequence of the HEV/EV system. When the vehicle is in a running or parked state, if the interlock loop is broken due to a malfunction or known disconnection for service, the high-voltage battery turns off the power relays. The traction inverter, DC-DC converter, and onboard charger monitor the loop current. If an error is noticed in interlock loop current HEV-EV components will start fail safe turnoff sequence to stop the traction and discharge all high-voltage storage elements such as DC-Link capacitors.

A disconnect switch for the centralized high-voltage interlock must always be accessible to service personnel and first responders to bring the high-voltage system to a safe state. A crash signal can be interfaced to the interlock loop to turn off the high-voltage network to reduce the impact during and after a traffic accident. Unlike the industrial applications, interlock in an automotive environment needs to have protection for short circuit to low-voltage battery and ground. There is a need to have the diagnosis for appropriate functioning of interlock system to detect and differentiate possible failure.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX
Input voltage	12-V battery voltage DC	5 V	14 V	27 V
Interlock circuit current	14-V battery voltage, minimal load current of 100 µA	—	5mA	—
Accuracy of high-side current sense	R3 = 2.4 kΩ, Range: 5 to 100 mA	0.022%	0.82%	2.19%
Accuracy of low-side current sense	Input filter (R12, R13 = 10 Ω, C22 = 0.022 µF)	0.067%	1.093%	2.19%
Short circuit to ground	Interlock pin1 short to ground. Current limit from TPS2H000-Q1	—	117 mA	—
Short to battery	Extreme state of Interlock pin2 short to battery	53.8 mA	56 mA	75 mA
No load detection	Detection for TPS2H000-Q1	—	70 µA	75 µA
VCC INT	Configurable by potentiometer in TIDA-01445; Battery voltage must be 1 V higher than VCC INT	—	5 V	18 V

2 System Overview

2.1 Block Diagram

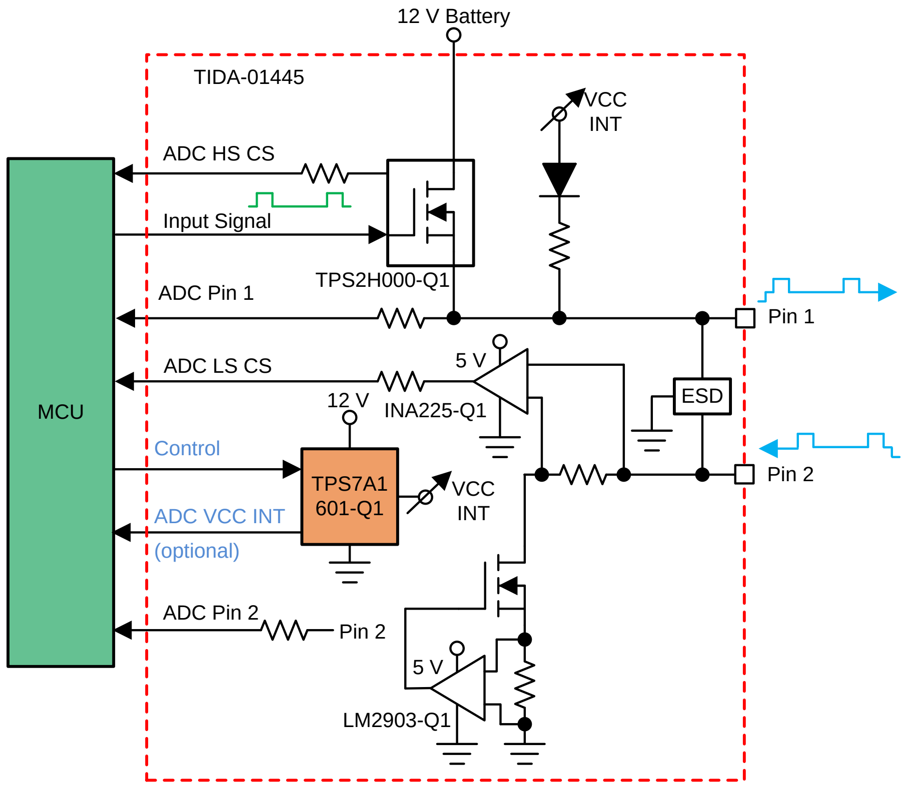


Figure 2. TIDA-01445 Block Diagram

2.2 Highlighted Products

2.2.1 TPS2H000-Q1

The TPS2H000-Q1 device is a smart high-side switch with internal charge pump and dual-channel integrated NMOS power FETs (see Figure 3). Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of the whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

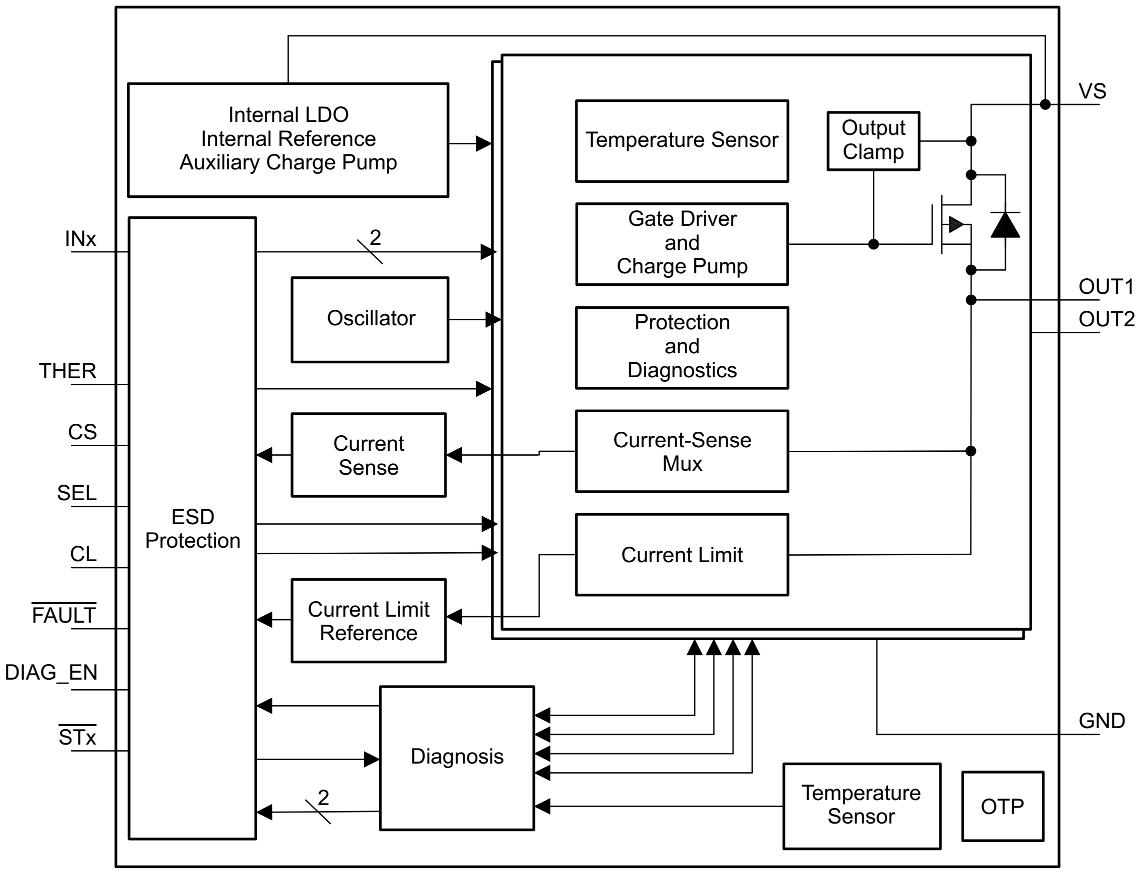


Figure 3. TPS2H000-Q1 Block Diagram

Key features of the TPS2H000-Q1 include:

- Dual-channel 1000-mΩ smart high-side switch with full diagnostics
- Ultra-low quiescent current: < 500 ηA
- Adjustable current limit with external resistor ±20% under >100-mA load
- Wide operating voltage: 3.4 to 40 V
- Thermal shutdown with latch-off option and thermal swing
- Short-to-ground protection by current limit (internal or external)
- Loss of ground and loss of battery protection

2.2.2 INA225-Q1

The INA225-Q1 is a voltage-output, current-sense amplifier that senses drops across current-sensing resistors at common-mode voltages that vary from 0 to 36 V, independent of the supply voltage (see Figure 4). The device is a bidirectional, current-shunt monitor that allows an external reference to be used to measure current flowing in both directions across a current-sensing resistor.

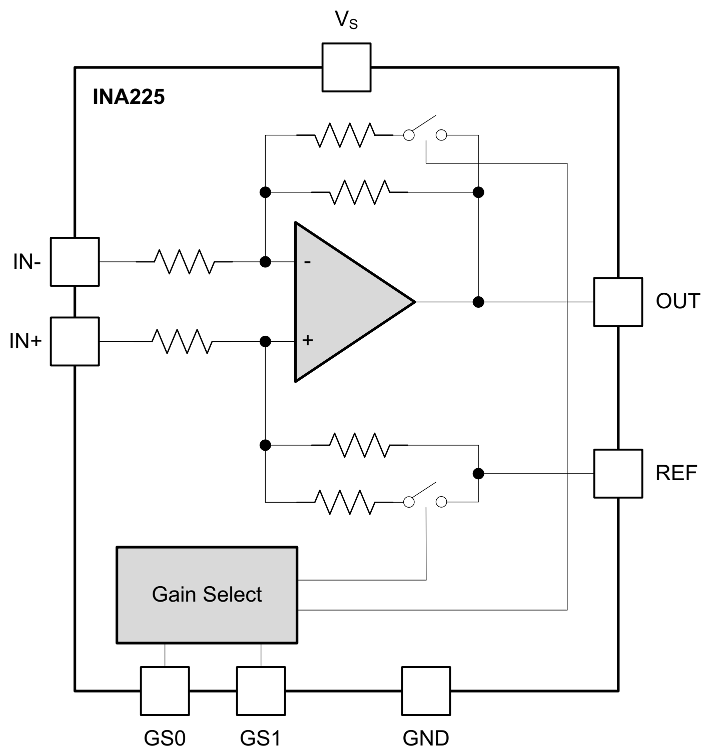


Figure 4. INA225-Q1 Block Diagram

Key features of the INA225 include:

- Offset voltage: ±150 µV (max, all gains)
- Offset voltage drift: 0.5 µV/°C (Max)
- Programmable gains of 25 V/V, 50 V/V, 100 V/V, and 200 V/V
- Bandwidth: 250 kHz (gain = 25 V/V)
- Quiescent current: 350 µA (max)

2.2.3 TPS7A1601-Q1

The TPS7A1601-Q1 device is designed for continuous or sporadic (power backup) battery-powered applications where ultra-low quiescent current is critical to extending system battery life (see Figure 5). This device offers an enable pin (EN) compatible with standard CMOS logic and an integrated open-drain active-high power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

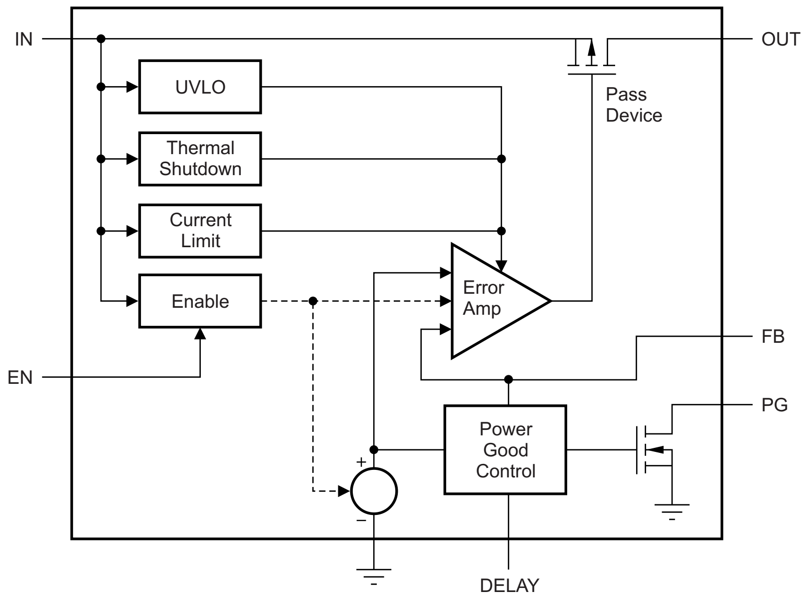


Figure 5. TPS7A1601-Q1 Block Diagram

Key features of the TPS7A1601-Q1 include:

- Ultra-low quiescent current: 5 μA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Adjustable output voltage: 1.2 to 18.5 V
- Current-limit and thermal shutdown protections

2.2.4 TPS7B6950-Q1

The TPS7B6950-Q1 high-voltage linear regulator operates over a 4- to 40-V input voltage range (see Figure 6). The device has an output current capability of 150 mA and offers fixed output voltages of 5 V. The device features a thermal shutdown and short-circuit protection to prevent damage during over temperature and over current conditions.

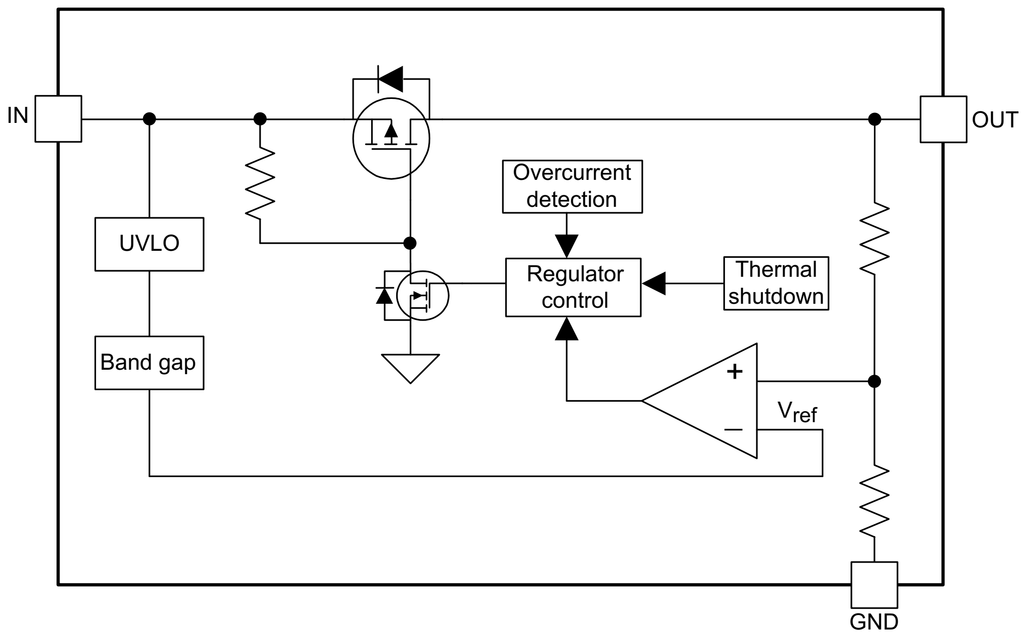


Figure 6. TPS7B6950-Q1 Block Diagram

Key features of the TPS7B6950-Q1 include:

- 4- to 40-V wide VI input voltage range with up to 45-V transient
- Low quiescent current (I_Q): 15-µA typical at light loads, 25-µA maximum under full temperature
- 450-mV typical low dropout voltage at 100-mA load current
- Integrated fault protection thermal shutdown, short-circuit protection
- Maximum output current: 150 mA

2.3 System Design Theory

The interlock system design is based on OEM requirements. This reference design can handle most user requirements with the given topology and diagnosis requirements. The topology of the reference design can be easily tweaked to get the required performance of interlock system. As shown in Figure 1, interlock is interfaced to every high-voltage component. Interlock signal is mostly generated and closely monitored by the battery because this source of power can quickly turn off the high-voltage power contactors.

2.3.1 TIDA-01445 Operation

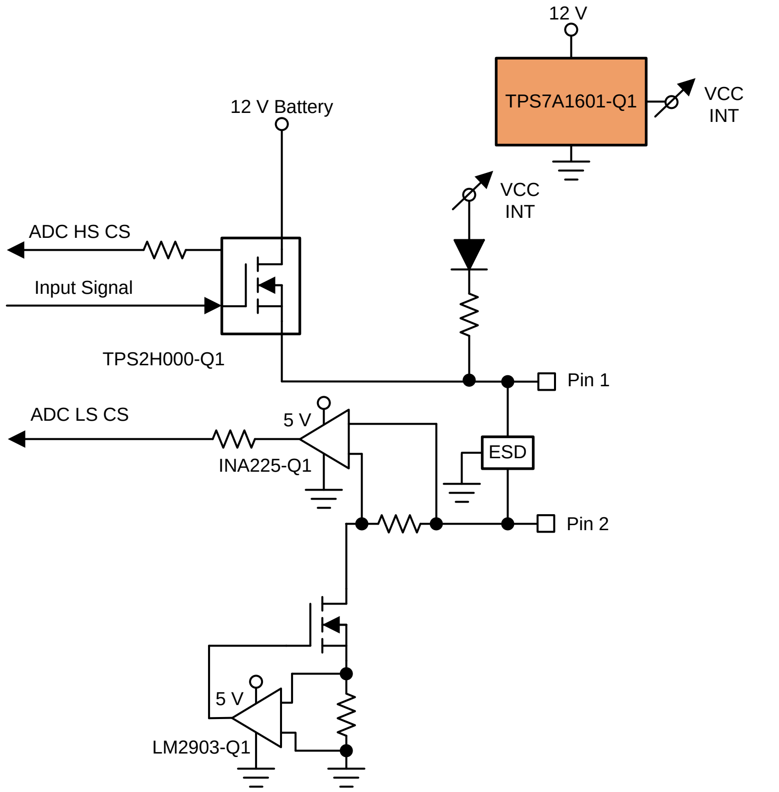


Figure 7. Functional Block Diagram

As shown in Figure 7, the TPS2H000-Q1 smart high-side switch is used to turn on the interlock loop current. The TPS2H000-Q1 with version B is used to monitor the high-side current of interlock loop. The TPS7A1601-Q1 is used to generate the variable voltage *VCC INT* to create the static state of the interlock system. Internal 5V supply from DC-DC/SBC can also be used for VCC INT. The INA225-Q1 is used to monitor the interlock loop current at low side and plays an important role in diagnosing the state of interlock. The LM2903-Q1 with an normal N-channel MOSFET is used to create the low-side current limit circuit.

This reference design is tested to support a unidirectional interlock system. The interlock load has a reference current and switch current, which can be attained by the static state and dynamic state of interlock operation, respectively.

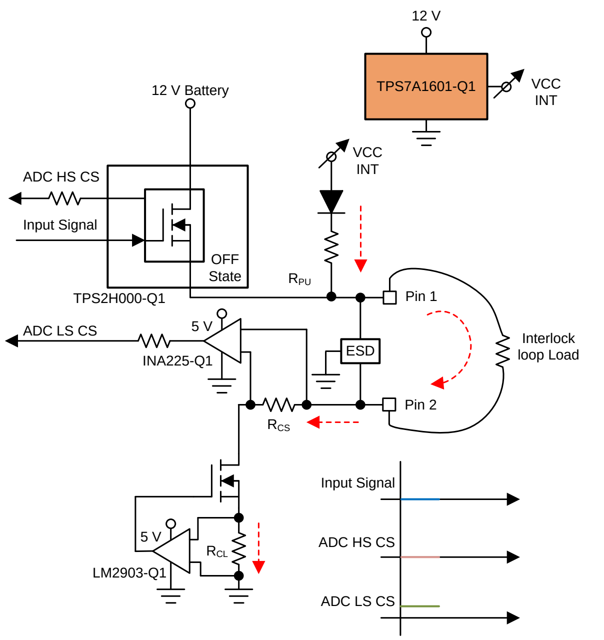


Figure 8. TIDA-01445 Static State

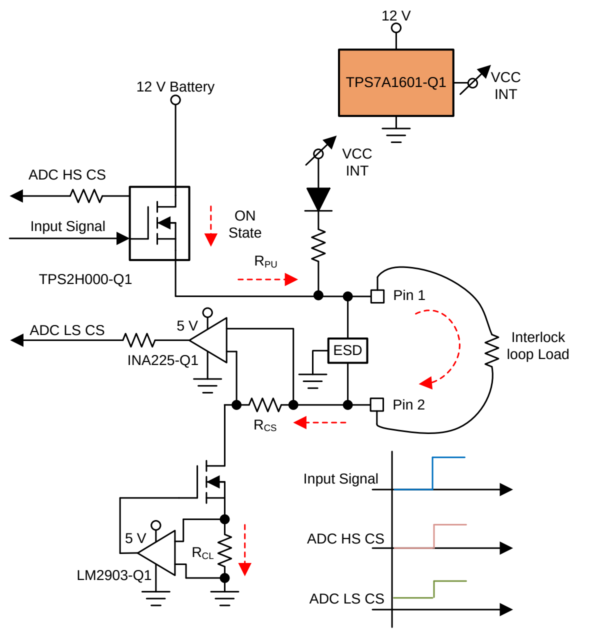


Figure 9. TIDA-01445 Dynamic State

The static state of interlock is seen when the input signal is zero as shown in Figure 8. In this case, interlock load current depends on VCC INT (variable), internal, and external resistance. The design has to make sure that the load current of static state interlock with minimum interlock load must be significantly less than the low-side current limit. The INA225-Q1 is operating at zero reference; as shown in Figure 8, ADC LS CS is purely an interlock current. This TI Design can allow the load current of the static state interlock load current to change by varying the VCC INT. Runtime configurable VCC INT supports to improve the diagnosis at high interlock load resistance.

The dynamic state of interlock can been achieved by toggling the input of high-side switch as shown in Figure 9. When input signal is high, the high-side switch turns on, which increases the interlock loop current. Based on the design and interlock loop load, the interlock load current is limited by the low-side current limiter. Change in the load current can be monitored in the smart high-side switch and current sense INA225-Q1 at low side.

Interlock state can be monitored by interfacing the high-side current sense, interlock pin 1 voltage, interlock pin 2 voltage, and low-side current sense. If the VCC INT is run-time variable, it can also be interfaced to the ADC input to diagnose the complete board. Based on OEM and safety requirements for interlock, the number of ADC signals interfaced to the ADC can be reduced.

Important parameters to monitor for an interlock system are loop current and load resistance. ADC LS CS gives the interlock loop current with the defined gain set in the hardware (see Equation 5 and Equation 7 for more details). Loop resistance can be attained by two methods.

2.3.1.1 *Method 1: Fewer ADC Pins*

In static state, the interlock loop is always less than the current limiter of the low-side circuit. Interlock load resistance is as per Equation 1:

$$\text{Interlock Load Resistance}\left(R_{LOAD}\right) = \frac{\text{VCC INT} - \text{Diode Drop}}{\text{ADC LC CS}} - R_{PU} - R_{CS} - R_{CL} \qquad (1)$$

This method has limitations in accuracy for the complete range of interlock load resistance. Tolerance of resistors (R_{PU}, R_{CS}, R_{CL}) can impact accuracy of calculations on interlock load resistance.

2.3.1.2 Method 2: More Accurate and Independent

In this method, interlock resistance can be measured irrespective of the system state. Interlock pin 1, pin 2, and interlock load current can be used for Equation 2:

$$\text{Interlock Load Resistance}\left(R_{LOAD}\right)=\frac{\text{ADC Pin 1}-\text{ADC Pin 2}}{\text{ADC LC CS}} \quad (2)$$

Interlock pin 1 and pin 2 can be directly interfaced to the microcontroller or they can be interfaced through a differential amplifier to save microcontroller pins. Use this method for better accuracy of interlock resistance.

2.3.2 Protection and Diagnosis

This reference design is built to have protection for most of the automotive output lines. As interlock wires are routed across the multiple subsystems of HEV/EVs, there is room for errors in the wiring harness to have a short circuit or open connection.

2.3.2.1 Short to Ground (SCG)

Interlock lines can be short to ground due to any external fault connection or wanted pulled down of interlock pin in an external subsystem. When interlock pins are short to ground, current from the 12-V battery is limited by the smart high-side switch, TPS2H000-Q1.

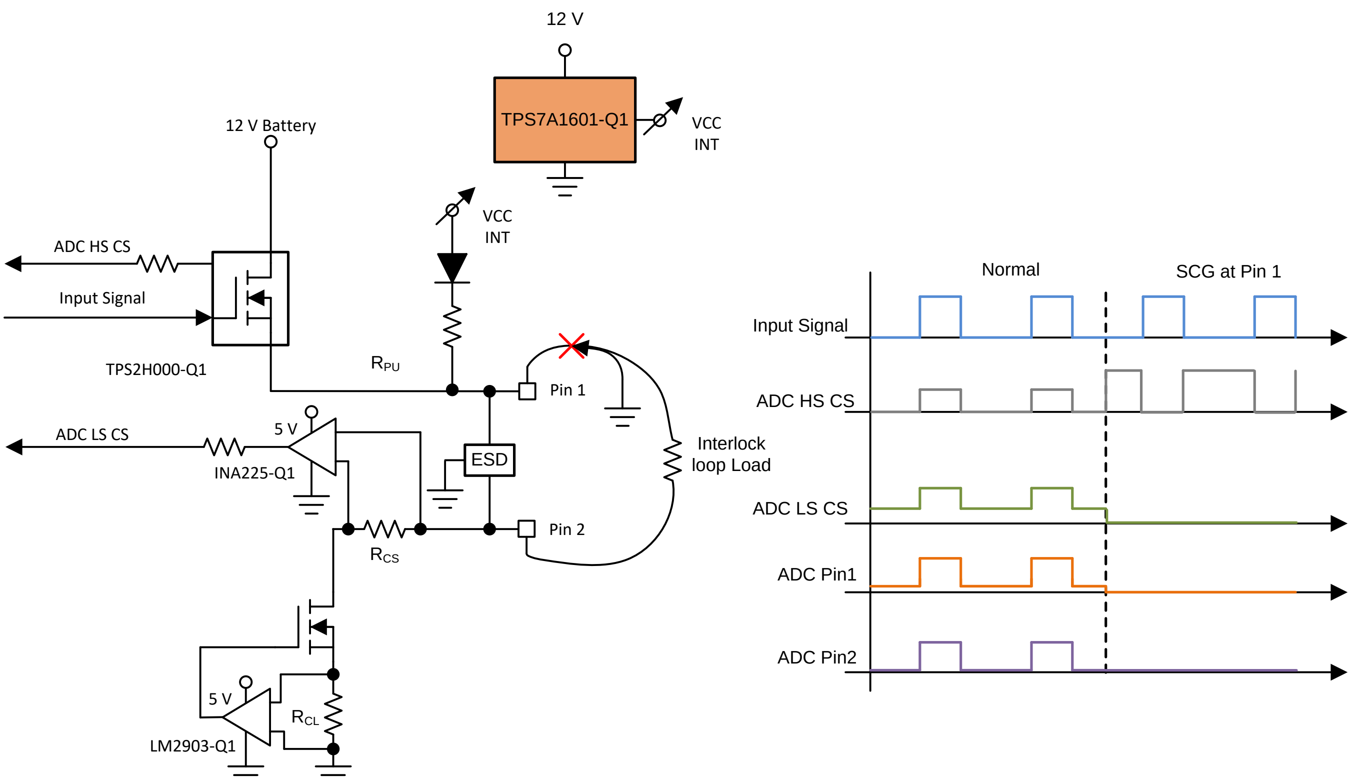


Figure 10. Interlock Line Short Circuit to Ground

As shown in Figure 10, interlock loop current is zero from the point, which was impacted by short circuit. ADC LS CS, which monitors the loop current, will be zero. Pullup resistor R_{PU} must be set to limit the current from VCC INT and handle the power dissipation during the short-circuit-to-ground conditions.

No interlock loop current measured from ADC LS CS and high supply current from the high-side switch measured by ADC HS CS can be considered as significant parameters to consider this as short circuit to ground.

2.3.2.2 Short to Battery (SCB)

Due to improper wiring connections, problems in the connector and service personnel can lead to short the 12-V battery to interlock pins. This reference design can detect and protect the design for short-to-battery connections until the 12-V battery. System performance can vary when higher voltage batteries (24 V, 48 V, and so on) are shorted to interlock pins.

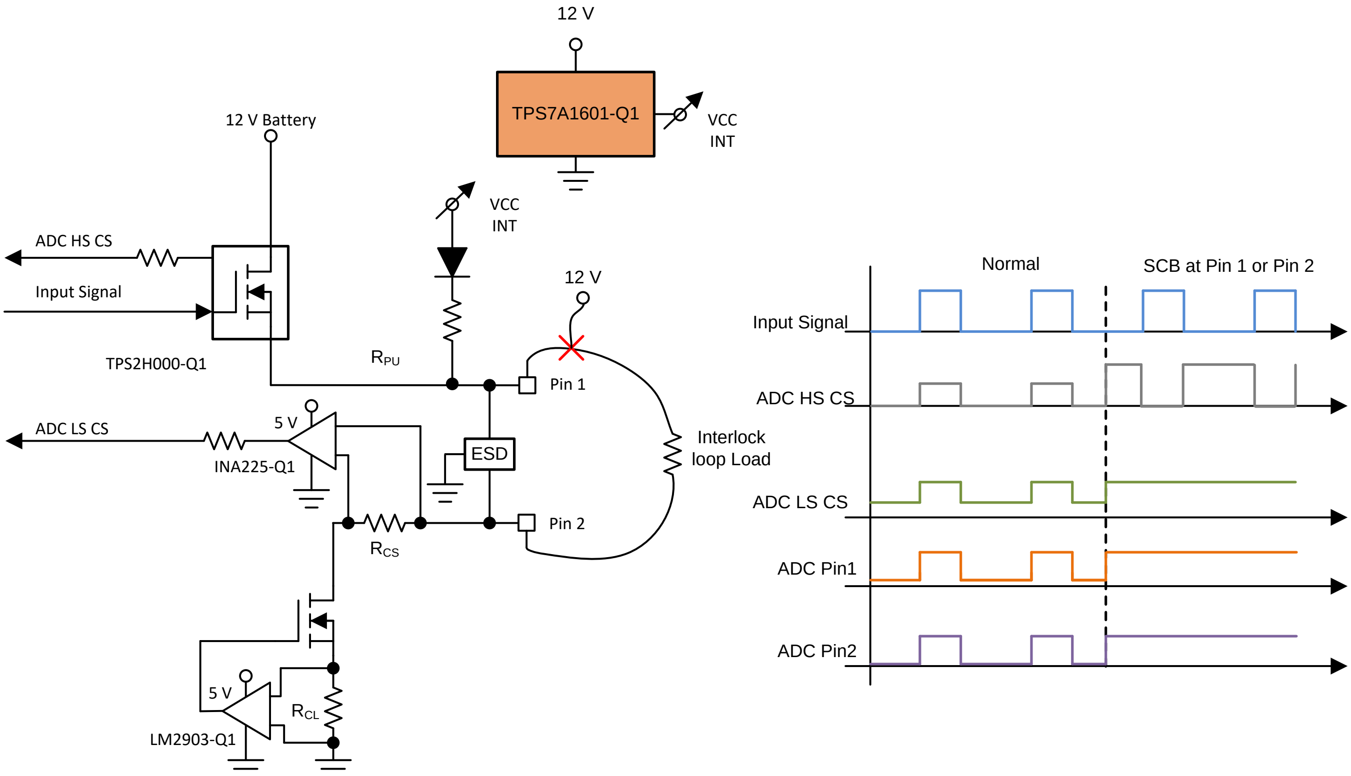


Figure 11. Interlock Line Short to 12-V Battery

During short-to-battery conditions, battery voltage is directly seen across the interlock pins irrespective of the state of input signal. The current limit of the low-side foldback circuit limits the current in pin 2 and the low-side circuit. Short circuit to battery can happen anywhere between interlock pin 1 and pin 2. Based on the location of the error and battery voltage, power dissipation in the low-side MOSFET can vary.

A sign for short to battery at the interlock load is when the interlock load current does not toggle based on the input signal. Impact of the short to battery error can be diagnosed based on the voltage difference between pin 1 and pin 2. The location of the short-to-battery error can be estimated based on the resistors chosen in the high-voltage components. ADC pin 1 and ADC pin 2 voltages shown in Figure 11 can vary based on the interface circuit from interlock pin 1 and pin 2, respectively.

2.3.2.3 Open Load

An open load condition can happen to due to a service disconnect switch, disconnecting the high-voltage connectors, or due to loose connections in wiring harness. It is hard to diagnose the location of an open load error because the behavior of the circuit is same in all conditions.

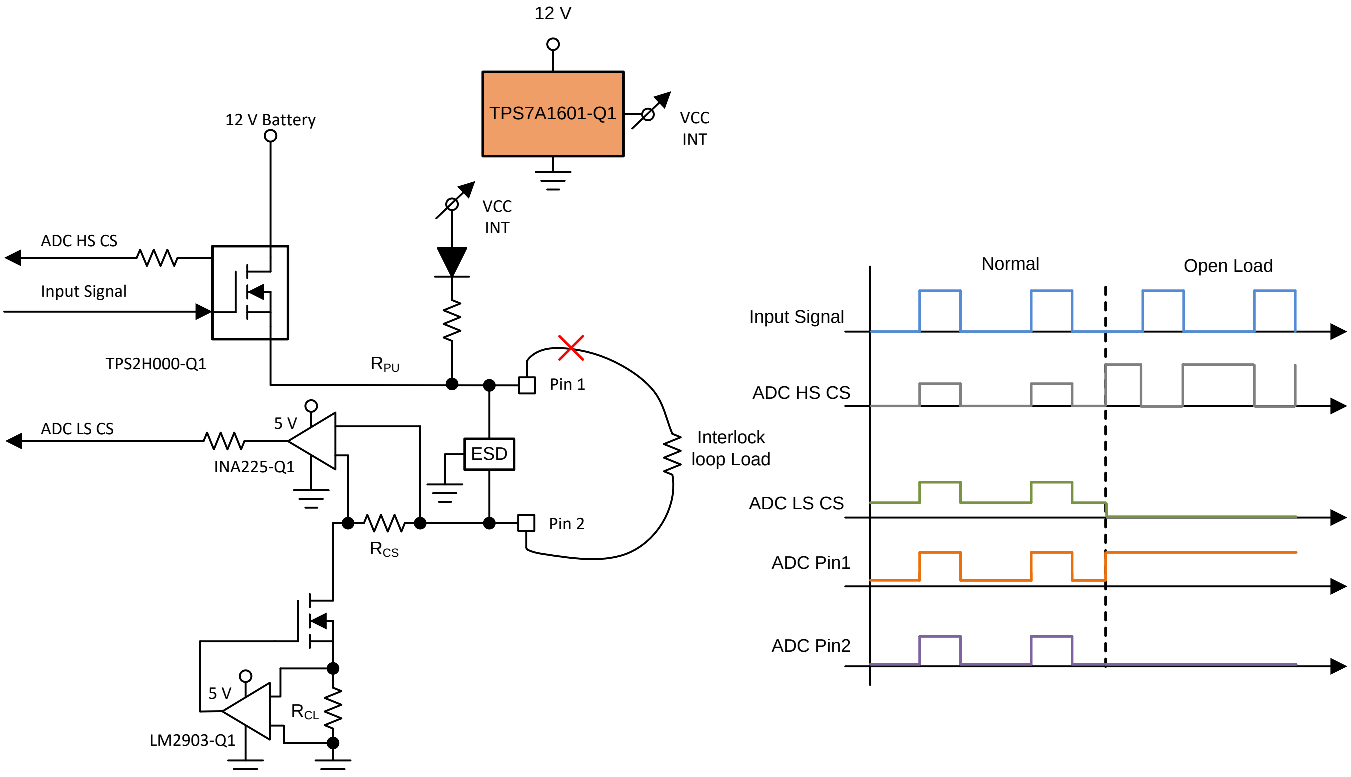


Figure 12. Interlock Line Open Load

The interlock loop current is zero during the open load conditions. The high-side switch toggles based on the input signal from the controller. ADC pin 1 voltage depends on VCC INT, R_{PU}, and the interface circuit to the TPS2H000-Q1.

Behavior of ADC LS CS is same in both open load and short circuit to ground. Behavior of ADC HS CS is the difference in open load and short circuit to ground.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

Figure 13 is categorized into three sections to explain the design more towards the application:

- Interlock high side
- Interlock low side
- Interlock power

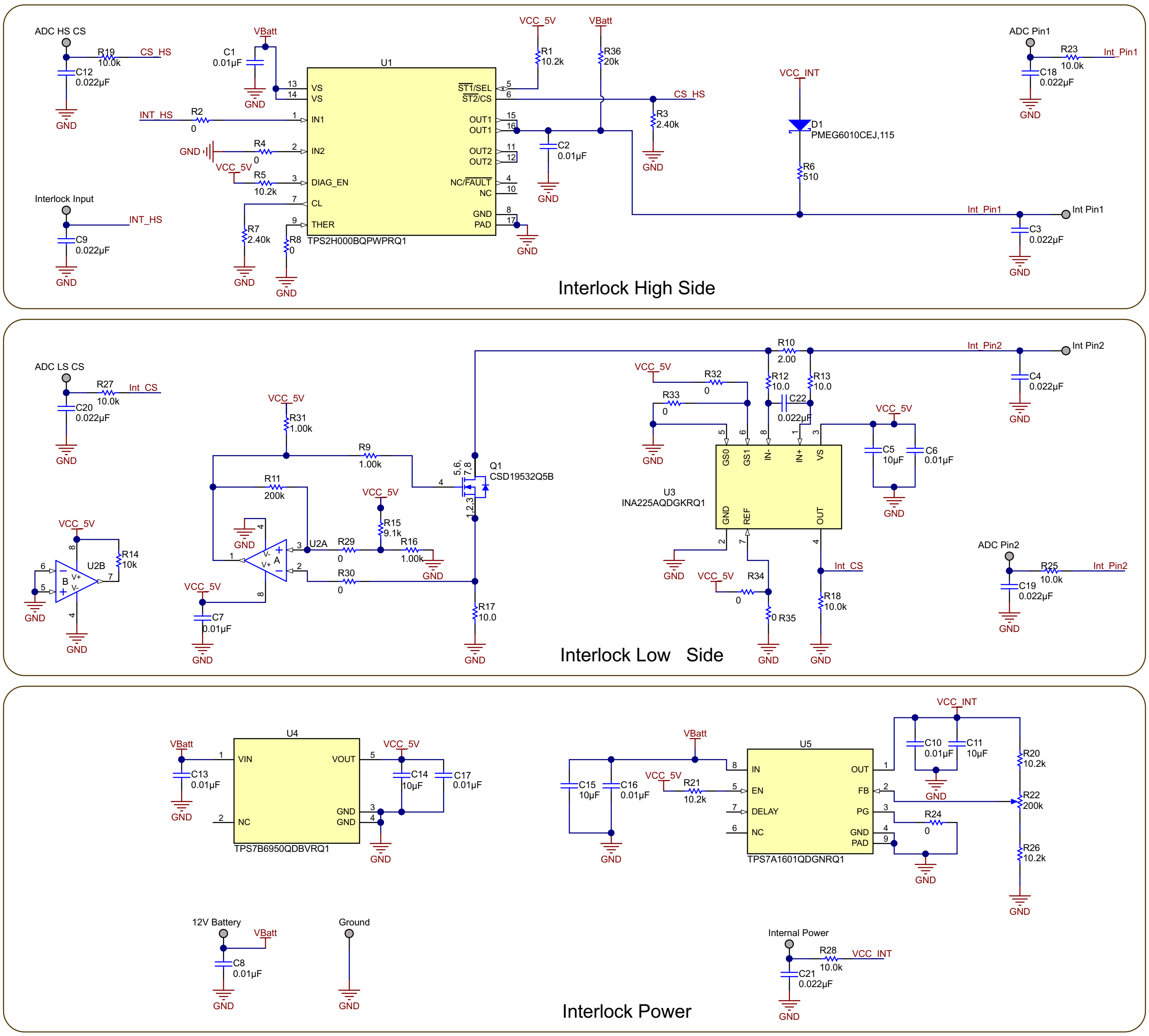


Figure 13. TIDA-01445 Schematic

The TPS2H000-Q1 is used for the interlock high-side switch. Current sense and current limit are critical features to consider when using the TPS2H000-Q1 for interlock applications. R7 is used to limit the current from U1 (TPS2H000-Q1) during the overload conditions. As per the TPS2H000-Q1 datasheet, the external resistor R7 (as per the reference design) sets the current limit threshold.

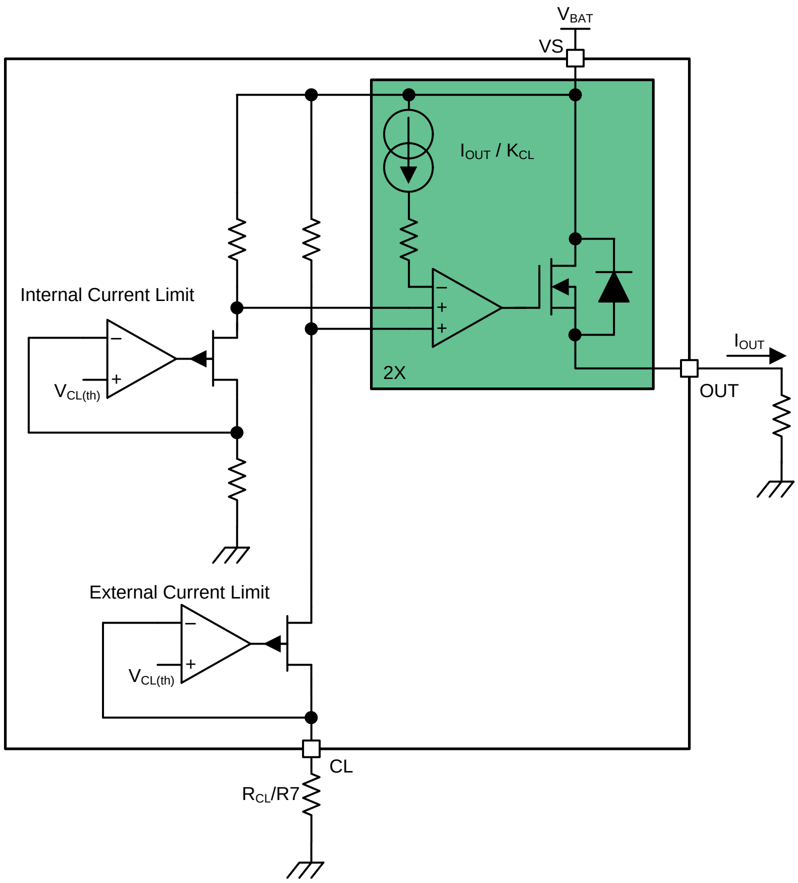


Figure 14. TPS2H000-Q1 Current Limit

The internal current limit is not used in this reference design. The external current limit is used to avoid the high-load currents during short circuit to ground conditions. $V_{CL(th)}$ is the internal band-gap voltage where as K_{CL} is the ratio of the output current and the current limit set value, which is mostly constant across temperature and battery voltage.

$$\text{Current Limit Resistor R7 } (R_{CL}) = \frac{V_{CL(th)} \times K_{CL}}{I_{LOAD}\,(I_{LIMIT})} \tag{3}$$

The current-limit ratio (K_{CL}) is typically 300. The typical $V_{CL(th)}$ current limit internal threshold ($V_{CL(th)}$) is 0.8 V. Interlock currents are typically low. The current limit set for the reference design is 100 mA by populating R7 with 2.4 kΩ. Tolerance of current limit resistor has an impact on the accuracy of the current limit. As per the TPS2H000-Q1 datasheet, by default the device has a ±20% tolerance for a current limit of 100 mA. Consider the current limit of 100 mA with tolerance for peak power dissipation to components in line from the battery to possible short circuit to ground.

The current sense load resistor R3 is used to monitor the current of TPS2H000-Q1 (version B). The current monitor circuit is shared between two channels and can be selected based on the input to pin 5 (Sel). In this reference design, only one channel is used to drive the interlock loop current. Pin 5 can be left open or shorted to ground for measuring the current in channel 1. The integrated current mirror can source 1 / K_{CS} of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. K_{CS} is the ratio of the output current and the sense current. The ratio is a constant value across the temperature and supply voltage.

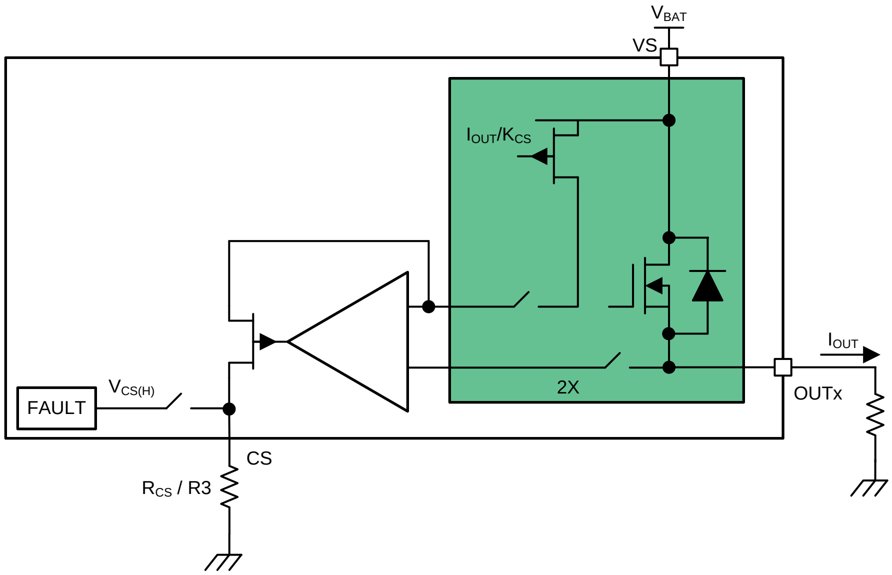


Figure 15. TPS2H000-Q1 Current Sense

R3 can be selected based on the range of load current. In the interlock application of this reference design, the current limit is set to 100 mA. Current sense resistor R3 must be selected to get the appropriate range of current measurements until 100 mA. V_{CSH} is enabled when the TPS2H000-Q1 has reached the current limit, indicating an overload fault. In normal operation, the interlock voltage at CS (ADC HS CS) is always less than 4 V (based on selecting R_{CS} / R3). Interlock high-side load current is calculated as per Equation 4:

$$\text{High-Side Load Current} = \frac{\text{ADC HS CS} \times K_{CS}}{\text{R3}} \tag{4}$$

For the TPS2H000-Q1, K_{CS} is typically 80, whereas current sense accuracy varies based on load current. For 5 mA of load current, accuracy can be ±10%; for 25 mA, it can be as good as ±3%; and in the best case for 100 mA, it can have a maximum deviation of ±2.5%. Tolerance of R3 and a signal conditioning circuit play a role for the final calculation of accuracy.

VCC INT is the internal power supply created from the TPS1601-Q1. This supply is an adjustable output voltage based on the feedback voltage. R20, R26, and potentiometer R22 is used to set the output voltage VCC INT. Potentiometer R22 is not ideal for mass production to change the output voltage of LDO. The output voltage of the TPS7A1601-Q1 can be set constant based on the design of the system. VCC INT can be varied in run time by using one of the options shown in Figure 16.

- Option 1: Feedback pin of TPS7A1601-Q1 can be controlled by a PWM output of a microcontroller by interfacing with the MOSFET and resistor. The duty cycle of the PWM can vary the output voltage of the TPS7A1601-Q1 in run time. The precision of LDO output voltage is not mandatory as the VCC INT is used to define the Interlock static state current. Option 1 needs an additional timer resource of the controller along with ADC input for feedback.

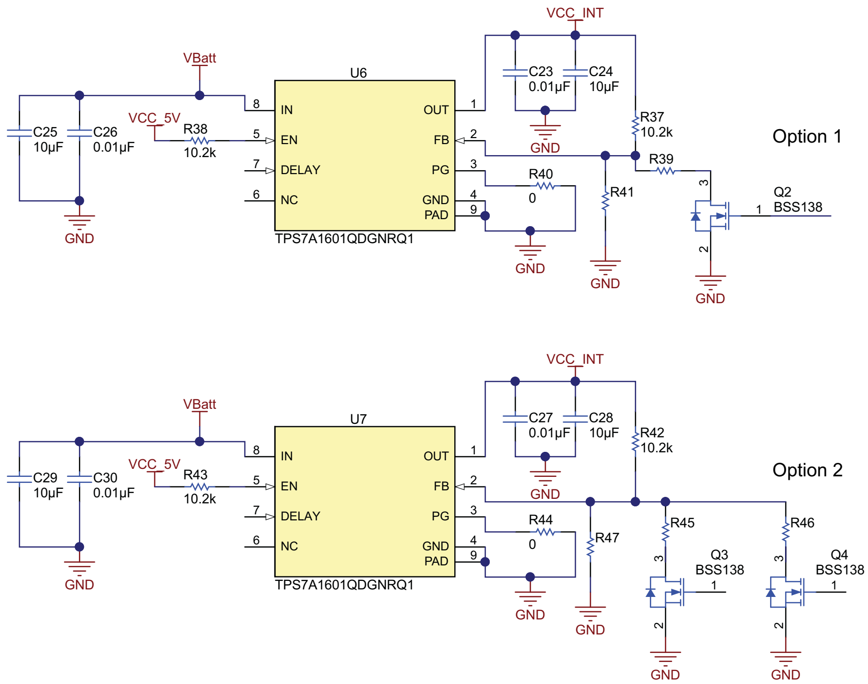


Figure 16. Configurable VCC INT

- Option 2: Output voltages of VCC INT are fixed by the design with multiple resistive ladders. MOSFETs can be varied based on the requirement of output voltage. This option needs multiple digital output pins of the microcontroller to control the MOSFETs.

Diode D1 and R6 are used to support the static state of interlock. D1 is used to avoid any damage to the LDO (TPS7A1601-Q1) and support unidirectional current through R6. R6 is used to protect the LDO (TPS7A1601-Q1) during the short circuit to ground conditions. As shown in Figure 8, interlock static current for the design is shown as per Equation 5:

$$\text{Interlock Static State Current} = \frac{\text{VCC INT} - \text{Vfd}}{\text{R6} + \text{R10} + \text{R17} + R_{\text{DSon(Q1)}} + R_{\text{LOAD}}} \tag{5}$$

A change in R6 and R_{LOAD} has a direct impact on the current of the interlock static state. For a given VCC INT and minimum interlock static current, R6 must be fixed to support the maximum interlock load resistor R_{LOAD}. During short circuit to ground conditions, R6 reaches its maximum power dissipation; consider this parameter while selecting the package of R6 and D1.

$$\text{Max Power Dissipation of R6 (during SCG)} = \left(\frac{\text{VCC INT} - \text{Vfd}}{\text{R6}}\right)^2 \times \text{R6} \tag{6}$$

The INA225-Q1 is used to monitor the interlock load current. Shunt sensor R10 must be set based on the type of interlock, unidirectional or bidirectional. For a bidirectional interlock, the reference or offset and a single range for interlock load currents play an important role in calculating the shunt resistor. The reference design is a unidirectional interlock system. R35 is populated to set the reference to zero.

This reference design is built to support interlock load currents from 0 to 100 mA. The maximum current flown in R10 can be set by the current limit circuit used in the interlock low side. R32 and R33 are used to set the gain stage of U3 (INA225-Q1). This reference design can set gain stages of 25 and 50. The design has been tested for a gain of 25 by populating only R33. R12, R13, and C22 are used to filter the noise of the interlock current. R12 and R13 contribute to the offset based on input bias currents of the INA225-Q1. The values of R12 and R13 must be kept below 10 Ω. C22 must not be more than 50 nF as this affects the response time of the interlock output current.

Neglecting errors due to bias currents (R12 and R13) and a leakage drop of R27, the interlock current can be calculated from ADC LS CS using Equation 7:

$$\text{Interlock Load Current } \left(I_{LOAD}\right) = \frac{\text{Voltage of ADC LS CS}}{R_{SHUNT}\left(R10\right) \times \text{Gain of INA225}} \tag{7}$$

When V_{SENSE} is 0 mV, the INA225-Q1 has a typical CMR of 105 dB, a max offset voltage of ±150 µV, a typical Input bias currents of 72 µA, and a typical input offset current of ±0.5 µA. The maximum gain error for the INA225-Q1 is 0.15% for 25 and 50. Tolerances of R10, R12, and R13 also contribute to calculating the error for interlock load current.

R17 is the shunt current sense element for the low-side current limit circuit. The LM2903 is used to compare the current sense input and control Q1. R15 and R16 are used to provide the reference to current limit. R11 provides hysteresis to the current limit circuit, which supports smooth operation. The current limit of low-side circuit can be modified by using two parameters:

- Change the current limit resistor.
- Change the reference voltage.

Current limit resistor R17 has to be defined appropriately based on interlock load current and reference. The very low value of the shunt resistor R17 results in a need for low reference voltage for a given interlock load current. For 50 mA of interlock current limit value, R17 has been populated with a 10-Ω resistance. Set the reference voltage for 0.5 V. The max value of R17 is limited by the minimum battery voltage, minimum interlock current for diagnosis, and maximum interlock load resistance.

Changing the reference voltage is possible by changing the R15 and R16 resistors. Accuracy of the reference voltage depends on VCC and tolerance of R15 and R16 resistors. Availability of an exact resistor value is one of the limiting factor for reference voltage.

To improve the stability of the current limit circuit during short to battery conditions, an additional resistor can be added on pin 2 line with appropriate power dissipation. For any additional resistors, consider the criteria to meet the minimum interlock load current during low battery voltages.

3.2 Testing and Results

This reference design is tested in multiple ways to check the normal operation, reliability, and its ability to diagnose an application.

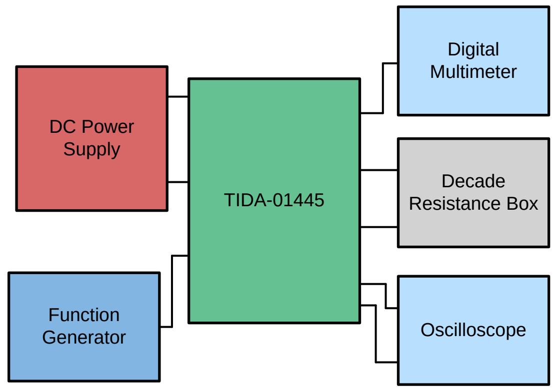


Figure 17. TIDA-01445 Test Setup

Accuracy of the high-side and low-side current sense circuits are calculated to check the performance of the TIDA-01445. The high-side switch is turned on continuously, and interlock load resistance is varied to have a constant current in both high- and low-side switches. Analog values for high-side and low-side current sense are monitored by an oscilloscope. A digital multimeter is used to monitor the interlock load current.

Table 2. Accuracy Calculations

INTERLOCK CURRENT	MEASURED OSCILLOSCOPE		CALCULATED CURRENT		ACCURACY	
	HIGH-SIDE	LOW-SIDE	HIGH-SIDE	LOW-SIDE	HIGH-SIDE	LOW-SIDE
4.991	0.153	0.255	5.100	5.10	2.194	2.194
10.050	0.304	0.510	10.133	10.20	0.829	1.493
14.997	0.454	0.763	15.133	15.26	0.909	1.754
20.060	0.606	1.017	20.200	20.34	0.698	1.396
24.996	0.755	1.254	25.167	25.08	0.683	0.336
30.020	0.899	1.500	29.967	30.00	0.178	0.067
40.030	1.203	1.993	40.100	39.86	0.175	0.425
50.089	1.503	2.479	50.100	49.58	0.022	1.016
55.000	1.679	2.718	55.960	54.36	1.758	1.164

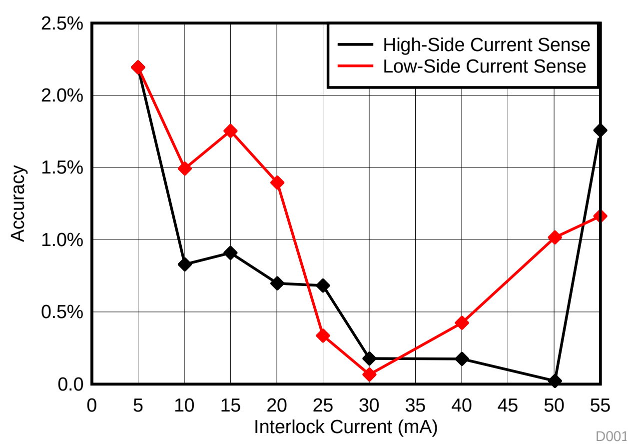


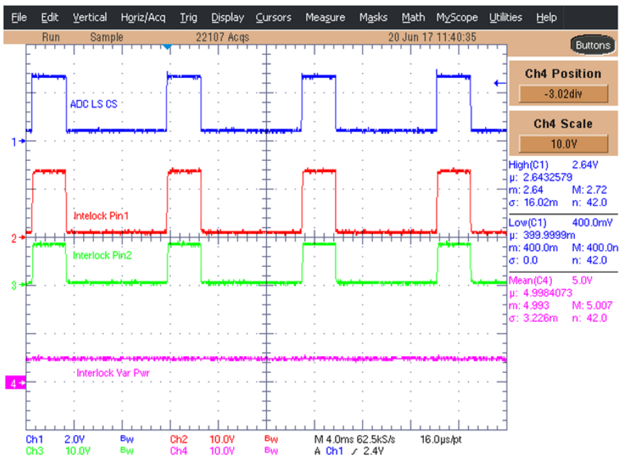
Figure 18. Accuracy of High-Side and Low-Side Current Sense

3.2.1 Performance Tests

3.2.1.1 VCC INT

Interlock performance for variable interlock static currents is only possible by changing the variable power supply to interlock. The potentiometer of the reference design is varied to change the variable supply for interlock.

NOTE: For the following tests:
Battery voltage = 14 V, Interlock load resistance = 100 Ω, Frequency = 100 Hz



CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 400 mV, high = 2.64 V

8-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 8.03 mA

Figure 19. Interlock VCC at 5 V

CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 480 mV, high = 2.64 V

9.6-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 9.63 mA

Figure 20. Interlock VCC at 6 V

CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 560 mV, high = 2.64 V

11.2-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 11.23 mA

Figure 21. Interlock VCC at 7 V

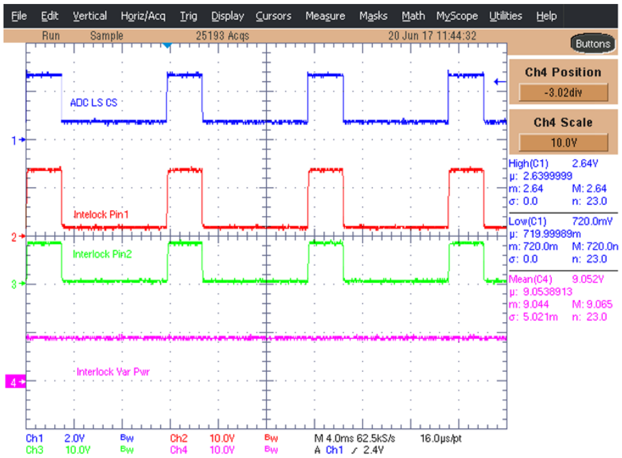
CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 640 mV, high = 2.64 V

12.8-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 12.841 mA

Figure 22. Interlock VCC at 8 V



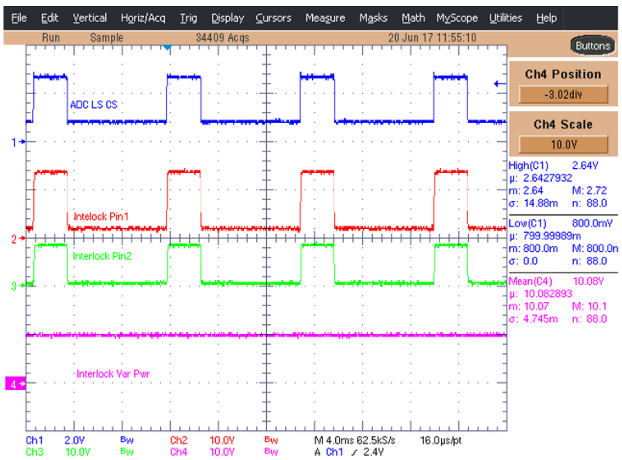
CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 720 mV, high = 2.64 V

14.4-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 14.446 mA

Figure 23. Interlock VCC at 9 V



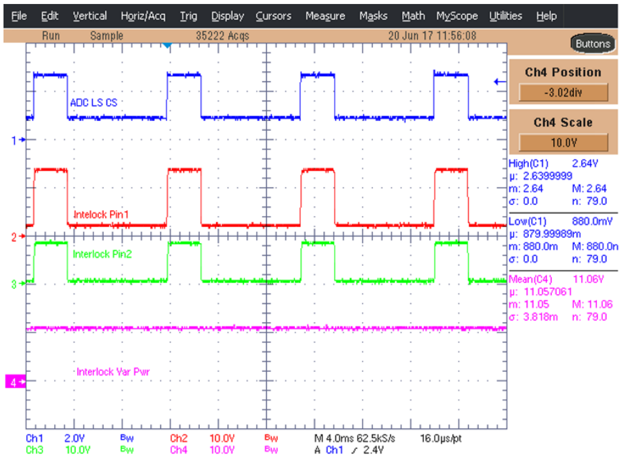
CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 800 mV, high = 2.64 V

16-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 16.05 mA

Figure 24. Interlock VCC at 10 V



CH1: Interlock load current
CH2: Voltage at interlock pin 1
CH3: Voltage at interlock pin 2
CH4: Interlock variable voltage

NOTE: ADC LS CS: Low = 880 mV, high = 2.64 V

17.6-mA current flown in static state, 52.8 mA during dynamic state

Theoretical static current: 17.656 mA

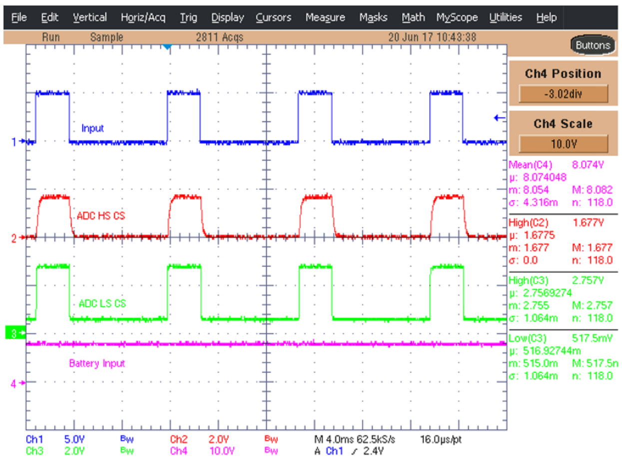
Figure 25. Interlock VCC at 11 V

These figures shows an increase in the interlock static current. Based on interlock resistance required by OEM, R6 and VCC INT can be set to get the required static state current.

3.2.1.2 Variable Battery Voltage

The reference design is checked at variable battery voltages. The potentiometer for the variable interlock supply (VCC INT) remains constant.

NOTE: For the following tests:
Battery voltage = Variable, Interlock load resistance = 100 Ω , Frequency = 100 Hz



CH1: Interlock input to high side
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Battery input voltage

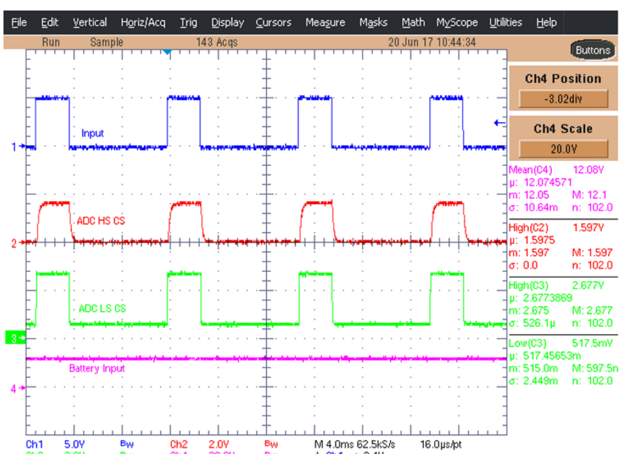
NOTE: ADC HS CS: High = 1.677 V

ADC LS CS: Low = 517.5 mV, high = 2.757 V

Static state: 10.34 mA

Dynamic state: 55.9 mA as per high side, 55.14 mA as per low-side current sense

Figure 26. TIDA-01445 at 8 V



CH1: Interlock input to high side
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Battery input voltage

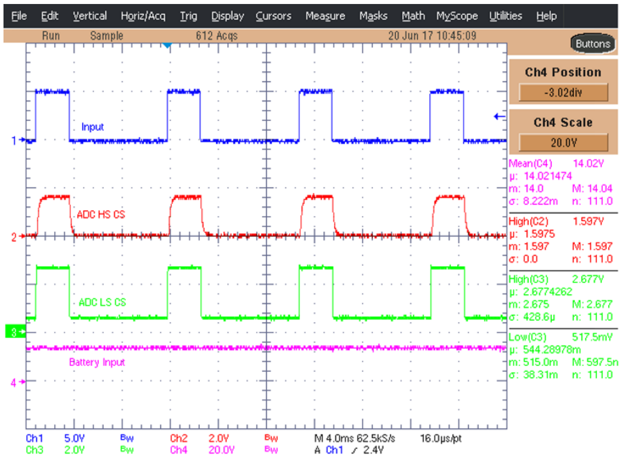
NOTE: ADC HS CS: High 1.597 V

ADC LS CS: Low = 517.5 mV, high = 2.677 V

Static state: 10.35 mA

Dynamic state: 53.233 mA as per high side, 53.34 mA as per low side current sense

Figure 27. TIDA-01445 at 12 V



CH1: Interlock input to high side
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Battery input voltage

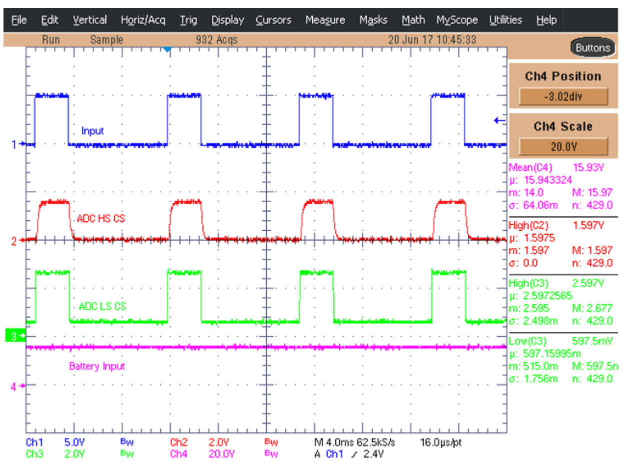
NOTE: ADC HS CS: High = 1.597 V

ADC LS CS: Low = 517.5 mV, high = 2.677 V

Static state: 10.35 mA

Dynamic state: 53.233 mA as per high side, 53.54 mA as per low-side current sense

Figure 28. TIDA-01445 at 14 V



CH1: Interlock input to high side
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Battery input voltage

NOTE: ADC HS CS: High = 1.597 V

ADC LS CS: Low = 597.5 mV, high = 2.597 V

Static state: 11.95 mA

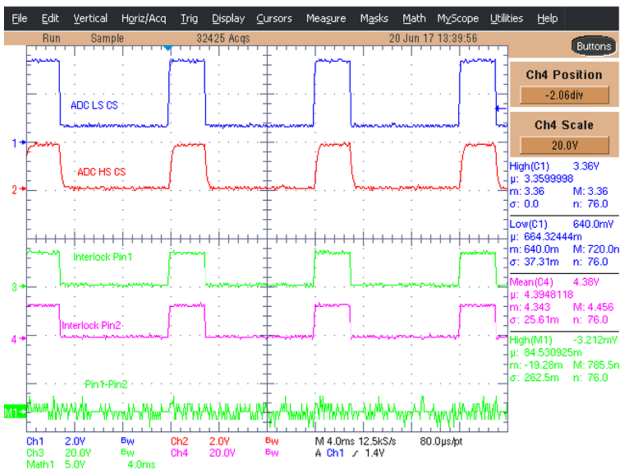
Dynamic state: 53.233 mA as per high side, 51.94 mA as per low-side current sense

Figure 29. TIDA-01445 at 16 V

3.2.1.3 Variable Interlock Resistance

This reference design is checked at variable interlock load resistance.

NOTE: For the following tests:
Battery voltage = 14 V, VCC INT = 7 V, Frequency = 100 Hz



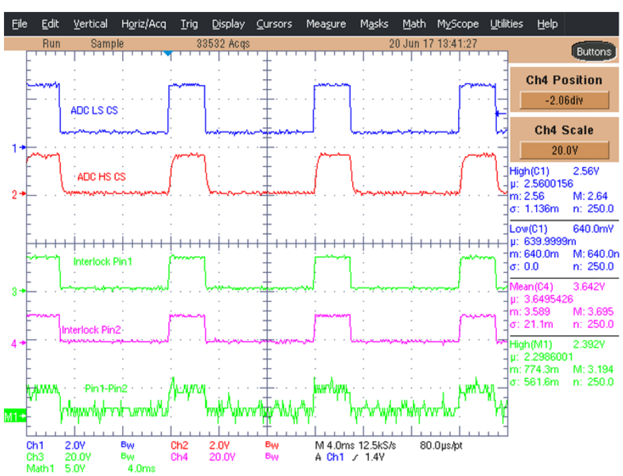
CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Interlock pin 2
M1: Interlock pin 1 - Interlock pin 2

NOTE: ADC LS CS: Low = 640 mV, high = 3.36 V

Static state: 12.8 mA

Dynamic state: 67.2 mA

Figure 30. TIDA-01445 at 0-Ω Load Resistance



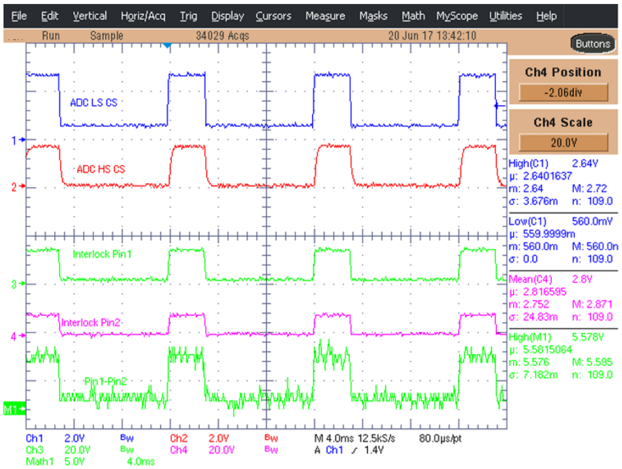
CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Interlock pin 2
M1: Interlock pin 1 - Interlock pin 2

NOTE: ADC LS CS: Low = 640 mV, high = 2.56 V

Static state: 12.8 mA

Dynamic state: 51.2 mA

Figure 31. TIDA-01445 at 50-Ω Load Resistance



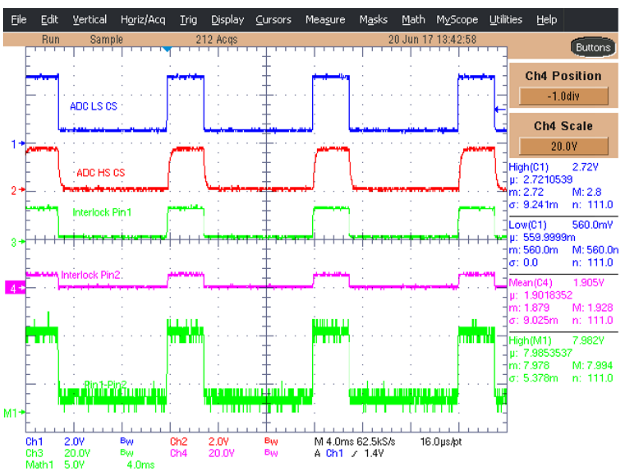
CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Interlock pin 2
M1: Interlock pin 1 - Interlock pin 2

NOTE: ADC LS CS: Low = 560 mV, high = 2.64 V

Static state: 11.2 mA

Dynamic state: 52.8 mA

Figure 32. TIDA-01445 at 100-Ω Load Resistance



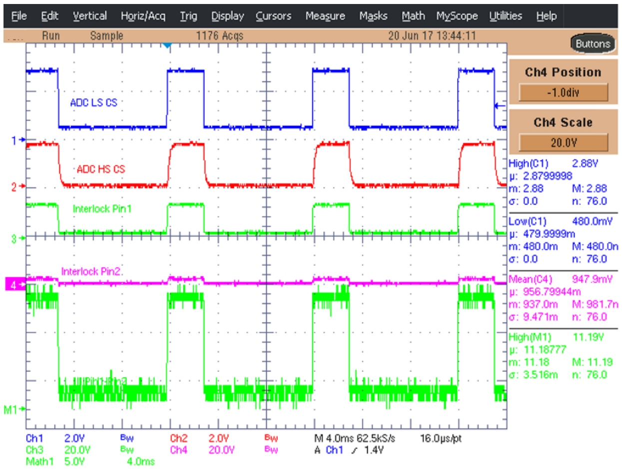
CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Interlock pin 2
M1: Interlock pin 1 - Interlock pin 2

NOTE: ADC LS CS: Low = 560 mV, high = 2.64 V

Static state: 11.2 mA

Dynamic state: 52.8 mA

Figure 33. TIDA-01445 at 150-Ω Load Resistance



CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Interlock pin 2
M1: Interlock pin 1 - Interlock pin 2

NOTE: ADC LS CS: Low = 480 mV, high = 2.88 V

Static state: 9.6 mA

Dynamic state: 57.6 mA

Figure 34. TIDA-01445 at 200-Ω Load Resistance

3.2.1.4 Runtime Characteristics

The internal characteristics of the reference design are measured and shown in this section. Frequency and duty cycle of the input signal to the high-side switch is varied to check the performance.

NOTE: For the following figures:
Battery voltage = 14 V, VCC INT = 7 V

CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: Current sensing from high side and low side is significant for 50 Hz and 50% duty cycle interlock system at an interlock load of 100 Ω.

Figure 35. TIDA-01445 for 50 Hz and 50% Duty Cycle

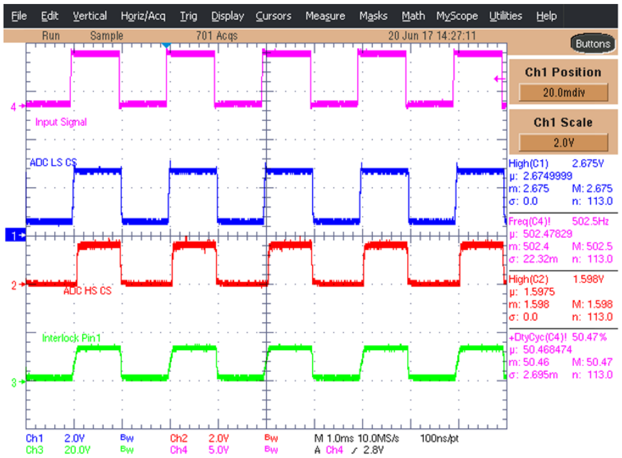


Figure 36. TIDA-01445 for 500 Hz and 50% Duty Cycle

CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: Current sensing from high side and low side is significant for 500 Hz and 50% duty cycle interlock system at an interlock load of 100 Ω.

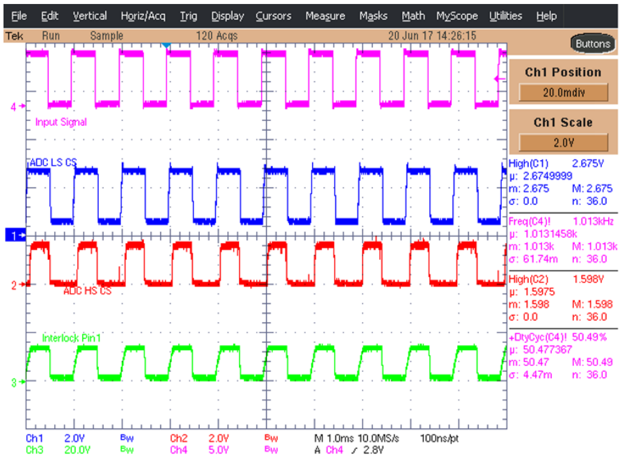


Figure 37. TIDA-01445 for 1 kHz and 50% Duty Cycle

CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: Current sensing from high side and low side is significant for 1 kHz and 50% duty cycle interlock system at an interlock load of 100 Ω.

Figure 38. TIDA-01445 for 95 Hz and 10% Duty Cycle

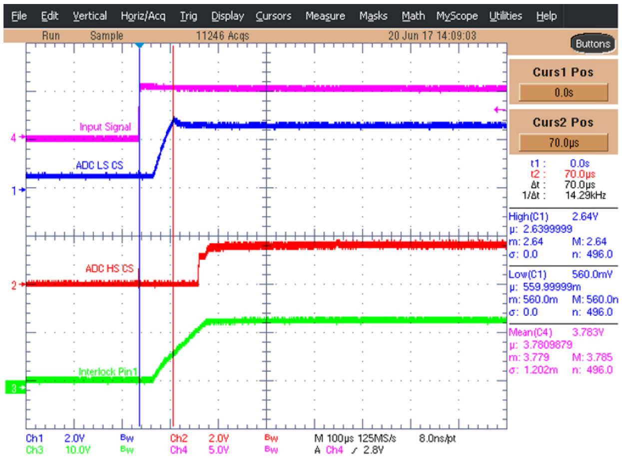
CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: Current sensing from high side and low side is significant for 95 Hz and 10% duty cycle interlock system at an interlock load of 100 Ω.

Figure 39. TIDA-01445 for 90 Hz and 25% Duty Cycle

CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

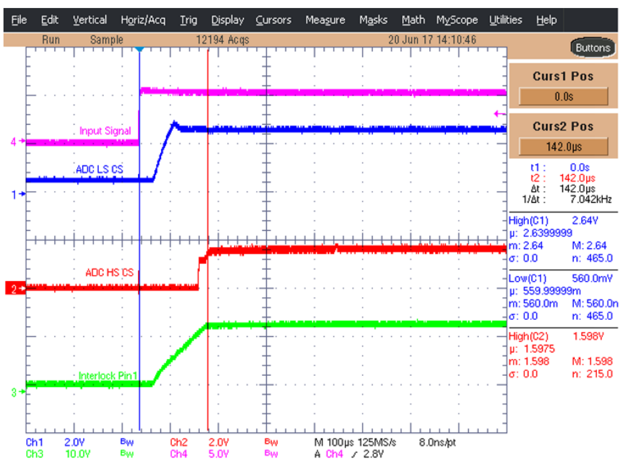
NOTE: Current sensing from high side and low side is significant for 95 Hz and 10% duty cycle interlock system at an interlock load of 100 Ω.



CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: The low-side current sense settling time and response time is 70 µs. In actual system, it may vary based on the load and circuit impedance.

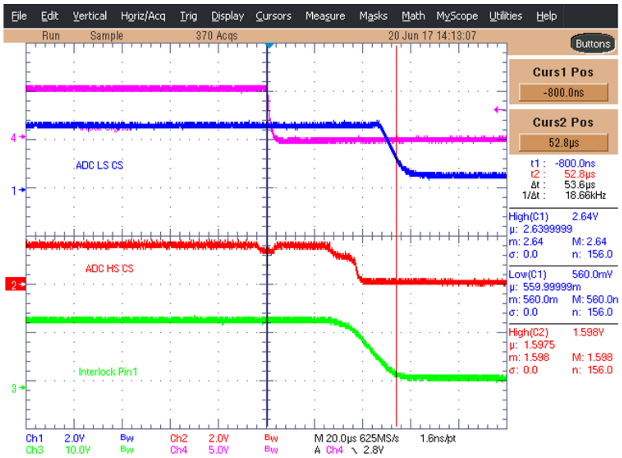
Figure 40. TIDA-01445 Low-Side Current Sense



CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: The high-side current sense settling time is 142 µs. The high-side response time from the ADC may vary based on the filter circuit.

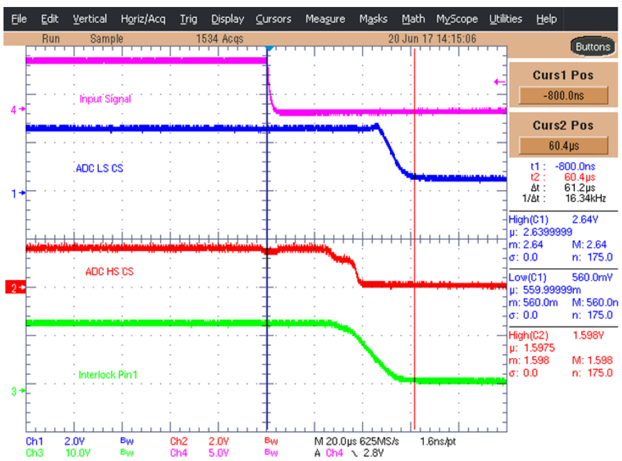
Figure 41. TIDA-01445 High-Side Current Sense



CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: The fall time of interlock pin 1 voltage is the turnoff time of the TPS2H000-Q1, which is 53.6 µs. It may vary if there is any resistor in between the high-side switch and interlock pin 1.

Figure 42. TIDA-01445 TPS2H000-Q1 Turnoff Time

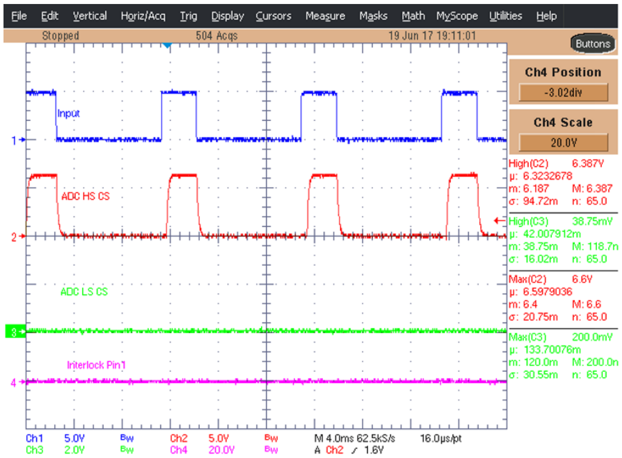


CH1: Low-side current sense (INA225-Q1)
CH2: High-side current sense (TPS2H000-Q1)
CH3: Interlock pin 1
CH4: Input signal for TPS2H000-Q1

NOTE: The settling time of the low-side current sense turnoff sequence is 61.2 µs.

Figure 43. TIDA-01445 Low-Side Current Sense (Fall Time)

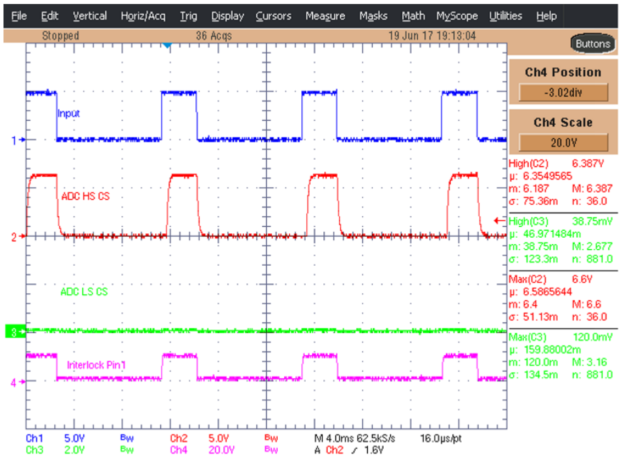
3.2.2 Reliability Tests



CH1: Input signal for TPS2H000-Q1
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Interlock pin 1

NOTE: No current in the low-side current sense pin and fault current sense voltage for high side(TPS2H000-Q1) is an indication of SCG. No voltage on pin indicates the fault location at pin 1.

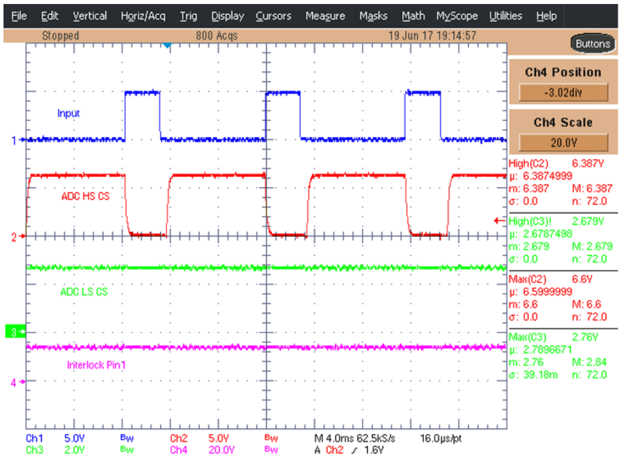
Figure 44. TIDA-01445 Short Circuit to Ground at Pin 1



CH1: Input signal for TPS2H000-Q1
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Interlock pin 1

NOTE: No current in the low-side current sense pin, and fault current sense voltage for high side(TPS2H000-Q1) is an indication of SCG. Voltage on pin 1 gives the resistive location for the SCG fault.

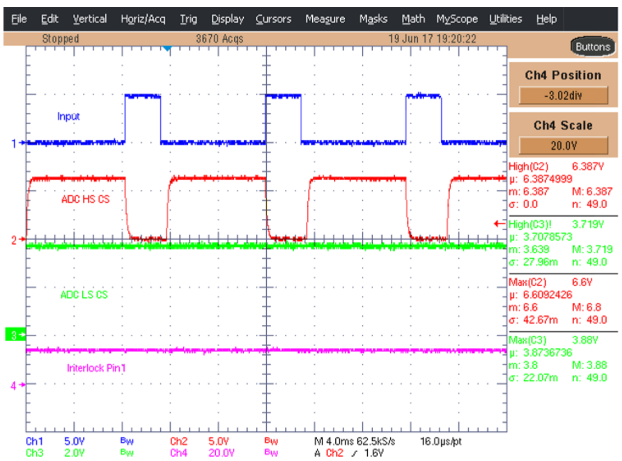
Figure 45. TIDA-01445 Short Circuit to Ground at Pin 2



CH1: Input signal for TPS2H000-Q1
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Interlock pin 1

NOTE: Low-side current sense indicates 53.38 mA continuously. This current is an indication of faulty high-side switch or short circuit to battery at pin 1.

Figure 46. TIDA-01445 Short Circuit to Battery at Pin 1



CH1: Input signal for TPS2H000-Q1
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Interlock pin 1

NOTE: Low-side current sense indicates 74 mA continuously. This current is an indication of short circuit to battery at pin 2.

Figure 47. TIDA-01445 Short Circuit to Battery at Pin 2

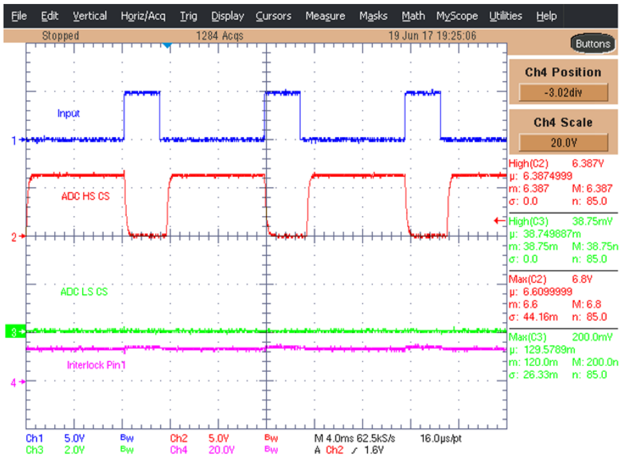


Figure 48. TIDA-01445 Open Load Condition

CH1: Input signal for TPS2H000-Q1
CH2: High-side current sense (TPS2H000-Q1)
CH3: Low-side current sense (INA225-Q1)
CH4: Interlock pin 1

NOTE: No current on low side current sense . High side current sense toggle the state for indicating the open load scenario.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01445.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01445.

4.3 PCB Layout Recommendations

The PCB layout of an interlock module must be done based on the arrangement and floor plan of a complete PCB.

- Place EMC capacitors C3 and C4 near to Interlock pins of the connector.
- Place R10. R12, and R13 with C22 in Kelvin connection to IN+ and IN– pins of the INA225-Q1.
- Place R3, R7 current sense and current limit resistors near to high side switch, TPS2H000-Q1

Follow the layout guides in the datasheet for TPS2H000-Q1 and INA225-Q1.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01445.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01445.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01445.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01445.

5 Software Files

To download the software files, see the design files at TIDA-01445.

6 Related Documentation

1. Texas Instruments, *TI Precision Labs - Op Amps* TI Training (https://training.ti.com/ti-precision-labs-op-amps)
2. Texas Instruments, *Integrated Load Switches versus Discrete MOSFETs*, Application Note (SLVA716)
3. Texas Instruments, *Standard Amplifier Quick Select Guide*, Marketing Selection Guide (SLYT601)

6.1 Trademarks

All trademarks are the property of their respective owners.

7 About the Author

RAMA KAMBHAM (Rama Chandra Reddy) is an automotive system engineer working in Texas Instruments Deutschland. Rama brings to this role his extensive experience in battery management systems and engine management systems in the automotive domain. Rama earned his bachelor of engineering degree from Osmania University Hyderabad, India.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2017) to A Revision **Page**

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