Description

This reference design illustrates a method to control a bidirectional interleaved continuous conduction mode (CCM) totem pole (TTPL) bridgeless power factor correction (PFC) power stage using a C2000™ microcontroller (MCU) and LMG3410R070. This power topology is capable of bidirectional power flow (PFC and grid-tied inverter) and it uses Gallium Nitride (GaN) devices, which enables higher efficiency and reduction in size of the power supply. The design supports phase shedding and adaptive dead time for efficiency improvements, input cap compensation scheme for improved power factor at light loads, and non-linear voltage loop to reduce voltage spikes under transient in PFC mode. The hardware and software available with this reference design accelerates time to market.

Features

- Interleaved, 3.3-kW, Single-Phase, Bidirectional Bridgeless CCM Totem Pole PFC Stage
- 100-kHz Pulse Width Modulation (PWM) Switching
- Programmable Output Voltage, 380-V DC Output Nominal
- Less Than 2% Total Harmonic Distortion (THD)
- Greater Than 98% Peak Efficiency
- powerSUITE™ Support for Easy Adaptation of Design for User Requirement
- Software Frequency Response Analyzer (SFRA) for Quick Measurement of Open Loop Gain
- Soft Starting of PWM for Reduced Zero Current Spike in TTPL PFC
- Software Support for F28004x Using Driver Library
- Same Source Code Maintained When Running Control Loop on C28x or CLA

Applications

- Onboard Chargers for Electronic Vehicles (EVs)
- Telecom Rectifier
- Drives, Welding, and Other Industrial
- Energy Storage System (ESS)
1 System Description

Bidirectional interleaved TTPLPFC is an attractive topology for EV chargers, industrial applications and grid-tied energy storage systems with the trend for higher power, higher efficiency, and higher power density. Figure 1 shows the implementation of the bidirectional TTPL bridgeless PFC as it is on the TIDM-02008 board.

1.1 Key System Specifications

Table 1 describes the bidirectional interleaved CCM TTPL PFC reference design power specifications.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input voltage</strong></td>
<td>AC 120 Vrms VL-N, 60 Hz or AC 230 Vrms VL-N, 50 Hz</td>
</tr>
<tr>
<td><strong>Input current</strong></td>
<td>16-A RMS maximum</td>
</tr>
<tr>
<td><strong>Output voltage</strong></td>
<td>380-V DC bus Nominal</td>
</tr>
<tr>
<td><strong>Output current</strong></td>
<td>10-A maximum</td>
</tr>
<tr>
<td><strong>Power rating</strong></td>
<td>1.65 KW at single phase 120 Vrms or 3.3 KW at single phase 230 Vrms</td>
</tr>
<tr>
<td><strong>Current THD</strong></td>
<td>&lt;2% at 120-Vrms L-N rated load</td>
</tr>
<tr>
<td><strong>Efficiency</strong></td>
<td>Peak 98.7% at 230-Vrms input, peak &gt;97.7% at 120-Vrms input</td>
</tr>
<tr>
<td><strong>Primary filter inductor</strong></td>
<td>478 µH</td>
</tr>
<tr>
<td><strong>Output capacitance</strong></td>
<td>880 µF</td>
</tr>
<tr>
<td><strong>PWM switching frequency</strong></td>
<td>100 kHz</td>
</tr>
</tbody>
</table>
WARNING

TI intends this reference design to be operated in a lab environment only and does not consider it to be a finished product for general consumer use.

TI intends this reference design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are accessible high voltages present on the board. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.
CAUTION

Do not leave the design powered when unattended.

High voltage! There are accessible high voltages present on the board. Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with over-voltage and over-current protection is highly recommended.

TI considers it the user’s responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. When energized, do not touch the design or components connected to the design.

Hot surface! Contact may cause burns. Do not touch!

Some components may reach high temperatures >55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

2 System Overview

Bidirectional interleaved TTPL PFC is an attractive topology for EV chargers and ESS with the trend for higher power, higher efficiency, and higher power density. Figure 1 shows the implementation of the bidirectional TTPL bridgeless PFC as it is in this reference design.

2.1 Block Diagram

Figure 1 shows the block diagram of this reference design with key TI components highlighted.
2.2 Design Considerations

The following detail the sensing circuit that is on this design. One can also refer to the calculations.xlsx file, which is available under the C2000Ware Digital Power SDK Install directory at <install_location>/solutions/tidm_1007/hardware for details on sensing circuit.

2.2.1 Input AC Voltage Sensing

The line and the neutral voltages are sensed by resistor divider to the ground of the board as shown in Figure 2. The two readings are subtracted on the controller to get the Vac sensing.

\[
\text{Vac_L} - \text{Vac_N} = \frac{R_e}{R_f} (V_{\text{bus}} - V_{\text{Rear}})
\]

Figure 2. Input AC Voltage Sensing

2.2.2 Bus Voltage Sensing

Similarly the bus voltage is sensed by a resistor divider network as shown in Figure 3.

\[
V_{\text{bus}} = \frac{R_e}{R_f} V_{\text{In}} + V_{\text{off}}
\]

Figure 3. Bus Voltage Sensing Circuit

2.2.3 AC Current Sensing

A Hall effect sensor senses the total current. The Hall effect sensor has an inbuilt offset, and the range is different than what ADC can measure. Hence, the voltage is scaled to match the ADC range using the circuit as shown in Figure 4.

\[
I_{\text{invfdbk}} = \frac{R_f}{R_e} (I_{\text{Inv}} \times \frac{V_{\text{nominal}}}{V_{\text{nominal,max}}} + V_{\text{off}})
\]

Figure 4. Current Sensing Using Hall Effect Sensor
2.2.4 Sense Filter

An RC filter filters the signals before connecting to the controller. A common RC filter is used for all the sensing signals on this design as shown in Figure 5.

\[
\text{Output} = \frac{1}{1 + \frac{R_{\text{trip}}}{C_{\text{trip}}}} \times \text{Input}
\]

**Figure 5. RC Filter**

2.2.5 Protection (CMPSS)

Most power electronics converters require protection from overcurrent event. For this design multiple comparators are required, and references for the trip must be generated, as shown in Figure 6.

**Figure 6. Trip Generation for PWM Using Comparators and Reference Generators**

All this circuitry is avoided when using C2000 MCUs, such as TMS320F28377D, which have on-chip windowed comparator as part of the CMPSS that are internally connected to the PWM module that can enable fast tripping of the PWM. An on-chip windowed comparator saves board space and cost in the end application as extra components can be avoided using on-chip resources, as shown in Figure 7.

**Figure 7. CMPSS Used for Overcurrent Protection**
2.3 Highlighted Products

2.3.1 C2000™ MCU F28004x

C2000 MCUs are part of an optimized MCU family for real-time control application. Fast and high-quality analog-to-digital controller enables accurate measurement of the current and voltage signals, and an integrated comparator subsystem (CMPSS) provides protection for overcurrent and overvoltage without use of any external devices. The optimized CPU core enables fast execution of control loop. Trigonometric operations are accelerated using the on-chip trigonometric math unit (TMU). The solution also provides an option to use the control law accelerator (CLA) on the F28004x and F2837x. The CLA is a co-processor that can be used to alleviate CPU burden and enable faster-running loops or more functions on the C2000 MCU.

2.3.2 LMG3410R070

The LMG3410R070 single-channel GaN power stage contains a 70-mΩ, 600-V GaN power transistor and specialized driver in an 8-mm × 8-mm QFN package. Direct drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off through its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally-generated negative voltage supply. The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and undervoltage lockout (UVLO) protections help create a fail-safe system. The device’s status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

2.3.3 UCC27714

The UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability that is targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to –8 VDC on HS pin (at VDD = 12 V).

2.4 System Design Theory

2.4.1 PWM

Figure 8 shows a simplified diagram of a single phase of the interleaved TTPL PFC topology. To control this rectifier the duty cycle is controlled to regulate the voltage directly. This regulation is possible if the software variable Duty or D is set so that when it is equal to 1, Q3 is always ON, and the setting makes the voltage \( V_{\text{IN}} \) equal to the \( V_{\text{bus}} \) voltage. When Duty is set to 0, Q3 never turns on, and Q4 is always connected to \( V_{\text{bus}} \), which makes the \( V_{\text{IN}} \) voltage go to 0.
The same control loop model applies to both PFC and grid-tied inverter operation. To understand the current loop model, first look at the inductor current closely. In Figure 8 the Duty cycle (D) is provided to the PWM modulator, which is connected to the switch Q3 and Q4. From here, Equation 1 is written as:

\[ V_{\text{IN}} = D \times V_{\text{BUS}} \]  

(1)

**NOTE:** When D is set to 1, Q3 is on all the time, and when D is 0, Q3 is off all the time.

To modulate the current through the inductor, the voltage \( V_{\text{IN}} \) is regulated using the duty cycle control of Q3 and Q4 switches. It is assumed that the direction of current is positive in the direction from the AC line into the rectifier and that the grid is fairly stiff when using the DC bus feedforward and the AC voltage feedforward. Figure 9 shows the simplified current loop, and the current loop plant model is written as Equation 2.

\[ H_{p-i} = \frac{i_{Li}}{D} = \frac{1}{K_{v\_gain}} \times K_{i\_gain} \times K_{i\_fltr} \times G_d \times \frac{1}{Z_i} \]  

(2)

Where:

- \( K_{v\_gain} \) is the inverse of maximum bus voltage sensed,
- \( K_{v\_gain} \) is the inverse of maximum AC voltage sensed, (A factor to normalize this is applied in the feedforward and hence the current loop model is only dependent on the \( K_{v\_gain} \))
- \( K_{i\_gain} \) is the inverse of maximum AC current sensed, \( I_{AC\_MaxSense} \)
- \( K_{i\_fltr} \) is the response of the RC filter connected from the current sensor to the ADC pin
- \( G_d \) is the digital delay associated with the PWM update and digital control is the current command
- \( i_{Li} \) is the current command

**NOTE:** The negative sign on the reference is because the current loop is thought to be regulating the voltage, \( V_{\text{IN}} \). To increase the current, \( V_{\text{IN}} \) must be reduced—hence, the opposite sign for reference and feedback in Figure 9.

This current loop model is then used to design the current compensator. A simple proportional integral controller is used for the current loop.

Now, in the case of three interleaved phases, the current is simply three times more as the same duty cycle is provided to each leg. Hence, the plant model is given as Equation 3.
\[ H_{p,i} = \frac{i_i}{D} = 3 \times \frac{1}{K_{v\_gain}} \times K_{i\_gain} \times i_{i\_fltr} \times G_d \times \frac{1}{Z_i} \]  

This model is verified on this design using the SFRA library. Figure 10 shows the model versus measured open loop frequency response, which shows good correlation between the two.

![Figure 10. Gi, Current Open Loop Gain Measured Versus Modelled](image)

2.4.3 DC Bus Regulation Loop (for PFC mode only)

The DC bus regulation loop is assumed to provide the power reference. The power reference is then divided by the square of the line voltages RMS to provide the conductance, which is further multiplied by the line voltage giving the instantaneous current command.

Small signal model of the DC bus regulation loop is developed by linearizing Equation 4 around the operating point.

\[ i_{DC} V_{bus} = \eta V_{N\_rms} i_{N\_rms} \Rightarrow i_{DC} = \eta \frac{V_{N\_rms}}{V_{bus}} i_{Li} \]  

(4)

For a resistive load the bus voltage and current are related as shown in Equation 5.

\[ \hat{V}_{bus} = \frac{R_i}{1 + sR_i C_o} \hat{i}_{DC} \]  

(5)
The DC voltage regulation loop control model can be drawn as shown in Figure 11. An additional Vbus feedforward is applied to make the control loop independent of the bus voltage, and hence, the plant model for the bus control can be written as Equation 6.

\[
H_{p_{bus}} = H_{\text{load}} \times \eta \times K_{i_{gain}} \times K_{v_{gain}} \times K_{v_{filt}}
\]

\[
\begin{align*}
\hat{v}_{bus} & \to G_{v_{filt}} \to \left( \frac{1}{V_{N} \times K_{v_{gain}} \times K_{v_{filt}}} \right) \to v_{bus, \text{avg}} \to G_{p} \to \eta \times \nu_{ms} \to \hat{v}_{bus}
\end{align*}
\]

\[
G_{v} \times K_{v_{gain}}
\]

Figure 11. DC Voltage Loop Control Model

Using Figure 11, a proportional integrator (PI) compensator is designed for the voltage loop. The bandwidth of this loop is kept low as it is in conflict with the THD under steady state.

SFRA library is used to measure the frequency response on the voltage loop and verify the model. Figure 12 shows the modelled versus measured plots for the voltage loop.
2.4.4 Soft Start Around Zero Crossing for Eliminate or Reduce Current Spike

Zero crossing current spikes is a challenging issue for TTPL PFC topologies. This issue is solved by implementing a soft start scheme with a state machine to turn on and off switches in a particular sequence.

![Diagram showing PWM sequence with soft starting to reduce current spike at zero crossing.](image)

**Figure 13. PWM Sequence With Soft Starting to Reduce Current Spike at Zero Crossing**

Figure 13 shows the switching sequence when the AC wave goes from negative to positive. During the negative half, Q1 is ON, Q3 is the active FET, and Q4 is the sync FET. During this time, the voltage across Q2 is the DC bus voltage. When the AC cycle changes, Q2 must be on 100% or close to 100%. If Q2 is turned ON immediately, a huge positive spike results. Therefore, a soft-start sequence is used to turn Q4 ON as shown in Figure 13. The tuning of this soft start depends on the inductance value and other power stage parameters such as device Coss.

Another reason for a negative current spike around zero crossing is the relatively low AC voltage around the zero crossing. When Q3 is turned ON, though the duty cycle is low, a high-voltage difference is applied and can result in a high negative current spike. Therefore, a sufficient delay is applied before Q3 starts switching back again.

Similarly, Q2 is turned on after some delay after the soft start has started.
3Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This section details the hardware and the different sections on the board. If only using the firmware of the design through powerSUITE, this section may not be valid.

3.1.1.1 Base Board Settings

The design follows a HSEC control card concept, and any device for which HSEC control card is available from the C2000 MCU product family can be potentially used on this design. The key resources used for controlling the power stage on the MCU are listed in Table 2. Figure 14 shows the key power stage and connectors on the design board. Table 3 lists the key connectors and their functions. To get started:

1. Make sure no power source is connected to the design.
2. Insert the control card in the J600 slot.
3. Connect a 12-V, 1-A DC power supply at TP604. For the ground terminal, use TP606. Do not power up the supply.
4. Connect a 5-V, 1-A DC power supply at TP608. For the ground terminal, use TP609. Do not power up the supply.
5. Turn both the 12-V and 5-V power supply ON. The LED on the control card lights up and indicates the device is powered.

NOTE: The bias for the MCU is separated from the power stage, which enables safe bring up of the system in this set of instructions. The bias supply design that works with this converter is PMP20396

6. To connect JTAG, use a USB cable from the control card and connect it into a host computer.
7. For PFC mode, a single phase AC power supply can be connected to the input J100. Optionally in some incremental builds a DC source may be required to test out the system safely. A resistive load of approximately 500 \( \Omega \) and 400 W should be connected to the output at J104.
8. For Inverter mode, a DC power supply can be connected to the input J100. A resistive load of approximately 125 \( \Omega \) and 200 W should be connected to the output at J104.
9. Current and voltage probes can be connected to observe the input current, input voltage, and output voltages, as shown in Figure 14.

![Figure 14. Board Overview](image-url)
### Table 2. Key Controller Peripherals Used for Control of Power Stage on Board

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>HSEC PIN NUMBER</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM-1A</td>
<td>49</td>
<td>PWM: low-frequency MOSFET leg, high-side switch</td>
</tr>
<tr>
<td>PWM-1B</td>
<td>51</td>
<td>PWM: low-frequency MOSFET leg, low-side switch</td>
</tr>
<tr>
<td>PWM-2A</td>
<td>53</td>
<td>PWM: high frequency GaN leg, high side switch, phase one</td>
</tr>
<tr>
<td>PWM-2B</td>
<td>55</td>
<td>PWM: high-frequency GaN leg, low-side switch, phase one</td>
</tr>
<tr>
<td>PWM-3A</td>
<td>50</td>
<td>PWM: high-frequency GaN leg, high-side switch, phase two</td>
</tr>
<tr>
<td>PWM-3B</td>
<td>52</td>
<td>PWM: high-frequency GaN leg, low-side switch, phase two</td>
</tr>
<tr>
<td>PWM-4A</td>
<td>54</td>
<td>PWM: high-frequency GaN leg, high-side switch, phase three</td>
</tr>
<tr>
<td>PWM-4B</td>
<td>56</td>
<td>PWM: high-frequency GaN leg, low-side switch, phase three</td>
</tr>
<tr>
<td>lac</td>
<td>18</td>
<td>ADC with CMPSS: AC return current measurement</td>
</tr>
<tr>
<td>IL1</td>
<td>15</td>
<td>ADC with CMPSS: inductor current measurement Ph1</td>
</tr>
<tr>
<td>IL2</td>
<td>21</td>
<td>ADC with CMPSS: inductor current measurement Ph2</td>
</tr>
<tr>
<td>IL3</td>
<td>25</td>
<td>ADC with CMPSS: inductor current measurement Ph3</td>
</tr>
<tr>
<td>VL</td>
<td>20</td>
<td>ADC: AC voltage line</td>
</tr>
<tr>
<td>VN</td>
<td>17</td>
<td>ADC: AC voltage neutral</td>
</tr>
<tr>
<td>Vbus</td>
<td>24</td>
<td>ADC: bus voltage</td>
</tr>
<tr>
<td>In Rush Relay</td>
<td>57</td>
<td>GPIO: used to control the inrush relay</td>
</tr>
<tr>
<td>GaN Fault 1</td>
<td>58</td>
<td>GPIO: GaN fault signal phase one</td>
</tr>
<tr>
<td>GaN Fault 2</td>
<td>60</td>
<td>GPIO: GaN fault signal phase two</td>
</tr>
<tr>
<td>GaN Fault 3</td>
<td>62</td>
<td>GPIO: GaN fault signal phase three</td>
</tr>
<tr>
<td>AC Current Sense Gain Change</td>
<td>63</td>
<td>GPIO: controls the gain stage</td>
</tr>
</tbody>
</table>

### Table 3. Key Connectors and Function

<table>
<thead>
<tr>
<th>CONNECTOR NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J100</td>
<td>PFC: Input AC voltage</td>
</tr>
<tr>
<td>J104</td>
<td>PFC: Output DC bus voltage</td>
</tr>
<tr>
<td>TP604</td>
<td>PFC: Input bias supply, 12-VDC, 1 A</td>
</tr>
<tr>
<td>TP608</td>
<td>PFC: Input bias supply, 5-VDC, 1 A</td>
</tr>
<tr>
<td>TP606/TP609</td>
<td>PFC: GND</td>
</tr>
<tr>
<td>J600</td>
<td>PFC: HSEC control card connector slot</td>
</tr>
</tbody>
</table>
3.1.1.2 Control Card Settings

Certain settings on the device control card are required to communicate over JTAG and use the isolated UART port. The user must also provide a correct ADC reference voltage. The following are the required settings for revision A of the F280049M control card. One can also refer to the info sheet located inside C2000Ware at <install_path>\c2000ware\boards\controlcards\TMDSCNCD280049C or alternatively get it from the document http://www.ti.com/lit/pdf/spruic4

1. S1:A on the control card must be set on both ends to “ON (up)” position to enable JTAG connection to the device and UART connection for SFRA GUI. If this switch is “OFF (down)” one cannot use the isolated JTAG built in on the control card nor can SFRA GUI communicate to the device.

2. J1:A is the connector for the USB cable that is used to communicate to the device from a host PC on which Code Composer Studio™ (CCS) runs.

3. A 3.3-V reference is desired for the control loop tuning on this design. Internal reference of the F28004x is used and for this S8 switch must be moved to the left i.e. pointing to VREFHI

4. A capacitor is connected between the isolated grounds on the control card, C26:A. It is advised to remove this capacitor for the best performance of this reference design.

3.1.2 Software

The software of this design is available inside C2000Ware Digital Power SDK and is supported inside the powerSUITE framework.
3.1.2.1 Opening Project Inside CCS

To start:
1. Install CCS from the Code Composer Studio (CCS) Integrated Development Environment (IDE) tools folder, CCSV9.3 or above is recommended.
2. Install C2000Ware DigitalPower SDK at the C2000Ware Digital Power SDK tools folder.
   • Note: powerSUITE is installed with the SDK in the default install.
3. Go to View → Resource Explorer. Below the TI Resource Explorer, go to C2000Ware DigitalPower SDK.

To open the reference design software as it is (opens firmware as it was run on this design and hardware, requires the board to be exactly the same as this reference design).
1. Under C2000Ware DigitalPower SDK, select Development Kits → CCM Totem Pole PFC TIDM-02008, and click on Run <Import> Project.
2. These steps import the project, and the development kit or designs page show up. This page can be used to browse all the information on the design including this user guide, test reports, hardware design files, and so forth.
3. Click Import <device_name> Project.
4. This action imports the project into the workspace environment, and a cfg page with a GUI similar to Figure 16 shows up.
Open reference design software for adaptation. The user can modify power stage parameters, which are then used to create the model of the power stage in Compensation Designer and can also modify scaling values for voltages and currents for a custom design.

1. Under C2000Ware Digital Power SDK click on powerSUITE → Solution Adapter Tool.
2. Select Single Phase CCM Totem Pole PFC from the list of solutions presented.
3. Select the device this solution must run on the next page.
4. Once the icon is clicked, a pop-up window shows up asking for a location to create the project. One can also save the project inside the workspace itself. Once the location is specified, a project is created, and a GUI page appears with modifiable options for the solution (Figure 16).
5. This GUI can be used to change the parameters for an adapted solution, like power rating, inductance, capacitance, sensing circuit parameters, and so forth.

Figure 16. powerSUITE Page for CCM TTPL PFC Solution
3.1.2.2 Project Structure

Once the project is imported, the project explorer appears inside CCS as shown in Figure 17.

![Project Explorer View of Solution Project](image)

Figure 17. Project Explorer View of Solution Project
The general structure of the project is shown in Figure 18.

![Figure 18. Project Structure Overview](image)

NOTE: Figure 18 shows the project for F28004x; however, if a different device is chosen from the powerSUITE page, the structure is similar.

Solution specific and device independent files are `<solution>.c/h`. This file consist of the main.c file of the project and is responsible for the control structure of the solution.

For this design `<solution>` is `pfc1ph3ilttpl`.

Board-specific and device-specific files are `<solution>_board.c/h`. This file consists of device specific drivers to run the solution.

The powerSUITE page can be opened by clicking on the `main.syscfg` file, listed under the project explorer. The powerSUITE page generates the `<solution>_settings.h` file. This file is the only file used in the compile of the project that is generated by the powerSUITE page. The user must not modify this file manually as the changes are overwritten by powerSUITE every time the project is saved. User can modify several settings in `<solution>_user_settings.h` file.

The `Kit.json` and `solution.js` files are used internally by the powerSUITE and must also not be modified by the user. Any changes to these files results in project not functioning properly.

The `setupdebugenv_build.js` are provided to autopopulate the watch window variables for different builds.

The `*.graphProp` files is provided to auto populate settings for the data logger graph.

The project consists of an interrupt service routine, which is called every PWM cycle, and a current controller is run inside this ISR. In addition to this, there is a slower ISR of approximately 10 kHz that is called for running the voltage loop and the instrumentation ISR. A few background tasks (A0-A4 and B0-B4) are called in a polling fashion and can be used to run slow tasks for which absolute timing accuracy is not required, such as SFRA background and so on.
Figure 19 shows the software flow diagram of the firmware.

To simplify the system bring up and design the software of this reference design is organized in nine incremental builds (INCR_BUILD). The incremental build from 1 to 3 are designed to validate PFC operation and the incremental build from 4 to 6 are designed to validate the inverter operation.

- **PFC Operation**
  - **INCR_BUILD 1**: Open Loop Check, DC
Using CLA on C2000 MCU to Alleviate CPU Burden

The control law accelerator (CLA) is a co-processor available on the C2000 MCU family of devices. This co-processor enables offloading the control-ISR functions from the main C28x CPU core.

To run the control ISR on the CLA for solutions supported in powerSUITE, selection is achieved through a drop-down menu on the powerSUITE CFG page. The software structure of the powerSUITE solution is designed such that offloading the task to the CLA is simply a drop-down menu selection. The code is not duplicated and a single source for the solution algorithm is maintained even when code is run on the CLA or the C28x. This configuration enables flexible debugging of the solution.

The CLA features of each device varies slightly. For example, on the F2837xD, F2837xS, and F2807x, the CLA can support only one task at a given time, and there is no nesting capability. This configuration means that the task is not interruptible. Only one ISR can be offloaded to the CLA. On the F28004x, the CLA supports a background task from which a regular CLA task can nest. This configuration enables offloading two ISRs on the CLA.

The CLA supports a background task from which it can nest into a CLA task. This configuration allows offloading two ISRs functions to the CLA. For the F28004x, both the control ISR (100 kHz) for the current loop and the voltage loop and instrumentation ISR (10 kHz) are offloaded to the CLA. On the F28004x, the CPU use is approximately 42% for the 100 kHz loop (not including advanced options such as phase shedding, adaptive dead time, SFRA running, and so forth) and 11% for the 10 kHz loop that runs the voltage loop and instrumentation functions. Thus, the total CPU use is approximately 53%. With the CLA option, the CPU burden is reduced to 0% when both ISRs are offloaded to the CLA.

For more information on the CLA, visit the CLA Hands-On Workshop and the respective device technical reference manuals.

Running the Project

3.1.2.4.1 INCR_BUILD 1: Open Loop, DC (PFC Mode)

In this build the board is excited in open loop fashion with a fixed duty cycle. The duty cycle is controlled with dutyPU_DC variable. This build verifies the sensing of feedback values from the power stage and also operation of the PWM gate driver and ensures there are no hardware issues. Additionally calibration of input and output voltage sensing can be performed in this build. The software structure for this build is shown in Figure 20. There are two ISR in the system: fast ISR for the current loop and a slower ISR to run the voltage loop and instrumentation functions. Modules that are run in each ISR are shown in Figure 20.
Figure 20. Build Level 1 Control Software Diagram: Open Loop Project
Hardware setup is assumed to be similar to what was outline in the previous section. Figure 21 recaps the hardware setup for build level 1 test.

Power Flow

![Power Flow Diagram]

Figure 21. HW Setup for Build Level 1

3.1.2.4.1.1 Setting Software Options for BUILD 1

1. powerSUITE Settings: On the powerSUITE page select under Project Options section:
   - Select Open Loop for the build level under INCR_BUILD option.
   - Select input to be DC under INPUT options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

2. If this is an adapted solution, edit the setting under Voltage and Current Sensing Parameters. One can refer to the calculations.xlsx file which is available under the C2000Ware DigitalPower SDK Install directory at <install_location>/solutions/idm_1007/hardware for details on sensing circuit and how max range is computed for the powerSUITE page

3. Under Power Stage Parameters specify the switching frequency, the dead band, and the power rating. Save the page.

3.1.2.4.1.2 Building and Loading Project

1. Right click on the project name, and click Rebuild Project.
2. The project builds successfully.
3. In the Project Explorer make sure the correct target configuration file is set as Active under targetconfigs (Figure 17).
4. Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
5. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.
3.1.2.4.1.3 Setup Debug Environment Windows

1. To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the setupdebugenv_build1.js script file located inside the project folder. This script file populates the watch window with appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous update of values from the controller. The watch window appears as shown in Figure 22.

2. Run the project by clicking on .

3. Now Halt the processor by using the Halt button on the toolbar.

3.1.2.4.1.4 Using Real-Time Emulation

Real-time emulation is a special emulation feature that allows windows within CCS to be updated while the MCU is running. This feature allows graphs and watch views to update but also allows the user to change values in watch or memory windows and see the effect of these changes in the system without halting the processor.

1. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar and clicking the button.

2. A message box may appear. If so, select YES to enable debug events. This action sets bit 1 (DGBM bit) of status register 1 (ST1) to a 0. The DGBM is the debug enable mask bit. When the DGBM bit is set to 0, memory and register values can be passed to the host processor for updating the debugger windows.
### 3.1.2.4.1.5 Running Code

1. Now run the project again by clicking on ![play](image)

2. In a few seconds the inrush relay clicks, the software is programmed to do so in the build level with DC. The trip clears, and a duty cycle of 0.5 is applied.

3. In the watch view, check if the `guiVin`, `guiVbus`, `guiIi`, variables are updating, periodically.
   - **Note:** As no power is applied right now, this value is close to zero.

4. Now slowly increase the input DC voltage from zero to 120 V. The output voltage shows a boosted voltage as a steady duty cycle of 0.5 PU is applied as default setting. If a high current is drawn, verify if the voltage terminals are swapped. If true, reduce the voltage to zero first and correct the issue before resuming the test.

5. Verifying the voltage sensing: Make sure `guiVin` and `guiVbus` display the correct values, for 120-V DC input, `guiVbus` is close to 240V. This verifies the voltage sensing of the board in some manner.

6. Verifying the current sensing: Notice the `guiIIi` for the given test condition; this value is close to 1 A.

7. This verifies at a basic level the PWM driver and connection of hardware, user can change the `dutyPU_DC` variable to see operation under various boost conditions.

8. Once finished, reduce the input voltage to zero and watch for the bus voltages to reduce down to zero.

9. This completes the check for this build, the following items are verified on successful completion of this build:
   - Sensing of voltages and currents and scaling to be correct
   - Interrupt generation and execution of the BUILD 1 code in the current loop ISR and Voltage Loop Instrumentation ISR
   - PWM driver and switching
   - If any issue is observed a careful inspection of the hardware may be required to eliminate any build issues and so forth.

10. The controller can now be halted, and the debug connection terminated.

11. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the **Halt** button on the toolbar or by using **Target → Halt**. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU by clicking on .

12. Close CCS debug session by clicking on **Terminate Debug Session** (Target → Terminate all).
3.1.2.4.2 **INCR_BUILD 2: Closed Current Loop DC (PFC)**

In this build, BUILD 2, the inner current loop is closed that is the inductor current is controlled using a current compensator $G_i$. Both DC bus and output voltage feed forward are applied to the output of this current compensator to generate the duty cycle of the inverter, Equation 7. This makes the plant for the current compensator simple and a proportional (P) controller can be used to tune the loop of the inner current. The model for the current loop was derived in section Section 2.4.2. Complete software diagram for this build is illustrated in Figure 24.

$$duty_{PU} = \frac{(ac\_cur\_meas - ac\_cur\_ref\_inst) \times G_i + ac\_vol\_sensed}{vBus\_sensed}$$

(7)

Complete software diagram for this build as illustrated in Figure 24.
3.1.2.4.2.1 Setting Software Options for BUILD 2

1. Make sure the hardware is setup as outlined in Figure 21. Do not supply any high voltage (HV) power to the board yet.

2. powerSUITE Settings: On the powerSUITE page select under Project Options section:
   - Select Closed Current Loop for the build level under INCR_BUILD option.
   - Select input to be DC under INPUT options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

3. Assuming all other options are same as specified earlier in Section 3.1.2.4.1.1

4. Under Control Loop Design, options for the current loop tuning automatically be selected (Tuning → Current Loop → COMP1 → DCL_PI_C1). Now click on the Compensation Designer icon ( ).

3.1.2.4.2.2 Designing Current Loop Compensator

1. Compensation Designer launches with the model of the current loop plant with parameters specified on the powerSUITE page. PI-based controller can be tuned from a pole zero perspective to ensure stable closed loop operation. Stability of the system when using the designed compensator can be verified by observing the gain and phase margins on the open loop transfer function plot in the Compensation Designer, as shown in Figure 25.

2. Once satisfied with the open loop gain, click on Save COMP. This action saves the compensator values into the project.
• Note: If the project was not selected from the solution adapter, changes to the compensator are not allowed. Select the solution through the solution adapter.

3. Close the Compensation Designer, and return to the powerSUITE page.

3.1.2.4.2.3 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click Rebuild Project. The project builds successfully. Click Run → Debug, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the setupdebugenv_build2_dc.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as Figure 26.

![Figure 26. Build Level 2: Closed Current Loop Expressions View](image)

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.

4. Run the project by clicking .

5. Now Halt the processor by using the Halt button on the toolbar ( ).

3.1.2.4.2.4 Running Code

1. The project is programmed to drive the inrush relay and clear the trip after a set amount of time, that is, autoStartSlew==100. The software is programmed to do so in the build level with DC. An input voltage must be applied after hitting run and before this autoslew counter reaches 100. If the counter reaches 100, before voltage is applied at the input, the code must be reset. For which the controller must be brought out of real time mode, a reset performed and restarted. Repeat steps from

2. Now run the project by clicking .
3. Apply an input voltage of approximately 50 V before the autoStartSlew reaches 100. As soon as autoStartSlew reaches 100, the inrush relay is triggered, and PWM trip is cleared along with closing the current loop flag.

4. The input current regulates around 0.7 A, and the output voltage boosts to approximately 128 V.

5. Now slowly increase ac_cur_ref to 0.1, that is, 2.5-A input.

6. Next slowly increase Vin = 120 V, and the output voltage will be greater than 350 V.

7. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the SFRA icon. SFRA GUI appears.

8. Select the options for the device on the SFRA GUI. For example, for F28004x select floating point. Click on Setup Connection. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Ensure Boot on Connect is deselected. Click OK. Return to the SFRA GUI, and click Connect.
9. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking **Start Sweep**. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears. Comparing this with the measured plots, there is good correlation between the modeled and measured as shown in Figure 29. This verifies that the designed compensator is indeed stable and the model accurate.

Note: the deviation at low frequency, less than 200 Hz, is expected and is a known phenomena, also the measurement shown here was taken with a DC source, if an AC source is used to emulate a DC source the output impedance of the AC source can result in deviations from the graph plotted below.

![Gi OL Gain Model vs Measured with DC input](image)

**Figure 29. SFRA Run vs Modeled Closed Current Loop, Open Loop Gain**

The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run.

10. Optionally one can use the measured frequency response of the plant to design the current compensator by clicking on the Compensation Designer again from the CFG page and choose **SFRA Data** for plant option on the GUI. This uses the measured plant information to design the compensator. This option can be used to fine-tune the compensation. By default the compensation designer points to the latest SFRA run. If a previous SFRA run plant information must be used the user can select the SFRAData.csv file by browsing to it by clicking on **Browse SFRA Data**.

11. This action verifies the current compensator design.

12. To bring the system to a safe stop, bring the input DC voltage down to zero, observe the guiVbus comes down to zero as well.

13. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the **Halt** button on the toolbar or by using **Target → Halt**. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU .

14. Close the CCS debug session by clicking **Terminate Debug Session (Target → Terminate all)**.
3.1.2.4.3 **INCR_BUILD 2: Closed Current Loop, AC (PFC)**

In this build, BUILD 2, the inner current loop is closed, that is, the inductor current is controlled using a current compensator $G_i$. Both DC bus and output voltage feedforward are applied to the output of this current compensator to generate the duty cycle of the inverter along with soft start for PWM around the zero crossing.

Complete software diagram for this build as illustrated in **Figure 30**.
To run this build level make sure the hardware is setup as shown in Figure 31. Do not supply any HV power yet to the board.

### Power Flow

![Power Flow Diagram](image)

**Figure 31. HW Setup for AC Input**

#### 3.1.2.4.3.1 Setting Software Options for BUILD 2

1. powerSUITE Settings: On the powerSUITE page assuming options were selected at outlined in under Project Options section, select Closed Current Loop and AC input for the build level. Save the page.
2. Current compensator from the previous build is re-used in this build so no additional steps are required for tuning the current loop in the build level.
3.1.2.4.3.2 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click Rebuild Project. The project builds successfully. Click Run → Debug, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the setupdebugenv_build2_ac.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as .

![Figure 32. Build Level 2 AC: Closed Current Loop Expressions View](image)

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.
### 3.1.2.4.3.3 Running Code

1. The project is programmed to wait for input voltage to exceed approximately 70Vrms to drive the inrush relay, and clear the trip.

2. Run the project by clicking ![Play](image).

3. Now apply an input voltage of approximately 120 V, the board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and a small amount of current of approximately 0.55-A RMS is drawn. The watch window looks similar to **Figure 33**. The bus voltage is close to 180 V.

   ![Figure 33. Watch Expression, Build Level 2, AC After Closed Current Loop Operation Begins](image)

   4. Now slowly increase ac_cur_ref to 0.14, that is, 2.4-A input, and the bus voltage rises to 380 V. The voltage and current waveform are shown in **Figure 34**.

   ![Figure 34. Input AC input, Current and Output DC Voltage Waveform](image)

5. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the **SFRA** icon. SFRA GUI appears.

6. Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on **Setup Connection**. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click **OK**. Return to the SFRA GUI, and click **Connect**.
7. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking Start Sweep. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears, Figure 35. This is similar to the plot seen under DC conditions; however, some additional noise is visible due to AC harmonic frequencies close to the measured frequencies. The BW, PM, and GM numbers are very similar to the DC case. Note the graph shown in Figure 35 was taken with direct grid AC input. When using AC source interaction of the AC source output, impedance can be observed, which can affect the control margins.

8. To bring the system to a safe stop, switch off the output from the AC power supply thus bring the input AC voltage down to zero, observe the guiVbus comes down to zero as well.

9. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ) .

10. Close the CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).
3.1.2.4.4 INCR_BUILD 3: Closed Voltage and Current Loop (PFC)

In this build the outer voltage loop is closed with the inner current loop closed. The model of the outer voltage loop was derived in Section 2.4.3. A PI-based compensator is used and tuned through the compensation designer for the outer voltage loop.

Figure 36 shows the software diagram for this build.

3.1.2.4.4.1 Setting Software Options for BUILD 3

1. Make sure the hardware is setup as outlined in Figure 31. Do not supply any HV power yet to the board.

2. powerSUITE Settings : On the powerSUITE page select under Project Options section:
   - Select Closed Voltage & Current Loop for the build level under INCR_BUILD option.
   - Select input to be AC under INPUT options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

3. Assuming all other options are same as specified earlier in Section 3.1.2.4.1.1
4. Under Control Loop Design, select Tuning as Voltage Loop. Style presets to DCL PI_C3 Save the page by Ctrl + S, and click on the Compensation Designer button ( ).

5. Make sure the load connected at the output of the board is correctly entered on the powerSUITE cfg page because this load value is used in the design of the voltage compensator.

3.1.2.4.4.2 Designing Voltage Loop Compensator

1. Compensation designer then launches with the model of the voltage loop plant, as shown in Figure 37. The PI compensator can be edited to get the desired gain and phase margin, keeping in mind the bandwidth of the voltage loop has an inverse relationship with the THD achieved. Typically in a PFC application, this bandwidth is kept at approximately 10 Hz.

![Figure 37. Voltage Loop PI Compensation Tuning Using Compensation Designer](image)

2. Once satisfied with the compensator design, click on Save COMP. This action saves the compensator values into the project.
   - Note: If the project was not selected from the solution adapter, changes to the compensator are not allowed. To design one's own, select the solution through the solution adapter.

3. Close the Compensation Designer, and return to the powerSUITE page. Save using Ctrl + S.
### Building and Loading Project and Setting up Debug

1. Right click on the project name, and click **Rebuild Project**. The project builds successfully. Click **Run → Debug**, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window, click **View → Scripting Console** to open the scripting console dialog box. On the upper-right corner of this console, click on **Open** to browse to the `setupdebugenv_build3.js` script file located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on the **Continuous Refresh** button ( ![Continuous Refresh](https://www.ti.com/lit AN/ds/symlink/slvsds501b.pdf)) on the watch window to enable continuous update of values from the controller. The watch window appears as shown in **Figure 38**.

![Figure 38. Build Level 3: Expressions View](https://www.ti.com/lit AN/ds/symlink/slvsds501b.pdf)

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar and clicking the ![Real-time Mode](https://www.ti.com/lit AN/ds/symlink/slvsds501b.pdf) button.

4. Run the project by clicking on ![Run](https://www.ti.com/lit AN/ds/symlink/slvsds501b.pdf)

5. Now Halt the processor by using the **Halt** button on the toolbar ( ![Halt](https://www.ti.com/lit AN/ds/symlink/slvsds501b.pdf)).
3.1.2.4.4.4 Running Code

1. The project is programmed to wait for input voltage to excel at approximately 70 Vrms to drive the inrush relay, and clear the trip.

2. Run the project by clicking 📀.

3. Now apply an input voltage of approximately 120 V. The board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and the output rises to 380-V DC. A sinusoidal current is drawn from the AC input. Figure 39 shows the watch window when the program is running at this stage.

4. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA, keep the project running, and from the cfg page, click on the SFRA icon. SFRA GUI appears.

5. Select the options for the device on the SFRA GUI. For example, for F28004x, select floating point. Click on Setup Connection, and on the pop-up window, uncheck the boot on connect option and select an appropriate COM port. Click OK. Return to the SFRA GUI, and click Connect.

![Figure 39. Build Level 3: Expressions View After AC Voltage is Applied](image-url)
6. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking Start Sweep. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears, as seen in Figure 40. This action verifies that the designed compensator is indeed stable.

Figure 40. SFRA Run on Closed Voltage Loop

The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run.
Note the measured gain and phase margin are close to the modeled values, as shown in Figure 12.

7. Optionally, Click on the Compensation Designer again from the CFG page, and choose SFRA Data for plant option on the GUI. This option uses the measured plant information to design the compensator, and can be used to fine tune the compensation. By default the Compensation Designer points to the latest SFRA run. If a previous SFRA run plant information must be used the user can select the SFRAData.csv file by browsing to it by clicking on Browse SFRA Data. Close the Compensation Designer to return to the cfg page once done.

8. This verifies the voltage compensator design.

9. To bring the system to a safe stop bring the input AC voltage down to zero, observe the guiVBus comes down to zero as well.

10. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).

11. Close CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).

3.1.2.4.5 **INCR_BUILD 4: Open loop, DC (Inverter)**

In this build the board is excited in open loop fashion with a fixed duty cycle for inverter mode operation. The duty cycle is controlled with dutyPU_DC variable. The test procedure is similar to incremental build 1 open loop DC. The software structure for this build is the same as the one in INCR_BUILD1 shown in Figure 20. It should be noted that HW setup for INCR_BUILD4 is different from INCR_BUILD1. In this build, dc power supply has to be connected to J104 and the resistive load has to be moved to J100.

**Power Flow**

![Power Flow Diagram]

**Figure 41. HW Setup for Build Level 4**

3.1.2.4.5.1 **Setting Software Options for BUILD 4 (DC)**

1. powerSUITE Settings : On the powerSUITE page select under Project Options section:
   - Select INV Open Loop for the build level under INCR_BUILD option.
   - Select output to be DC under PFC INPUT/INV OUTPUT options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

2. If this is an adapted solution, edit the setting under Voltage and Current Sensing Parameters. One can refer to the calculations.xlsx file which is available under the C2000Ware DigitalPower SDK Install directory at <install_location>\solutions\idm_02008\hardware for details on sensing circuit and how max range is computed for the powerSUITE page

3. Under Power Stage Parameters specify the switching frequency, the dead band, and the power rating.
3.1.2.4.5.2 Building and Loading Project

1. Right click on the project name, and click Rebuild Project.
2. The project builds successfully.
3. In the Project Explorer make sure the correct target configuration file is set as Active under targetconfigs (Figure 17).
4. Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
5. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

3.1.2.4.5.3 Setup Debug Environment Windows

1. To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the setupdebugenv_build4.js script file located inside the project folder. This script file populates the watch window with appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous update of values from the controller.

![Figure 42. Build Level 4 dc Expressions View](image)

2. Run the project by clicking ⏯️.
3. Now Halt the processor by using the Halt button on the toolbar (❑)

3.1.2.4.5.4 Running Code

1. Now run the project again by clicking ⏯️.
2. In a few seconds the inrush relay clicks, the software is programmed to do so in the build level with DC. The trip clears, and a duty cycle of 0.5 is applied.
3. In the watch view, check if the guiVin, guiVbus, guiIi, variables are updating, periodically.
   • Note: As no power is applied right now, this value is close to zero.
4. Now slowly increase the input DC voltage from zero to 240 V. The output voltage shows a step down voltage (buck converter operation) as a steady duty cycle of 0.5 PU is applied as default setting. If a high current is drawn, verify if the voltage terminals are swapped. If true, reduce the voltage to zero first and correct the issue before resuming the test.
5. Verifying the voltage sensing: Make sure guiVin and guiVbus display the correct values, for 240-V DC input, guiVin is close to 120V. This verifies the voltage sensing of the board in some manner.
6. Verifying the current sensing: Notice the guiIIi for the given test condition; this value is close to 1 A.
7. Once finished, reduce the input voltage to zero and watch for the bus voltages to reduce down to zero.

8. This completes the check for this build, the following items are verified on successful completion of this build:
   - Sensing of voltages and currents and scaling to be correct
   - Interrupt generation and execution of the BUILD 4 code in the current loop ISR and Voltage Loop Instrumentation ISR
   - PWM driver and switching
   If any issue is observed a careful inspection of the hardware may be required to eliminate any build issues and so forth.

9. The controller can now be halted, and the debug connection terminated.

10. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the **Halt** button on the toolbar ( ) or by using **Target → Halt**. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU by clicking on .

11. Close CCS debug session by clicking on **Terminate Debug Session (Target → Terminate all)**.

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3.1.2.4.6 **INCR_BUILD 4: Open loop, AC (Inverter)**

3.1.2.4.6.1 **Setting Software Options for BUILD 4 (AC)**

In this build the board is excited in open loop fashion with a sinusoidal duty cycle for inverter mode operation. The duty cycle is controlled with dutyPU variable. The test procedure is similar to incremental build 4 open loop DC. HW setup is identical to INCR_BUILD4 open loop dc test shown in Figure 41.

3.1.2.4.6.2 **Setting Software Options for BUILD 4 (AC)**

Setting Software Options for BUILD 1 powerSUITE Settings : On the powerSUITE page select under **Project Options** section:
   - Select INV Open Loop for the build level under INCR_BUILD option.
   - Select output to be AC under PFC INPUT/INV Output options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

3.1.2.4.6.3 **Building and Loading Project and Setting up Debug**

1. Right click on the project name, and click **Rebuild Project**. The project builds successfully. Click **Run → Debug**, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on
the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the setupdebugenv_build4.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as

![Figure 44. Build Level 4 ac Expressions View](image)

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.

3.1.2.4.6.4 Running Code

1. Now run the project again by clicking .
2. The inrush relay is closed when the DC bus voltage is higher than 110 V. The trip clears, and a sinusoidal duty cycle is applied.
3. In the watch view, check if the guiVin, guiVbus, guiIi, variables are updating, periodically.
   • Note: As no power is applied right now, this value is close to zero.
4. Now slowly increase the input DC voltage from zero to 240 V.
5. Verifying the voltage sensing: Make sure guiVinrms and guiVbus display the correct values, for 240-V DC input, guiVrms is close to 85V. This verifies the voltage sensing of the board in some manner.
6. Verifying the current sensing: Notice the guiIrms for the given test condition; this value is close to 0.65 A.

![Figure 45. Build Level 4 ac: Watch Expression Showing Measured Voltage and Currents](image)

7. The controller can now be halted, and the debug connection terminated.
8. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU by clicking on .

9. Close CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).

3.1.2.4.7 **INCR_BUILD 5: Closed Current Loop, DC (Inverter with resistive load)**

In this build, BUILD 5, the inner current loop is closed that is the inductor current is controlled using a current compensator \( G_i \). The current loop model is identical to PFC mode operation shown in Section 3.1.2.4.2 but the current reference direction is opposite to PFC mode (negative current reference).

3.1.2.4.7.1 **Setting Software Options for BUILD 5 (DC)**

1. Make sure the hardware is setup as outlined in Figure 41. Do not supply any high voltage (HV) power to the board yet.

2. powerSUITE Settings : On the powerSUITE page select under Project Options section:
   - Select INV Closed Current Loop (Resistive Load) for the build level under INCR_BUILD option.
   - Select input to be DC under PFC INPUT/INV Output options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

3. Assuming all other options are same as specified earlier in Section 3.1.2.4.5.1.

4. Under Control Loop Design, options for the current loop tuning automatically be selected (Tuning → Current Loop → COMP1 → DCL_PI_C1). Now click on the Compensation Designer icon.

3.1.2.4.7.2 **Designing Current Loop Compensator**

The compensator design for inverter mode is identical to PFC mode. The compensator design procedures are provided in Section 3.1.2.4.2.2.

3.1.2.4.7.3 **Building and Loading Project and Setting up Debug**

1. Right click the project name, and click Rebuild Project. The project builds successfully. Click Run → Debug, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the setupdebugenv_build2_dc.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as Figure 46.
3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the 
   button.

4. Run the project by clicking on 

5. Now Halt the processor by using the Halt button on the toolbar 

### 3.1.2.4.7.4 Running Code

1. The project is programmed to drive the inrush relay and clear the trip after a set amount of time, that
   is, autoStartSlew==100. The software is programmed to do so in the build level with DC. An input
   voltage must be applied after hitting run and before this autoslew counter reaches 100. If the counter
   reaches 100, before voltage is applied at the input, the code must be reset. For which the controller
   must be brought out of real time mode, a reset performed and restarted.

2. Now run the project by clicking 

3. Apply an input voltage of approximately 120 V before the autoStartSlew reaches 100. As soon as autoStartSlew reaches 100, the inrush relay is triggered, and PWM trip is cleared along with closing the current loop flag.

4. ac_cur_ref is set to -0.03 by default and the output voltage is close to 120 V and output current is close to 1 A.

5. Now slowly increase Vbus=240 V and see if output voltage and current stay in 120 V and 1 A.

6. In this build, SFRA can measure the frequency response. However the resistive load changes the plant pole location and the measurement result is different from Figure 35. SFRA for inverter mode will be revisited in incremental build level 6.

7. To bring the system to a safe stop, bring the input DC voltage down to zero, observe the guiVin comes down to zero as well.

8. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).

9. Close the CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).

3.1.2.4.8 INCR_BUILD 5: Closed Current Loop, AC (Inverter with resistive load)

In this build, BUILD5, the inner current loop is closed that is the inductor current is controlled using a current compensator Gi. Both DC bus and output voltage feedforward are applied to the output of this current compensator to generate the duty cycle of the inverter along with soft start for PWM around the zero crossing. The current loop model is identical to PFC mode operation shown in Section 3.1.2.4.2 except for the direction of the reference current.

3.1.2.4.8.1 Setting Software Options for BUILD 5 (AC)

1. Make sure the hardware is setup as outlined in Figure 21. Do not supply any high voltage (HV) power to the board yet.

2. powerSUITE Settings : On the powerSUITE page select under Project Options section:
   - Select INV Closed Current Loop (Resistive Load) for the build level under INCR_BUILD option.
   - Select output to be AC under PFC INPUT/INV Output options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding.
3. Assuming all other options are same as specified earlier in Section 3.1.2.4.5.1.

4. Under Control Loop Design, options for the current loop tuning automatically be selected (Tuning → Current Loop → COMP1 → DCL_PI_C1). Now click on the Compensation Designer icon.

3.1.2.4.8.2 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click Rebuild Project. The project builds successfully. Click Run → Debug, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the setupdebugenv_build2_dc.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button on the watch window to enable continuous update of values from the controller. The watch window appears as Figure 46.

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.

4. Run the project by clicking .

5. Now Halt the processor by using the Halt button on the toolbar.

3.1.2.4.8.3 Running Code

1. The project is programmed to wait for dc bus voltage to exceed approximately 110V to drive the inrush relay, and clear the trip.

2. Run the project by clicking .

3. Now apply an input voltage of approximately 120 V, the board comes out of the undervoltage condition and inrush relay is driven and change pwmSwState from pwmSwState_defaultState to pwmSwState_normalOperation to enable pwm output. The pwm output is turned off by default and the inverter does not work without selecting this option.

4. Slowly increase the bus voltage to 240 V and set ac_cur_ref = -0.05. The watch window looks similar to Figure 33. The RMS value of inverter output voltage and current are close to 100 V and 0.8 A respectively.
5. To bring the system to a safe stop, switch off the output from the AC power supply thus bring the input AC voltage down to zero, observe the guiVbus comes down to zero as well.

6. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).

7. Close the CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).

3.1.2.4.9 INCR_BUILD 6: Closed Current Loop (Grid Connected Inverter)

In this build, BUILD6, the inner current loop is closed under the grid-tied condition. Both DC bus and output voltage feedforward are applied to the output of this current compensator to generate the duty cycle of the inverter along with soft start for PWM around the zero crossing. The current loop model is identical to PFC mode operation shown in Section 3.1.2.4.2.

3.1.2.4.9.1 Setting Software Options for BUILD 6

1. powerSUITE Settings: On the powerSUITE page select under Project Options section:
   - Select INV Closed Current Loop (Resistive Load) for the build level under INCR_BUILD option.
   - Select input to be DC under PFC INPUT/INV Output options
   - Also disable the other options such as Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding

2. Assuming all other options are same as specified earlier in Section 3.1.2.4.5.1.

3. Under Control Loop Design, options for the current loop tuning automatically be selected (Tuning → Current Loop → COMP1 → DCL_PI_C1). Now click on the Compensation Designer icon ( ).

3.1.2.4.9.2 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click Rebuild Project. The project builds successfully. Click Run → Debug, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

2. To add the variables in the watch and expressions window click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open to browse to the
setupdebugenv_build2_dc.js script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on Continuous Refresh button (搡) on the watch window to enable continuous update of values from the controller. The watch window appears as Figure 46.

![Watch Window Image]

**Figure 50. Build Level 6: Closed Current Loop (Grid-connected) Expressions View**

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.

4. Run the project by clicking on  ⏯️ .

5. Now Halt the processor by using the Halt button on the toolbar ( ⏸️ ).

### 3.1.2.4.9.3 Running Code: Emulated Grid-tied Condition (Verification purpose only)

**Power Flow**

![Power Flow Diagram]

**Figure 51. HW setup for Build 6 Emulated Grid Condition**

1. The project is programmed to wait for dc bus voltage(Vbus) and ac source voltage (guiVrms) to exceed approximately 340 V and 75 Vrms to drive the in rush relay, and clear the trip.

2. Run the project by clicking ⏯️ .

3. Now apply an input voltage of approximately 340 V, the board comes out of the undervoltage
condition. To run the solution, ac voltage has to be higher than 75 V rms and inrush relay is driven. ac_cur_ref is set to -0.03 by default.

4. Change `pwmSwState` from `pwmSwState_defaultState` to `pwmSwState_normalOperation` to enable pwm output. The pwm output is turned off by default and the inverter does not work without selecting this option.

5. Slowly increase ac_cur_ref to -0.05 and inverter output current is close to 0.8 A in RMS value. The voltage of inverter output is determined by the ac voltage source.

---

**Figure 52. Build Level 6: Closed Current Loop (Grid-connected) after close the current loop**

6. To bring the system to a safe stop, switch off the output from the AC power supply thus bring the input AC voltage down to zero, observe the guiVbus comes down to zero as well.

7. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the `Halt` button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).

8. Close the CCS debug session by clicking Terminate Debug Session (Target → Terminate all).
3.1.2.4.9.4 Running Code: Grid-tied Condition

1. The project is programmed to wait for dc bus voltage (Vbus) and ac source voltage (guiVrms) to exceed approximately 340 V and 75 Vrms to drive the in rush relay, and clear the trip.

2. Run the project by clicking ⚡.

3. Now apply an input voltage of approximately 340 V, the board comes out of the undervoltage condition. To run the solution, ac voltage has to be higher than 75 V rms and inrush relay is driven.

4. Change pwmSwState from pwmSwState_defaultState to pwmSwState_normalOperation to enable pwm output. The pwm output is turned off by default and the inverter does not work without selecting this option.

5. Then slowly increase the ac_cur_ref to -0.3 and inverter output current is close to 5.3 A in RMS value. The voltage of inverter output is determined by the grid.

6. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click the SFRA icon. SFRA GUI appears.
7. Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on **Setup Connection**. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click OK. Return to the SFRA GUI, and click **Connect**.

**Figure 55. Voltage and current waveform (Build Level 6 Grid-Connected Condition)**
8. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking Start Sweep. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears, Figure 35. This is similar to the plot seen under DC conditions; however, some additional noise is visible due to AC harmonic frequencies close to the measured frequencies. The BW, PM, and GM numbers are very similar to the DC case. Note the graph shown in Figure 35 was taken with direct grid AC input. When using AC source interaction of the AC source output, impedance can be observed, which can affect the control margins.

![Figure 56. SFRA Run, Closed Current Loop, Open Loop Gain (Inverter mode)](image)

9. To bring the system to a safe stop, switch off the output from the AC power supply thus bring the input AC voltage down to zero, observe the guiVbus comes down to zero as well.

10. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the Halt button on the toolbar ( ) or by using Target → Halt. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).

11. Close the CCS debug session by clicking on Terminate Debug Session (Target → Terminate all).

3.1.2.5 Running Code on CLA

This solution is supported with an option to run the code on the CLA. This option is selected using a drop-down box under project option on the powerSUITE main.cfg page. Running on CLA can be selected for any build level option.
NOTE: SFRA library does not support CLA, hence the SFRA cannot be run when using CLA. 
DLOG is also not used when using CLA, hence the datalogging graphs will not work when using CLA.

Once the option is changed, the CFG file must be saved and the project re-compiled. Once recompiled, 
follow the steps as outlined in the specific incremental build level documentation.

Depending on the device, for example for F28004x CLA supports CLA tasks and a background task, thus 
both 100kHz ISR and 10kHz IST can be offloaded to the CLA. By default if the selection from the 
powerSUITE page is made the faster ISR is moved to the CLA task and the slower ISR is moved to the 
background task by default. If the user does not want to run the 10kHz ISR on the CLA, the option to do 
so is available under the <solution>_user_settings.h file.

```c
#if CONTROL_RUNNING_ON == CLA_CORE
#define INSTRUMENTATION_ISR_RUNNING_ON CLA_CORE
#else
#define INSTRUMENTATION_ISR_RUNNING_ON C28x_CORE
#endif
```

3.1.2.6 Advanced Options

In this section some advanced setting that improve the power factor are discussed one by one and their 
relative impact quantified with test results

3.1.2.6.1 Input Cap Compensation for PF Improvement Under Light Load

Input cap causes PF degradation if the current reference is maintained perfectly in sync with the voltage 
as shown in Equation 8 and in Figure 57(a).

\[ i_{\text{ref, dpllvcc}} = i_{\text{ref}} \sin(\omega t) - i_{\text{input, cap, comp}} \cos(\omega t) \] (8)

The current reference can be adjusted with vectors to offset the PF degradation, Equation 9, Figure 57(b ). 
As the angle from the phase locked loop is used to compute the vector this technique is called the digital 
phase locked loop vector cancellation (DPLLVC) technique. This improves PF at light load and high line 
significantly.

\[ i_{\text{ref, DPLLVC}} = i_{\text{ref}} \sin(\omega t) - i_{\text{input, cap, comp}} \cos(\omega t) \] (9)

The amount of correction applied depends on the input capacitor value, for example on this design the 
input cap is 2.2 µF. Which means at high line a capacitive current equal to

\[ \frac{220}{\frac{1}{2} \times \pi \times 60 \times 2.2 \, \mu F} = 0.1823 \, A \]

is drawn. Under light loads, this is significant amount of current and causes power factor loss. The current 
sensor gain on this design is approximately 24 A, so this translates to an adjustment of approximately 0.01 
pu for the high-line condition.
Furthermore, there is a tracking error under low power conditions. This tracking error can be offset by an adjustment to the current command shown in Figure 57©). The amount of this tracking error is adjusted empirically for the best performance from the system. Thus the total current reference is given by Equation 10.

\[ i_{\text{ref}_\text{DPLLVC_TC}} = i_{\text{ref}} \sin(\omega t) - i_{\text{input_cap_comp}} \cos(\omega t) - i_{\text{tracking_error}} \left. \right|_{\text{power dependent}} \cos(\omega t) \]  

\[ (10) \]

Figure 57. Power Factor (a) No Adjustment (b) DPLLVC ©) DPLLVC Plus Tracking Error Compensation

The result for PF improvement are graphed in Figure 58.

Figure 58. PF Graph vs Power at 220 Vrms Highlighting Improvement With Input Cap Current Compensation

This feature can be turned off or on by writing to the INPUT_CAP_COMPENSATION #define variable in the <solution>_user_settings.h file. This setting can be modified by the user. The value of the adjustment is controlled using the #defines HIGH_LINE_INPUT_CAP_COMP_ADJUST & LOW_LINE_INPUT_CAP_COMP_ADJUST. These are in per-unit format and how this value is determined was explained earlier in this section.

#define INPUT_CAP_COMPENSATION 1
#define HIGH_LINE_INPUT_CAP_COMP_ADJUST -0.02
#define LOW_LINE_INPUT_CAP_COMP_ADJUST -0.01

3.1.2.6.2 Adaptive Dead Time for Efficiency Improvements

In continuous conduction mode, the dead-time control for synchronous rectification is critical in terms of short-circuit protection and efficiency. With the optimal dead time, the risk of shoot through can be eliminated and it also prevents an excessive conduction loss from body diode conduction of Sync FET. Therefore, the goal of optimal dead time is not to turn on the Active FET and Sync FET simultaneously while minimize a redundant third quadrant conduction of Sync FET.

This optimal dead time can be calculated from the measured current and the device output capacitance, this is given by Equation 11.
Figure 59 shows the block diagram for implementation.

\[
t_{\text{deadtime\_optimal}} = \frac{2C_{\text{o}} V_{\text{out}}}{I_{\text{peak}}}
\]

(11)

The option enables power saving, which is shown for the high line case in Figure 60 compared to a fixed dead time from which it can be inferred that avoiding the shoot through at low power levels results in significant power savings. However, once the shoot through is avoided the power savings drop first and then progressively increase as power increases and the diode conduction time is reduced by implementing adaptive dead-time adjustment.

To enable adaptive dead-time, select the drop down box under Project Options on the powerSUITE page of the solution. For FED the fixed value that is specified on the main.syscfg is used. When adaptive dead time is enabled the RED is modulated and the minimum and maximum bounds are specified in the <solution>_user_settings.h. The following are the #define that can be adjusted:

```c
#define GAN_COSS (float32_t) 0.000000000145
#define PFC_DEADBAND_RED_MIN_US (float32_t) 0.020
#define PFC_DEADBAND_RED_MAX_US (float32_t) 0.200
```

Following these adjustments the project must be saved, re-compiled, and loaded on the controller when this option is changed. Hardware setup and software instructions as outlined in Section 3.1.2.4.4 can be followed to see the behavior of the board and measure efficiency.
3.1.2.6.3 Phase Shedding for Efficiency Improvements

Phase shedding can be an effective technique to improve efficiency in interleaved application by optimizing for the conduction and the switching losses. In this design there are three phases, so three different configurations are possible as shown in Figure 61.

Figure 61. Phase Shedding Options on TTPL PFC

In each of these modes the phase shift between each of them must be adjusted. When in two-phase mode, a 180° phase shift is desired between the PWMs, and when in three-phase mode, a 120° of phase shift is desired.

The decision to do phase shedding can be made on different parameters, such as the RMS current, power, the peak inductor current, and so on. When using RMS current the change of phases can be significantly delayed. Figure 62 shows phase shedding when the decision is based on RMS current. Code takes multiple AC cycles before the phases are added.

Figure 62. Waveform When Decision to Add Phases is Based on RMS Calculation
This delay may not be acceptable for many applications. Thus, the voltage controller output is chosen as the decision point to drop or add phases. A state machine is constructed as shown in Figure 63, with some hysteresis built around the phase shedding points.

![State Machine for Phase Shedding Control](image)

Bringing a phase in and out can cause inadvertent pulses to be generated. Hence the implementation to drop and add phase is done through the GPIO and PWM peripheral switch using the GPIO pin Mux registers. All PWM capable pins are configured and GPIO outputs and driven low. Now based on how many phases must be applied the GPIO pin mux is changed accordingly. It is safe to enable and disable the phases using the GPIO pin mux switch at any point in the AC cycle as the registers in the PWM are shadowed. Figure 64 shows details of the implementation of phase shedding on the C2000 MCU.

![Implementation of Phase Shedding on TTPL PFC Using C2000™ MCU](image)

To enable phase shedding setting can be set in the `<solution>_user_settings.h` file and modifying `PHASE_SHEDDING_ENABLED` define. The points at which phases are brought in and out are set by changing the `PHASE_SHEDDING_1PH_2PH_TRANSITION_CURRENT` and `PHASE_SHEDDING_2PH_3PH_TRANSITION_CURRENT` define, which correspond to I1 and I2 as shown in Figure 64. Recompile the code, load the code, and repeat the steps as outlined in Section 3.1.2.4.4 to test this feature. With this feature implemented, under transients the phases are dropped and added quickly.
Figure 65 and Figure 66 show the transient at 110 Vrms of 1.3 KW to 150 W and vice versa. The phases are added back quickly and dropped quickly under transients as the decision is based on the voltage loop generated current reference.

**Figure 65. Phase Added Quickly Under Transient at 120 Vrms, 60 Hz**

**Figure 66. Phase Shed Quickly Under Transient at 120 Vrms, 60 Hz**
Similarly at high line, a transient greater than 2 KW is applied, and the phase goes from single to three phase almost instantly. Figure 67 and Figure 67 show the test waveform at high line under transient of 2.16 KW to 150 W and vice versa.

![Figure 67. Phase Added Quickly Under Transient at 230 Vrms, 50 Hz](image1)

![Figure 68. Phase Shed Quickly Under Transient at 230 Vrms, 50 Hz](image2)

Figure 69 shows the efficiency improvement at 230 Vrms with phase shedding.

![Figure 69. Efficiency Comparison at 230 Vrms With Phase Shedding and Without](image3)
3.1.2.6.4 Non-Linear Voltage Loop for Transient Reduction

The PFC stage control is composed of an inner current loop, which tries to follow the input voltage and an outer voltage loop that tries to maintain a constant DC bus voltage at the output. The voltage loop is thus in conflict with the current loop and hence must be designed to be very low bandwidth (approximately 10 Hz) in order to achieve good power factor. The slow voltage loop results in significant overshoot and undershoot under transients (see Figure 70).

![Figure 70. Non-Linear Voltage Loop with Hysteresis](image)

To improve voltage overshoot and undershoot, while maintaining good power factor a non-linear voltage control loop is implemented as shown in Figure 71. A hysteresis band is added in the non-linear voltage loop to avoid oscillation between high-gain and low-gain mode. Furthermore the gain change is slewed to avoid any sudden changes. Figure 72 shows the result with non-linear voltage loop.

![Figure 71. Voltage Transient Without Non-Linear Voltage Loop, Vin 120 Vrms, 880 W to 0 W Transient, Overshoot 51.2 V](image)

![Figure 72. Voltage Transient With Non-Linear Voltage Loop, Vin 120 Vrms, 880 W to 0 W Transient, Overshoot 16.8 V](image)
To enable non-linear voltage loop, select the drop down box under Project Options on the powerSUITE page of the solution. Default value of five times the gain is applied for the proportional term under transient condition. This value can be adjusted under the <solution>_user_settings.h file by modifying the NON_LINEAR_V_LOOP_KP_MULTIPLIER define. The project must be saved, re-compiled, and loaded on the controller when this option is changed. Hardware setup and software instructions for the Build Level 3 can be followed to see the behavior of the board under transients.

3.1.2.6.5 Software Phase Locked Loop Methods: SOGI - FLL

To meet industry standards, the design must be tested under frequency transients. This poses a problem when using PLL angle for the drive of the PWM signal if the PLL cannot adapt to the frequency change. A frequency locked loop scheme, as proposed in Grid Synchronization of Power Converters Using Multiple Second Order Generalized Integrators [1], can be used to make the software phase locked loop frequency adaptive.

The module follows the same basic structure as the SOGI PLL module, with implementation discussed in Software PLL Design Using C2000 MCUs Single Phase Grid Connected Inverter [2]. A frequency adaptive feature through a frequency locked loop is added as shown in Figure 73.

![Figure 73. Software Phase Locked Loop Structure Based on Second Order Generalized Integrator and Frequency Locked Loop](image)

To select a PLL method go to the <solution>_user_settings.h. The following are the #define that can be adjusted:

```c
#define SPLL_METHOD_SELECT SPLL_1PH_SOGI_FLL_SEL
```

Following this adjustment the project must be saved, re-compiled, and loaded on the controller. Hardware setup and software instructions for the Build Level 3 can be followed to see the behavior of the board with the new PLL scheme.
3.2 Testing and Results

3.2.1 Test Results at Input 120 Vrms, 60 Hz, Output 380-V DC

3.2.1.1 Startup

The startup sequence of the power stage is shown in Figure 74 with input single phase of 120 Vrms VL-N, an output bus regulated at 380 V, and a 1.6-KW load and no load.

![Figure 74. Startup of PFC Operation at 120-Vac IN, 380-V DC OUT and 1.6-KW Load](image)

Figure 75 shows the startup under no load.

![Figure 75. Startup of PFC at 120-Vac IN, 380-V DC Output, and 0% Load](image)

3.2.1.2 Steady State Condition

Steady state current waveforms are shown in Figure 76, Figure 77, and Figure 78 at different load conditions. Phase shedding is disabled for these readings.

![Figure 76. Steady State 120-Vac IN, 380-V DC OUT 300W, iTHD 5.5%](image)
Table 4 lists the detailed test results of this design under varying load conditions with 120-Vac input and 380-V DC output. For this data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard-switched edge, and the soft switching edge dead time varies between 20 ns and 200 ns.

**Table 4. Detailed Test Results with 120-Vac IN, 380-V DC OUT, and Different Power Levels**

<table>
<thead>
<tr>
<th>Vin (V RMS)</th>
<th>Vout (V)</th>
<th>Pin (W)</th>
<th>Iout (A)</th>
<th>Pout (W)</th>
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<th>ITHD %</th>
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3.2.1.3 Transient Test With Step Load Change

3.2.1.3.1 0% to 50% Load Step Change

Figure 79 shows the transient response when input is 120 Vrms and a load step of 50% is applied to the power stage.

![Figure 79. Transient Response, 120 Vrms, 60 Hz, 0% to 50% Load Step](image)

3.2.1.3.2 50% to 100% Load Step Change

Figure 80 shows the transient response when input is 120 Vrms and load is stepped up from 50% to 100%.

![Figure 80. Transient Response, 120 Vrms, 60 Hz, 50% to 100% Load Step](image)

3.2.1.3.3 100% to 50% Load Step Change

Figure 81 shows the transient response when the input is 120 Vrms and load is stepped down from 100% to 50%.

![Figure 81. Transient Response, 120 Vrms, 60 Hz, 100% to 50% Load Step](image)
3.2.1.3.4 50% to 100% Load Step Change

Figure 82 shows the transient response when input is 120Vrms and load is stepped down from 50% to 0%.

![Figure 82. Transient Response, 120 Vrms, 60 Hz, 50% to 0% Load Step](image)

3.2.2 Test Results at Input 230 Vrms, 50 Hz, Output 380 V DC

3.2.2.1 Startup

Figure 83 shows the startup sequence of the power stage with input single phase 230-Vrms VL-N and output bus regulated at 380V and a 880-W load.

![Figure 83. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at 880-W Load](image)

Figure 84 shows the startup of PFC at no load at 230 Vrms.

![Figure 84. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at no Load](image)
3.2.2.2 Steady State Condition

Figure 85, Figure 86, and Figure 87 show the steady state current waveform at different load conditions. Phase shedding is disabled for these readings.

**Figure 85.** Steady State 230-Vac IN, 380-V DC OUT, 1.1KW, iTHD 3.14%

**Figure 86.** Steady State 230-Vac IN, 380-V DC OUT, 2.2KW, iTHD 2.62%

**Figure 87.** Steady State 230-Vac IN, 380-V DC OUT, 3.3KW, iTHD 2.69%
Table 5 lists the detailed test results of this design under varying load conditions with 230-Vac input and 380-V DC output. For the following data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard switched edge, and the soft-switching edge dead time varies between 20 ns to 200 ns.

![Graph 1](image1.png)

### Table 5. Detailed Test Results With 230-Vac IN, 380-V DC OUT and Different Power Levels

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3.2.2.3 **Transient Test With Step Load Change**

Following sections show the transient test results with step load change.

3.2.2.3.1 **33% to 100% Load Step Change**

Figure 88 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

![Graph 2](image2.png)

**Figure 88. Transient Response, 230 Vrms 50 Hz, 33% to 100% Load Step**
**3.2.2.3.2 100% to 33% Load Step Change**

Figure 89 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

**3.2.3 Test Results Graphs**

Figure 90 shows the efficiency data plotted under different test conditions for this design.

Figure 91 shows the THD data plotted under these test conditions.
Figure 92 shows the PF data plotted under these test conditions.

Figure 92. PF at 230 Vrms and 120Vrms With Varying Load
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDM-1007.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDM-1007.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints
To download the layer plots, see the design files at TIDM-1007.

4.4 Altium Project
To download the Altium project files, see the design files at TIDM-1007.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDM-1007.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDM-1007.

5 Software Files
To download the software files, see the design files at TIDM-1007.

6 Related Documentation

- Texas Instruments, *How to reduced current spike at AC zero crossing for totem-pole PFC Technical Brief*
- Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers Data Sheet*
- Texas Instruments, *LMG3410 600-V 12-A Single Channel GaN Power Stage Data Sheet*
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7 About the Author

MANISH BHARDWAJ is a Systems Application Engineer with C2000 Microcontrollers System Solutions Group at Texas Instruments, where he is responsible for developing reference design solutions for digital power, motor control, and solar power applications. Before joining TI in 2009, Manish received his Masters of Science in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta in 2008 and his Bachelor of Engineering from Netaji Subhash Institute of Technology, University of Delhi, India in 2007.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (June 2018) to C Revision

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Changes from A Revision (March 2018) to B Revision

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Revision History

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