

TI Designs: TIDA-01519

Fire and Carbon Monoxide Alarm Detector Reference Design With Low BOM Cost and Integrated Battery Backup



Description

This reference design is a carbon monoxide (CO) and fire alarm detector that can identify typical alarm sounds and has the wireless capabilities to alert the user if one is detected. This design is intended for home automation and "smart" environmental sensing. Once a 3-kHz or 520-Hz signal frequency is identified based on FFT power spectral density analysis, this system determines whether an alarm is occurring, which can then be used with Sensor to Cloud to alert the homeowner in the case of an alarm outside of their detectable hearing range.

Resources

TIDA-01519	Design Folder
TLV2313	Product Folder
CC1310	Product Folder
UCC28881	Product Folder
TPS27081A	Product Folder
LM2903	Product Folder
TPS780	Product Folder
TPD1E10B06	Product Folder

Features

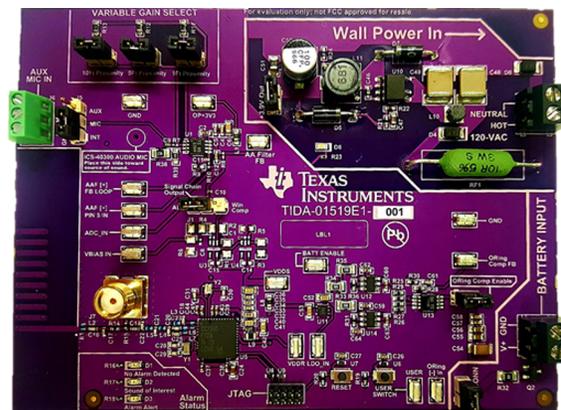
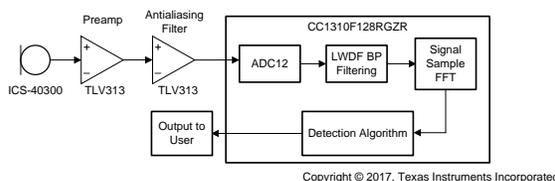
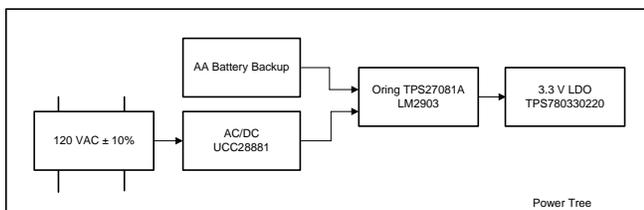
- 3-kHz and 520-Hz Alarm Target Frequencies
- Carbon Monoxide (CO) and Fire Alarm Detection
- Wall Powered Design
- Auxiliary Battery Backup During Power Outages
- Low BOM Cost Design
- Variable Microphone Gain Based on Proximity to Alarm
- Sub-1 GHz Wireless Communication Enabled for Sensor-to-Cloud Configuration

Applications

- Alarm Detection
- "Smart" Sensor Ecosystem
- Fire Safety
- Building Automation



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1 System Description

Many residential and commercial building are required to have fire and carbon monoxide (CO) detectors located in specific places around the structure as regulations permit. These alarm systems can be cut off from other sections of the building or home, making an isolated fire more likely to spread to other sections of the building if the alarm is outside of the inhabitants' hearing range. To address this problem, devices developed today can detect and relay this alarm to a person—in some cases, anywhere in the world. Most of these systems run on battery or wall power only, potentially increasing the likelihood of an undetected fire or CO situation should the batteries die or the power go out for a period of time.

Enabled by Texas Instruments' low-power amplifiers, comparators, load switches, and the SimpleLink™ ultra-low-power wireless MCU platform, the Fire and Carbon Monoxide Alarm Detector Reference Design With Low BOM Cost and Integrated Battery Backup demonstrates a fire and CO detector while optimizing both cost and power sourcing.

At a high level, this design consists of a 120-V AC wall-powered rectification subsystem, composed of both discrete components as well as the UCC28881. The signal chain consists of a two-channel TLV313 low-power, precision op amp used for both amplification as well as an antialiasing filter. The microphone input to this signal chain is an InvenSense ICS-40300 MEMs microphone with a wide dynamic range. The power ORing consists of an LM2903 comparator and two TPS27081 load switches. This ORing circuitry is designed to seamlessly switch between the 3.9-V output rail of the UC28881 and a 3.7-V Li-Ion battery, providing the TPS78033022 with the voltage needed for the 3.3-V regulated output. These peripherals along with the integrated CC1310 device and detection firmware make up this reference design.

This design guide addresses the component selection, design theory, and the testing results of this reference design system. The scope of this design guide gives system designers a head-start in integrating TI's low-power, cost-optimized analog components, and the SimpleLink ultra-low-power wireless MCU platform.

The following subsections describe the various blocks within this reference design and what characteristics are most critical to best implement the corresponding function.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS			DETAILS
	MIN	TYP	MAX	
120-V AC to DC efficiency	70%	—	—	Section 2.3.1.1
3.3-V LDO efficiency	80%	—	—	Section 2.3.1.3
Current consumption (no alarm)	7.38 mA	—	17.50 mA	Section 3.2.2.3
Current consumption (alarm detected)	11.32 mA	—	21.45 mA	Section 3.2.2.3
Detectable alarm frequencies	520 Hz	—	3.5 kHz	—
UL217-Regulated detectable audio temporal patterns	CO alarm and fire alarm audio temporal patterns			—
Minimum alarm SPL level (dB)	85-dBm SPL			—
Detection range	>10 ft (dependent on gain settings)			—
Wireless communication protocol	Sub-1 GHz (868 or 915 MHz)			—
Audio input gain level	4.59 V/V	—	437 V/V	Section 2.3.2.2
Backup battery requirements	3.7-V AA LI-Ion battery			—

2 System Overview

2.1 Block Diagram

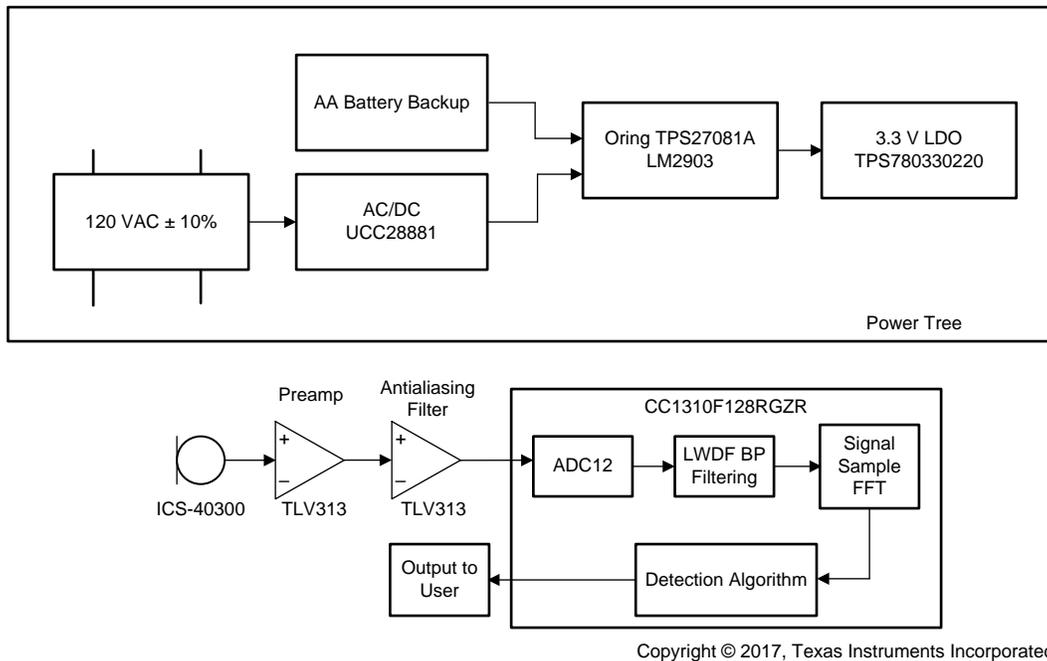


Figure 1. TIDA-01519 Block Diagram

2.2 Highlighted Products

2.2.1 CC1310F128RGZR

The CC1310 is a member of the CC26xx and CC13xx family of cost-effective, ultra-low-power, 2.4-GHz and Sub-1 GHz RF devices. Very low active RF and microcontroller (MCU) current consumption, in addition to flexible low-power modes, provide excellent battery lifetime and allow long-range operation on small coin-cell batteries and in energy-harvesting applications.

The CC1310 device is the first device in a Sub-1 GHz family of cost-effective, ultra-low-power wireless MCUs. The CC1310 device combines a flexible, very low-power RF transceiver with a powerful 48-MHz Cortex®-M3 MCU in a platform supporting multiple physical layers and RF standards. A dedicated radio controller (Cortex-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultra-low power and flexibility. The low-power consumption of the CC1310 device does not come at the expense of RF performance; the CC1310 device has excellent sensitivity and robustness (selectivity and blocking) performance.

The CC1310 device is a highly integrated, true single-chip solution incorporating a complete RF system and an on-chip DC-DC converter.

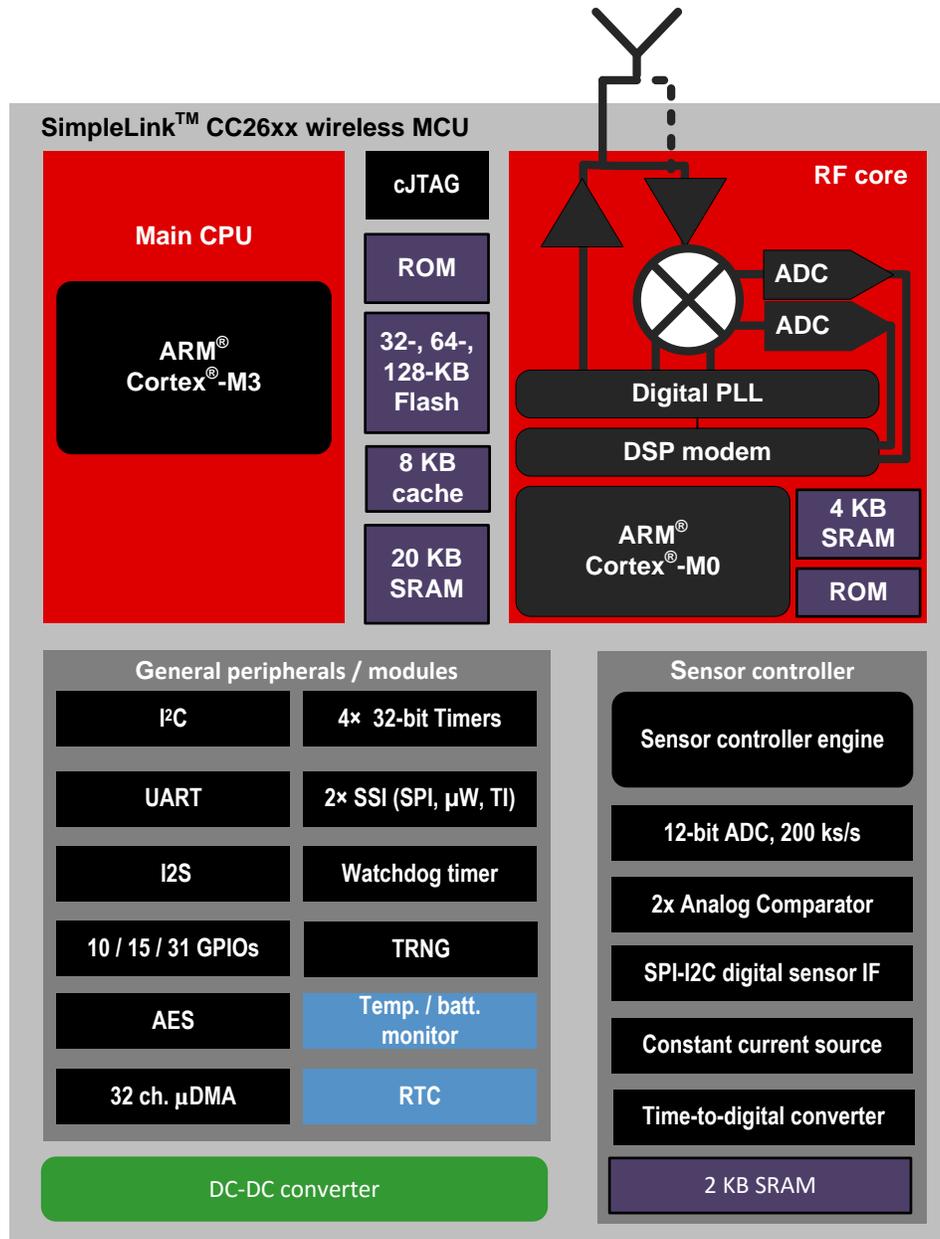
Sensors can be handled in a very low-power manner by a dedicated autonomous ultra-low-power MCU that can be configured to handle analog and digital sensors; thus the main MCU (Cortex-M3) can maximize sleep time.

The CC1310 power and clock management and radio systems require specific configuration and handling by software to operate correctly, which has been implemented in the [TI-RTOS](#). TI recommends using this software framework for all application development on the device. The complete TI-RTOS and device drivers are offered in source code free of charge.

- MCU:
 - Powerful ARM® Cortex-M3 Processor

- EEMBC CoreMark® Score: 142
- EEMBC ULPBench™ Score: 158
- Clock speed up to 48 MHz
- 32KB, 64KB, and 128KB of in-system programmable flash
- 8KB of SRAM for cache (or as general-purpose RAM)
- 20KB of ultra-low-leakage SRAM
- 2-pin cJTAG and JTAG debugging
- Supports over-the-air (OTA) update
- Ultra-low-power sensor controller:
 - Can run autonomously from the rest of the system
 - 16-bit architecture
 - 2KB of ultra-low-leakage SRAM for code and data
- Efficient code-size architecture, placing parts of TI-RTOS, drivers, and Bootloader in ROM
- Peripherals
 - All digital peripheral pins can be routed to any GPIO
 - Four general-purpose timer modules (eight 16-bit or four 32-bit timers, PWM Each)
 - 12-Bit ADC, 200 ksamples/s, 8-channel Analog MUX
 - Continuous time comparator
 - Ultra-low-power clocked comparator
 - Programmable current source
 - UART
 - 2× SSI (SPI, MICROWIRE, TI)
 - I²C, I2S
 - Real-time clock (RTC)
 - AES-128 k
 - True random number generator (TRNG)
 - Support for eight capacitive sensing buttons
 - Integrated temperature sensor
- External system
 - On-chip internal DC-DC converter
 - Seamless integration with the SimpleLink CC1190 range extenders
- Low power
 - Wide supply voltage range: 1.8 to 3.8 V
 - RX: 5.4 mA
 - TX at 10 dBm: 13.4 mA
 - Active-Mode MCU 48 MHz running Coremark: 2.5 mA (51 μ A/MHz)
 - Active-Mode MCU: 48.5 CoreMark/mA
 - Active-Mode sensor controller at 24 MHz: 0.4 mA + 8.2 μ A/MHz
 - Sensor controller, one wakeup every second performing one 12-bit ADC sampling: 0.95 μ A
 - Standby: 0.7 μ A (RTC running and RAM and CPU retention)
 - Shutdown: 185 nA (Wakeup on external events)
- RF core:
 - Excellent receiver sensitivity: –124dBm using long-range mode, –110dBm at 50 kbps (Sub-1 GHz)
 - Excellent selectivity (\pm 100 kHz): 56 dB
 - Excellent blocking performance (\pm 10 MHz): 90 dB

- Programmable output power up to 15 dBm
- Single-ended or differential RF interface
- Suitable for systems targeting compliance with worldwide radio frequency regulations:
 - ETSI EN 300 220, EN 303 204 (Europe)
 - FCC CFR47 Part 15 (US)
 - ARIB STD-T108 (Japan)
- Wireless M-Bus and selected IEEE® 802.15.4g PHY
- RoHS-compliant package:
 - 7-mm × 7-mm RGZ VQFN48 (30 GPIOs)
 - 5-mm × 5-mm RHB VQFN32 (15 GPIOs)
 - 4-mm × 4-mm RSM VQFN32 (10 GPIOs)
- Tools and development environment:
 - Full-feature and low-cost development kits
 - Multiple reference designs for different RF configurations
 - Sensor Controller Studio
 - SmartRF™ Studio
 - SmartRF Flash Programmer 2
 - IAR Embedded Workbench® for ARM
 - Code Composer Studio™ (CCS) IDE



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Figure 2. CC1310 Block Diagram

2.2.2 TLV2313IDGKR

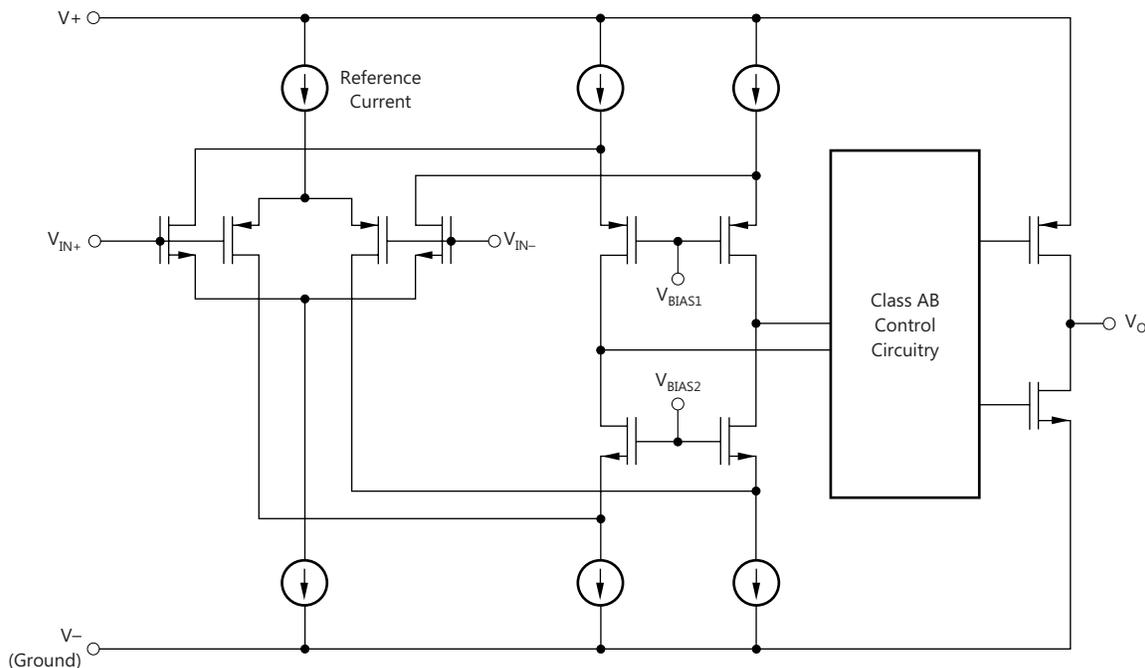
The TLV313 family of single-, dual-, and quad-channel precision op amps combine low-power consumption with good performance. This combination makes this device suitable for a wide range of applications such as wearables, utility metering, building automation, currency counters, and more. The family features rail-to-rail input and output (RRIO) swings, low quiescent current (65 μA , typical), wide bandwidth (1 MHz), and very low noise (26 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz), making it attractive for a variety of battery-powered applications that require a good balance between cost and performance. Further, low-input-bias current enables these devices to be used in applications with $\text{M}\Omega$ source impedances.

The robust design of the TLV313 devices provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 150 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

The devices are optimized for operation at voltages as low as 1.8 V (± 0.9 V) and up to 5.5 V (± 2.75 V), and are specified over the extended temperature range of -40°C to 125°C .

The single-channel TLV313 device is available in both SC70-5 and SOT23-5 packages. The dual-channel TLV2313 device is offered in SOIC-8 and VSSOP-8 packages, and the quad-channel TLV4313 device is offered in a TSSOP-14 package.

- Precision amplifier for cost-sensitive systems
- Low I_Q : 65 $\mu\text{A}/\text{ch}$
- Wide supply range: 1.8 to 5.5 V
- Low noise: 26 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
- Gain bandwidth: 1 MHz
- Rail-to-rail input/output
- Low input bias current: 1 pA
- Low offset voltage: 0.75 mV
- Unity-gain stable
- Internal RF/EMI filter
- Extended temperature range: -40°C to 125°C



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Figure 3. LV2313IDGKR Functional Block Diagram

2.2.4 TPS780

The TPS780 family of low-dropout (LDO) regulators offer the benefits of ultra-low-power, miniaturized packaging, and selectable dual-level output voltage levels with the V_{SET} pin.

The ultra-low-power and dynamic voltage scaling (DVS) capability which provides dual-level output voltages let designers customize power consumption for specific applications. Designers can now shift to a lower voltage level in a battery-powered design when the microprocessor is in sleep mode, further reducing overall system power consumption. The two voltage levels are preset at the factory and are stored using EPROM and are available on fixed output voltage devices.

The TPS780 series of LDOs are designed to be compatible with the TI MSP430 and other similar products. The enable pin is compatible with standard CMOS logic. The TPS780 series also come with thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C . For more cost-sensitive applications requiring a dual-level voltage option and only *on par* I_Q , consider the [TPS781 series](#), with an I_Q of $1.0\ \mu\text{A}$ and dynamic voltage scaling.

- Low I_Q : 500 nA
- 150-mA, low-dropout regulator with pin-selectable dual voltage level output
- Low dropout: 200 mV at 150 mA
- 3% accuracy over load, line, and temperature
- Available in dual-level, fixed-output voltages from 1.5 to 4.2 V
- Available in an adjustable version from 1.22= to 5.25 V or a dual-level output version
- V_{SET} pin toggles output voltage between two factory-programmed voltage levels
- Stable with a 1.0- μF ceramic capacitor
- Thermal shutdown and overcurrent protection
- CMOS logic level-compatible enable pin
- Available in DDC (TSOT23-5) or DRV (2-mm \times 2-mm SON-6) package options

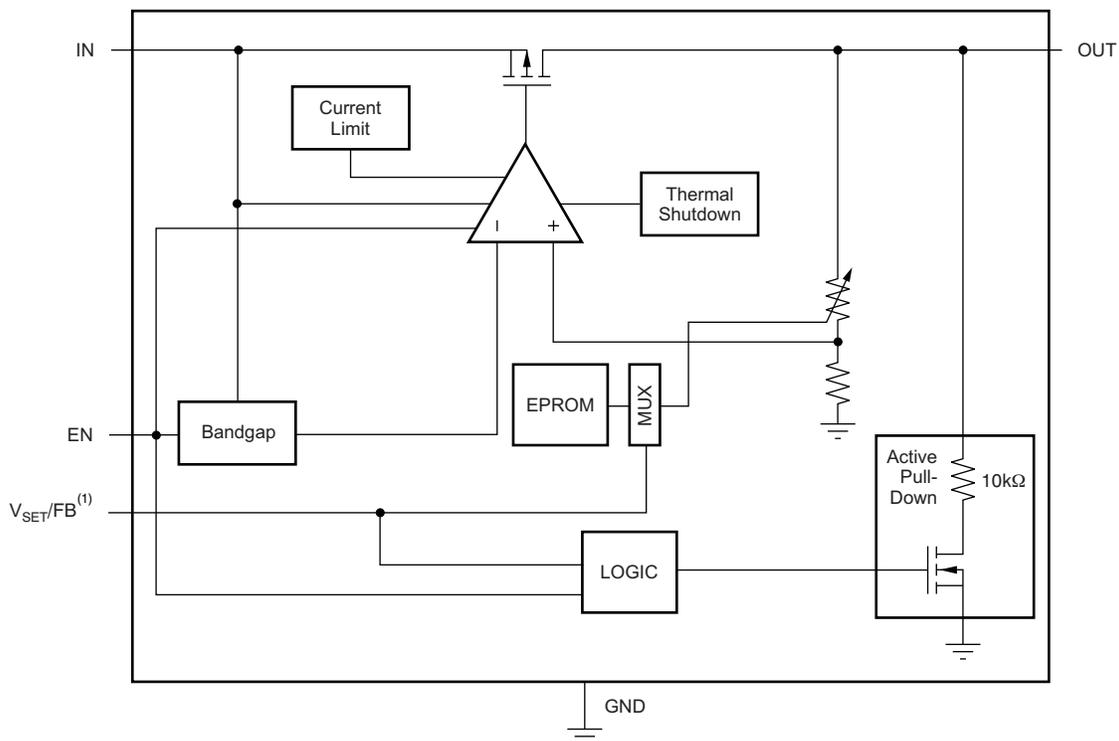


Figure 5. TPS780330220DRVR Functional Block Diagram

2.2.5 TPS27081A

The TPS27081A device is a high-side load switch that integrates a power P-FET and a Control N-FET in a tiny package. The TPS27081A features industry-standard ESD protection on all pins providing better ESD compatibility with other onboard components. The TPS27081A level shifts ON/OFF logic signal to V_{IN} levels and supports as low as 1-V CPU or MCU logic to control higher voltage power supplies without requiring an external level-shifter.

Switching a large value output capacitor C_L through a fast ON/OFF logic signal may result in an excessive inrush current. To control the load inrush current, connect a resistor R_2 and add an external capacitor C_1 as shown in the simplified schematic.

A single pull-up resistor R_1 is required in standby power switch applications. In such applications, connect the R2 pin of the TPS27081A to the system ground when inrush current control is not required.

- Low ON-resistance, high-current P-FET:
 - $R_{DS(on)} = 32\text{ m}\Omega$ at $V_{GS} = -4.5\text{ V}$
 - $R_{DS(on)} = 44\text{ m}\Omega$ at $V_{GS} = -3\text{ V}$
 - $R_{DS(on)} = 82\text{ m}\Omega$ at $V_{GS} = -1.8\text{ V}$
 - $R_{DS(on)} = 93\text{ m}\Omega$ at $V_{GS} = -1.5\text{ V}$
 - $R_{DS(on)} = 15\text{ m}\Omega$ at $V_{GS} = -1.2\text{ V}$
- Adjustable turnon and turnoff slew rate control through external R_1 , R_2 , and C_1
- Supports a wide range of 1.2- to 8-V supply inputs
- Integrated NMOS for PFET control
- NMOS ON/OFF supports a wide range of 1- to 8-V control logic interface
- Full ESD protection (all pins):
 - HBM 2 kV, CDM 500 V
- Ultra-low leakage current in standby (typical 100 nA)
- Available in tiny 6-pin package:
 - 2.9 mm × 2.8 mm × 0.75 mm SOT (DDC)

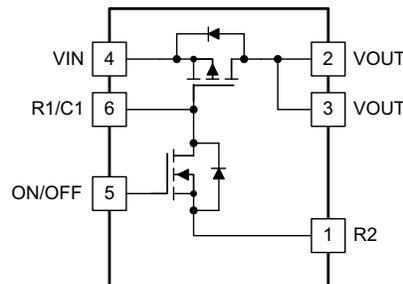


Figure 6. TPS27081A Functional Block Diagram

2.2.6 LM2903DGKR

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 to 36 V, and VCC is at least 1.5 V more positive than the input common-mode voltage. The current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM193 device is characterized for operation from -55°C to 125°C . The LM293 and LM293A devices are characterized for operation from -25°C to 85°C . The LM393 and LM393A devices are characterized for operation from 0°C to 70°C . The LM2903 device is characterized for operation from -40°C to 125°C .

- Single-supply or dual supplies
- Wide range of supply voltage:
 - Maximum rating: 2 to 36 V
 - Tested to 30 V: Non-V devices
 - Tested to 32 V: V-suffix devices
- Low supply-current drain independent of supply voltage: 0.4 mA (typical) per comparator
- Low input bias current: 25 nA (typical)
- Low input offset current: 3 nA (typical) (LM139)
- Low input offset voltage: 2 mV (typical)
- Common-mode input voltage range includes ground
- Differential input voltage range equal to maximum-rated supply voltage: ± 36 V
- Low output saturation voltage
- Output compatible with TTL, MOS, and CMOS
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters

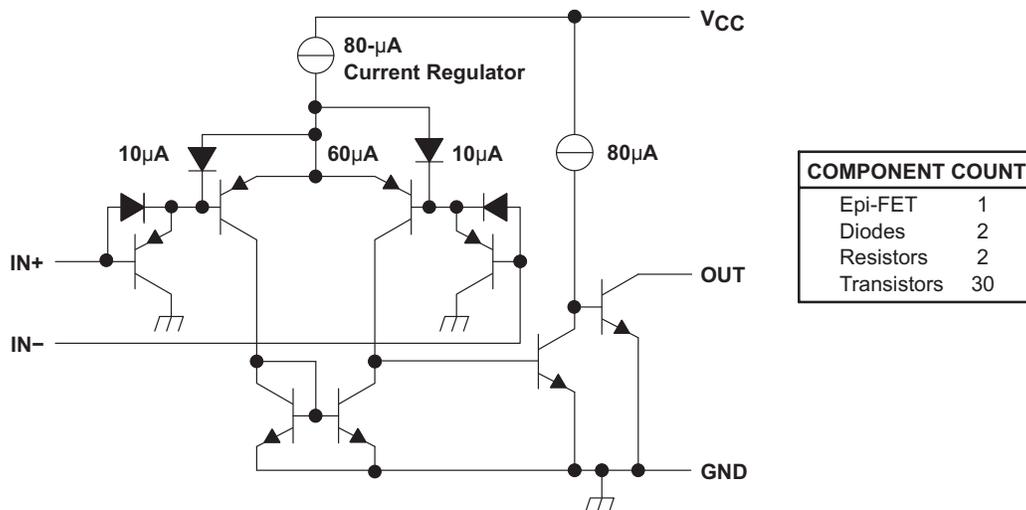


Figure 7. LM2903DGKR Functional Block Diagram

2.3 System Design Theory

The following subsections outline the system design theory associated with this reference design. These methods are used to determine the system-specific component values and may be applicable to other audio detection designs applying the same methods as in this reference design.

2.3.1 System Power Design Theory

2.3.1.1 120-V AC to DC Power Conversion

The primary power source for this design is a 120-V AC wall outlet with a $\pm 10\%$ variation accounted for. To convert this voltage into a suitable DC source for the remainder of the circuitry, the UCC28881DR offline converter is used in conjunction with high-voltage rated rectification diodes as shown in [Figure 8](#):

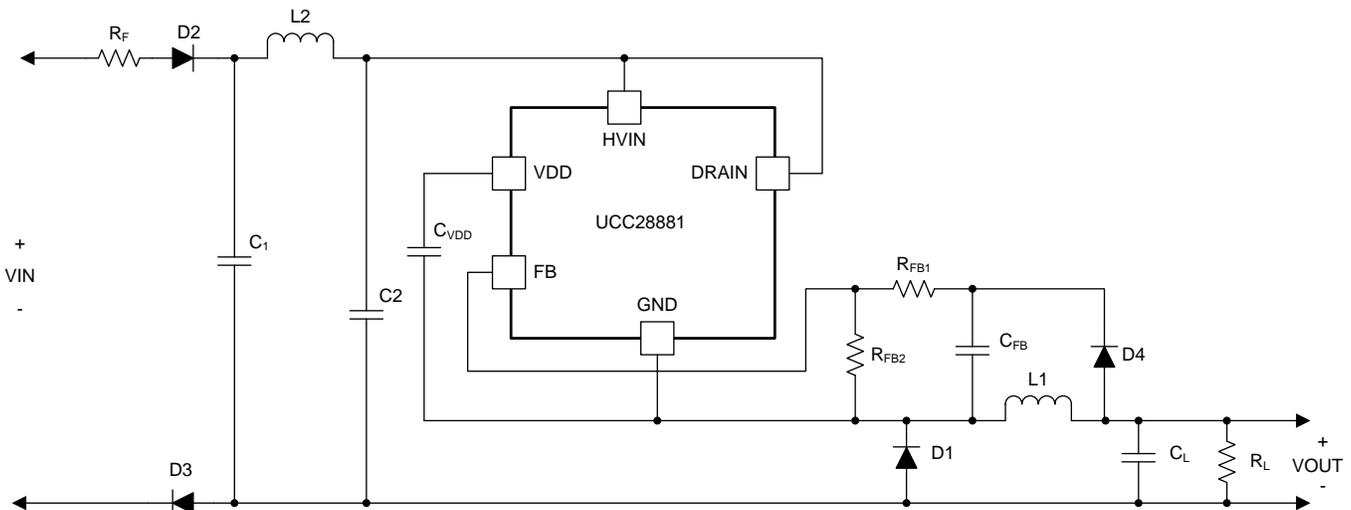


Figure 8. 120-V AC to DC Conversion Circuit, 3.9-V and 100-mA Output

2.3.1.1.1 Design Requirements

[Table 2](#) shows the requirements for this fire and carbon monoxide alarm detector reference design regarding the 120-V AC to DC conversion. These requirements are used for calculating the discrete component values needed for the main power supply subsystem circuit shown in [Figure 8](#).

Table 2. 120-V AC to DC Circuit Design Specifications

DESCRIPTION	MIN	TYP	MAX	UNIT
DESIGN INPUT				
V_{IN} AC input voltage	115	120	135	V_{RMS}
f_{LINE} Line frequency	57	60	63	Hz
I_{OUT} Output current	—	100	200	mA
DESIGN REQUIREMENTS				
V_{OUT} Output voltage	3.7	3.9	4.1	V
ΔV_{OUT} Output voltage ripple	—	—	350	mV
η Converter full-load efficiency	70%	—	—	—

2.3.1.1.2 Component Value Calculations

The following sections outline the methods and calculations used to derive the required value for the discrete components shown in [Figure 8](#).

2.3.1.1.2.1 Input Stage (R_F , $D2$, $D3$, $C1$, $C2$, $L2$)

- Resistor R_F is a flame-proof fusible resistor. R_F limits the inrush current, and also provide protection in case any component failure causes a short circuit. Value for its resistance is generally selected between 4.7 to 15 Ω .
- A half-wave rectifier is chosen and implemented by diode $D2$ (CGRM4007). It is a general purpose 1-A, 600-V rated diode. Diode $D3$ is added for improved common-mode-conducted EMI noise performance. $D3$ can be removed and replaced by a short if not needed.
- EMI filtering is implemented by using a single differential-stage filter ($C1$ - $L2$ - $C2$).

Capacitors $C1$ and $C2$ in the EMI filter also acts as storage capacitors for the high-voltage input DC voltage (V_{IN}). The required input capacitor size can be calculated according [Equation 1](#).

$$C_{BULK(min)} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \left[\frac{1}{RCT} - \frac{1}{2 \times \pi} \times \arccos \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{2 \times V_{IN(min)}^2 - V_{BULK(min)}^2}$$

where:

- $C_{BULK(min)}$ is minimum value for the total input capacitor value ($C1 + C2$ in the schematic of [Figure 8](#)).
 - $RCT = 1$ in case of half wave rectifier and $RCT = 2$ in case of full-wave rectifier .
 - P_{IN} is the converter input power.
 - $V_{IN(min)}$ is the minimum RMS value of the AC input voltage.
 - $V_{BULK(min)}$ is the minimum allowed voltage value across bulk capacitor during converter operation.
 - $f_{LINE(min)}$ is the minimum line frequency when the line voltage is $V_{IN(min)}$.
- (1)

The converter maximum output power can be calculated as follows:

$$P_{OUT} = I_{OUT} \times V_{OUT} = 0.1 \text{ A} \times 3.9 \text{ V} = 390 \text{ mW}$$

Assuming the efficiency $\eta = 68\%$ the input power is $P_{IN} = P_{OUT}/\eta = 574 \text{ mW}$. Use the following values for the other parameters:

- $V_{BULK(min)} = 200 \text{ V}$
- $V_{IN(min)} = 115 V_{RMS}$ (from design specification table)
- $f_{LINE(min)} = 57 \text{ Hz}$

$C_{BULK(min)} = 1.48 \mu\text{F}$. Considering that electrolytic capacitors, generally used as bulk capacitor, have 20% of tolerance in value, the minimum nominal value required for C_{BULK} is:

$$C_{BULKn(min)} > \frac{C_{BULK}}{1 - \text{TOL}_{CBULK}} = 1.85 \mu$$
(2)

Select $C1$ and $C2$ to be 1 μF each ($C_{BULK} = 1 \mu\text{F} + 1 \mu\text{F} = 2 \mu\text{F} > C_{BULKn(min)}$).

2.3.1.1.2.2 Regulator Capacitor (C_{VDD})

Capacitor C_{VDD} acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF, 10-V rated ceramic capacitor is enough for proper operation of the device's internal LDO.

2.3.1.1.2.3 Freewheeling Diode (D1)

The freewheeling diode has to be rated for high-voltage with as short as possible reverse-recovery time (t_{rr}).

The maximum reverse voltage that the diode should experience in the application, during normal operation, is given by [Equation 3](#).

$$V_{D1(max)} = \sqrt{2} \times V_{IN(max)} = \sqrt{2} \times 135 \text{ V} = 191 \quad (3)$$

A margin of 20% is generally considered.

The use of a fast recovery diode is required for the buck-freewheeling rectifier. When designed in CCM, the diode reverse recovery time should be less than 35 ns to keep low reverse recovery current and the switching loss. For example, STTH1R06A provides 25-ns reverse recovery time. When designed in DCM, slower diode can be used, but the reverse recovery time should be kept less than 75 ns. UF4004TA can fit the requirement.

2.3.1.1.2.4 Output Capacitor (C_L)

The value of the output capacitor impacts the output ripple. Depending on the combination of capacitor value and equivalent series resistor (R_{ESR}). A larger capacitor value also has an impact on the start-up time. For a typical application, the capacitor value can start from 47 μF to hundreds of μF . A guide for sizing the capacitor value can be calculated by the following equations:

$$C_L > 20 \times \frac{I_{LIMIT} - I_{OUT}}{f_{SW(max)} \times \Delta V_{OUT}} = 20 \times \frac{20 \text{ mA} - 100 \text{ mA}}{62 \text{ kHz} \times 350 \text{ mV}} = 92.1 \mu\text{F} \quad (4)$$

$$R_{ESR} < \frac{\Delta V_{OUT}}{I_{LIMIT}} = 1.75 \Omega \quad (5)$$

Take into account that both C_L and R_{ESR} contribute to output voltage ripple. A first pass capacitance value can be selected and the contribution of C_L and R_{ESR} to the output voltage ripple can be evaluated. If the total ripple is too high the capacitance value has to increase or R_{ESR} value must be reduced. In this application, C_L is selected (100 μF) and it has an R_{ESR} of 0.36 Ω . So the R_{ESR} contributes for 4% of the total ripple. The formula that calculates C_L is based on the assumption that the converter operates in burst of twenty switching cycles. The number of bursts per cycle could be different, the formula for C_L is a first approximation.

2.3.1.1.2.5 Pre-Load Resistor (R_L)

The pre-load resistor connected at the output is required for the high-side buck topology. In low-side buck topology, the output voltage is directly sensed; however, in high-side buck topology, the output is sampled and estimated. At no-load condition, because the feedback loop runs with its own time constant, the buck converter operates with a fixed minimum switching frequency. Select the pre-load resistor or using a Zener diode to prevent output voltage goes too high at no-load condition.

A simple Zener diode is a good choice without going through the calculation. Besides the simplifying the calculation, Zener diode does not consumes power at heavy load condition, which helps to improve the converter heavy-load efficiency.

A simple resistor can also be used to limit the output voltage at no-load condition. However, this resistor connects to the output all the time and it reduces the full-load efficiency. The pre-load resistor can be calculated based on [Equation 6](#) or based on experiments. In [Equation 6](#), the V_{MAX} is allowed maximum output voltage, and V_{REG} is the regulated output voltage.

$$R_L = \frac{4 \times V_{MAX}^2 \times (V_{MAX} - V_{REG})}{V_{MAX} + V_{REG}} \times \frac{C_{FB} \times (R_{FB1} + R_{FB2})}{L_1 \times I_{LIMIT}^2} \quad (6)$$

2.3.1.1.2.6 Inductor (L1)

In the initial calculations, half of the peak-to-peak ripple current at full load is:

$$\Delta I_L = 2 \times (I_{LIMIT} - I_{OUT}) \quad (7)$$

When operating in DCM, the peak-to-peak current ripple is the peak current of the device.

Average MOSFET conduction minimum duty cycle at continuous conduction mode is:

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} \quad (8)$$

If the converter operates in discontinuous conduction mode:

$$D_{MIN} = 2 \times \frac{I_{OUT}}{I_{LIMIT}} \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} \quad (9)$$

Maximum allowed switching frequency at $V_{IN(max)}$ and full load:

$$f_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}} \quad (10)$$

Switching frequency has a maximum value limit of $f_{SW(max)}$.

The worst case $I_{LIMIT} = 200$ mA, but assuming $\Delta I_L = 100$ mA.

The converter works in continuous conduction mode ($\Delta I_L < I_{LIMIT}$) so based on $V_{OUT} = 3.9$ V, $V_d = 1$ V, and $V_{IN(max)} = 191$ V.

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} = 3.66\% \quad (11)$$

The maximum allowed switching frequency is 62 kHz because the calculated value exceeds it.

$$f_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}} = 81 \text{ kHz} > f_{SW(max)} = 62 \text{ kHz} \quad (12)$$

The duty cycle does not force the MOSFET on time to go below t_{ON_TO} . If $D_{MIN}/T_{ON_TO} < f_{SW(max)}$, the switching frequency is reduced by current runaway protection and the maximum average switching frequency is lower than $f_{SW(max)}$, the converter cannot support full load.

The minimum inductance value satisfies both the following conditions:

$$L > \frac{V_{OUT} + V_d}{f_{SW_VIN(max)} \times \Delta I_L} = 680 \mu\text{H} \quad (13)$$

$$L > \frac{V_{IN(max)}}{I_{LIMIT}} \times t_{ON_TO} = \frac{191 \text{ V}}{200 \text{ mA}} \times 450 \text{ ns} \cong 430 \mu\text{H} \quad (14)$$

In the application example, 680 μH is selected as the minimum standard value that satisfy [Equation 13](#) and [Equation 14](#). [Figure 9](#) shows the AC to DC conversion circuit used for this reference design, along with the efficiency curve and power dissipation for a voltage range satisfying the input voltage range of the design.

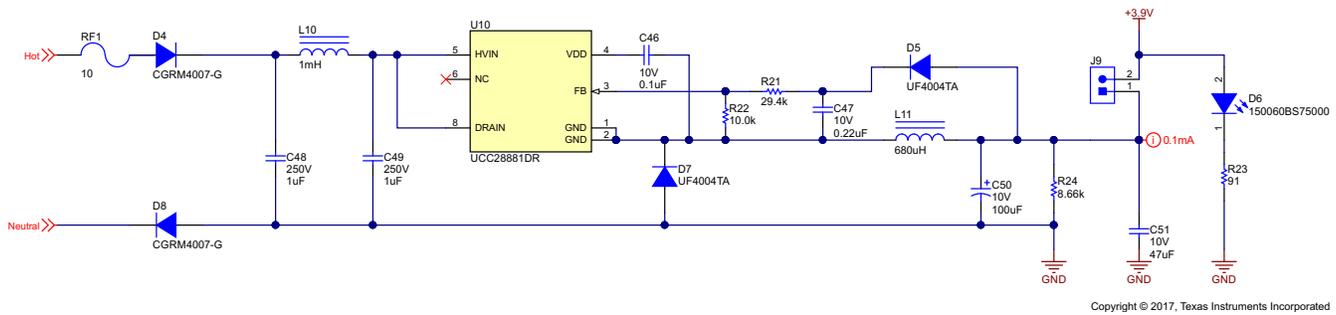


Figure 9. TIDA-01519 120-V AC to DC Schematic

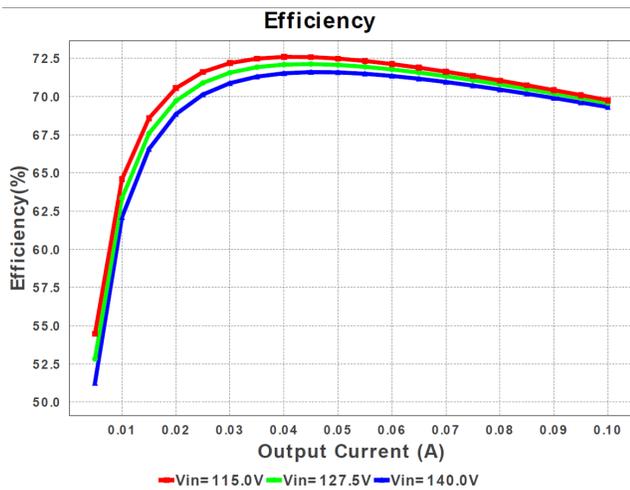


Figure 10. TIDA-01519 Efficiency Plot

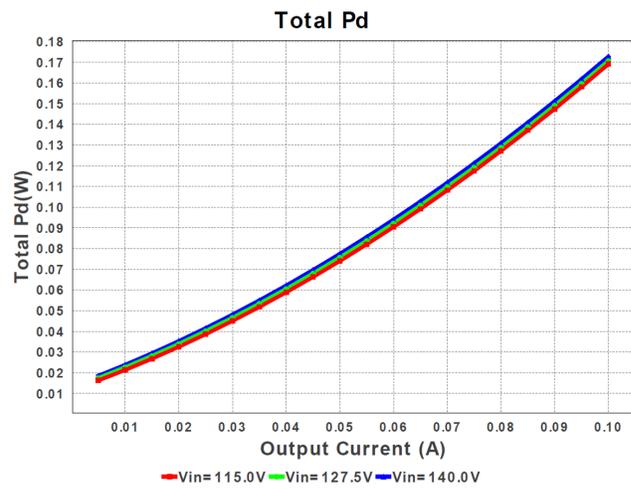
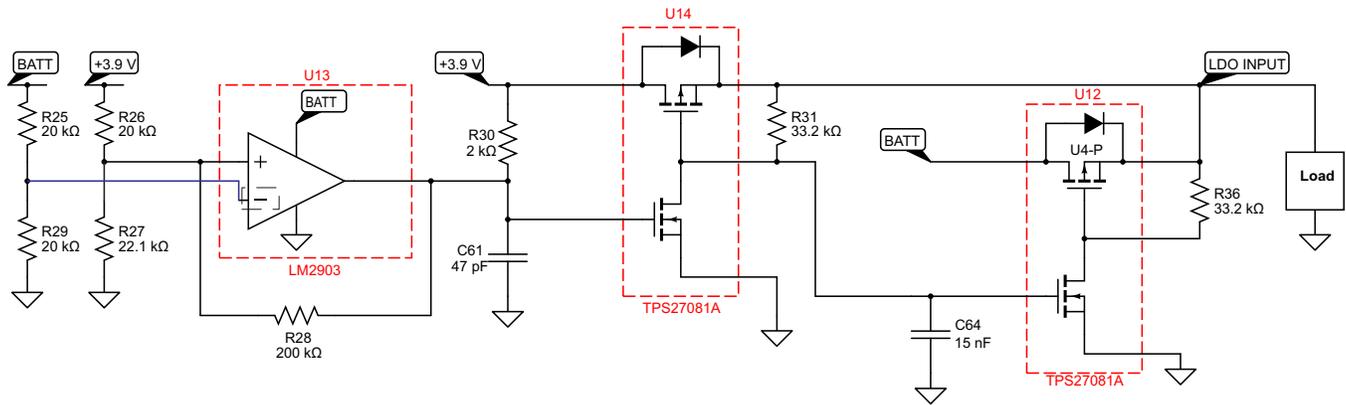


Figure 11. TIDA-01519 Total Power Dissipation Plot

2.3.1.2 Dual Power Source ORing

This reference design has two means of power designed into the board including 120-V AC wall power as well as battery backup in the event of a power outage. To accommodate both power paths, the power source ORing is used to select the preferred sourcing route. A simple diode-based ORing scheme is not suitable for this application due to the significant voltage drop across the diode. If one AA Li-Ion battery is used, assuming a nominal full voltage value of 3.7 V, the diode drop over the ORing network reduces the voltage below the minimum working value for the system. This reference design uses two integrated N-FET/P-FET pairs and a basic differential comparator to accomplish the power multiplexing capabilities at a significantly lower cost than an integrated solution. The ORing circuitry used in this reference design is shown in Figure 12.



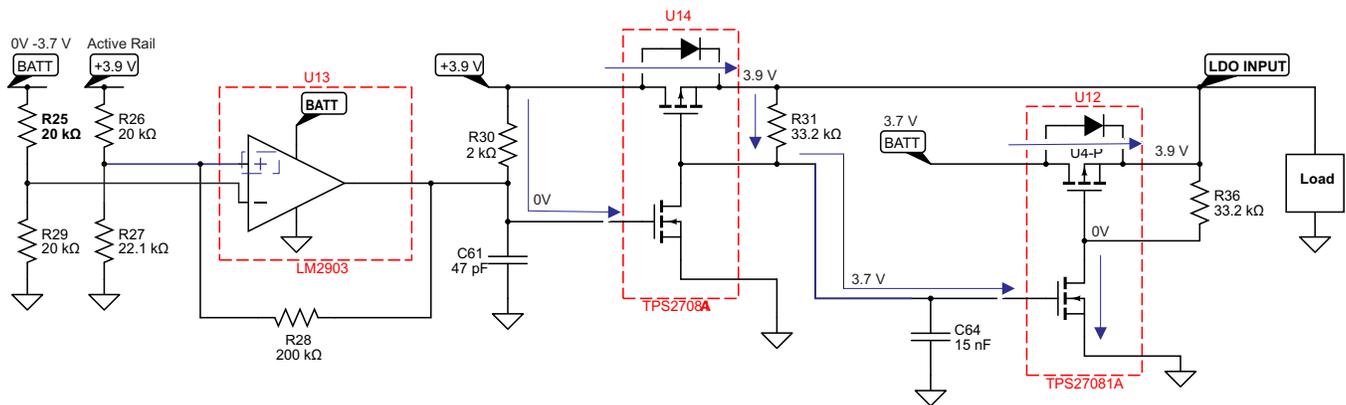
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Figure 12. TIDA-01519 ORing Circuit

2.3.1.2.1 120-V AC Used as Primary Power Supply

The 120-V AC power, and consequently the UCC28881 3.9-V rail, is considered the main power source for this system and must be prioritized above battery backup power. The ORing solution in this reference design is designed to prioritize one source over another—in this case, the UCC28881 output over battery backup.

Figure 13 provides a visual overview of the functionality when the UCC28881 output is providing power. The gate of the U3-N is pulled up through R30 to 3.9 V, thereby turning U14-N on and forcing the drain of the U14-N to GND. The drain of the U14-N is shorted to the gate of the U12-N. As a result, anytime U14-N is on, U12-N is off. U14-P is then turned on due to its gate being pulled to GND, and U12-P is turned off due to its gate being pulled up through R9. 3.9 V is then passed to the load.



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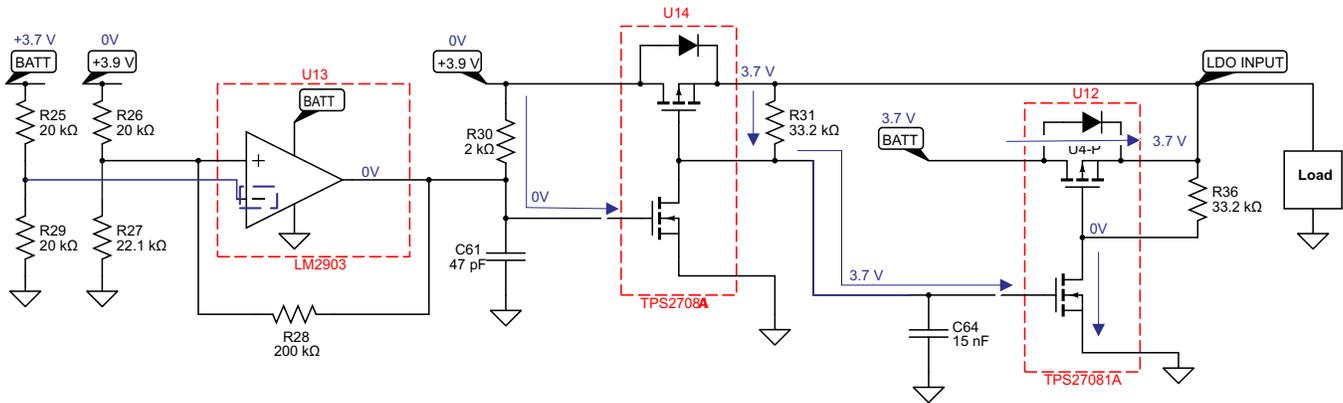
Figure 13. ORing: UCC28881 Primary Power Circuit Logic

The surrounding resistor values of the comparator are chosen to ensure the non-inverting terminal will be higher than the inverting terminal if the UCC28881 output rail is supplying power to the LDO, resulting in the comparator's output being Hi-Z and thus having virtually no effect on the circuit. This setup allows the UCC28881 output rail to dominate the ORing circuit over battery power if the batteries are inserted in when the UCC28881 output is already supplying power.

2.3.1.2.2 Battery Backup Used as Primary Power Supply

Figure 14 provides the visual overview of the ORing process when the battery is present and the 120-V AC power line is absent. In this scenario, the comparator is most needed.

When the UCC28881 output rail, Net "+3.9V", is absent and "BATT" is 2.6 to 3.7 V, the inverting input to the comparator becomes greater than the non-inverting input and the comparator drives the output terminal low, thereby turning off U14-N. With U14-N turned off, "BATT" drives the gate of U12-N and the gate of U14-P high, turning off U14-P and turning on U12-N. U12-P turns on as a result, and the battery voltage is passed to the load.



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Figure 14. ORing: Battery Primary Power Circuit Logic

2.3.1.2.3 ORing Circuit Component Calculations

The primary function of the comparator is to provide the system an active method to drive the U14 FETs off. When both sources are available, the comparator ensures that the U14 FETs does not latch should the 3.9-V UCC28881 output rail become unexpectedly unavailable (that is, 120-V AC power is unplugged). The comparator also prevents a voltage spike due to the drain-to-source capacitance from latching the U14 FETs on when USB is initially plugged in. Hysteretics is used on the comparator to ensure the device does not oscillate about the threshold voltage and ensures the U14 FETs are turned fully off when switching to USB power.

The resistors chosen must ensure that when the 3.9-V UCC28881 output rail is present, the BATT voltage required to drive the comparator low exceeds the maximum possible battery voltage use case. The BATT input voltage required to drive the comparator low must be larger than 3.7 V to ensure the condition never becomes true during operation. When the comparator output is High-Z, Rx is virtually in parallel with Rx thus raising the non-inverting terminal of comparator, requiring a higher battery voltage to drive the comparator's output low. The equivalent resistance of Rx in parallel with Rx is:

$$R_{eqH} = \frac{20 \text{ k}\Omega \times 200 \text{ k}\Omega}{20 \text{ k}\Omega + 200 \text{ k}\Omega} = 18.18 \text{ k}\Omega \quad (15)$$

Given the UCC28881 output rail is 3.9 V, the non-inverting input is calculated with a basic voltage divider:

$$IN (+)_{UCC} = +3.9 \text{ V} \times \left(\frac{R_{27}}{R_{27} + R_{eqH}} \right) = 3.9 \times \left(\frac{22.1 \text{ k}\Omega}{22.1 \text{ k}\Omega + 18.18 \text{ k}\Omega} \right) = 2.14 \text{ V} \quad (16)$$

Therefore, the inverting terminal must exceed 2.14 V. Because R25 and R29 are of equal resistance, 20 kΩ, the required BATT voltage output to drive the comparator low is twice the required inverting terminal.

$$IN (+)_{BATT} = 2 \times IN (+)_{UCC} = 2 \times 2.14 \text{ V} = 5.28 \quad (17)$$

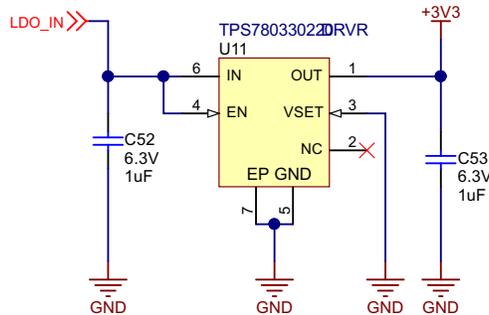
Because 5.28 V is higher than the maximum battery output voltage, the comparator cannot be driven low by a battery insertion if the UCC28881 3.9-V rail is already supplying power. To account for the opposite scenario, a battery is initially present and the UCC28881 3.9-V rail is subsequently provided, the same threshold calculations must be performed for when the comparator's output was initially low. This scenario is unlikely to occur in the specific end products this reference design targets; however, such a scenario is planned for regardless. When the battery is present with the 3.9-V UCC28881 output rail absent, the comparator output is low. Therefore, R28 is virtually in parallel with R27 providing an equivalent resistance:

$$R_{eqL} = \frac{22.1\text{ k}\Omega \times 200\text{ k}\Omega}{22.1\text{ k}\Omega + 200\text{ k}\Omega} = 19.9\text{ k}\Omega \quad (18)$$

Given BATT is at nominal 3.7 V, and thus the inverting terminal is 1.85 V through the voltage divider of R25 and R29, the required UCC28881 output voltage needed to produce a non-inverting terminal voltage greater than 1.85 V is calculated in as:

$$UCC_{Min_Out} = IN(-) \times \left(\frac{R_{eqL} + R_{29}}{R_{eqL}} \right) = 1.85\text{ V} \times \left(\frac{19.9\text{ k}\Omega + 20\text{ k}\Omega}{19.9\text{ k}\Omega} \right) = 3.71 \quad (19)$$

2.3.1.3 3.3-V Power Rail



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Figure 15. TPS780330220 Schematic

The 3.9-V UCC28881 output rail is the main supply for all major components of this reference design. The TPS780330220 is used as a simple LDO from the ORing circuitry to the remainder of the system. The TPS780330220 offers both low component cost as well as high efficiency. 1-µF capacitors are used at both the input and the output of the LDO to reduce any transient spikes seen in the ORing stage of the power supply. Figure 16 shows the efficiency curves for the TPS780330220 at three different expected input voltages to the device.

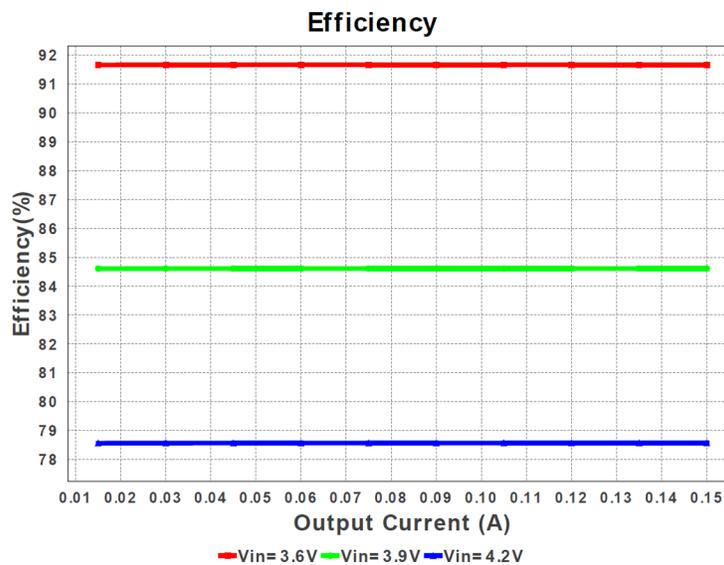


Figure 16. TPS780330220 Efficiency Curve Plot

2.3.2 Audio Gain and Filtering Stage Design Theory

The following subsections detail the design theory used to develop the audio signal chain used in this reference design.

2.3.2.1 Microphone Output Response Characterization

In this design, an InvenSense ICS-40300 MEMS microphone is used for audio analysis input from the surroundings. This particular microphone is chosen based on a balance between dynamic performance and cost. This microphone has a dynamic range from 6 Hz to > 20 kHz with a linear response up to 130 dB. To integrate the ICS-40300 microphone into the design, the analog output voltage needs to be characterized based on the input dB level.

To accomplish this, the output voltage level information can simply be extracted from the ICS-40300 datasheet and further analyzed. Referencing the UL217 regulations regarding the specified dB level versus distance, the alarm must have an 85-dB sound pressure level (SPL) at 10 ft. Using the inverse square law, the dB level at the closest distance from the alarm (1 ft selected arbitrarily) is calculated as:

$$\frac{l_2}{l_1} = \left[\frac{d_1}{d_2} \right]^2 = 105 \text{ d} \quad (20)$$

Using [Figure 18](#), which is a dB-to-volt output curve with polynomial curve fitting based on the ICS-40300 datasheet information, the voltage output range for the microphone is estimated to be roughly between 4 and 20 mV. This is extracted by using the MATLAB script shown in [Figure 19](#), which uses the poly-fit equation to calculate the output voltage for a given input dB SPL value. This data is also used below to calculate the required signal gain of the system.

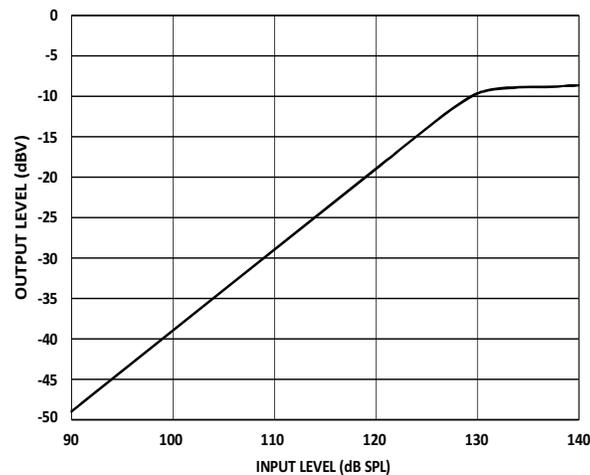


Figure 17. ICS-40300 dBV Output Curve

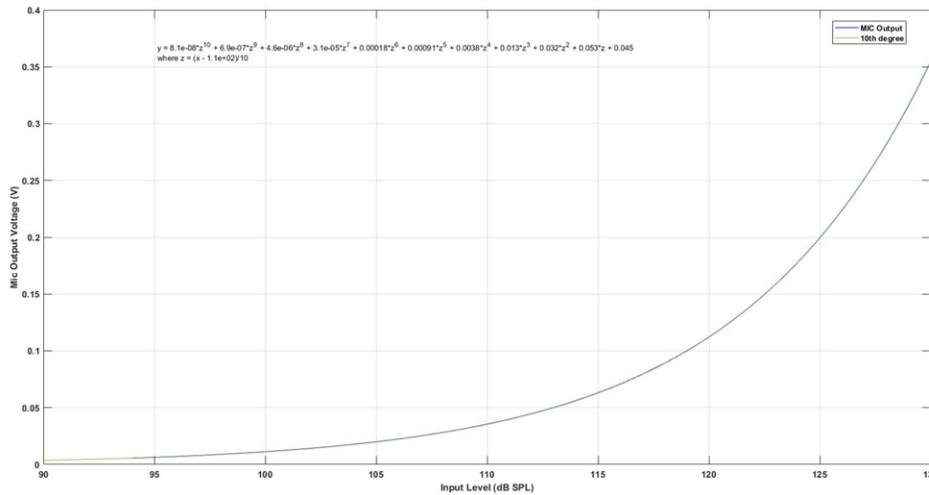


Figure 18. Microphone Voltage Output Using 10th Degree Poly-Fit Prediction Curve

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%--Define Extracted Polyfit Equation Variable
X = 85; %--- Target SPL Value
mu = 112;
sigma = 10.393;
z = (x-mu)/sigma;

%--Define Polyfit Coefficients:
p1 = 8.1244e-08;
p2 = 6.85e-07;
p3 = 4.6302e-06;
p4 = 3.0924e-05;
p5 = 0.00018207;
p6 = 0.00091308;
p7 = 0.0038146;
p8 = 0.012752;
p9 = 0.031974;
p10 = 0.053446;
p11 = 0.044668;

%--USE POLYFIT EQUATION TO PREDICT OUTPUT AT 85dB
y = p1*z^10 + p2*z^9 + p3*z^8 + p4*z^7 + p5*z^6 + p6*z^5 + ...
    p7*z^4 + p8*z^3 + p9*z^2 + p10*z + p11;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    
```

Figure 19. Poly-Fit Equation MATLAB Script

2.3.2.2 Audio Amplification Stage Design

Amplification of the signal is done based on the input requirements of the CC1310 ADC. For this design, input voltage scaling is disabled, so the input voltage to the CC1310 ADC must be below 1.5 V at all times. A safety factor is added to this limit, making the peak ADC input voltage ≤ 1.3 V. More information on the ADC parameters and settings can be found in the [CC1310 datasheet](#).

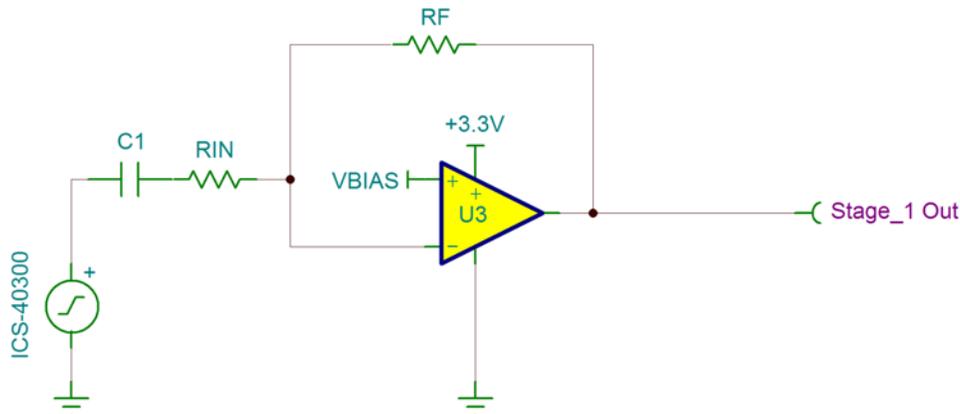


Figure 20. TIDA-01519 Circuit Structure of Audio Amplification

For this design, the amplification stage uses the TLV2313 general purpose op amp. This part is chosen due to its gain bandwidth product as well as low cost. Using the mid-range value of the microphone response output voltage (4 mV_{RMS}), calculate the peak-to-peak output voltage as:

$$V_{p-p} = (\sqrt{2} \times 4\text{mV}) \times 2 = 11.3 \text{ mV}_{p-p} \quad (21)$$

For a maximum amplifier output of 1.3 V_{p-p}, the required gain is calculated as:

$$G = \left[\frac{V_{\text{OUT}}}{V_{\text{IN}}} \right] = \frac{1.3 \text{ V}}{11.3 \text{ mV}} = 114.9 \frac{\text{V}}{\text{V}} \quad (22)$$

For the R_{IN} resistor value selection, note the need for DC offset removal from the microphone output in addition to signal amplification; In this particular case, the DC offset is approximately 0.7 V. A value of 2 kΩ is chosen as a known starting value for R_{IN}, allowing the remainder of the discrete component values to be calculated, while also providing a basis for the gain stage's R_F value derivation. To solve for the AC-coupling capacitor value required to implement the desired active input filter (C1), Equation 23 is used.

$$20 \text{ Hz} = \frac{1}{2\pi \times 2 \text{ k}\Omega \times C_1} \quad (23)$$

Re-arranging to solve for the value of C1 yields:

$$C_1 = \frac{1}{2\pi \times 2 \text{ k}\Omega \times 20 \text{ Hz}} = 4\mu \quad (24)$$

Solving the inverting op amp gain equation, the feedback resistance R_F value required for the target gain is:

$$R_F = R_1 \times 114.9 \frac{\text{V}}{\text{V}} = 229.8 \text{ k}\Omega \quad (25)$$

Using the same method shown above, the gain and R_F values for 1-ft and 10-ft proximity are also calculated and shown in Table 3. This gives the user the flexibility to vary the gain settings based on the proximity to the alarm. The resistance values used in this reference design are rounded up or down to the nearest typically available resistance value.

Table 3. R_F Values Used Based on Proximity to Alarm

PROXIMITY (ft)	MIC INPUT SPL (dB)	MIC RMS VOLTAGE RESPONSE (mV)	V _{p-p} (mV)	GAIN REQUIRED (V/V)	R _F VALUE SELECTED
10	85.00	2.1	2.97	437.00	432.0k
5	91.02	4.0	5.60	232.00	226.0k
1	105.00	20.0	28.30	4.59	45.3k

For the non-inverting input to the TLV2313, a 0.65-V reference voltage is applied to shift the output within the required bounds, half the output range of the gain stage. Simulating this active filtering gain stage circuit in TINA-TI yields the following output. This verifies the correct output range of the gain stage into the CC1310's 12-bit ADC.

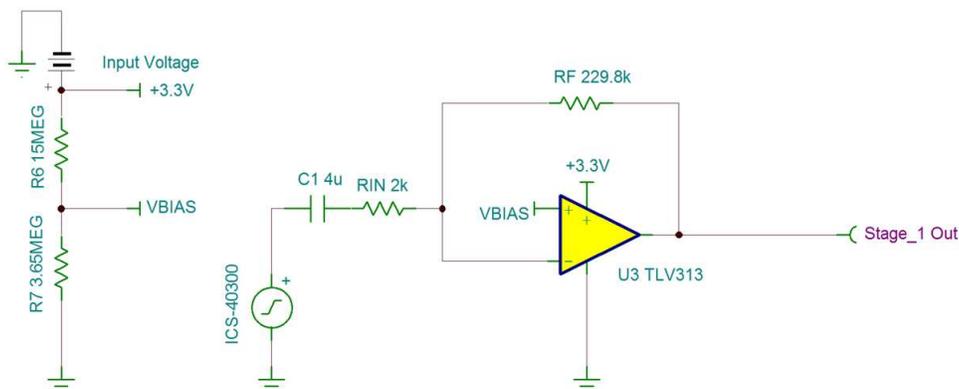


Figure 21. Active Filter and Gain Stage TINA-TI Simulation Schematic

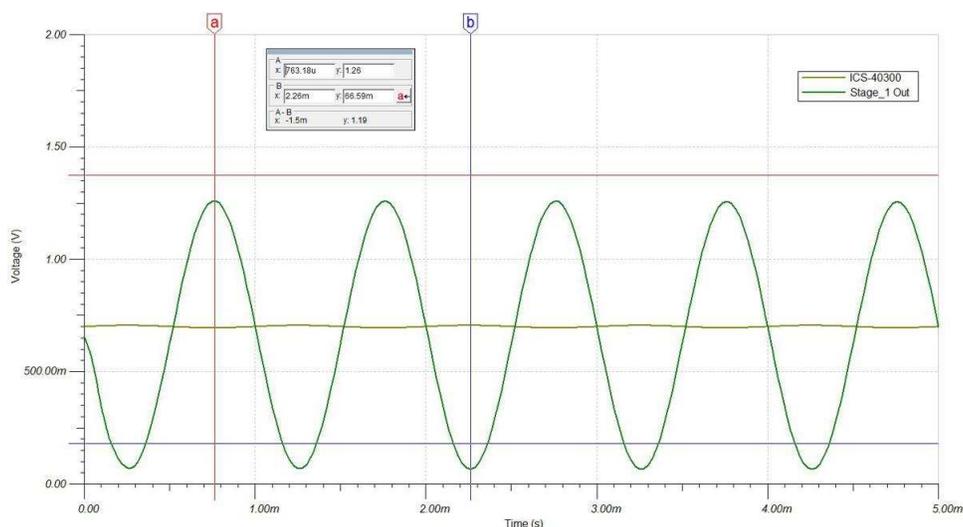


Figure 22. Active Filter and Gain Stage TINA-TI Simulation Results

2.3.2.3 Antialiasing Filter Design

This reference design uses an antialiasing filter in series with the initial gain stage of the signal chain to filter out higher frequencies not needed for analysis. The cutoff frequency for this filter is conservatively chosen at 8.5 kHz to ensure there is no signal attenuation for the 3-kHz alarm frequency response. An important design requirement for this antialiasing filter is staying within the 1-MHz gain bandwidth range of the TLV2313 op amp. The filter is chosen to have unity-gain and a single-stage second-order response to reduce the required design board space.

For the filter type and topology, a Butterworth filter is chosen with a Sallen-Key topology. Figure 23 shows the Sallen-Key topology used in this anti-aliasing filter design. Butterworth filters are termed maximally-flat-magnitude-response filters, optimized for gain flatness in the pass-band. The attenuation is -3 dB at the cutoff frequency. Above the cutoff frequency, the attenuation is -20 dB/decade/order. The Butterworth is considered by many to offer the best all-around filter response. The Sallen-Key topology selection is based on its inherent gain accuracy; this is because its gain is not dependent on component values. This topology is also not sensitive to component variation at unity gain.

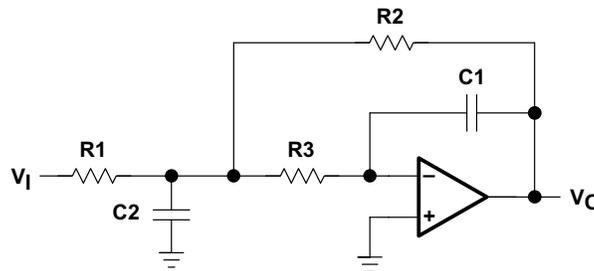


Figure 23. Second-Order Unity Gain Sallen-Key Low-Pass Filter Topology

The typical transfer function for a second-order low-pass filter is expressed as a function of frequency (f) as shown in Equation 26. For the antialiasing filter of this reference design, this is considered the standard form.

$$H_{LP}(f) = - \frac{K}{\left(\frac{f}{FSF \times f_c}\right)^2 + \frac{1}{Q} \frac{jf}{FSF \times f_c} + 1} \quad (26)$$

Referencing the coefficients from a filter-table listing for the Butterworth, the Q factor value is 0.707 and the FSF is 1, which can be substituted into Equation 26. To calculate the discrete component values needed for the Sallen-Key implementation of the derived transfer function, the ideal Sallen-Key transfer function Equation 27 must be modified to fit the standard form shown in Equation 26.

$$H(f) = \frac{R3 + R4}{R3} \frac{1}{(j2\pi f)^2 (R1R2C1C2) + j2\pi f \left(R1C1 + R2C1 + R1C2 \left(\frac{-R4}{R3} \right) \right) + 1} \quad (27)$$

To solve for the components in the standard transfer function form, let

$$K = \frac{R3 + R4}{R3} \quad (28)$$

$$FSF \times f_c = \frac{1}{2\pi \sqrt{R1R2C1C2}} \quad (29)$$

$$Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2 (1 - K)} \quad (30)$$

Using 8.5 kHz as the corner frequency of the filter and the previously mentioned equations, and assuming the relationship $R1 = \alpha R$, $R2 = R$, $C1 = C$, and $C2 = \beta C$, the values are calculated and shown in Table 4.

Table 4. Antialiasing Filter Calculated Discrete Component Values

COMPONENT DESIGNATOR	CALCULATED COMPONENT VALUE
α	0.649
β	2195.12
C1	8.2 nF
C2	18 μ F
R1	1.13 k Ω
R2	1.74 k Ω

Integrating these calculated component values into the antialiasing filter yields the following circuit, which is used in series with the audio amplification stage:

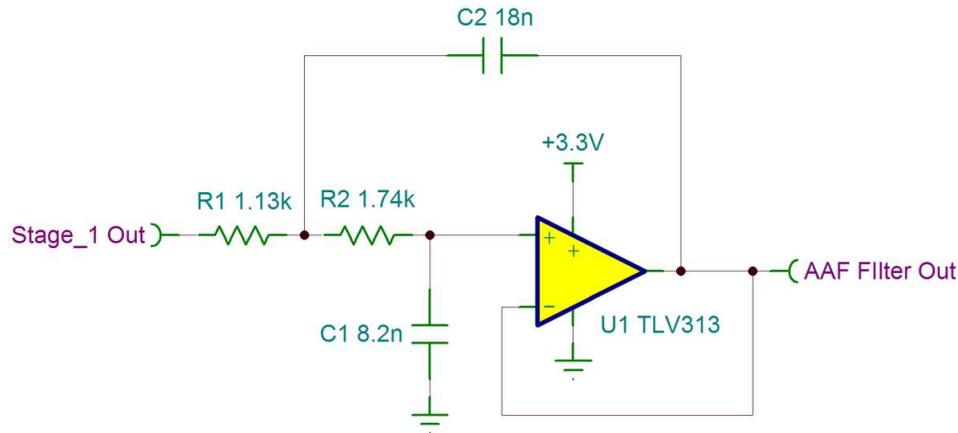


Figure 24. TIDA-01519 Antialiasing Filter Circuit

To verify the circuit functions as expected, the circuit undergoes an AC transfer characteristic simulation in TINA-TI as well as a secondary verification in TI's FilterPro software. Figure 25 shows the frequency response of the filter and Figure 26 shows the group delay of the filter.

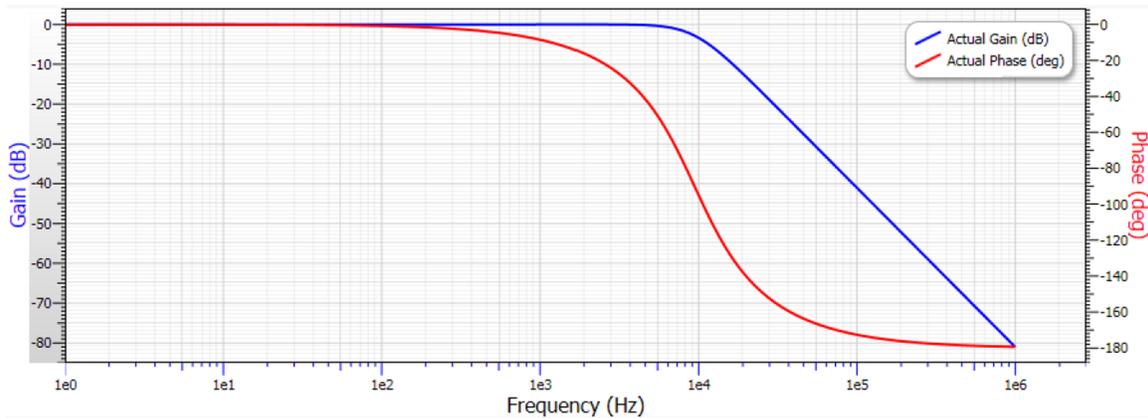


Figure 25. TIDA-01519 Antialiasing Filter Frequency Response Plot

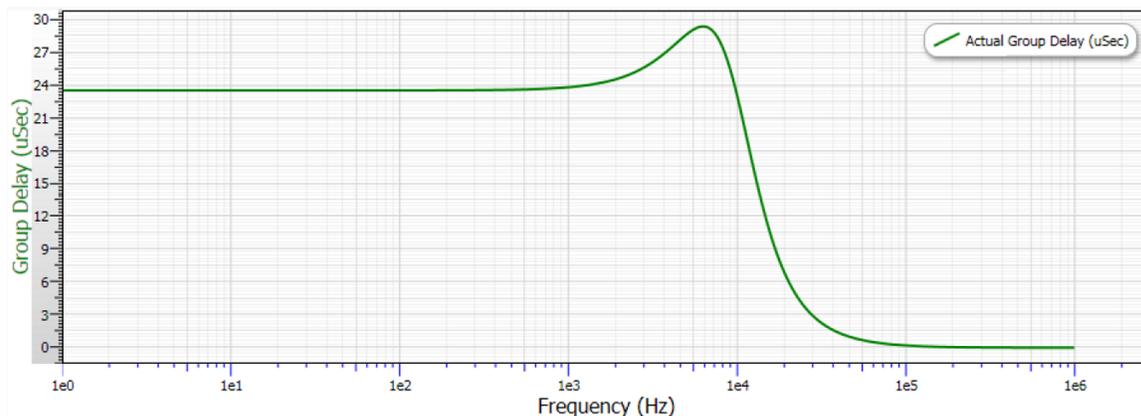


Figure 26. TIDA-01519 Antialiasing Filter Group Delay Plot

2.3.2.4 Complete TIDA-01519 Signal Chain

Figure 27 shows the combination of both previously designed filters connected together to form the complete microphone to CC1310 signal chain. This reference design also uses a final passive LP filter with a 16-kHz corner frequency. This is an added precaution to avoid any random transients that may occur in the preceding stages of the signal chain. After integrating the circuits, a TINA-TI transient analysis is preformed to verify correct amplification and filtering. The ICS-40300 simulation source is set to 1 kHz with a voltage of 11.3 mV_{P-P} and a F_B resistance value of 226k. Figure 27 shows the complete signal chain circuit used in this reference design, and Figure 28 shows the results of the simulation done in TINA-TI.

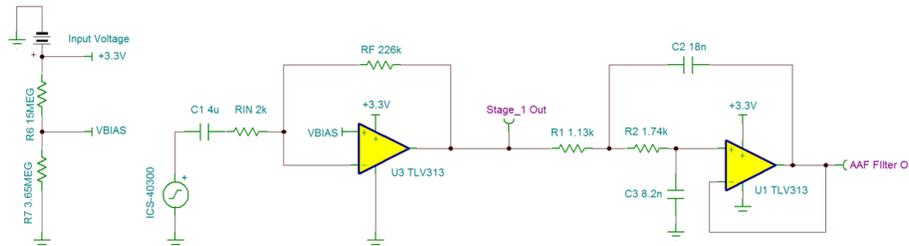


Figure 27. TIDA-01519 Signal Chain Simulation Schematic

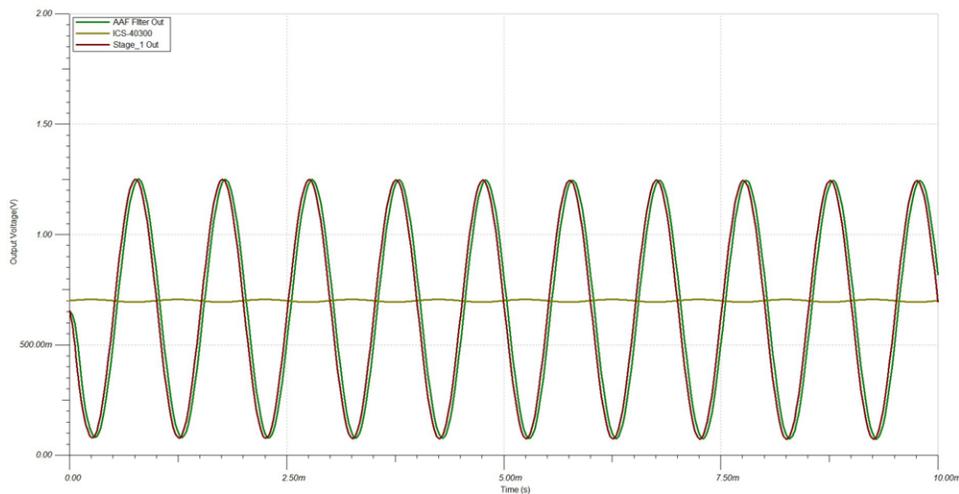


Figure 28. TINA-TI Simulation Output of TIDA-01519 Signal Chain

After running the TINA-TI simulations, the delay caused by the signal chain phase shift is measured to be 35.38 μ s.

2.3.3 Development Theory of Alarm Detection Algorithm

The following subsections show the development and derivation of the required software components used to implement fire and CO alarm detection capabilities with this reference design. This detection algorithm can be modified by the user to detect a variety of audio events and temporal audio patterns.

2.3.3.1 Initial Audio Response Characterization

To accurately analyze incoming microphone data to identify alarm frequencies and temporal patterns associated with these frequencies, the audio input from these events must be obtained and analyzed. The pattern for the alarm and duration for each sound pulse is shown in Equation 31.

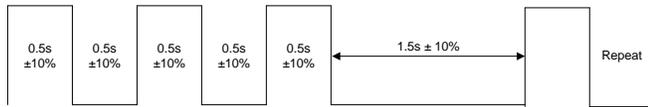


Figure 29. UL217 Temporal Pattern for Fire Alarms

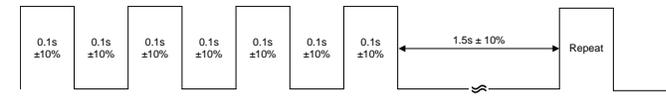


Figure 30. UL217 Temporal Pattern for CO Alarms

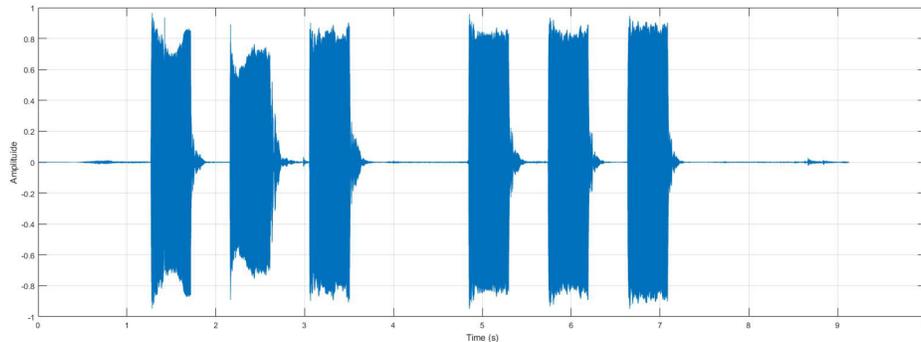


Figure 31. 3-kHz Fire Alarm Captured Audio Sample

Figure 31 shows the audio input receive from a 3-kHz fire alarm at 10 ft away. This pattern and is in keeping with that expected from Equation 31. Because the pattern repeats in this manner for the duration of smoke or CO presence detection, the analysis uses buffered samples with a duration determined by the probability of landing at any single point in the temporal sound pattern. The maximum delay between beeps for either alarm can be calculated from Figure 29 as:

$$D_{\max} = 5 \times (1 + 0.10) = 5.5 \tag{31}$$

By dividing this time by the maximum false alarm iterations before a variable reset occurs, six iterations in the case of this reference design and shown in Figure 40, alarm tones must be identifiable in a majority of the sample periods depending on alarm type. This allows alarms to be detected before the detection variables reset in the case of a CO alarm, where a higher delay time between alarm soundings occur. More information on the detection algorithms can be found in Section 2.3.3.4. It is worth mentioning this worst case scenario to enhance the robustness of the design. The sample period is set slightly longer at 0.95 s for an added detection safety factor. By using this method, there are also no issues with alarm sound reverberation or multiple alarms. Depending on the users processing power, this buffer sample period can be reduced to accurately pick up detailed audio temporal pattern information if desired.

2.3.3.2 Digital Band-Pass Filter Design

The digital band-pass filtering is used in this reference design to provide a significant attenuation of frequencies outside of the desired spectrum, namely 520 Hz and 3 kHz. One advantage of digital filtering is the superior results one can obtain from its use. The same results require many additional filtering stages if done by means of discrete components and in some cases may be impossible to replicate with analog components. MATLAB is used to generate the required filter and its respective parameters. Figure 33 shows the filter design interface used to create the necessary digital filter for the detection algorithm. The parameters used are specific to this design, but the user can modify the parameters for detecting various other audio events.

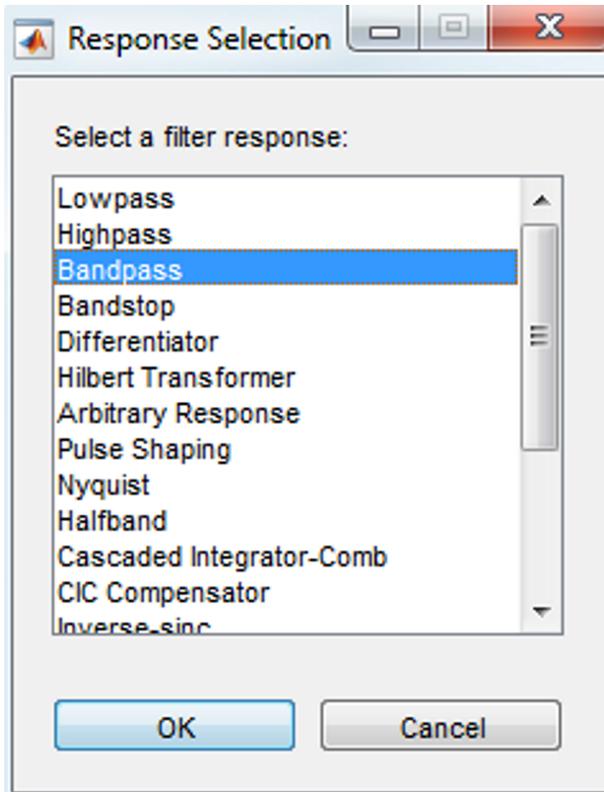


Figure 32. Selection Window for MATLAB Filter Designer

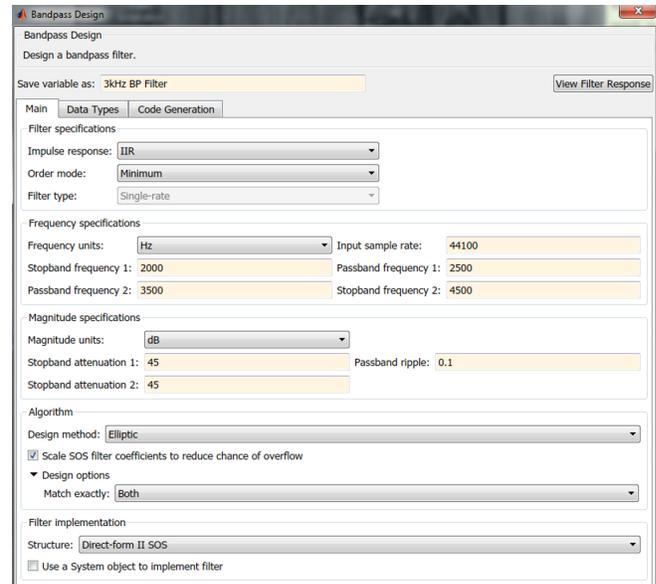


Figure 33. Main Graphical Interface of MATLAB Filter Design

Figure 34 shows the response of this digital filter design for the 3-kHz range band pass. The secondary stopband is extended outward to account for the variations in alarm frequency from the target center frequency of 3 kHz. This allows the system to capture audio data of slightly higher frequency alarms without attenuation due to a very narrow band-pass frequency spectrum in the digital filter.

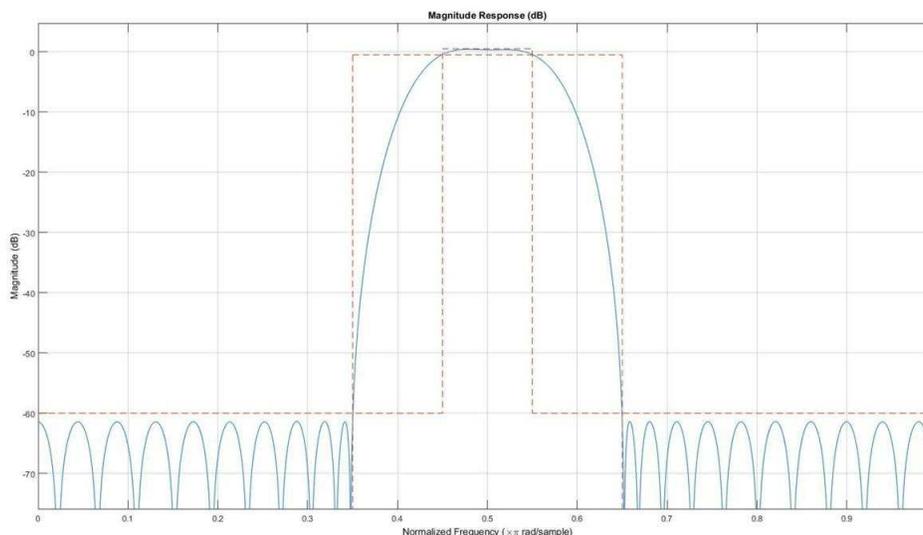


Figure 34. Magnitude Response of 3-kHz Digital Band-Pass Filter

The same digital filter design process is followed for the 520-Hz low tone alarm. Figure 35 and Figure 36 shows the filter design parameters and filter magnitude response of the filter used in this reference design for the 520-Hz low tone, respectively.

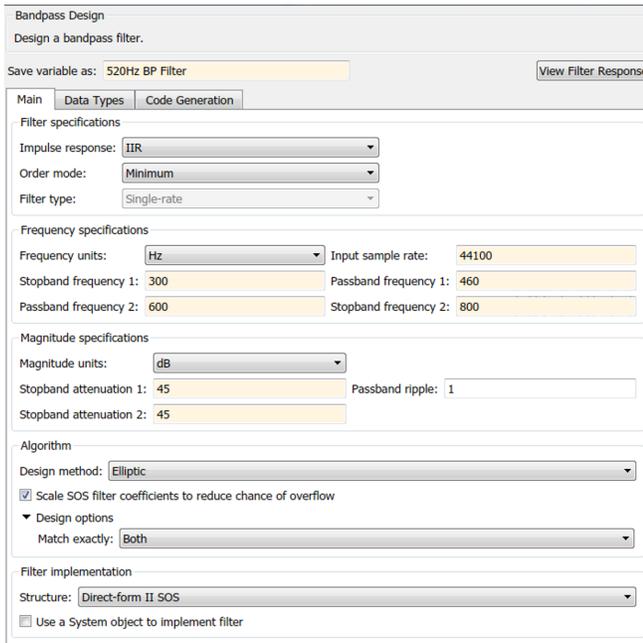


Figure 35. Parameter Definition of 520-Hz Digital Band-Pass Filter

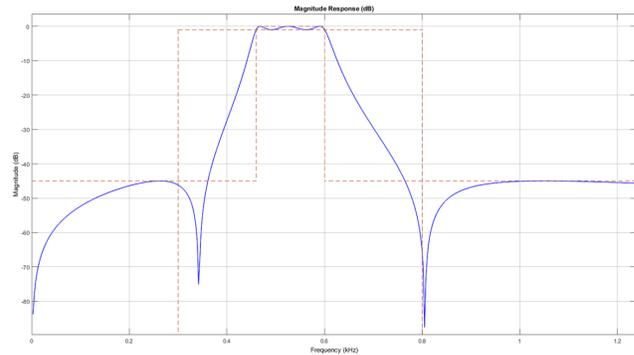


Figure 36. Magnitude Response of 520-Hz Digital Band-Pass Filter

2.3.3.3 FFT Analysis of Audio Sample

After the audio sample is fully conditioned based on the frequency requirements of this design, the sample can be converted from the time domain to the frequency domain for power spectral density analysis. Power spectral density analysis (PSD) is used to measure the energy at various frequencies, as opposed to just a simple Fourier transform. This is achieved by using the product of the fast Fourier transform (FFT) output and the complex conjugate result of the FFT as shown in Equation 32.

$$PSD = \text{fft}(x) \times \text{conj}[\text{fft}(x)] \tag{32}$$

where:

- $\text{fft}(x) = \sum_{j=1}^n x(j) W_n^{(j-1)(k-1)}$
- $W_n = e^{(-2\pi i)/n}$

The power spectral density can also be expressed by:

$$PSD = (\text{REAL}(X) + i \times \text{IMAG}(X)) \times (\text{REAL}(X) - i \times \text{IMAG}(X)) \tag{33}$$

where X denotes the resulting complex FFT result, separated into real and imaginary parts.

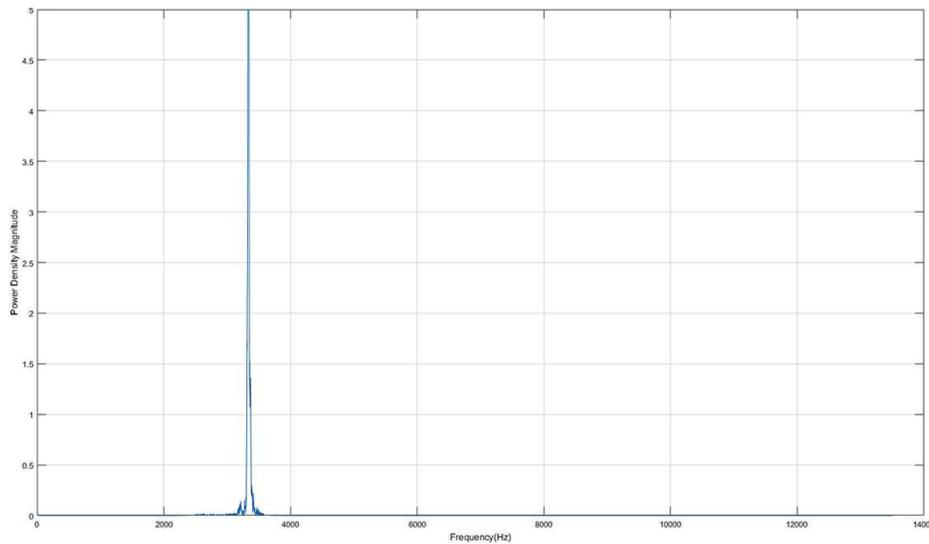


Figure 37. Power Spectral Density Plot of 3-kHz Alarm at 2-ft Proximity

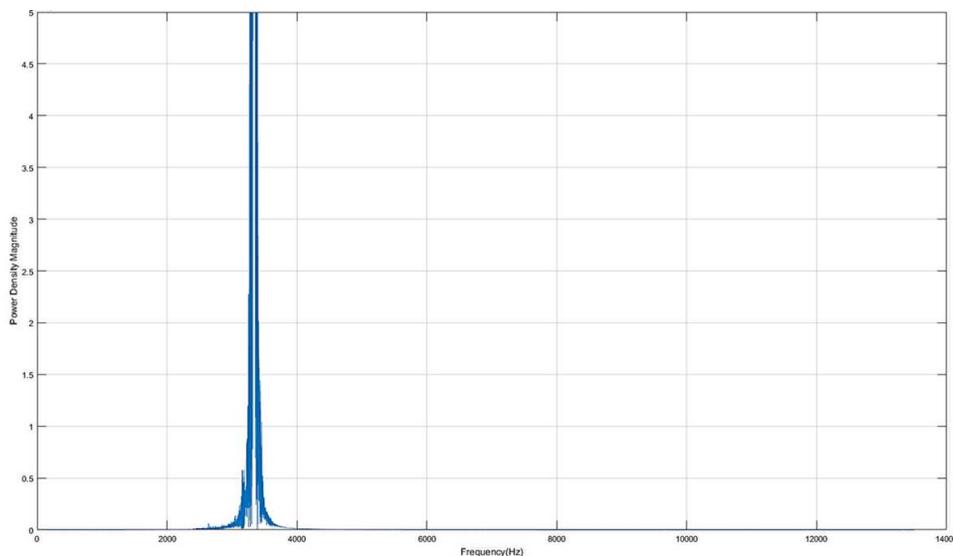


Figure 38. Power Spectral Density Plot of 3-kHz Alarm at 10-ft Proximity

This math function is included in the MATLAB function library, allowing for rapid prototyping of the algorithms mathematical front end with the ability to later convert the algorithm into both C and C++ once complete. [Figure 37](#) and [Figure 38](#) show the resulting spectral power density plot for a \approx 3-kHz fire alarm at two different distances from the microphone. As shown in the plots, there is a high power density magnitude in the target frequency range during a fire alarm test. This peak frequency location and magnitude is used in the detection algorithm as a first tier checkpoint for potential alarms.

2.3.3.4 Detection Algorithm Development

After collecting all the characteristic data for the fire and CO alarms, the obtained values for a particular sample set can be compared to known fire and CO alarm detection parameters to determine if a perceived alarm has occurred. The main distinguishing characteristics of the alarm that need to be analyzed are the frequency response as well as repetition in the signal sounding. Because this algorithm is based on total buffered sample results, there is no way to distinguish the alarm temporal pattern from a constant beep at the same target frequency. To accommodate such a detection method requires real-time audio analysis, which is outside the primary focus of this reference design.

For the main detection algorithm, the following data parameters are used and compared to expected parameters extracted from a known alarm:

- **is_Freq:** Used to determine if the location of the maximum magnitude value is in the target frequency range. This can be adjusted based on application.
- **is_Range:** Uses [Equation 34](#) to determine the ratio of target frequency magnitude over the total response magnitude sum, or simply calculating the percentage of magnitude in the target frequency spans.
- **is_Mag:** Checks for a non-zero value of **MThresh_Mag**, which is a peak detection algorithm using minimum peak distance and minimum peak prominence values to determine the detection threshold.

$$\text{Ratio} = \frac{\sum m_{\text{Target}}}{\sum m_{\text{Total}}} \quad (34)$$

For the counter section of the algorithm, the main purpose is to remove false alarms due to brief power density peaks in the target frequency spectrum. To account for this event, there must be multiple occurrences in a three- to five-sample period. If this condition is not replicated after five additional sample sets, the counter is reset and the data of interest is deemed a false alarm. The combination of counters for both possible outcomes, alarm detected or no alarm detected, allows for gaps in consecutive positive detections based on the no sound portion of the alarm pattern. This means that if two positive detect iterations occur but the next produces a false alarm, there must be four additional false alarm iterations before the alarm detected count resets back to zero. The user can change these parameter values to tighten or relax the detection window for more or less accuracy depending on the user system design requirements.

The complete fire and CO alarm detector algorithm is shown in [Figure 39](#) and [Figure 40](#).

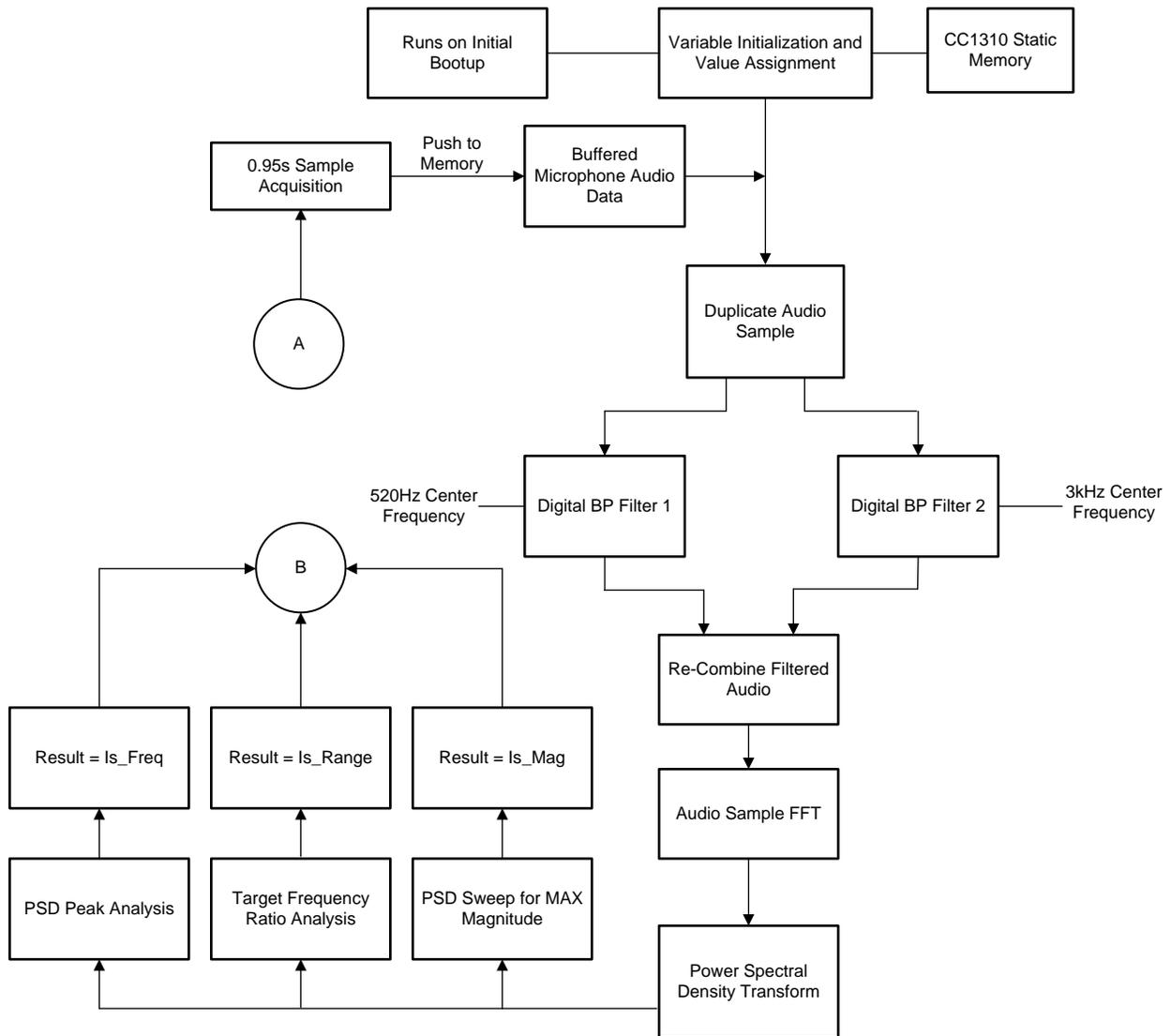


Figure 39. TIDA-01519 Audio Processing Flow Chart

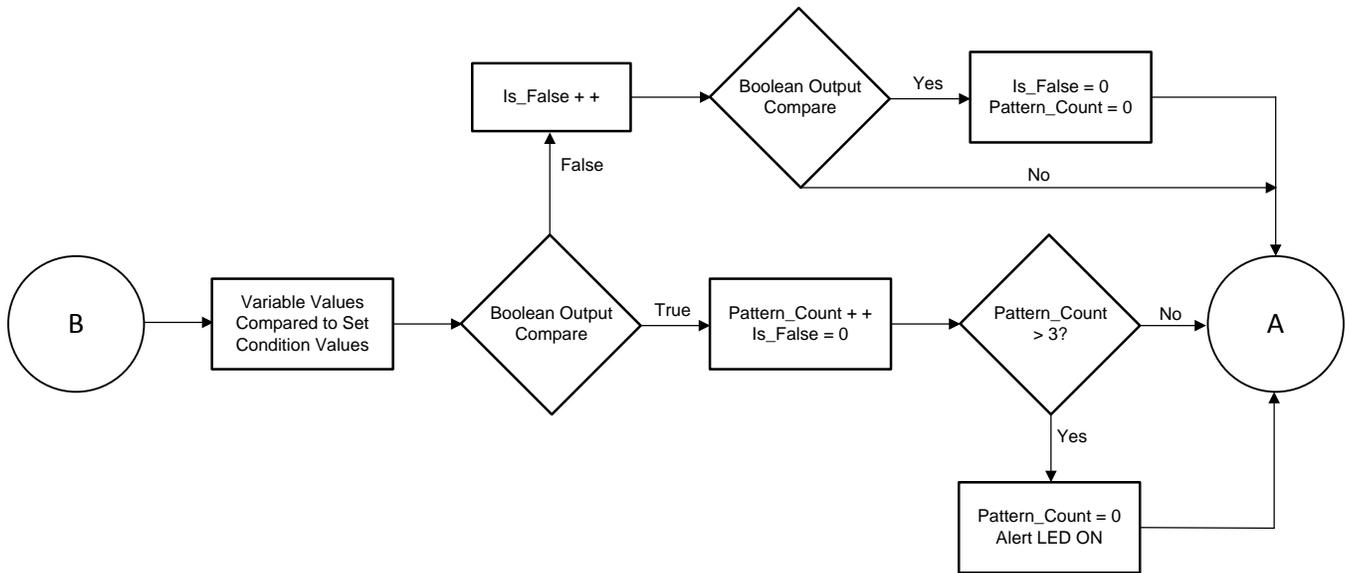


Figure 40. TIDA-01519 Alarm Detection Algorithm Software Flow Chart

3 Hardware, Software, Testing Requirements, and Test Results

The following information is used to test the this reference design and ensure the correct functionality as defined in the design theory section.

3.1 Required Hardware and Software

3.1.1 Hardware

For this design, [Figure 41](#) shows the main sections of the board that can be probed and tested by the user. It is important to remove the extra jumpers from the two gain select headers to have accurate gain feedback resistance.

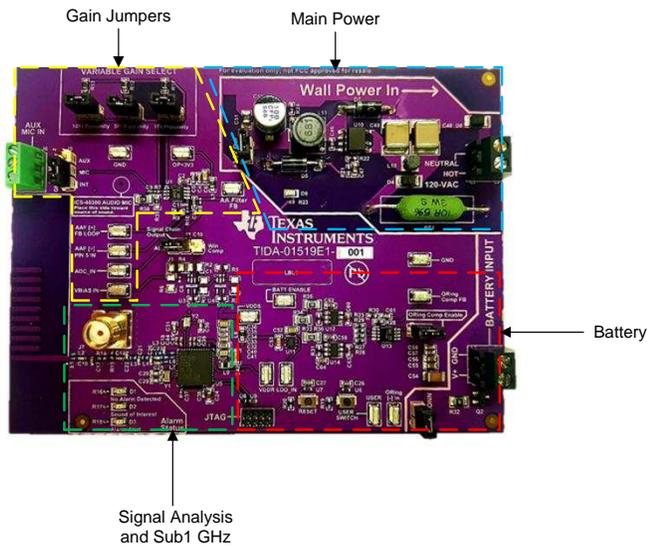


Figure 41. TIDA-01519 Top Board Overview



Figure 42. TIDA-01519 Bottom Board Overview

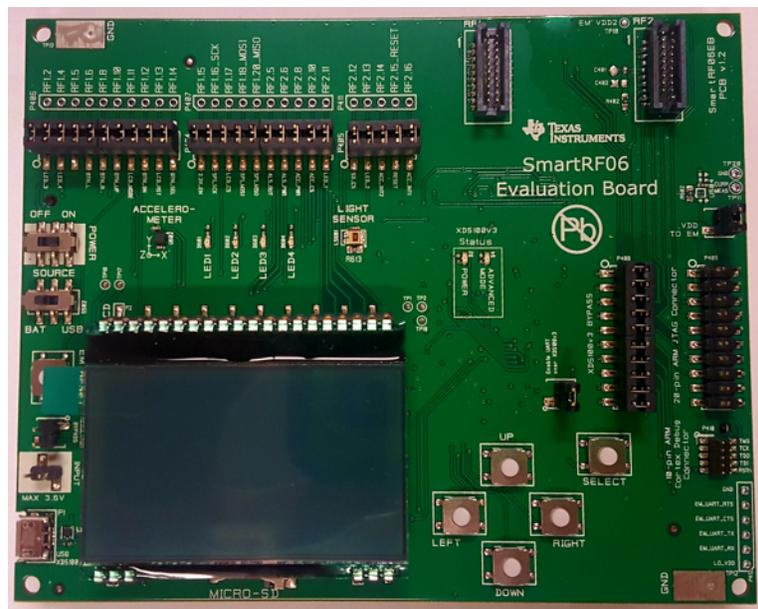


Figure 43. SmartRF06 Evaluation Board

3.1.2 Software

The following subsections outline the method used to successfully deploy the firmware of this reference design to the board for the purpose of evaluating the design.

3.1.2.1 Deploying Firmware to TIDA-01319 Board

The firmware used on this design is developed using TI's CCS software after initial development and testing in MATLAB. The IAR Embedded Workbench for ARM also supports the CC13xx line of SimpleLink products. To program or debug the design hardware, powering the board from a stable 3.0-V source is necessary and can be supplied at TP1. The GND path can be connected to either of the test points marked "GND". The design hardware is programmed by connecting the 10-pin mini ribbon cable from J8 to the SmartRF06 Evaluation Board (10-pin ARM Cortex Debug Connector, P418). See [Figure 44](#) for a photo of the correct setup for connecting the design hardware to the SmartRF06 evaluation board.

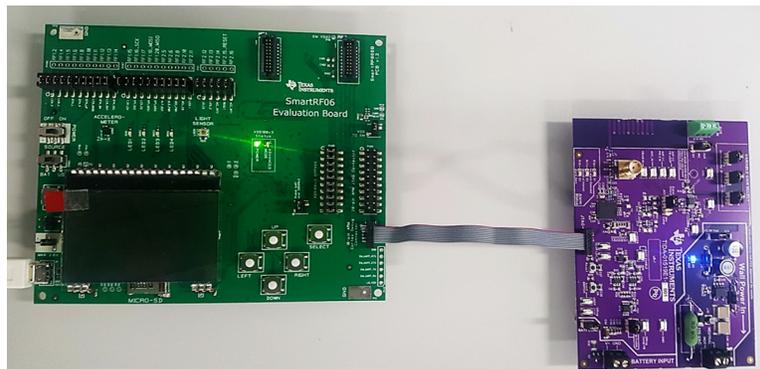


Figure 44. Proper SmartRF06 to TIDA-01519 Board Connection

3.2 Testing and Results

The ensuing subsections represent the test setup used to verify correct design functionality as well as the results obtained from these tests.

3.2.1 Test Setup

3.2.1.1 Test Setup of Audio Response

The first test is to verify the correct audio response from the signal chain circuitry described in [Section 2.3.2](#). For this test, the reference design board is placed at a range of 1 to 10 ft away from the audio source. The alarm is next put into test mode, where it sounds the alarm for both the fire alarm and the CO alarm. The amplification gain stage test pin and the ADC input pin are probed with an oscilloscope to record the response. This probe setup is shown in [Figure 46](#).

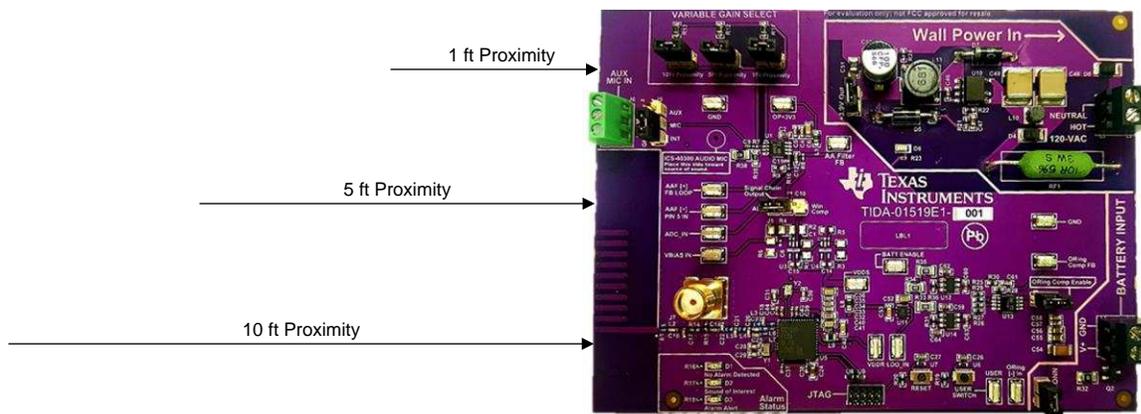


Figure 45. Test Setup of Audio Response Alarm

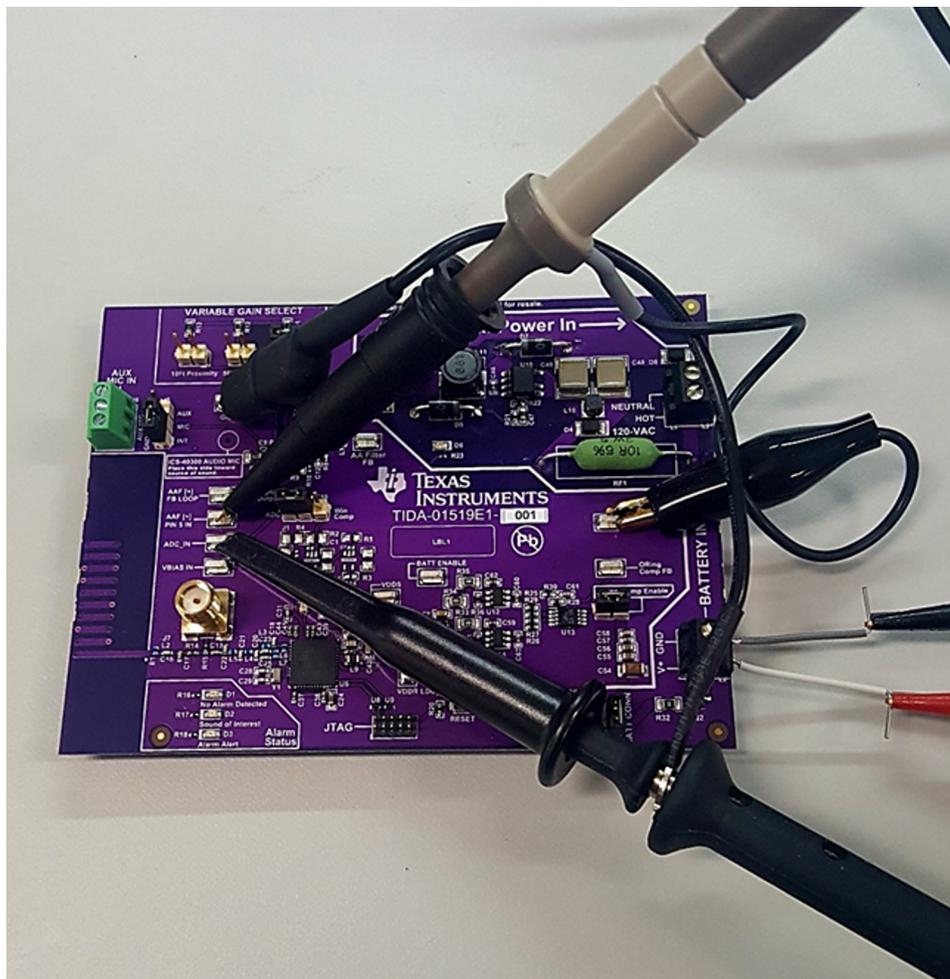


Figure 46. Setup of Audio Response Probe

3.2.1.2 Test Setup of Power Source ORing

For the power source ORing, the main signals that need to be observed are the power sources (3.9 V and BATT_IN), as well as the LDO input voltage, which indicates whether or not the ORing circuit is performing as expected. The PFET to NFET node of the first load switch is also monitored to verify the BATT_IN load switch is put in the "Off" mode in the case that UCC28881 power becomes available.

Figure 47 shows the probe points used to test the ORing functionality implemented in this reference design. For the ORing test, 3.9 V is supplied to the board from a DC power supply as is the case for the battery input as well.

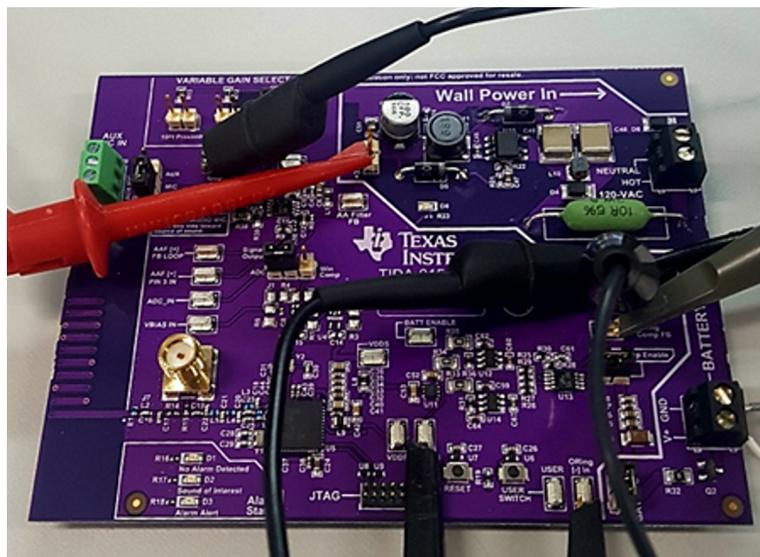


Figure 47. Test Setup of Power Source ORing

3.2.1.3 Test Setup of Current Consumption

For the current consumption testing, the battery power is removed from the system and a 3.9-V DC supply is connected in series to a current meter before being attached to the header pins of the UCC28881 power rail output. The current is measured while running the algorithm on the CC1310 in a quiet room and a louder environment. This is done to detect any current consumption changes that may arise based on the input audio SPL level.

The current consumption is also measured for the following events using the same setup described in Section 3.2.1.2. These values are obtained for both battery power as well as the UCC28881 power.

Table 5. TIDA-01519 Current Consumption Testing Plan

EVENT	DESCRIPTION	NUMBER OF MEASUREMENTS
Initial boot-up	Used to measure the initial current consumption of the board when it is first powered on	3
Quiet room	Testing relation between detected sound level and current consumption.	3
Loud room	Testing relation between detected sound level and current consumption.	3
Gain select 1 to 10 ft	Current measurements based on the gain level used	9 (3 for each case)
Fire or CO alarm detected	Current measurement when the device is going through the detection algorithm and alert	3
Battery + UCC28881	Current consumption based on ORing components	3

3.2.2 Test Results

The following subsections outline the results of the testing procedures shown in Section 3.2.

3.2.2.1 Audio Response Analysis Results

Figure 48 to Figure 53 show the acquired audio signals from fire and alarm testing. This pattern coincides with that of what is expected and at the target frequency. These tests are done at all three of the specified ranges and the delay and the phase from the gain stage output to the antialiasing filter output.

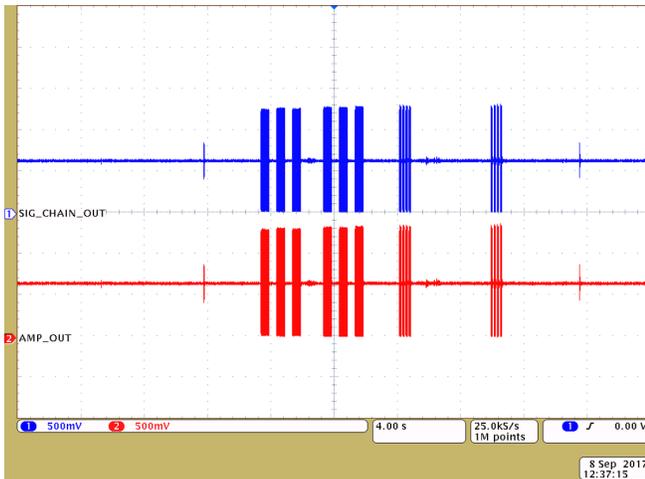


Figure 48. Signal Chain Response at 1-ft Proximity

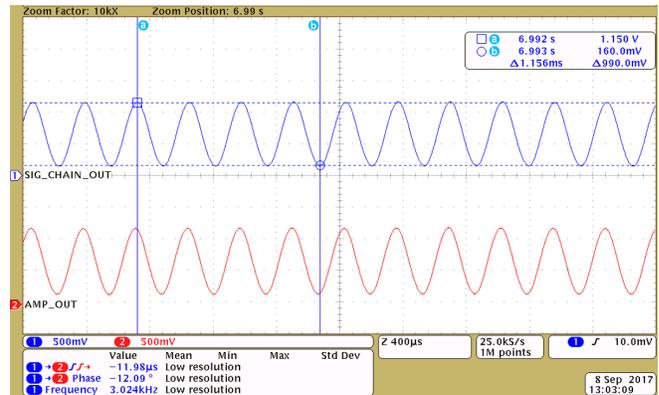


Figure 49. Delay, Phase, and Frequency Data Acquisition at 1-ft Proximity

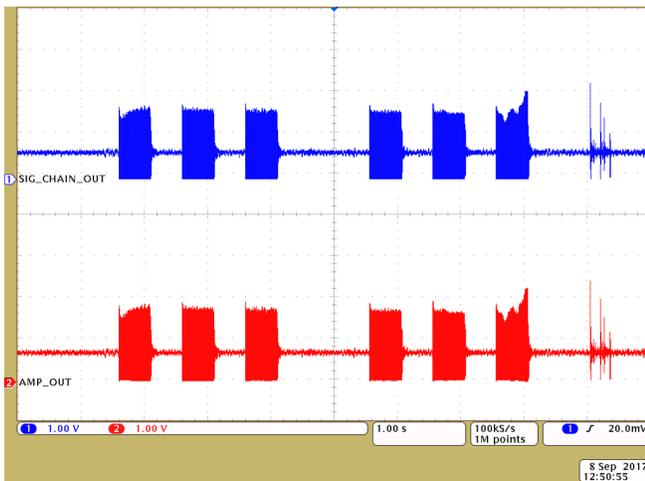


Figure 50. Signal Chain Response at 5-ft Proximity

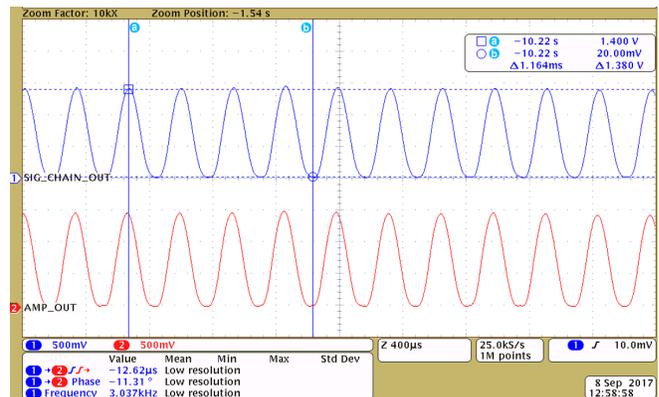


Figure 51. Delay, Phase, and Frequency Data Acquisition at 5-ft Proximity

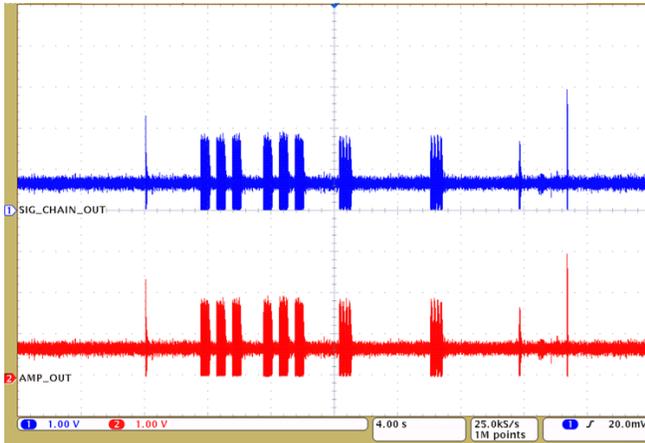


Figure 52. Signal Chain Response at 10-ft Proximity

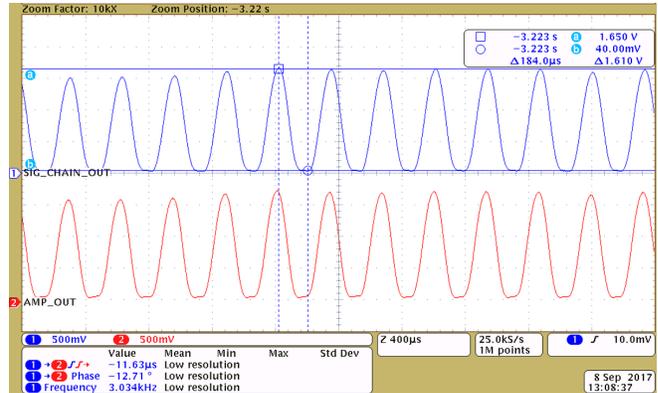


Figure 53. Delay, Phase, and Frequency Data Acquisition at 10-ft Proximity

Table 6 shows the results for all audio response testing at the three separate distances.

Table 6. Test Results of Signal Chain Audio Response

DISTANCE FROM SOURCE	INPUT-TO-OUTPUT DELAY	INPUT-TO-OUTPUT PHASE
1 ft	11.98 µs	-12.09°
5 ft	12.62 µs	-11.31°
10 ft	11.63 µs	-12.71°

Considering the simulation delay values extracted from TINA-TI, 35.38 µs, the delay and phase shift are much lower than the simulation prediction, approximately a third of the TINA-TI simulation estimates.

The audio response is also analyzed in the frequency domain in order to find the accuracy between the MATLAB simulations and the actual audio from the reference design board. Figure 54 shows the averaged frequency response of a typical household over a period of 24 hours. This is used to find the most accurate ambient room noise model.

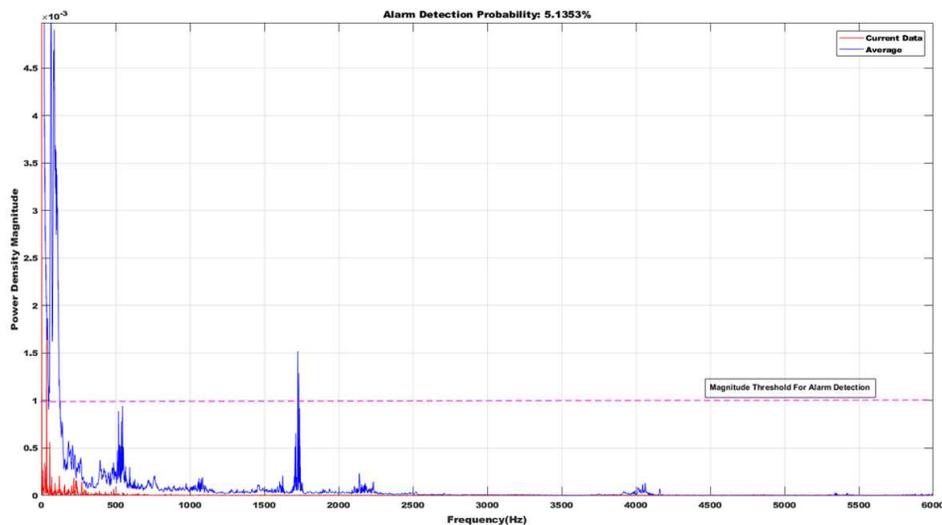


Figure 54. 24-Hour Proximity Averaged Spectral Power Density Response

Figure 55 shows the signal chain output from the design board. The data is transferred into MATLAB to be plotted. As can be seen from the graph in red, there is a high magnitude around the 500-Hz frequency. The magenta line represents the preset magnitude threshold set in the firmware. This threshold is one of three separate checks used to detect a fire or CO alarm. The blue waveform is a moving window average with a sample frequency of 20 kHz and a window size of 10. For this, the probability ratio is also used as the second check for possible alarms. In each case, the probability is over 90%.

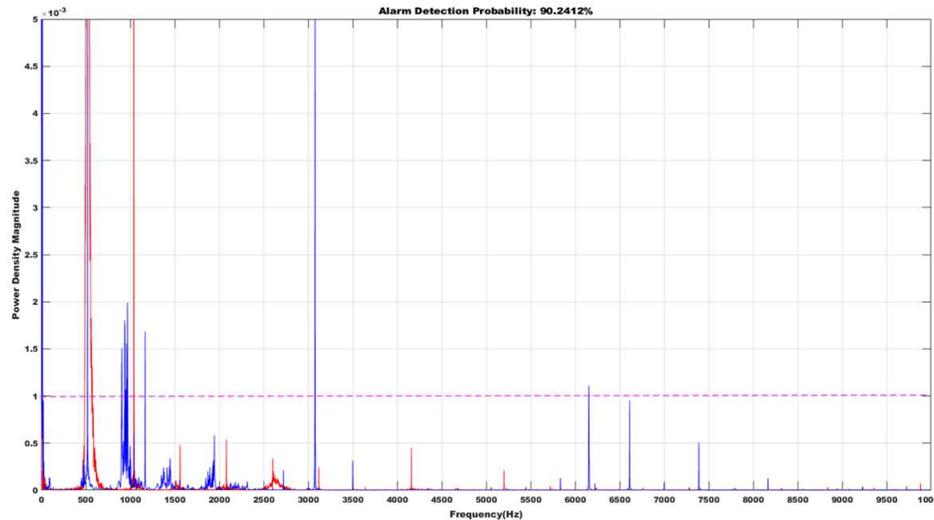


Figure 55. 520 Hz at 5-ft Proximity Alarm Detected Spectral Power Density Response

The 3-kHz alarm is also tested to ensure that both alarm frequencies were detectable using the same algorithm. Figure 56 shows the high magnitude 3-kHz frequency in red. In this case, the probability ratio increases to 91.4%. These test results verify the correct functionality of the signal chain of this reference design as well as the algorithm used to detect alarms.

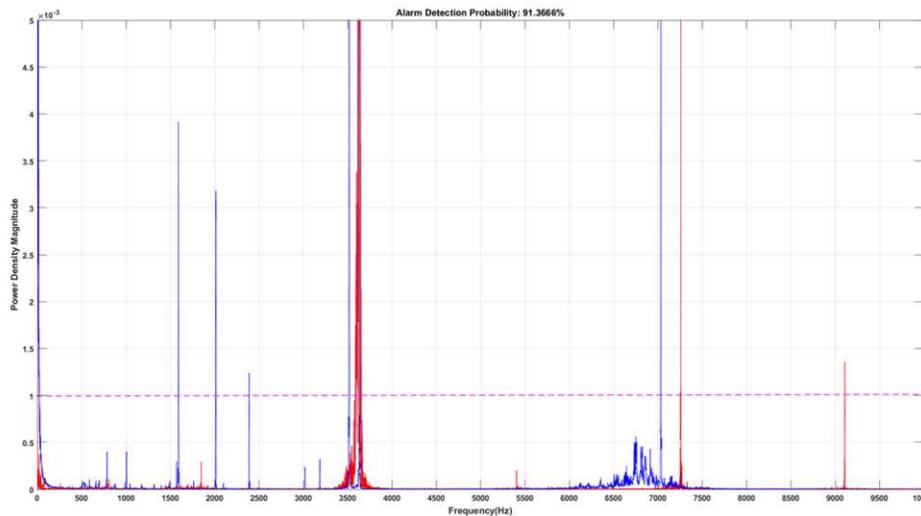


Figure 56. 3 kHz at 5-ft Proximity Alarm Detected Spectral Power Density Response

NOTE: The blue plots shown in Figure 55 and Figure 56 are not used in the algorithm to calculate any of the necessary values used for alarm detection. These plots are instead a comparison tool used to compare the current sample waveform (red) with that of the recent past (blue).

3.2.2.2 Test Results of Power ORing

This section represents the test results of the power tree ORing section of the design as discussed in Section 2.3.1.2. Figure 57 shows the results of the first of two scenarios tested for the power ORing. In this test, the battery is initially connected with no wall power applied. The battery enable is also monitored to ensure that the batter FET is disabled in the case that the UCC28881 power becomes available.

The LDO is shown to be a constant 3.3 V, supplied from the battery terminals. Once the UCC28881 output becomes available, the battery source is cut off by the BATT_ENABLE signal while the LDO voltage rises to the 3.9-V output from the UCC28881.

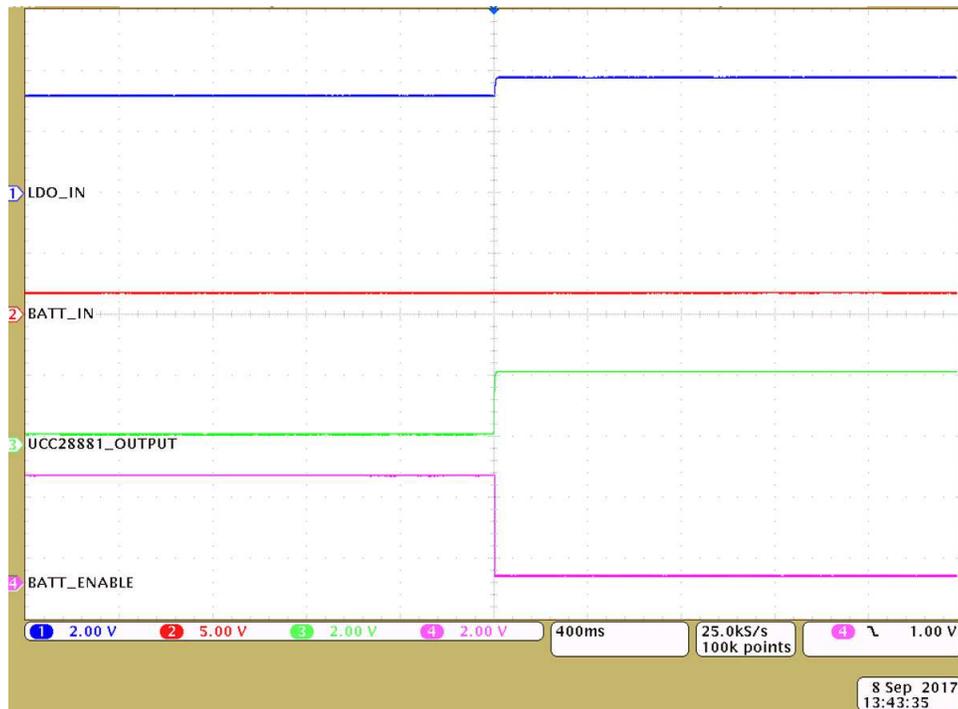


Figure 57. Test Results of Power ORing

For the next test, the power source scheme is reversed and the battery power is applied after the UCC28881 power rail. As shown in [Figure 58](#), there is a brief discontinuity before normal operation continues. This dip in supply power is due to the introduction of the battery source after the wall power is applied and the resulting power ORing circuitry response. There is no interruption to functionality in this scenario, but this occurrence is considered very rare and taken into account for design robustness.

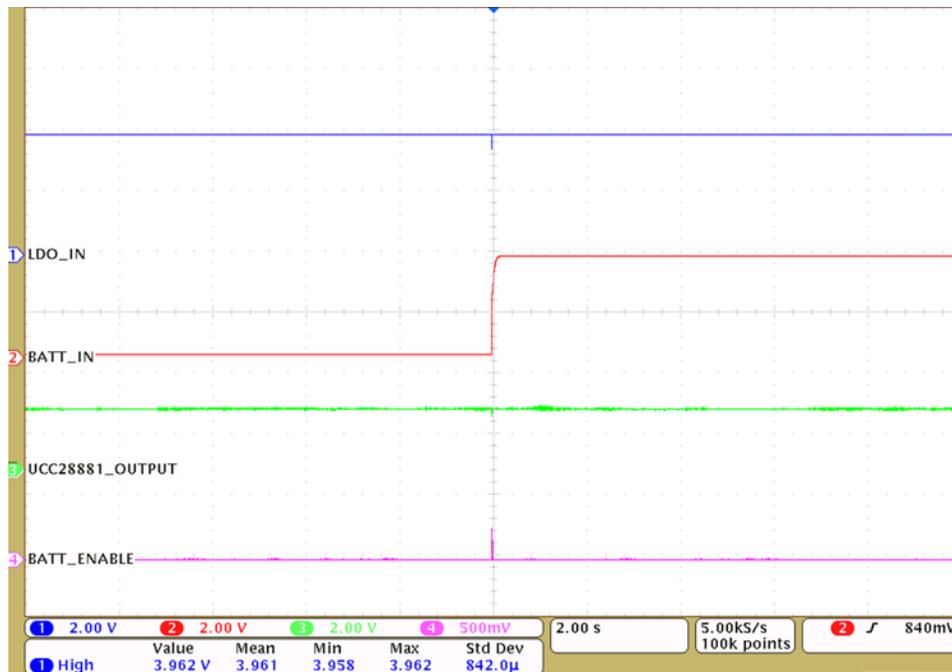


Figure 58. UCC28881 Power on With Battery Applied as Secondary Power Source

3.2.2.3 Test Results of Current Consumption

Table 7 and Table 8 show the results from the current testing of the design running under various conditions. The tables are separate based on the power source applied to the board.

Table 7. TIDA-01519 Battery Powered Current Consumption Testing Results

EVENT	MEASURED CURRENT VALUE									AVERAGE CURRENT CONSUMPTION
Initial boot-up	7.41 mA			7.49 mA			7.60 mA			7.50 mA
Quiet room	7.39 mA			7.38 mA			7.39 mA			7.39 mA
Loud room	7.41 mA			7.40 mA			7.39 mA			7.40 mA
Gain select 1 to 10 ft	1-ft PROXIMITY WITH BATTERY POWER			5-ft PROXIMITY WITH BATTERY POWER			10-ft PROXIMITY WITH BATTERY POWER			7.41 mA
	7.40 mA	7.39 mA	7.38 mA	7.39 mA	7.39 mA	7.39 mA	7.46 mA	7.44 mA	7.46 mA	
Fire or CO alarm detected	11.36 mA	11.37 mA	11.35 mA	11.51 mA	11.53 mA	11.36 mA	11.32 mA	11.32 mA	11.34 mA	11.38 mA
Battery + UCC28881	457.1 μ A			454.5 μ A			453.9 μ A			455.2 μ A

Table 8. TIDA-01519 UCC28881 Powered Current Consumption Testing Results

EVENT	MEASURED CURRENT VALUE									AVERAGE CURRENT CONSUMPTION
Initial boot-up	17.48 mA			17.50 mA			17.45 mA			17.48 mA
Quiet room	17.45 mA			17.50 mA			17.46 mA			17.47 mA
Loud room	17.66 mA			17.65 mA			17.49 mA			17.60 mA
Gain select 1 to 10 ft	1-ft PROXIMITY WITH UCC28881 POWER			5-ft PROXIMITY WITH UCC28881 POWER			10-ft PROXIMITY WITH UCC28881 POWER			17.47 mA
	17.46 mA	17.46 mA	17.46 mA	17.46 mA	17.5 mA	17.47 mA	17.46 mA	17.47 mA	17.47 mA	
Fire or CO alarm detected	21.40 mA	21.45 mA	21.40 mA	21.42 mA	21.42 mA	21.40 mA	21.38 mA	21.40 mA	21.41 mA	21.41 mA
Battery + UCC28881	17.43 mA			17.44 mA			17.44 mA			17.44 mA

NOTE: The majority of the current consumption is due to the LEDs used in this design. The LEDs are left in the design for verification purposes as well as visual indication of the current status of the firmware. The user can disable these CC1310 I/O pins to lower the current consumption significantly.

3.2.2.4 Alarm Detection Test Results

The following section shows the testing results of the final TIDA-01519 design. These represent the functionality of the system as a whole with respect to the following:

- Ambient monitoring with no detection
- Monitoring frequencies in the target range and providing visual indication to user
- Accurately detecting an alarm in the target frequency ranges and provide visual indication to user

Figure 59 shows the normal operation of the design in ambient conditions. There is a green LED indicating there is no activity and the detection algorithm is not currently being executed.

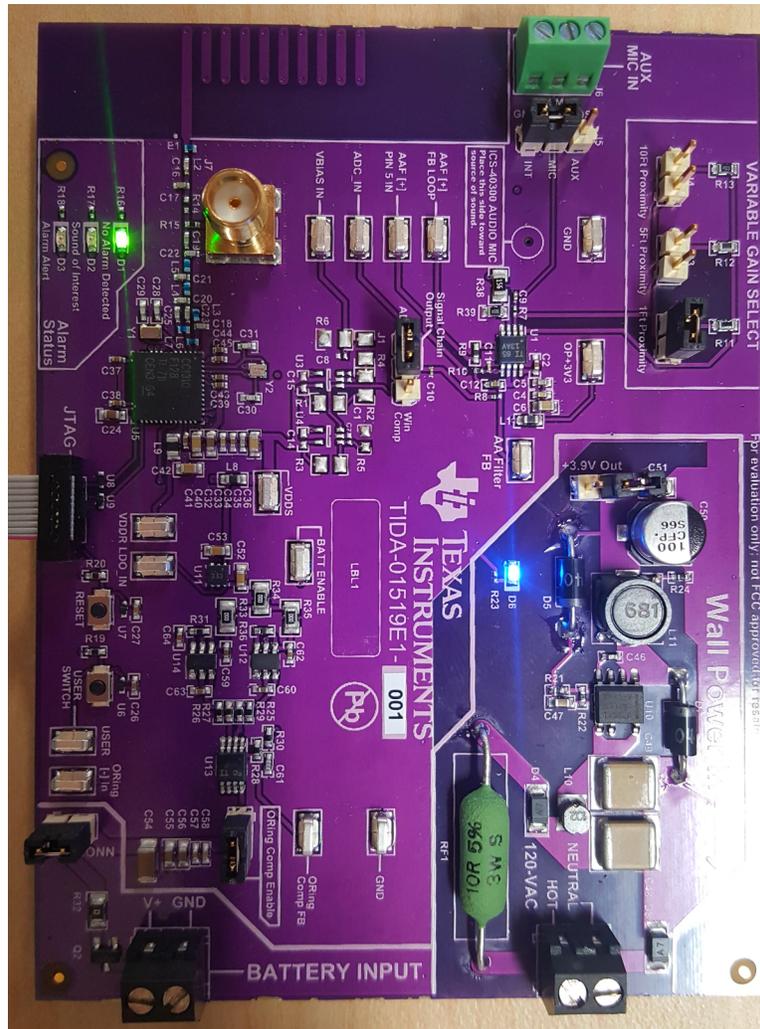


Figure 59. Ambient Environment System Status for No Activity

Next, the device is placed in the calculated proximity of the alarms and tested to verify the algorithm logic. Figure 60 shows the yellow LED on, indicating that the algorithm counter is active and buffering ADC data for the FFT computation.

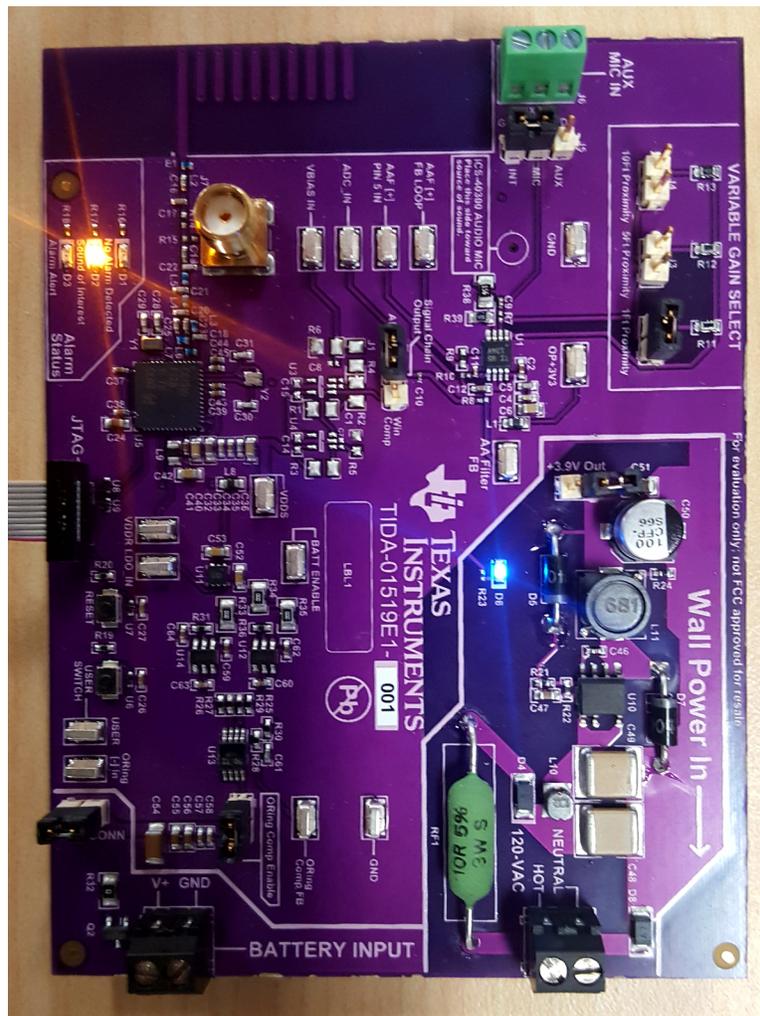


Figure 60. System Status for Detection Algorithm Active

Figure 61 is an additional visual feature created with the Sensor Controller Studio. The yellow and red lights are on simultaneously, indicating that the data buffer is currently being pushed to the FFT function to test for the predetermined target frequencies. If the return value of the FFT and detection algorithm is equal to one based on the software flow shown in Figure 40, the system halts and alerts the user with the red LED on only. If the FFT determines that there are no frequencies of interest in the data buffer sample, a return value of zero is given, which resets the algorithm and continues the polling process.

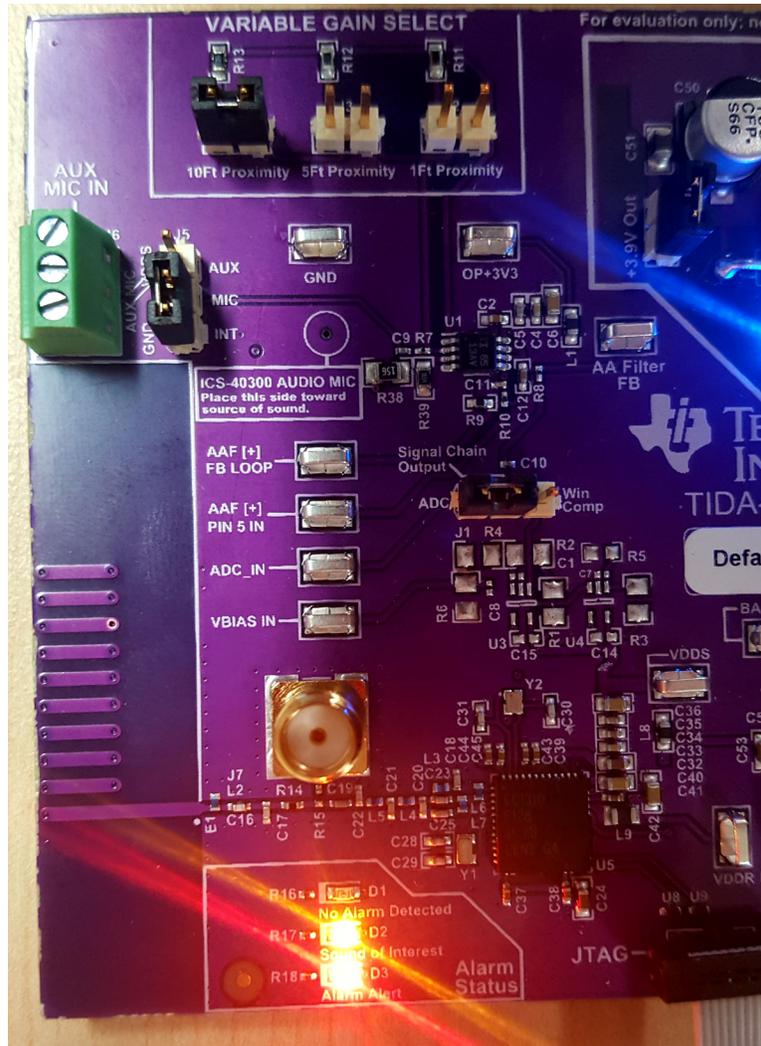


Figure 61. System Status for FFT Data Processing

Figure 62 shows the device status once an alarm is detected from the audio source. This indication can also be used with the wireless capabilities of the CC1310 to provide the user with remote access to fire and CO alarm alerts. This ability is even made simpler through the use of the Sensor Controller Studio, which provides examples on transmitting and receiving data packets in a user friendly interface.

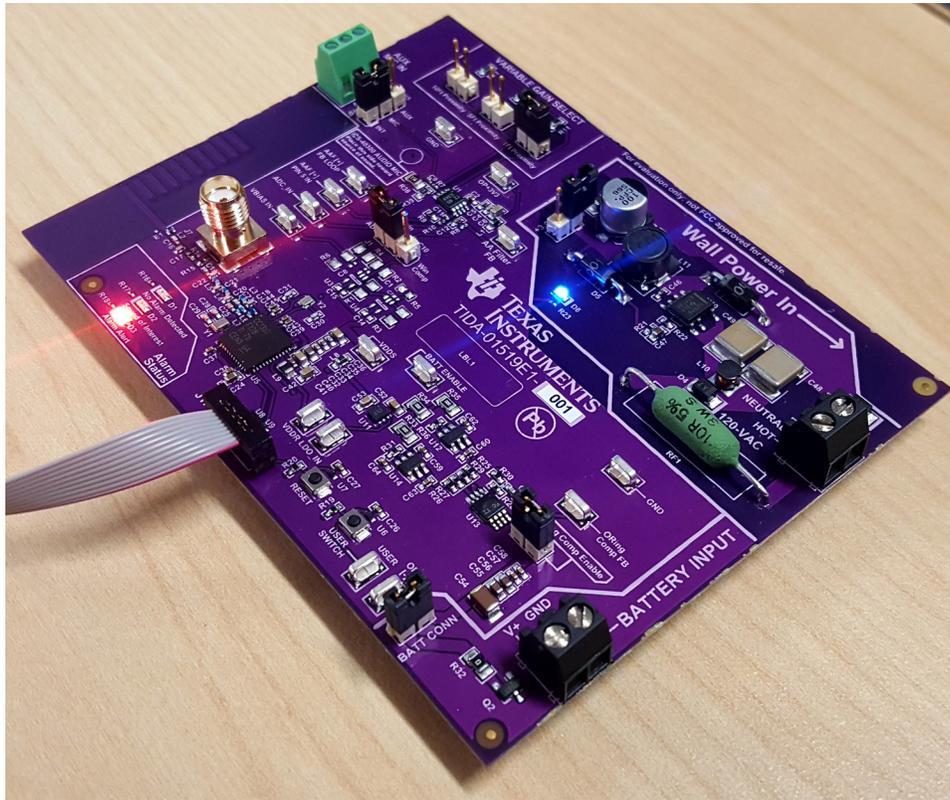


Figure 62. System Status for Alarm Detected

NOTE: For this testing, the polling interval and LED controls are implemented through the use of the Sensor Controller Studio development platform. To change these parameters, the user must open the included SCS_Source and run the project file. Note the location to which the program deploys newly produced output files. This location must reference the TIDA-01519_V1 files where the project files are located.

After loading and building the TIDA-01519 firmware, the user can add breakpoints in the debug section of CCS to watch the ADC input or any other values of interest.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-001519](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-001519](#).

4.3 PCB Layout Recommendations

4.3.1 PCB Antenna Layout Guidelines

The antenna on this reference design is the miniature helical PCB antenna for 868 MHz or 915 MHz. See the application note [DN038](#) (SWRA416) for more details about layout and performance.

4.3.2 TLV2313 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise may propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Chapter 17: Circuit Board Layout Techniques](#) (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.

4.3.3 UCC28881 Layout Guidelines

- In both buck and buck-boost low-side configurations, the copper area of the switching node DRAIN should be minimized to reduce EMI.
- Similarly, the copper area of the FB pin should be minimized to reduce coupling to feedback path. Minimize loop C_L, Q1, and R_{FB1} to reduce coupling to feedback path.
- In high-side buck and buck boost, the GND, V_{DD}, and FB pins are all part of the switching node, so optimize the copper area connected with these pins. A large copper area allows better thermal management, but it causes more common-mode EMI noise. Use the minimum copper area that is required to handle the thermal dissipation.
- Minimum distance between 700-V coated traces is 1.41 mm (60 mils).

4.3.4 TPS27081A Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Keep V_{IN} and V_{OUT} traces as short and wide as possible to accommodate for high current.
- Bypass the V_{IN} pin to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. Place this capacitor as close to the device pins as possible.
- Bypass the V_{OUT} pin to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{IN} bypass capacitor of X5R or X7R dielectric rating. Place this capacitor as close to the device pins as possible.

4.3.5 LM2903 Layout Guidelines

For accurate comparator applications without hysteresis, it is important maintain a stable power supply with minimized noise and glitches, which can affect the high-level input common-mode voltage range. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This must be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

4.3.6 TPS780 Layout Guidelines

To improve AC performance (such as PSRR, output noise, and transient response), design the PCB with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the output capacitor must be as close as possible to the ground pin of the device to provide a common reference for regulation purposes. High ESR capacitors may degrade PSRR.

4.3.7 Layout Prints

To download the layer plots, see the design files at [TIDA-001519](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-001519](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-001519](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-001519](#).

5 Software Files

To download the software files, see the design files at [TIDA-001519](#).

6 Related Documentation

1. InvenSense, [High SPL Analog Microphone with Extended Low Frequency Response](#), ICS-40300 Datasheet (https://store.invensense.com/datasheets/invensense/ICS-40300_ProductSpec_V1%200.pdf)
2. Texas Instruments, [Miniature Helical PCB Antenna for 868 MHz or 915/920 MHz](#), DN038 Application Report (SWRA416)
3. Texas Instruments, [WEBENCH® Design Center](#) (<http://www.ti.com/webench>)

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7 About the Author

BRIAN DEMPSEY is a systems design engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Brian brings to this role his extensive experience in HVAC systems, along with his experience with mixed signal systems. Brian earned his bachelor of science in electrical engineering (BSEE) from Texas A&M University in College Station, TX. Brian is a member of the Institute of Electrical and Electronics Engineers (IEEE).

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