Design Guide: TIDA-01513

Automotive High-Voltage and Isolation Leakage Measurements Reference Design

Description

The function of this reference design is to monitor the isolation resistance of a high-voltage bus to the chassis ground. Monitoring the isolation strength of coupling devices and components from high voltage to the chassis ground is a necessary feature in HEVs and EVs as battery management systems, traction inverters, DC/DC converters, onboard chargers, and other subsystems operate at high voltage (greater than 60 V).

Resources

TIDA-01513	Design Folder
AMC1301-Q1	Product Folder
TPSI2140-Q1	Product Folder
OPA2348-Q1	Product Folder
OPA320-Q1	Product Folder
SN6501-Q1	Product Folder
TL4050B25-Q1	Product Folder
TPS763-Q1	Product Folder

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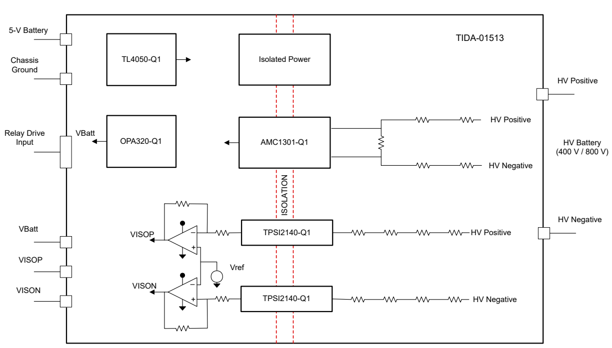
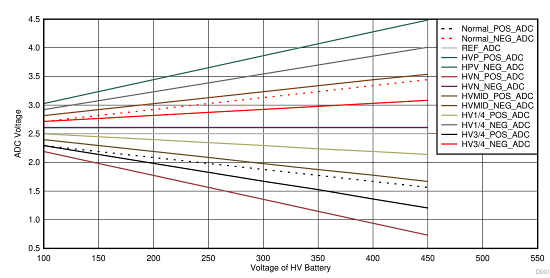
Features

- Accurate Isolation Voltage Measurement
- Estimated Isolation Resistance
- Accurate High-Voltage Measurement
- Accurate Leakage Current Estimation
- Scalable to Multiple Batteries

Applications

- Battery Management Systems
- Industrial Energy Storage Systems





1 System Description

In response to the latest changes in global environmental conditions and to reduce greenhouse gases, there is a need to have hybrid or electric traction units, which have very low or zero emissions. In a hybrid electric vehicle (HEV) or electric vehicle (EV), high-voltage batteries are used as storage elements to power the wheels. High-voltage batteries for automotive systems are defined as those with ≥ 60 V. Onboard chargers or external DC converters are used to source the power. Meanwhile, high-voltage batteries are used to store that energy. DC/DC converters and motor control inverters are used to power the wheels and other subsystems such as heating, ventilating, and air conditioning (HVAC). All these subsystems are working on high voltage.

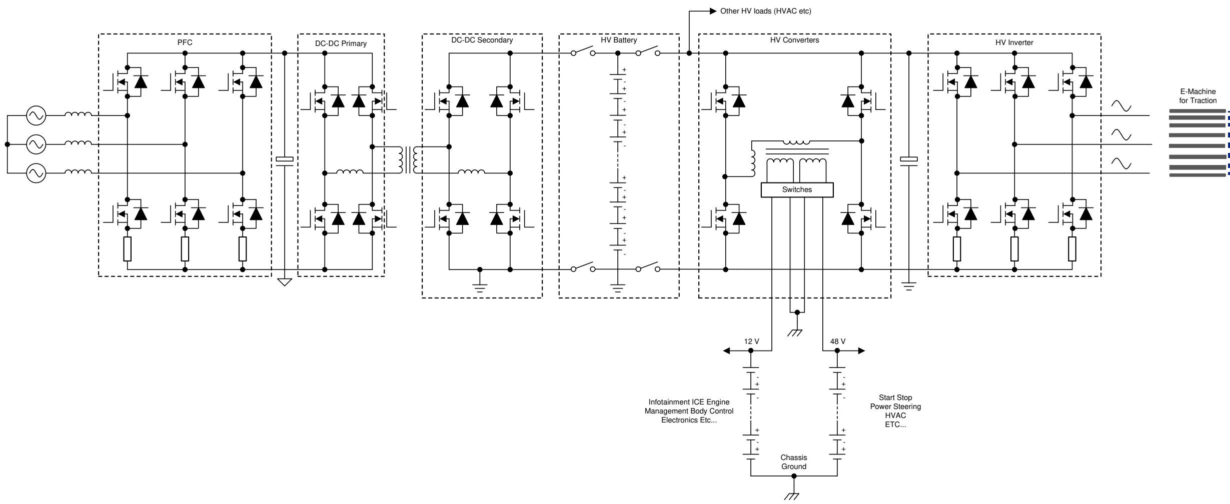


Figure 1-1. Typical HEV / EV Power Train

High-voltage components in HEV or EV systems are typically isolated from the chassis for functional and occupant safety reasons. The level of isolation in systems completely depends on the application, subsystem location within the vehicle, and the effective peak operating voltage. In general, HEVs and EVs use functional, basic, and reinforced isolation-based devices (see Figure 1-2). Functional isolation is used for protecting ground loops and the operation of those devices. Basic isolation is a single level of isolation which provides basic protection against electric shock. Reinforced isolation is a double level of isolation which provides higher protection against electric shock. Automotive power-train system developers should select basic or reinforced isolated components based on the voltage of the battery and peak voltages of the onboard charger and inverter.

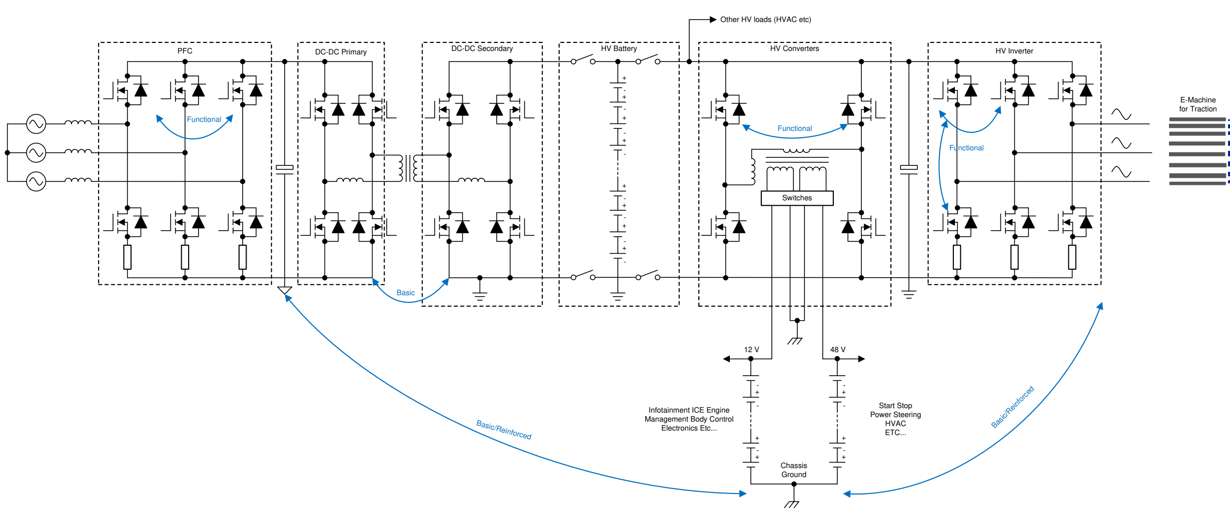


Figure 1-2. Isolation in HEV/EV

Isolation is a critical parameter for the safety of HEV and EV systems. Due to many factors such as improper motor winding, deteriorating wiring harnesses, general aging, and power dissipation, the operating temperature and peak electrical stress on semiconductors may lead to degradation or loss of isolation in these HEV and EV systems. Any single point for failure of isolation loss does not have much impact on the operation of the system, but it does become a potential life risk when operators make contact with this high-voltage operating environment. Vehicle manufacturers need to have a mechanism to detect every single point failure of isolation in a complete system and have a necessary preventive action in place. Measure isolation resistance and insulation leakage currents to check the safety of occupants in the HEV or EV system. As per FMVSS 305 specification, at least 500 Ω/V of isolation resistance must be maintained from high-voltage systems to chassis ground. Depending on the leakage current measured, HEV/EV system error-handling functions may be designed to take appropriate actions.. Functions or systems will be built to disconnect high-voltage relays and discharge the DC-link capacitors.

Checking the leakage or low ohmic resistance paths from high-voltage nets to the low-voltage chassis ground is important. The necessary isolation resistance is calculated based on battery voltage, creating a isolation breakage path and monitoring the deflections as explained in this design guide. Based on the vehicle architecture, the number of sampling points for isolation leakage measurements varies.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	MAXIMUM (MEASUREMENTS)
Voltage measurement accuracy	Measurements are done at room temperature. Deviations observed in measured values compared to calculated values.	0.624%
Isolated leakage current accuracy		0.621%
ISO_POS accuracy		0.48%
ISO_Neg accuracy		0.126%

2 System Overview

2.1 Block Diagrams

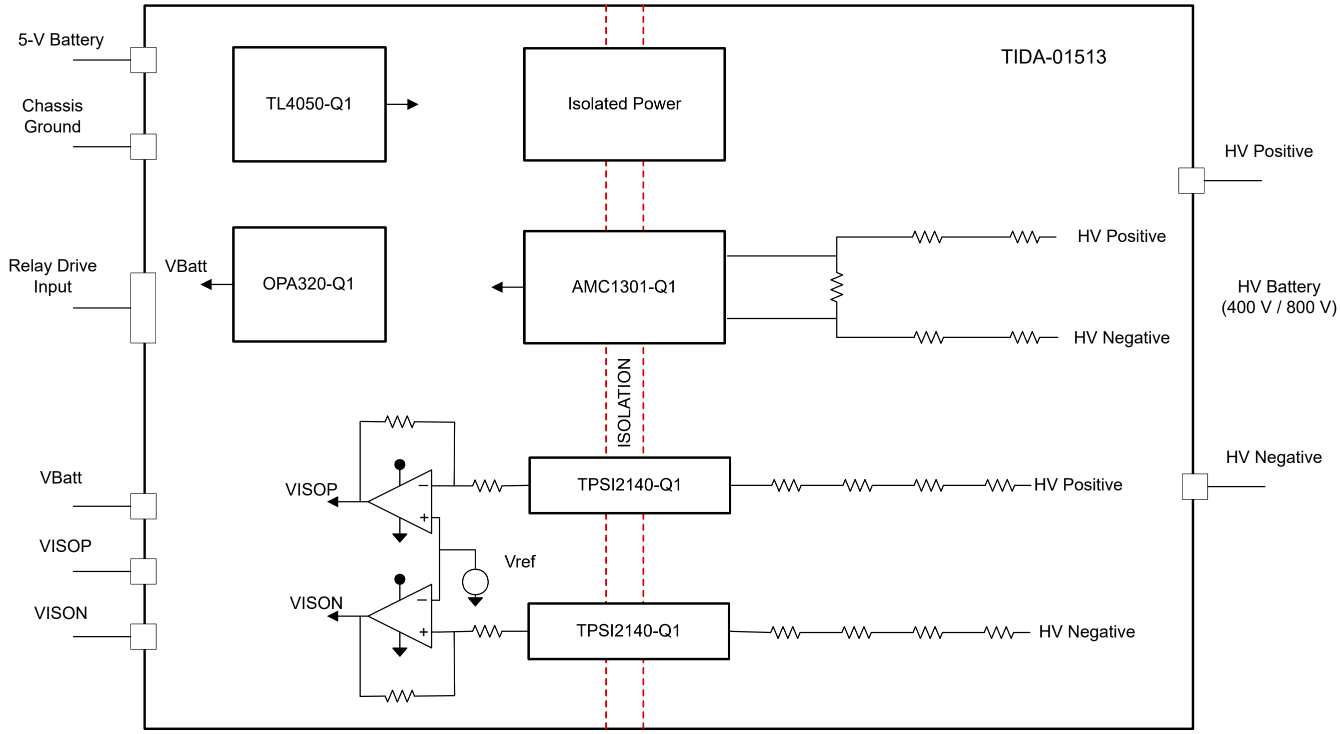


Figure 2-1. TIDA-01513 Block Diagram With SSR

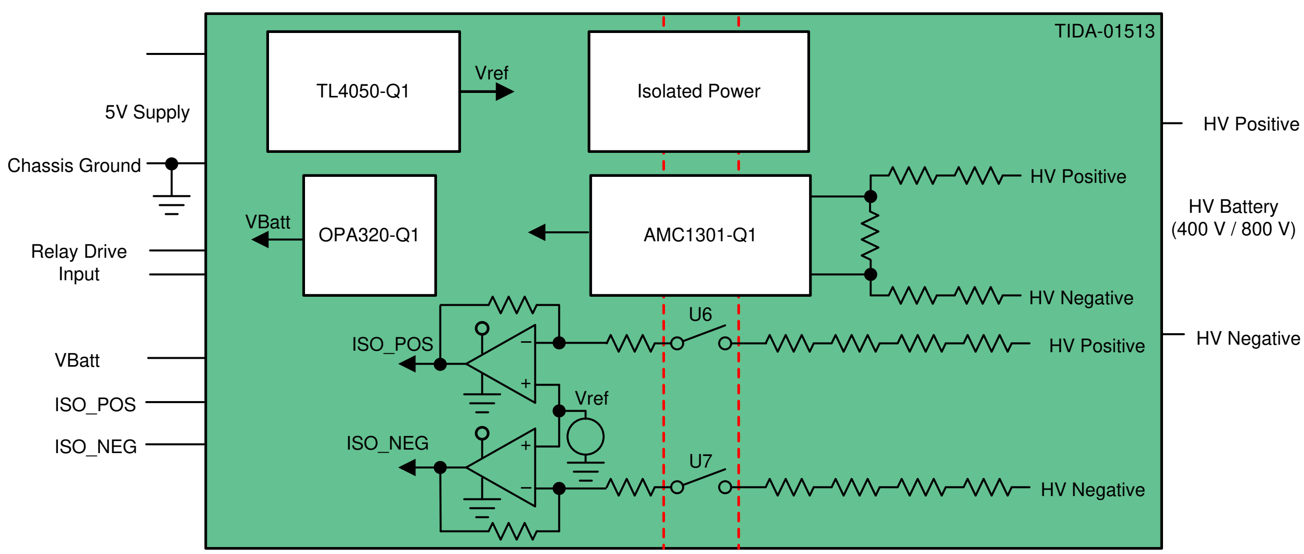


Figure 2-2. TIDA-01513 Block Diagram With EMR

2.2 Highlighted Products

2.2.1 TPSI2140-Q1

The TPSI2140-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. The primary side of the device consists of four differential drivers which deliver power and enable logic information to each of the internal MOSFETs on the secondary side. This device uses capacitive isolation technology in combination with its internal back-to-back MOSFETs to form a completely integrated solution requiring no secondary side power supply. When the enable pin is brought HI, the oscillator starts and the drivers send power and a logic HI across the barrier. When the enable pin is brought LO or the VDD falls below the UVLO threshold, the drivers are disabled. The lack of activity communicates a logic LO to the secondary side and the MOSFETs are disabled.

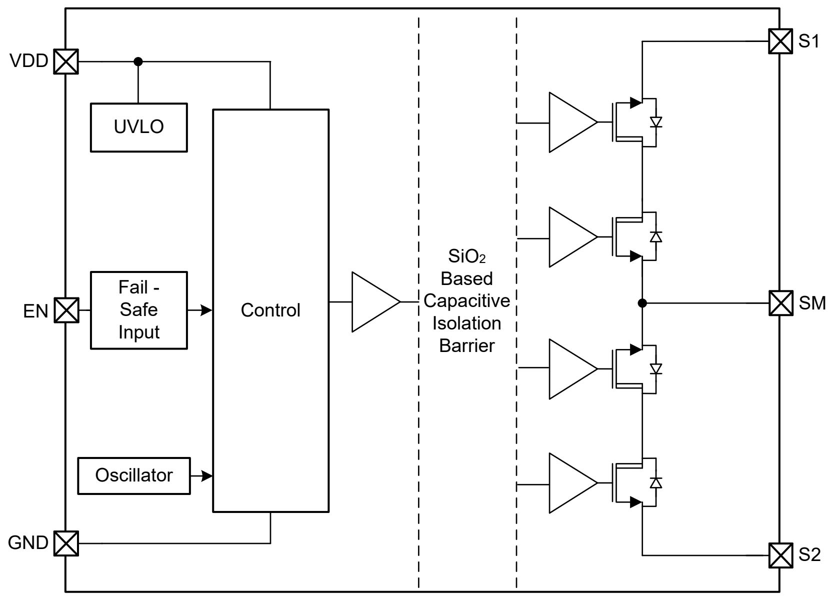


Figure 2-3. TPSI2140-Q1 Block Diagram

Key features include:

- Integrated MOSFETs with 2-mA avalanche rating
- 1200-V standoff voltage
- R_{ON} = 130 Ω (T_J = 25°C)
- T_{ON}, T_{OFF} < 700 µs
- Isolation rating, V_{ISO}, up to 3750 V_{RMS} / 5300 V_{DC}
- Low primary side supply current, 9-mA ON state current, 3.5-µA OFF state current

2.2.2 AMC1301-Q1

The AMC1301 device is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bit stream. The drivers transfer (TX) the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bit stream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device.

Figure 2-4 shows the AMC1301-Q1 block diagram.

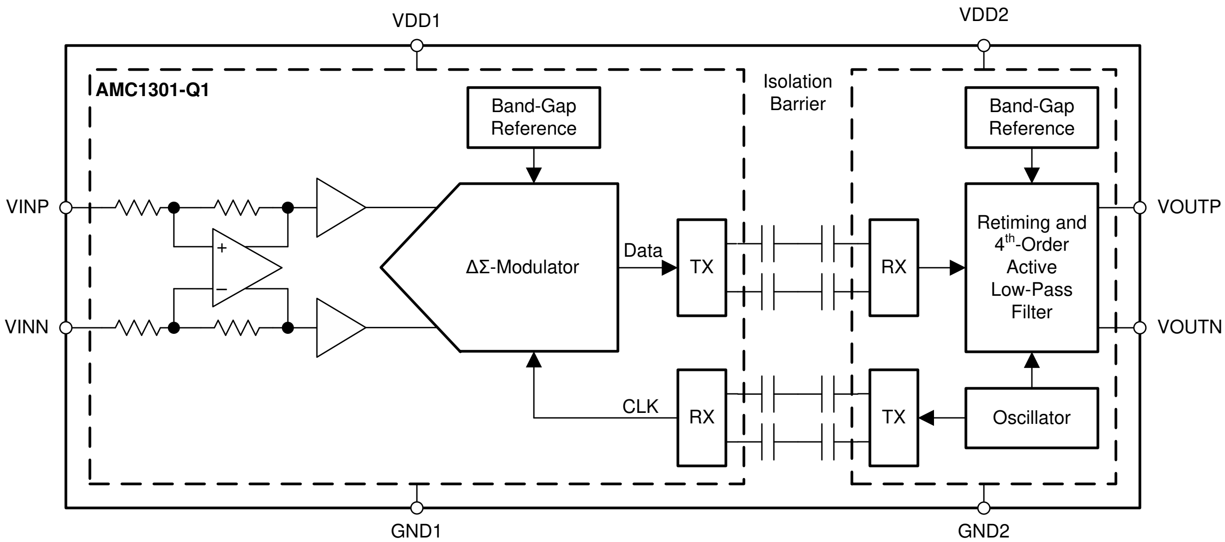


Figure 2-4. AMC1301-Q1 Block Diagram

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity* . The digital modulation used in the AMC1301 device and the isolation barrier characteristics result in high reliability and common-mode transient immunity (CMTI).

Key features include:

- ±250-mV input voltage range optimized for current measurement using shunt resistors
- Fixed gain: 8.2
- Very low gain error and drift: ±0.3% at 25°C, ±50 ppm/°C
- Very low nonlinearity and drift: 0.03%, 1 ppm/°C
- System-level diagnostic features

2.2.3 SN6501-Q1

The SN6501-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters using push-pull topology. The device includes an oscillator that feeds a gate drive circuit. The gate drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals that alternately turn the two output transistors ON and OFF. The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals with a 50% duty cycle. A subsequent BBM logic inserts a dead time between the high-pulses of the two signals. The resulting output signals present the gate-drive signals for the output transistors. As shown in Figure 2-5, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high impedance. Known as BBM time, this short period is required to avoid shorting out both ends of the primary.

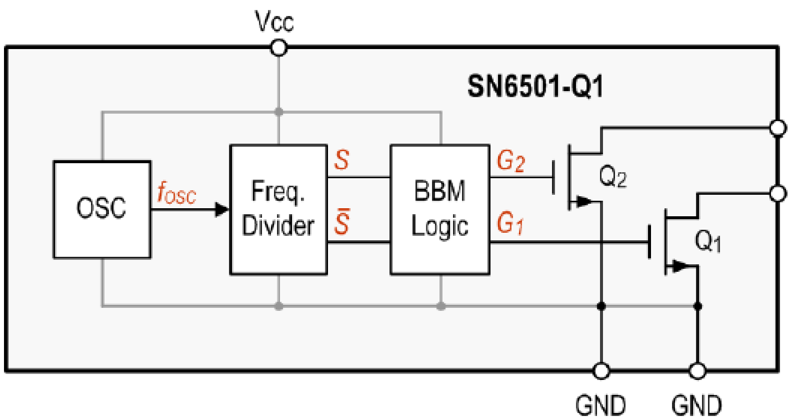


Figure 2-5. SN6501-Q1 Block Diagram

Key features include:

- AEC-Q100 qualified with –40°C to +125°C ambient operating temperature
- Push-pull driver for small transformers
- High primary-side current drive, 5-V supply: 350 mA (max)
- High primary-side current drive, 3.3-V supply: 150 mA (max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

2.3 System Design Theory

2.3.1 Isolation Leakage Current Theory

Isolation leakage measurements are typically performed in one of the subsystems in an HEV or EV system. Predicting the isolation breakage location is difficult and not possible to dousing isolated measurement techniques. The most effective way to measure isolated leakage current is by breaking the isolation of a complete system with a known resistance. If there is no current flowing between the switched path, then there is no parallel path which indicates that system is safe without any isolation breakages.

Designers must understand the type of failure and calculate the accurate isolation breakage parameters such as location (voltage) and resistance to classify the severity level. **Isolation leakage resistance** provides the information about the possible amount of leakage current for the second path, which can potentially electrocute the operator or passenger. To obtain a complete board diagnosis, break the isolation at two locations with known resistance paths.

Figure 2-6 is one of the examples of isolation breakage measurements using this reference design. S1 and S2 are relays used to switch the measurement paths. Rps1 and Rps2 are resistors used in the high-resistance path from the positive line whereas Rns1 and Rns2 are resistors used in the negative line. Rs1 and Rs2 are the series resistors used for isolation current measurements. An inverting op-amp configuration with V_{REF} (bias supply) is used for the measurements.

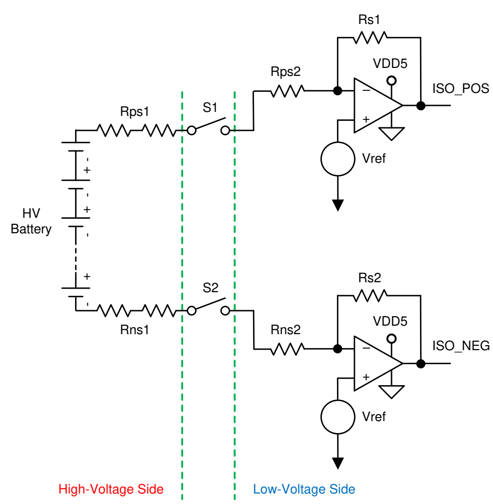


Figure 2-6. HEV and EV Isolation

During normal conditions when S1 is closed, no leakage enters the circuit because there is no closed path. The ideal condition is to set the V_{REF} potential at Rps1 and Rps2 with respect to chassis ground. ISO_POS must still stay at V_{REF} voltage when S1 is closed. In a practical circuit based on the type of op amp, its input differential voltage, and bias currents, variations will occur in ISO_POS voltage measurements. The circuit behavior is similar when only S2 is closed, as shown in Figure 2-7.

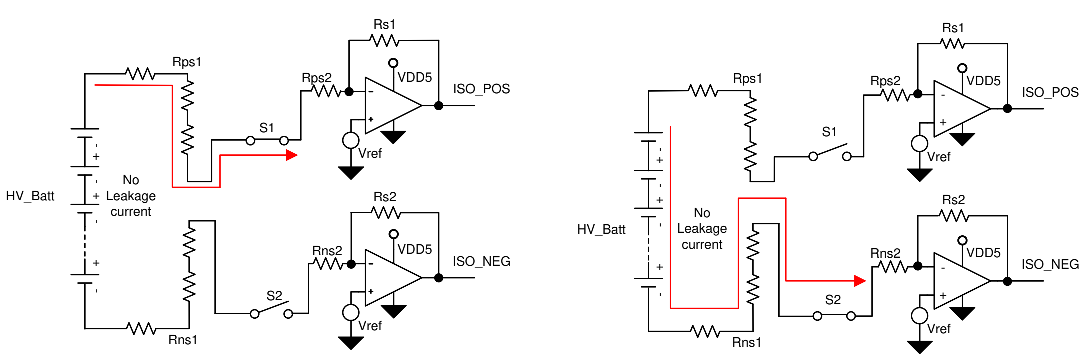


Figure 2-7. Normal Case: Only One Switch Closed

Figure 2-8 shows that, if both switches are closed, leakage current from a high-voltage battery flows using the chassis ground of the HEV or EV. Select resistors Rps1, Rps2, Rns1, and Rns2 such that they have very low leakage current (< 1 mA) in the chassis ground for the maximum battery voltage.

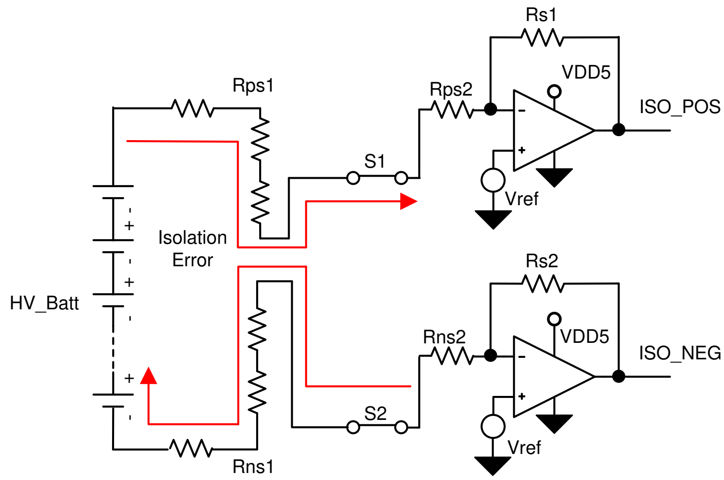


Figure 2-8. Normal Case: Both Switches Closed

As per Equation 1, the V_{REF} and resistors are fixed. Measure the ISO_POS with a 16-bit or 12-bit analog-to-digital converter (ADC) for better precision and resolution. Compare the measured value of ISO_POS with the known parameters of HV battery voltage and resistors used in the design. System calculations must have accurate voltage measurements. If the calculated value is beyond the tolerance level of the system, then consider it to be isolation breakage in the system. To minimize the error in the system, it is important to select high-precision metal electrode leadless face (MELF) resistors and op amps with low offset and bias currents. The designer can measure the offset voltage of the opamp and calibrate it in the system. Calibrating the input bias currents of opamps is difficult and they greatly influence measurements of the isolation leakage currents.

$$\mathrm{ISO\_POS} = V_{REF} - \frac{\mathrm{HV\_BATT} \times R_{S1}}{\left(R_{ps1} + R_{ps2} + R_{ns1} + R_{ns2}\right)} \tag{1}$$

$$\mathrm{ISO\_NEG} = V_{REF} + \frac{\mathrm{HV\_BATT} \times R_{S2}}{\left(R_{ps1} + R_{ps2} + R_{ns1} + R_{ns2}\right)} \tag{2}$$

As stated in Section 1, there are multiple root causes for the isolation breakage in the system. If the isolation breakage happens at the positive line of a high-voltage system, the circuit behavior is as shown in Figure 2-9. Riso is the isolation resistance from the high-voltage positive line to chassis ground, it can be as low as mΩ to MΩ. To perform the safety analysis, the designer must first identify the resistance of the isolation breakage and location. When only S1 is closed, there is no closed path for the high-voltage battery. Only leakage current flows from the low-voltage system due to the reference bias potential on the high-voltage line. The leakage current is negligible when only S1 is closed because the reference voltage is low (< 5 V) and the resistors are quite high (Rps1 + Rps2 > 500 kΩ).

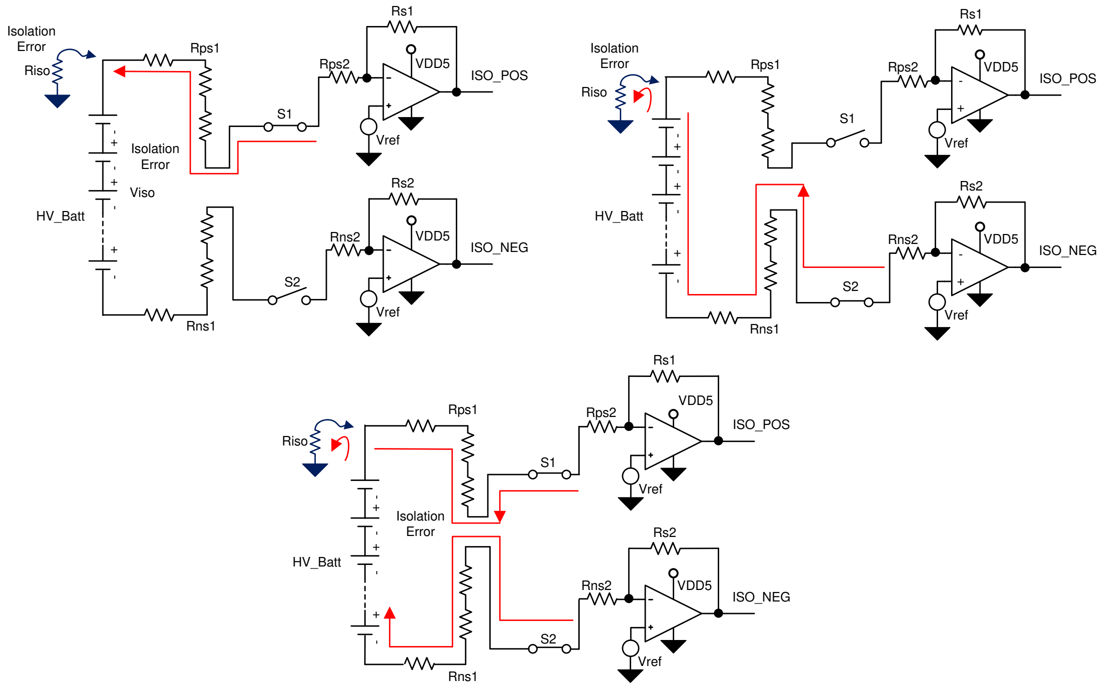


Figure 2-9. Isolation Error at Positive

When only S2 is closed, the high-voltage battery is in series with Rns1, Rns2, Riso, and V_{REF}. A significant leakage current flows from the high-voltage section to the chassis ground based on the battery voltage, Rns1, and Rns2. This is the actual leakage current from high-voltage to chassis ground, which can be measured at ISO_NEG.

$$ISO\_POS = V_{REF} + \frac{V_{REF} \times Rs1}{R_{ps1} + R_{ps2} + R_{iso}} \tag{3}$$

$$ISO\_NEG = V_{REF} + \frac{(HV\_BATT + V_{REF}) \times Rs2}{R_{ns1} + R_{ns2} + R_{iso}} \tag{4}$$

Figure 2-10 shows an equivalent circuit for isolation leakage current measurements when both S1 and S2 are closed. Considering that precision components are used in the circuit, input impedance, bias currents, and offset voltages of op amps are neglected.

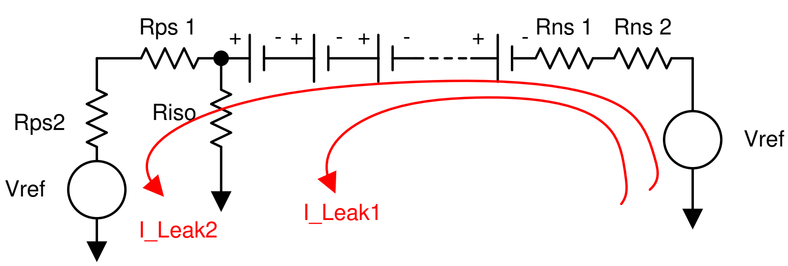


Figure 2-10. Equivalent Circuit for HV POS Isolation Leakage

Leakage currents in Figure 2-10 can be calculated by using the superposition of voltage sources. With the same reference supply and no offset voltage in the op amps, the leakage currents due to the V_{REF} supply is negligible and canceled in the circuit (because of symmetry). HV_BATT is the significant voltage source which contributes to leakage current in the chassis ground. If Riso is too low, then the I_Leak2 current shown in Figure 2-10 will be negligible. The key contributor variable leakage currents are the HV_BATT power source and isolation resistance. The measurements of ISO_N are significant because they can be used to find the leakage currents and isolation resistance when an isolation error occurs at a high-voltage positive terminal.

A similar analysis of the leakage currents is valid with the error at a negative potential. A couple of equations will change, but most of the theory remains the same. Measurements of ISO_POS are significant when an isolation error at the negative terminal of the high-voltage battery exists.

2.3.2 High-Voltage Measurement

High-voltage measurement is required to calculate the isolation leakage current. In TIDA-01537 , the AMC1301-Q1 device is used to perform these measurements. The AMC1311B has a high input resistance, a 2-V input range, and can also be used for high-voltage measurements.

As Figure 2-11 shows, the Rsh monitoring resistor is placed in series to a high-ohmic potential divider network. Voltage measurements are performed with a floating ground of the AMC1301-Q1. The OPA320-Q1 device is used to amplify the signal range and give a single-ended output to an MCU or logic interface. The AMC1301-Q1 can measure a bidirectional signal of ±250 mV. In HEV or EV motors, battery voltages are only in the positive range, so the usable range of the AMC1301-Q1 is 250 mV. A potential divider network must be chosen in such a way that the voltage drop in shunt resistance must be ≤ 250 mV at the maximum battery voltages.

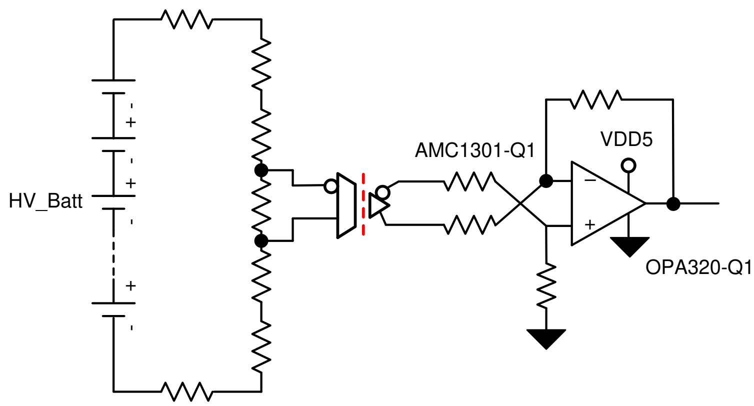


Figure 2-11. High-Voltage Measurements

Use Equation 5 to calculate the high battery voltage.

$$\text{HV\_BATT} = \frac{\text{VOUT\_OPA320} \times \text{Rs2}}{\text{R}_S \times \text{G\_AMC1301} \times \text{G\_OPA320}} \quad (5)$$

where

- V_{OUT_OPA320} is the output voltage measured by the ADC or relevant device from the output of the OPA320-Q1
- Rsx is the sum of the series resistors from HV_BATT positive to negative including the shunt resistor
- Rsh is the shunt resistor for the AMC1301-Q1
- G_AMC1301 is the gain of the AMC1301-Q1 internal circuit
- G_OPA320 is the gain set by the external resistors for the OPA320-Q1 circuit

Equation 5 is a simple equation that does not consider the influences of bias currents or offset voltages, which can lead to deviations in measurements.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

Hardware that measures isolation resistance is built with a high-voltage measurement circuit and isolation breaking circuit. As previous sections have explained, isolation measuring and a high-voltage monitoring circuit is implemented in the schematics and printed-circuit board (PCB). Use the OPA2348-Q1 and OPA320-Q1 op amps to reduce the error in high-voltage leakage current and voltage measurements.

As Figure 3-1 shows, MELF resistors R14, R15, R16, R17, and R18 are used for a potential divider circuit for the high-voltage positive line, whereas R21, R22, R23, R24, and R25 are used for a potential divider circuit for the high-voltage line. C17 and C22 are placed only in the schematic and layout to filter relay switching noise. These capacitors are not used in performance testings because they are a potential weak link for performance and reliability in mass production. MELF resistors are chosen to have less tolerance, high reliability, and a low temperature coefficient of resistance (TCR). Any deviation in resistor values have an impact on the error of interlock leakage current calculations.

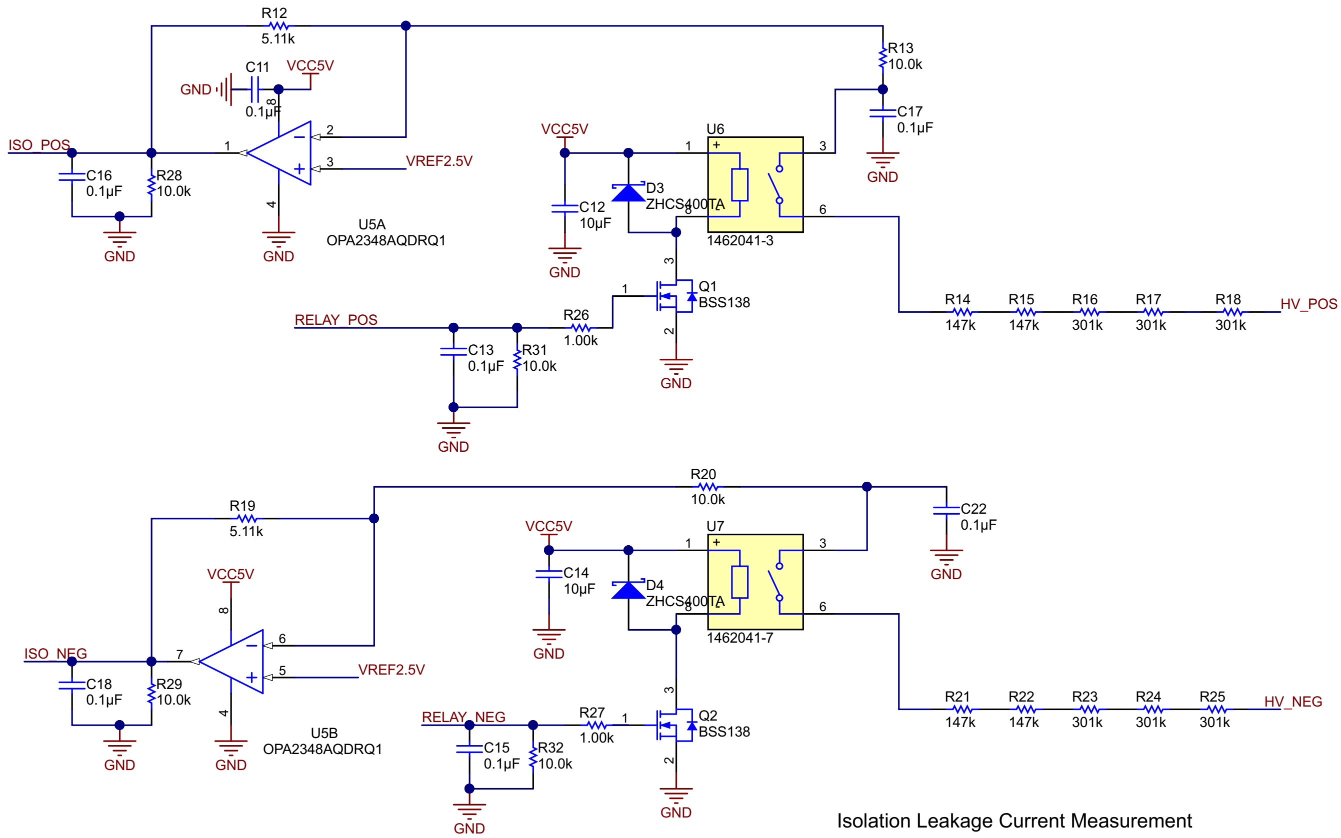


Figure 3-1. Leakage Current Measurement

R12 and R19 are chosen based on the battery voltage and signal range of isolation leakage current. Because the resistance and power dissipation is low, there is a possibility to select a high-precision resistance to calculate accurate leakage current. The OPA2348-Q1 is used for U5A and U5B, which support the voltage measurement with an applied offset given by VREF2.5V. The ISO POS and ISO NEG voltage change based on the state of battery voltage and the state of U6 and U7 relays. Q1 and Q2 are small signal transistors to control the relays. D3 and D4 are freewheeling diodes for relay coils (see Figure 3-2).

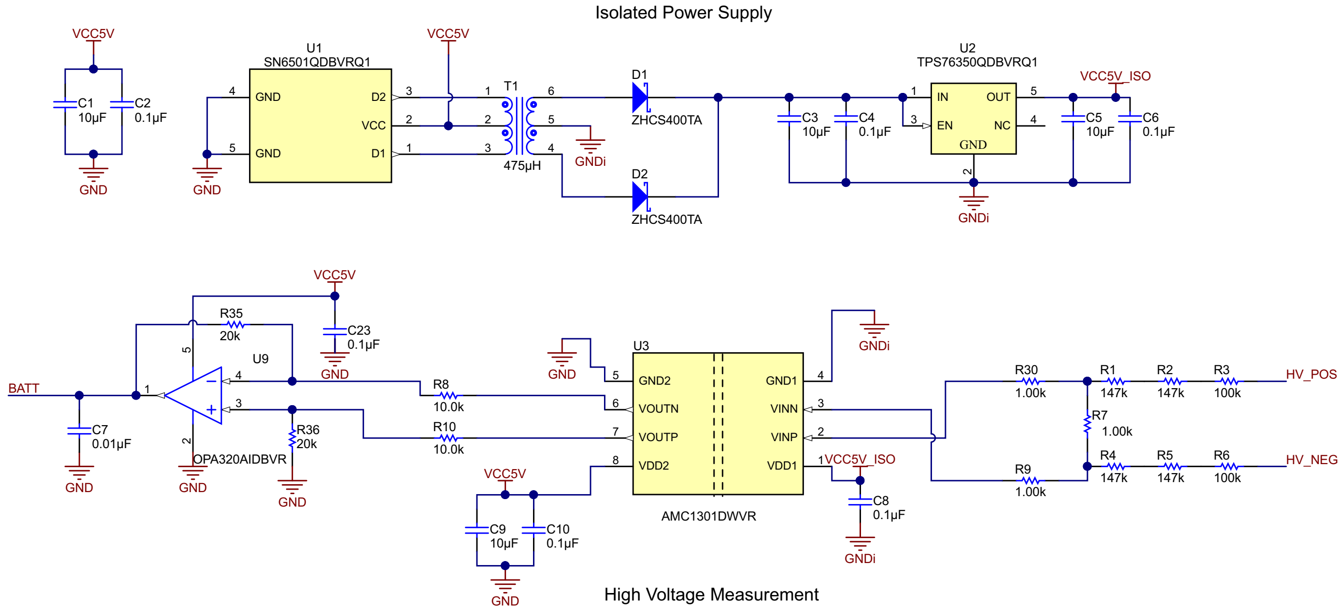


Figure 3-2. High-Voltage Measurement and Iso Power

Isolated power is required for isolated high-voltage measurements with the AMC1301-Q1 or AMC1311-Q1. The SN6501-Q1 transformer driver is used to transfer the power from T1 primary to secondary. D1 and D2 are used to rectify the power on the secondary side of the transformer. Based on turns ratio and operation of the SN6501-Q1, the output of D1 and D2 will be in the range of 6.2 V to 7 V. The TPS76350-Q1 device is used to regulate the output voltage to 5 V.

VCC5V_ISO is used to supply the secondary side of the AMC1301-Q1 device (see Figure 3-3). GNDi is completely floating in the high-voltage power line. R1, R2, R3, R4, R5, and R6 are the MELF resistors used for the potential divider. R7 is the shunt resistor for voltage measurement. Selecting R7 heavily depends on the input measurement range of the AMC1301-Q1 device (250 mV) and voltage range of the battery.

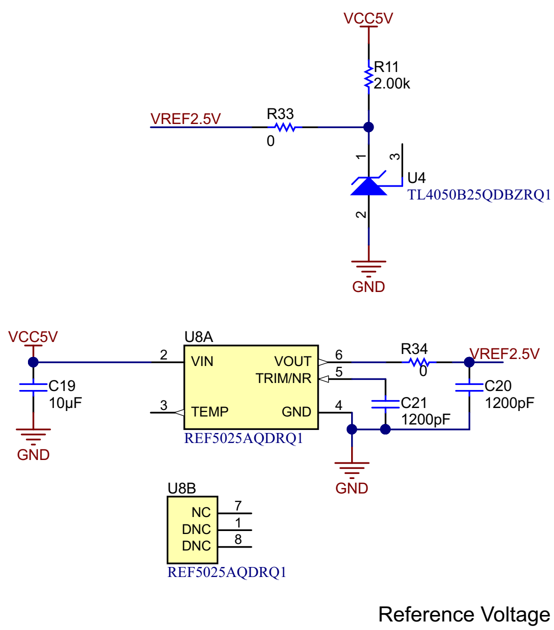


Figure 3-3. Reference Voltage (V_{REF} = 2.5 V)

VREF2.5V is generated by using the TL4050-Q1 or REF5025-Q1. R33 and R34 are the population variants for choosing the reference voltage. TL4050-Q1 is the typical choice for the reference voltage to support the isolation leakage current measurements.

Hardware with Solid-State Relay

Solid-State Relays used to replace EMRs in leakage current measurement.

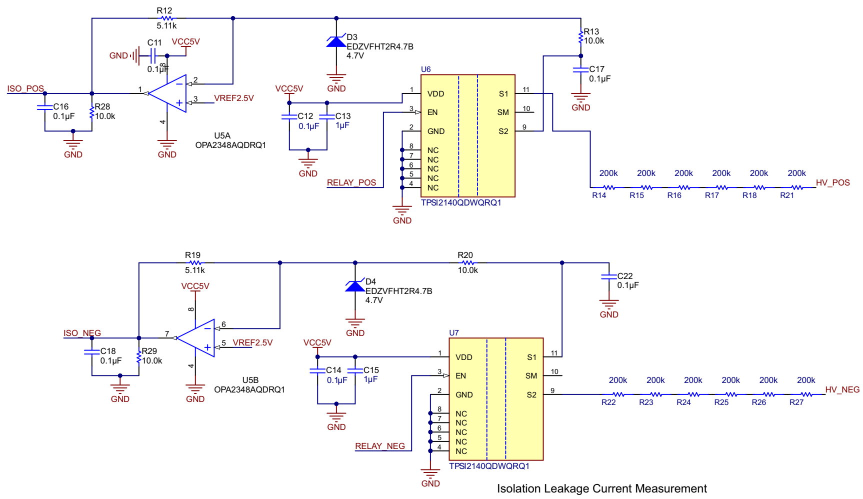


Figure 3-4. SSR Isolation Test Schematic

3.2 Testing and Results

Solid-State Relay test results are shown below original design testing see Solid-State Relay Isolation Tests

Measuring system isolation is possible by breaking the isolation internal to this reference design. For this task, build a load card to simulate the isolation error in the system. This card typically consists of various high-voltage resistors and switches to simulate different error conditions (see Figure 3-5).

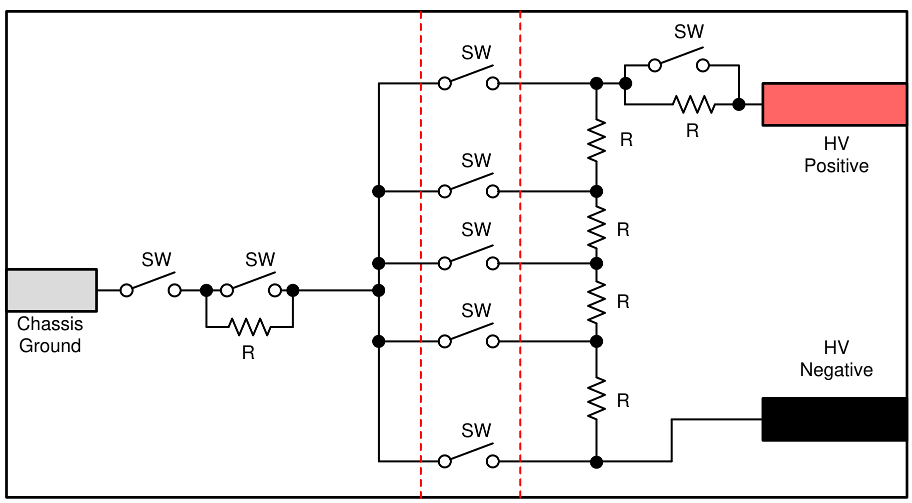


Figure 3-5. TIDA-01513 Isolation Breakage Load Card

When building the isolation breakage load card, be sure to follow high-voltage class safety precautions and laboratory safety requirements. Choose the resistors (R) based on high battery voltage, power dissipation, and the testing targets of the system. Switches (SW) must withstand the open contact voltage and support proper insulation for handling the switches. Build the load card based on the resources available and number of tests planned. Users can also build the load card by using relays with external controls through a signal generator or software.

3.2.1 Test Setup

Be sure to take safety precautions as provided by a lab safety team when performing isolation breakage tests. The test setup must comply with regional safety norms. Connect the reference design to the load card, power supplies, and measurement equipment as shown in Figure 3-6. Use a signal generator to control the relays of the design board. If any one of the relays is closed, isolation is broken on the respective voltage divider (positive or negative potential divider) to support the isolation measurements. Set a constant low-voltage supply to 5 V as per the design. Use an oscilloscope to monitor the analog voltages of the reference design. As part of the measurements, some of the tests are done to calculate the errors. Use a 6½ digit multimeter (DMM) to support the same. Connect the high-voltage power supply to both the design and its load card. Perform measurements at different voltages and at multiple error points with variable resistance.

To measure isolation leakage currents, R1, R2, R3, R4, R5, and R6 of the design are not populated. R14, R15, R16, R17, and R18 are populated to have 1.2 MΩ. This same resistor chain is used for R21, R22, R23, R24, and R25 to maintain symmetry. 100-kΩ resistors are populated in the load card, which support as potential dividers from the high-voltage to low-voltage section.

Due to test facility limitations, some of the measurements are performed at low voltage and prorated data to high voltage. Functional behavior, isolation leakage currents for these tests are maintained intact with appropriate changes to resistors and power source.

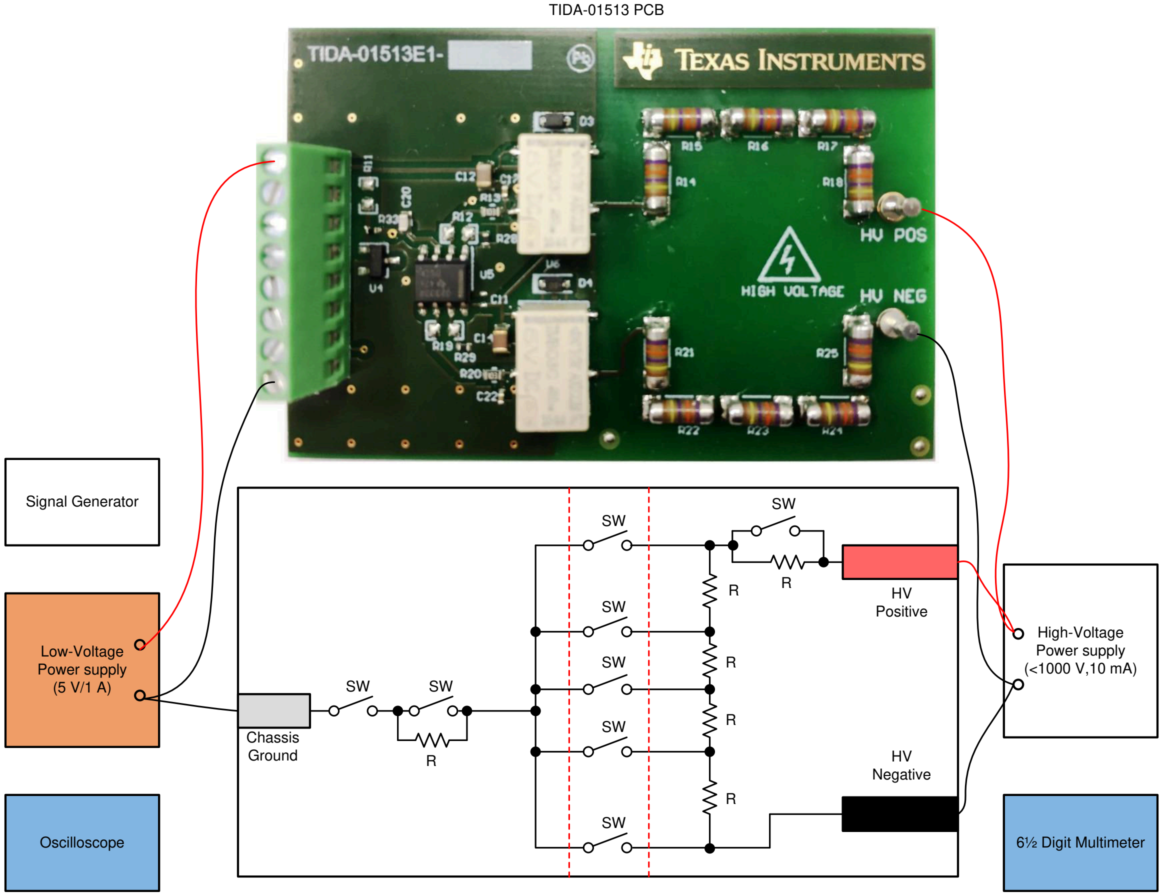
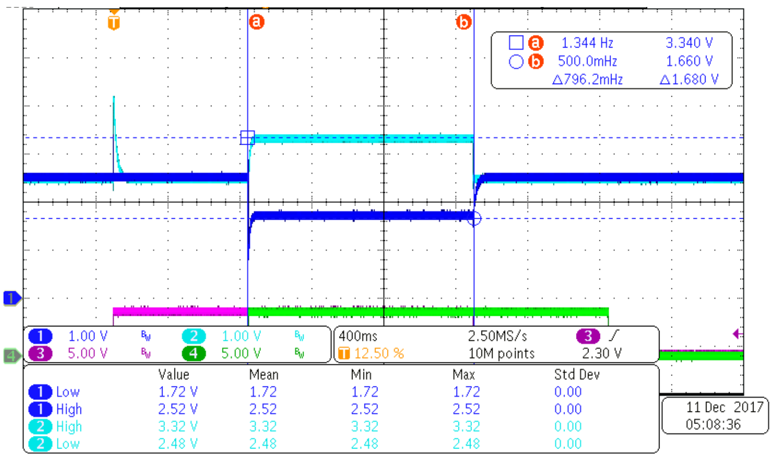


Figure 3-6. TIDA-01513 Test Setup

3.2.2 Isolation Tests

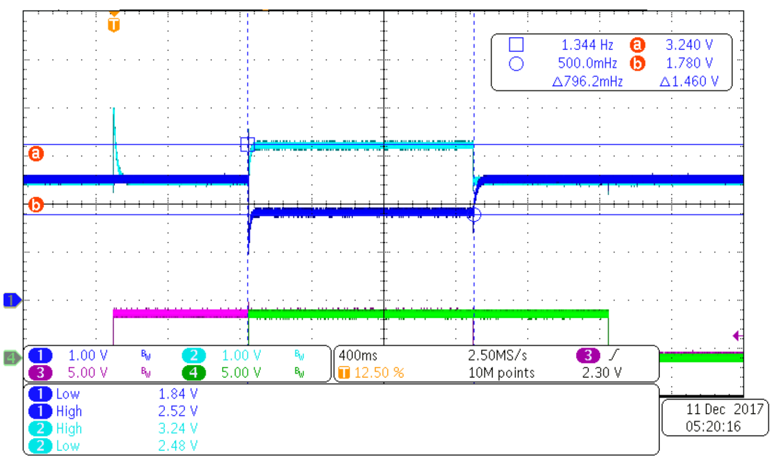
3.2.2.1 Normal Conditions

For normal condition tests, there are no connections to the load card. This reference design is connected with both high-voltage and low-voltage power supplies. The high battery voltage was varied to measure the performance of analog circuit.



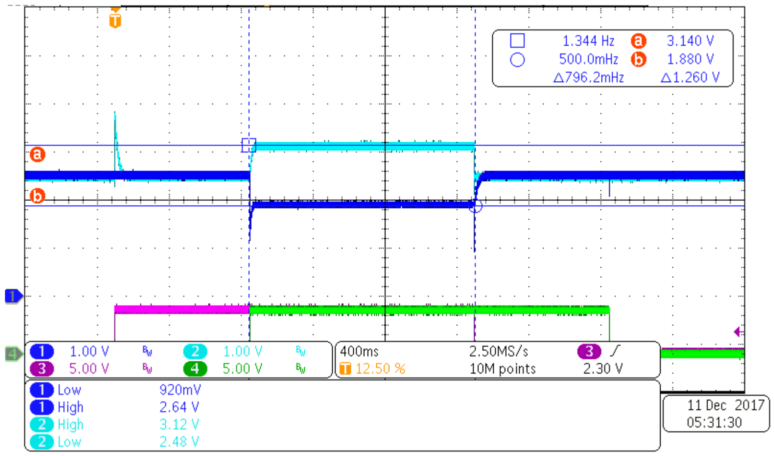
CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-7. Normal Conditions 400 V



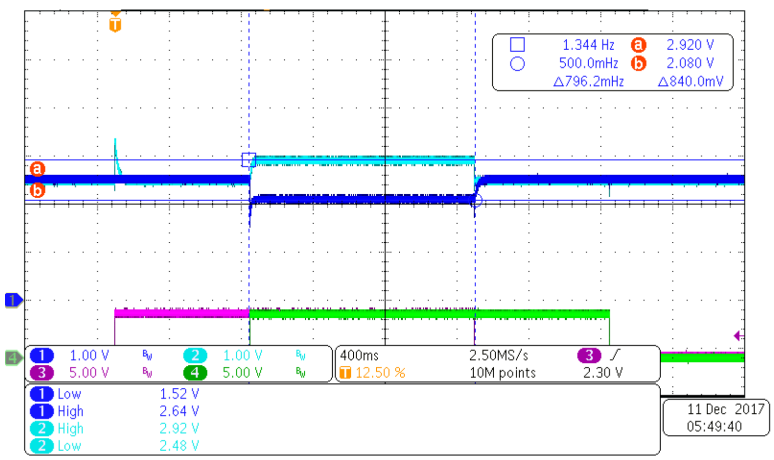
CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-8. Normal Conditions 350 V



CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-9. Normal Conditions 300 V



CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-10. Normal Conditions 200 V

Table 3-1 lists the voltage measurements at different points of the board.

Table 3-1. Measurements at Normal Condition

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100.006	2.505	2.295	2.714
150.008	2.504	2.19	2.819
200.003	2.504	2.086	2.923
250.004	2.504	1.982	3.027
300.004	2.504	1.878	3.131
350.004	2.504	1.774	3.235
400.006	2.504	1.669	3.34
450.007	2.504	1.565	3.444

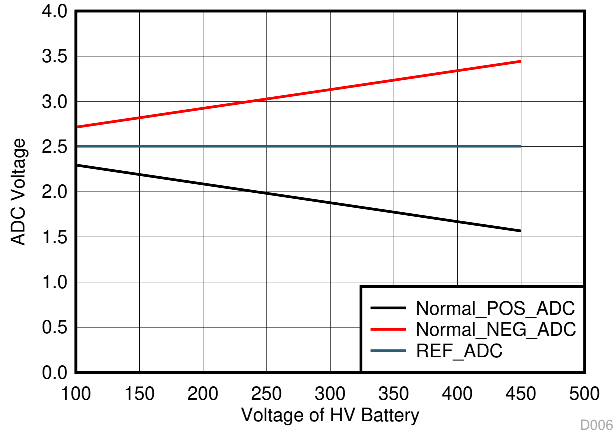
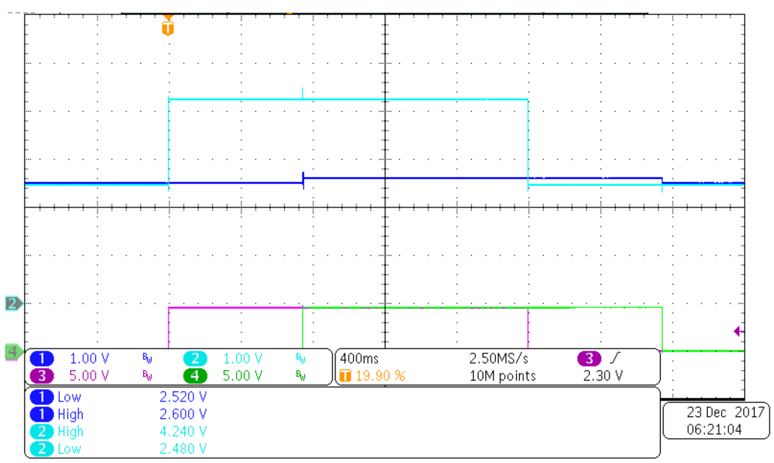


Figure 3-11. Behavior of Isolation Analog Outputs

3.2.2.2 Isolation Error at HV Positive

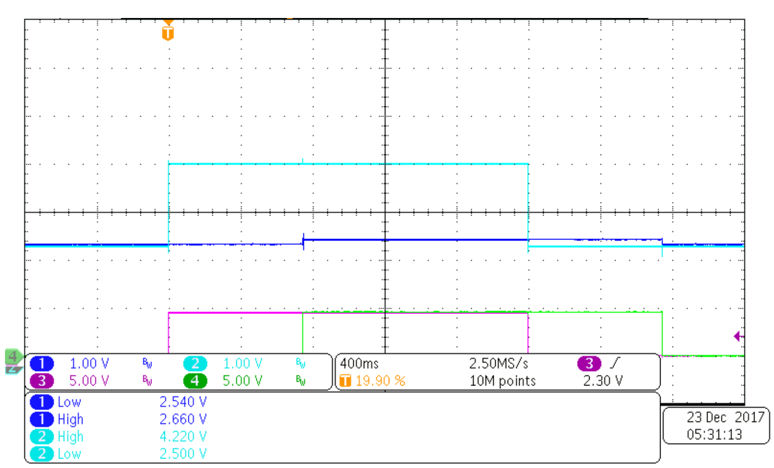
Simulate an isolation error condition by connecting the chassis ground line to HV positive. Change the switches on the load card appropriately to support the same. To understand the behavior of error conditions, the measurements were performed at different battery voltages.



No resistance from positive line to chassis ground

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-12. HV Positive Error 400 V at No Resistance



100-kΩ resistance from positive line to chassis ground

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-13. HV Positive Error 400 V at 100-kΩ Resistance

Table 3-2. Measurements at HV Positive Error

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	MEASURED PEAK ISO_POS VOLTAGE	MEASURED PEAK ISO_NEG VOLTAGE
100.006	2.505	2.606	3.027
150.008	2.504	2.606	3.236
200.003	2.504	2.608	3.444
250.004	2.504	2.608	3.652
300.004	2.504	2.608	3.861
350.004	2.504	2.608	4.069
400.006	2.504	2.608	4.278
450.007	2.504	2.608	4.484

Figure 3-14 shows the deviations of HV POS and HV NEG ADC voltages from the normal conditions. HV POS is above the reference voltage when U6 (positive relay) is closed. This behavior is observable only when the HV positive line is low ohmic or short to chassis ground.

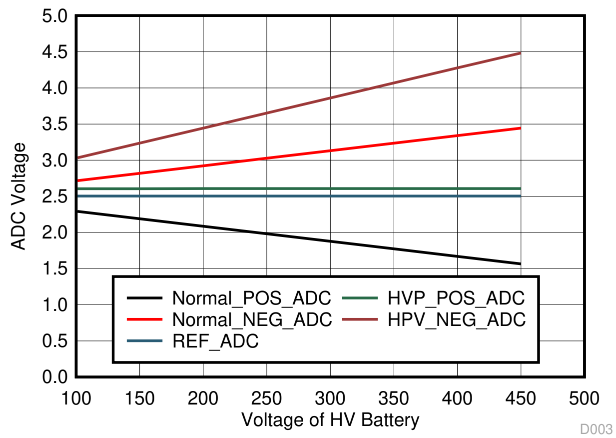
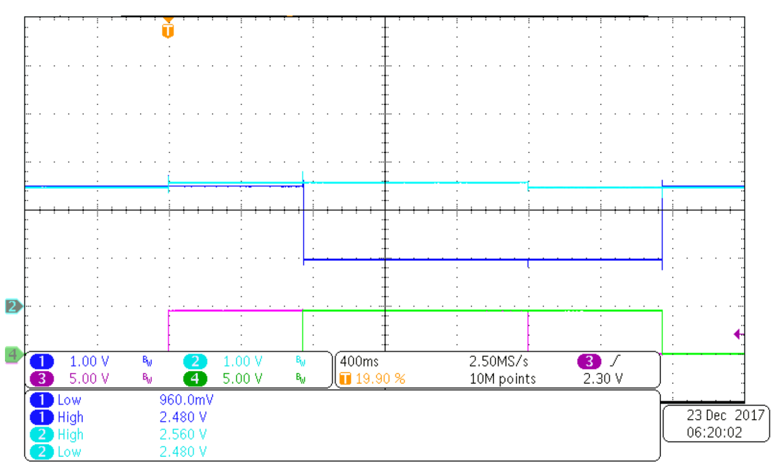


Figure 3-14. Behavior for HV Positive Isolation Error

3.2.2.3 Isolation Error at HV Negative

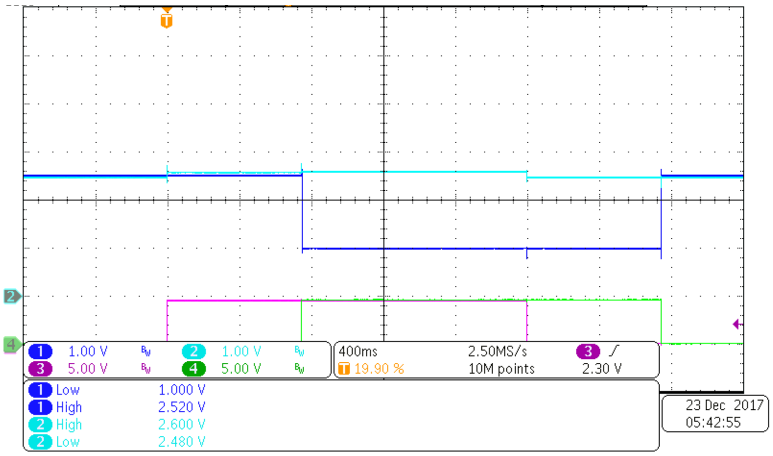
An error condition is created by connecting the HV negative line to chassis ground. To understand the behavior of error conditions, measurements were performed at different battery voltages.



No resistance from HV negative line to chassis ground

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-15. HV Negative Error 400 V at No Resistance



100-kΩ resistance from positive line to chassis ground

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-16. HV Negative Error 400 V at 100-kΩ Resistance

Table 3-3. Measurements at HV Negative Error

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	MEASURED PEAK ISO_POS VOLTAGE	MEASURED PEAK ISO_NEG VOLTAGE
100.006	2.505	2.191	2.61
150.008	2.504	1.982	2.61
200.003	2.504	1.774	2.61
250.004	2.504	1.565	2.61
300.004	2.504	1.357	2.61
350.004	2.504	1.148	2.61
400.006	2.504	0.939	2.61
450.007	2.504	0.731	2.61

Figure 3-17 shows the deviations of HV POS and HV NEG ADC voltages from the normal conditions. HV NEG ADC is slightly above the reference voltage and constant when U7 (negative relay) is closed. This behavior is observable only when the HV negative line is low ohmic or short to chassis ground.

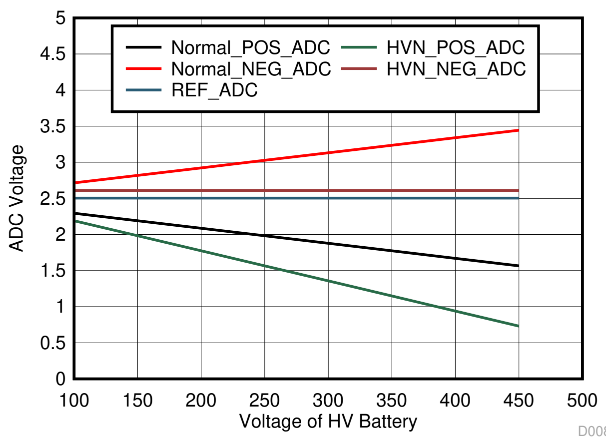
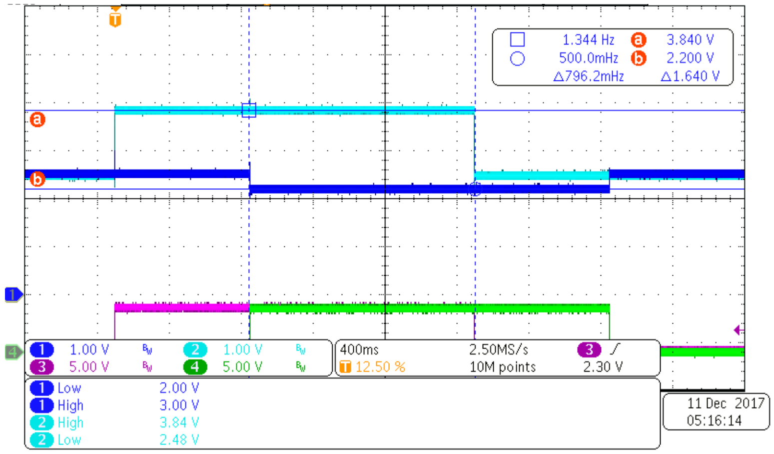


Figure 3-17. Behavior for HV Negative Isolation Error

3.2.2.4 Isolation Error at ¼ HV Battery Voltage

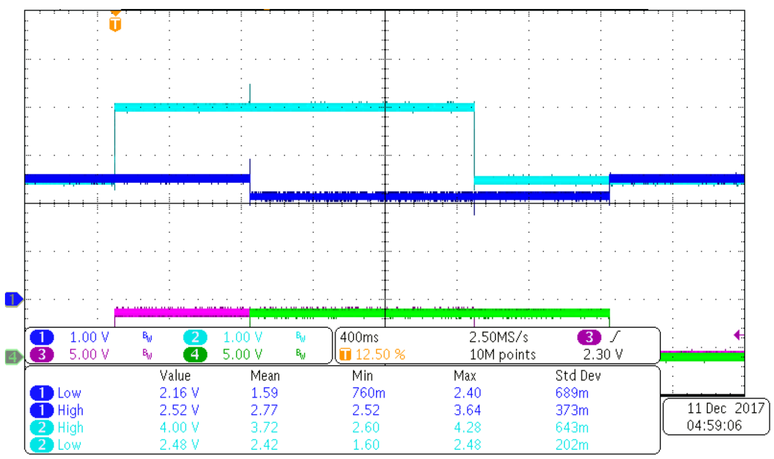
An error condition is created at ¼ HV battery voltage to chassis ground. To understand the behavior of error conditions, measurements were performed at different battery voltages.



Battery voltage = 400 V, isolation error = 100 V

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-18. Isolation Error at 100 V for 400-V Battery



Battery voltage = 450 V, isolation error = 112.5 V

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-19. Isolation Error at 112.5 V for 450-V Battery

Table 3-4. Measurements at ¼ HV Battery

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	MEASURED PEAK ISO_POS VOLTAGE	MEASURED PEAK ISO_NEG VOLTAGE
100.006	2.505	2.5	2.921
150.008	2.504	2.448	3.076
200.003	2.504	2.398	3.232
250.004	2.504	2.346	3.387
300.004	2.504	2.295	3.543
350.004	2.504	2.237	3.699
400.006	2.504	2.191	3.854
450.007	2.504	2.139	4.01

Figure 3-20 shows the deviations for POS ADC and NEG ADC voltages from normal conditions. POS and NEG are greater than expected and constant when relays are closed. This behavior resonates to an isolation error from the high-voltage section to chassis ground.

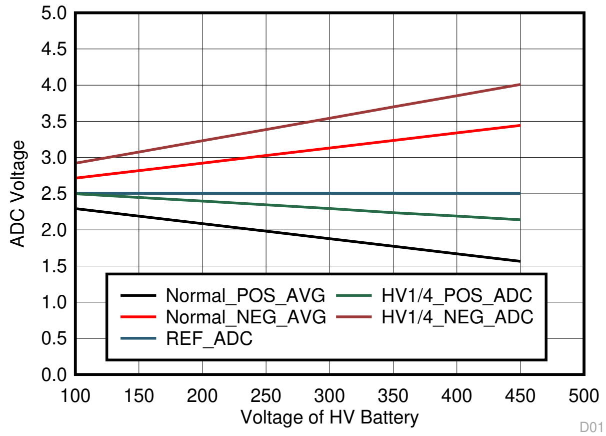
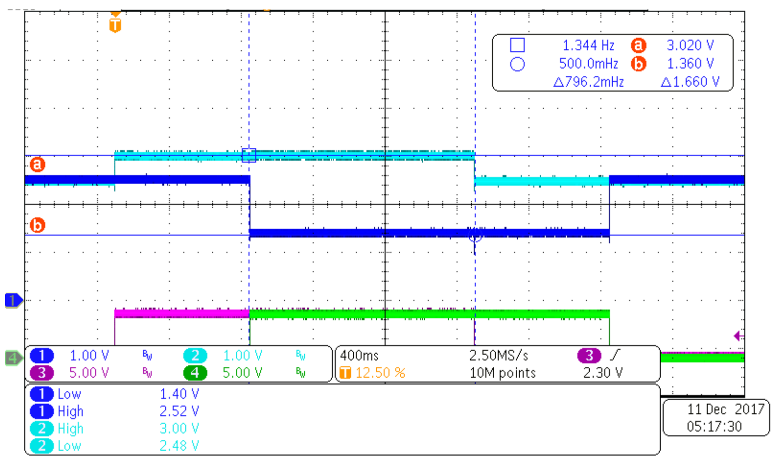


Figure 3-20. Behavior for Isolation Error at ¼ HV Battery

3.2.2.5 Isolation Error at ¾ HV Battery Voltage

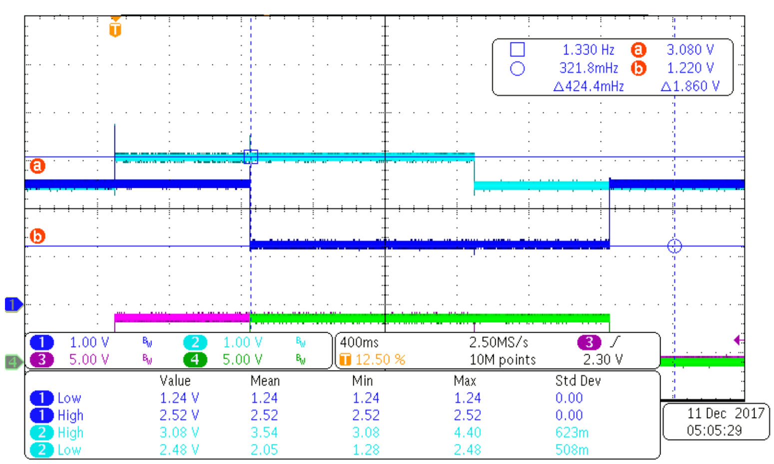
An error condition is created at ¾ HV battery voltage to chassis ground. To understand the behavior of error conditions, measurements were performed at different battery voltages.



Battery voltage = 400 V, isolation error = 300 V

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-21. Isolation Error at 300 V for 400-V Battery



Battery voltage = 450 V,
isolation error = 337.5 V

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-22. Isolation Error at 337.5 V for 450-V Battery

Table 3-5. Measurements at ¾ HV Battery

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	MEASURED PEAK ISO_POS VOLTAGE	MEASURED PEAK ISO_NEG VOLTAGE
100.006	2.505	2.294	2.715
150.008	2.504	2.139	2.767
200.003	2.504	1.984	2.82
250.004	2.504	1.828	2.873
300.004	2.504	1.672	2.925
350.004	2.504	1.526	2.978
400.006	2.504	1.362	3.031
450.007	2.504	1.206	3.084

Figure 3-23 shows the deviations for POS ADC and NEG ADC voltages from normal conditions. POS and NEG are less than expected and constant when relays are closed. This behavior resonates to an isolation error from the high-voltage section to chassis ground.

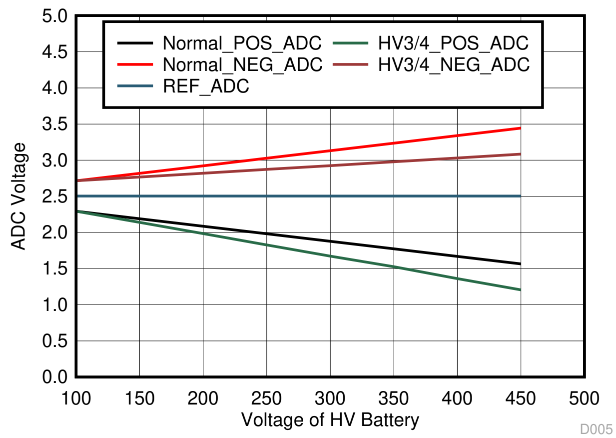
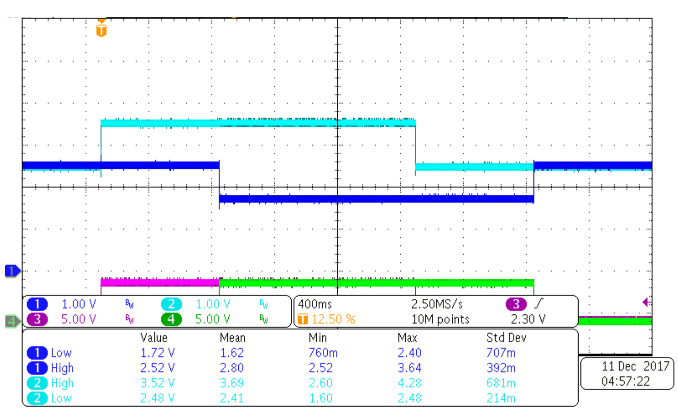


Figure 3-23. Behavior for Isolation Error at ¾ HV Battery

3.2.2.6 Isolation Error at the Middle of an HV Battery Voltage

An error condition is created at the middle of the HV battery voltage to chassis ground. To understand the behavior of error conditions, measurements were performed at different battery voltages.



Battery voltage = 450 V, isolation error = 225 V

CH1: ISO_POS
CH2: ISO_NEG
CH3: RELAY_NEG
CH4: RELAY_POS

Figure 3-24. Isolation Error at 225 V for 450-V Battery

Table 3-6. Measurements at Middle of HV Battery

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	MEASURED PEAK ISO_POS VOLTAGE	MEASURED PEAK ISO_NEG VOLTAGE
100.006	2.505	2.398	2.817
150.008	2.504	2.295	2.921
200.003	2.504	2.191	3.025
250.004	2.504	2.088	3.129
300.004	2.504	1.98	3.233
350.004	2.504	1.876	3.338
400.006	2.504	1.778	3.442
450.007	2.504	1.667	3.537

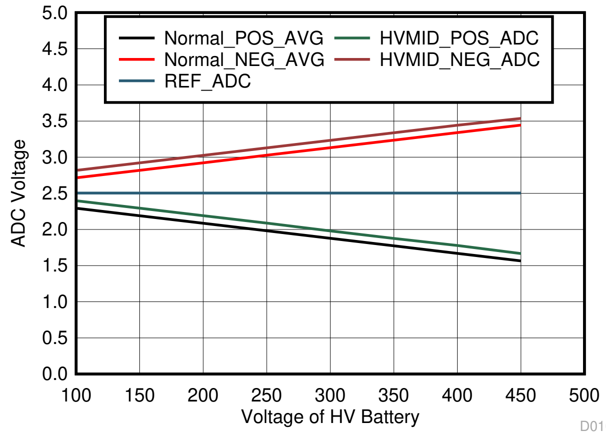


Figure 3-25. Behavior for Isolation Error at Middle of HV Battery

Figure 3-25 shows the deviations for POS ADC and NEG ADC voltages from normal conditions. POS and NEG are slight different and constant when relays are closed. This behavior resonates to an isolation error from the high-voltage section to chassis ground.

The circuit behavior changes when there is an isolation error. Figure 3-26 shows more information about the type of isolation errors and the impacts at different battery voltages.

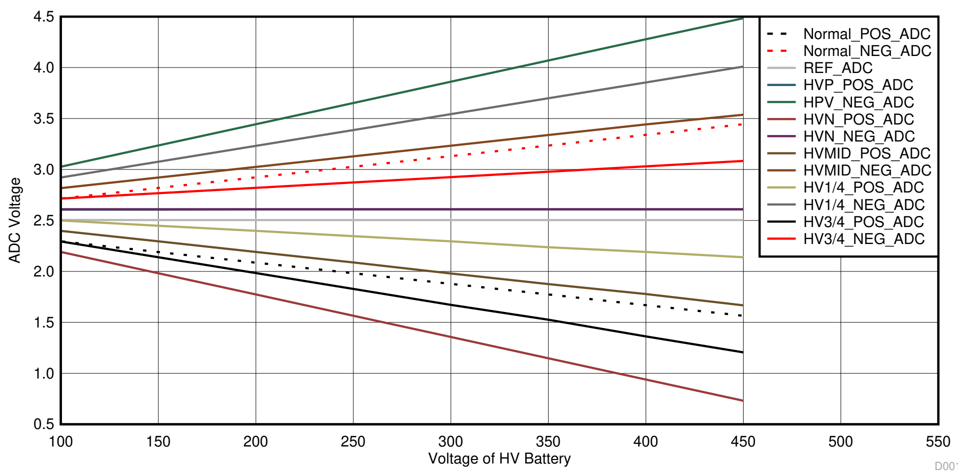


Figure 3-26. Behavior for Various Isolation Errors

3.2.3 Solid-State Relay Isolation Tests

Follows same testing procedure as previous isolation test, uses solid-state relay instead of EMR, tests performed from 100 V-400 V.

Testing Images: CH1:ISO_NEG, CH2:ISO_POS, CH3: RELAY_POS, CH4: RELAY_NEG

3.2.3.1 Normal Conditions

For normal condition tests, there is no isolation leakage. This reference design is connected with both high-voltage and low-voltage power supplies. The high battery voltage was varied to measure the performance of analog circuit.

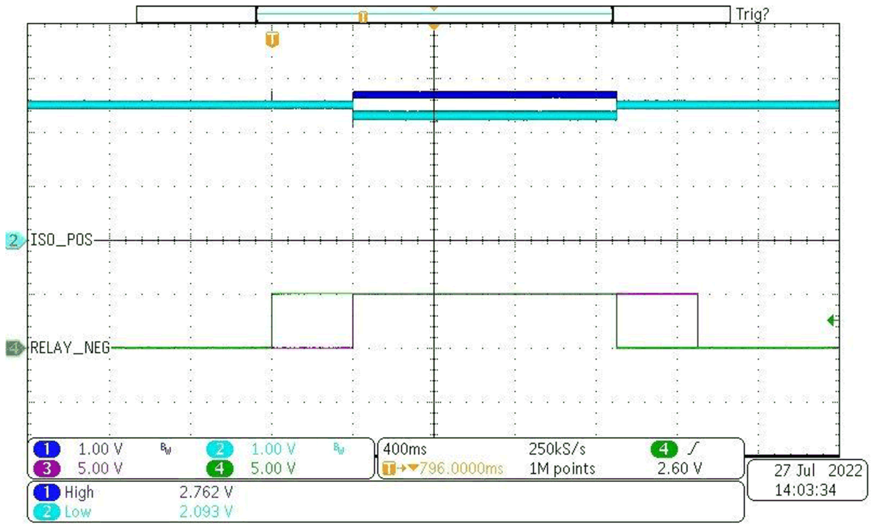


Figure 3-27. Normal Conditions 100V

Table 3-7. Measurements at Normal Condition

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.32	2.7456
200	2.499	2.109	2.9567
300	2.499	1.898	3.1676
400	2.499	1.687	3.3789

3.2.3.2 Isolation Error at HV Positive

Simulate an isolation error condition by connecting the chassis ground line to HV positive. To understand the behavior of error conditions, the measurements were performed at different battery voltages.

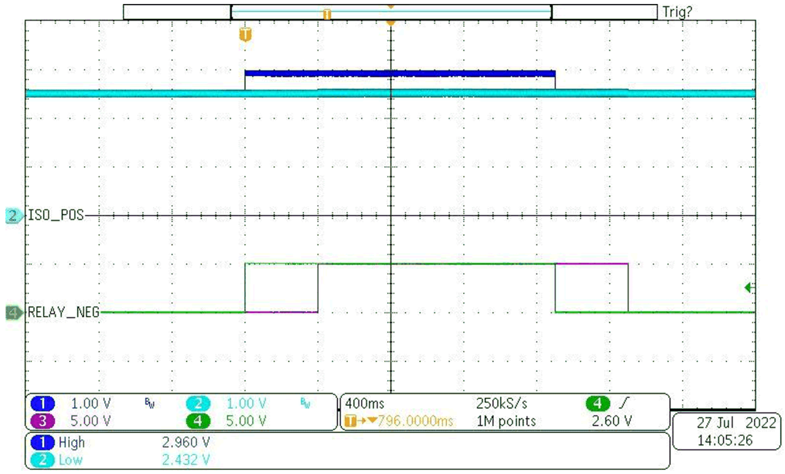


Figure 3-28. HV Positive Error 100 V at No Resistance

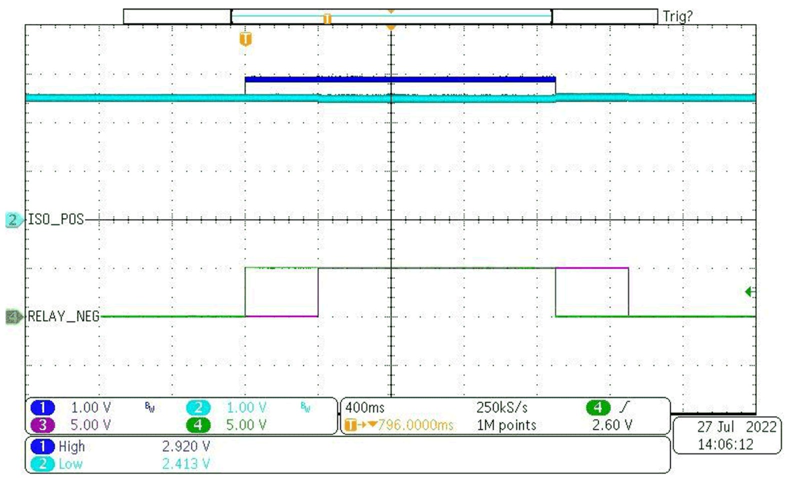


Figure 3-29. HV Positive Error 100 V at 100-kΩ Resistance

Table 3-8. Measurements at HV Positive Error of no resistance

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.542	2.9683
200	2.499	2.542	3.3904
300	2.499	2.542	3.8126
400	2.499	2.542	4.2352

Table 3-9. Measurements at HV Positive Error of 100-kΩ

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.511	2.9364
200	2.499	2.481	3.3284
300	2.499	2.45	3.7204
400	2.499	2.42	4.1128

3.2.3.3 Isolation Error at HV Negative

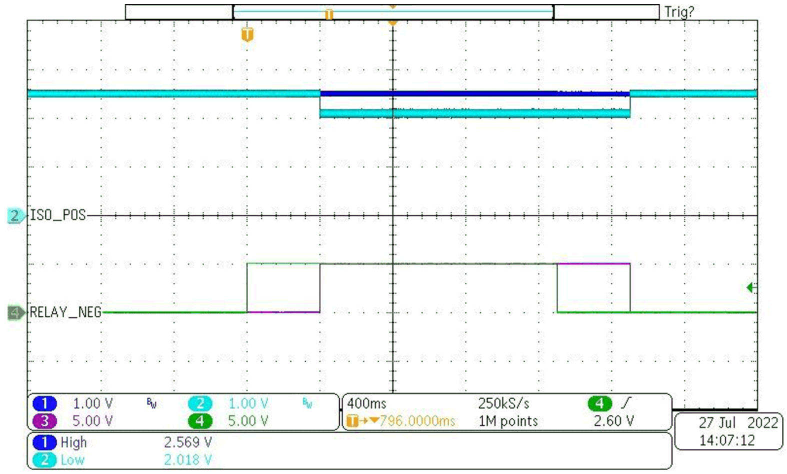


Figure 3-30. HV Negative Error 100 V at No Resistance

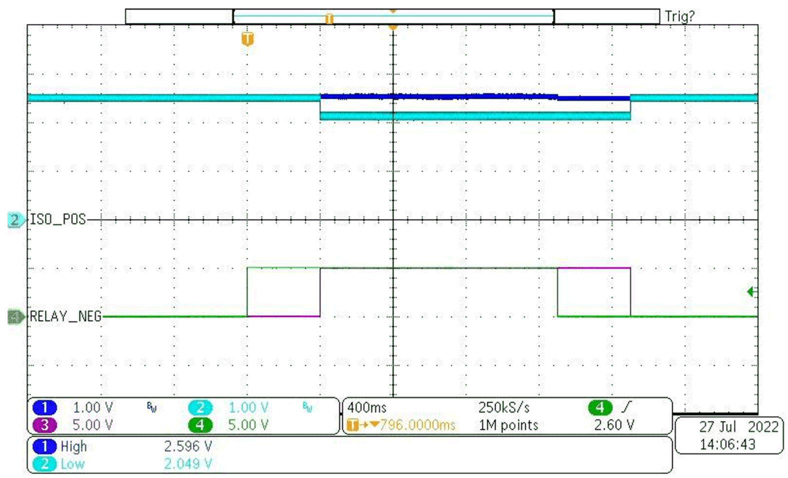


Figure 3-31. HV Negative Error 100 V at 100-kΩ Resistance

Table 3-10. Measurements at HV Negative Error of no Resistance

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.118	2.5438
200	2.499	1.696	2.5437
300	2.499	1.274	2.5438
400	2.499	0.852	2.5438

Table 3-11. Measurements at HV Negative Error of 100-kΩ

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.147	2.5736
200	2.499	1.755	2.6028
300	2.499	1.367	2.6327
400	2.499	0.971	2.6663

3.2.3.4 Isolation Error at ¼ HV Battery Voltage

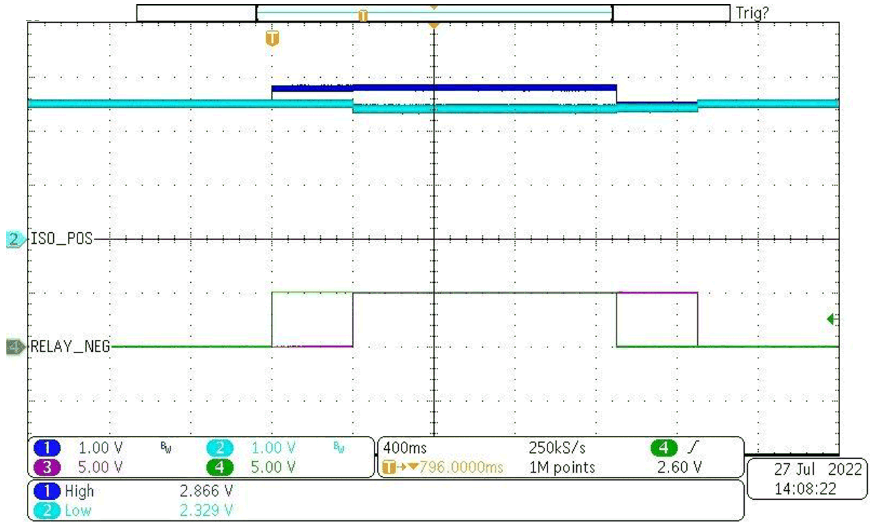


Figure 3-32. Isolation Error at 25 V for 100 V Battery

Table 3-12. Measurements at ¼ HV Battery Voltage

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.423	2.8493
200	2.499	2.306	3.1543
300	2.499	2.189	3.4592
400	2.499	2.072	3.7645

3.2.3.5 Isolation Error at ¾ HV Battery Voltage

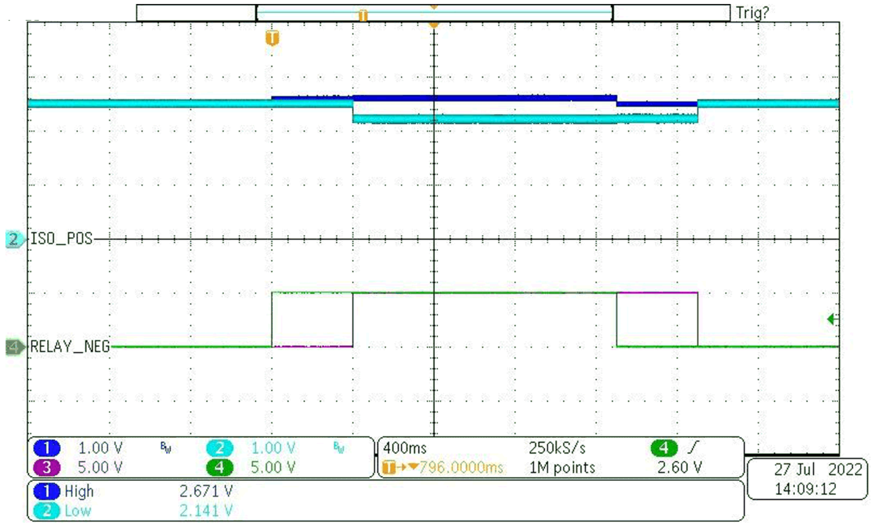


Figure 3-33. Isolation Error at 75 V for 100 V Battery

Table 3-13. Measurements at ¾ HV Battery Voltage

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.235	2.6604
200	2.499	2.101	2.9491
300	2.499	1.625	2.895
400	2.499	1.32	3.0125

3.2.3.6 Isolation Error at the Middle of an HV Battery Voltage

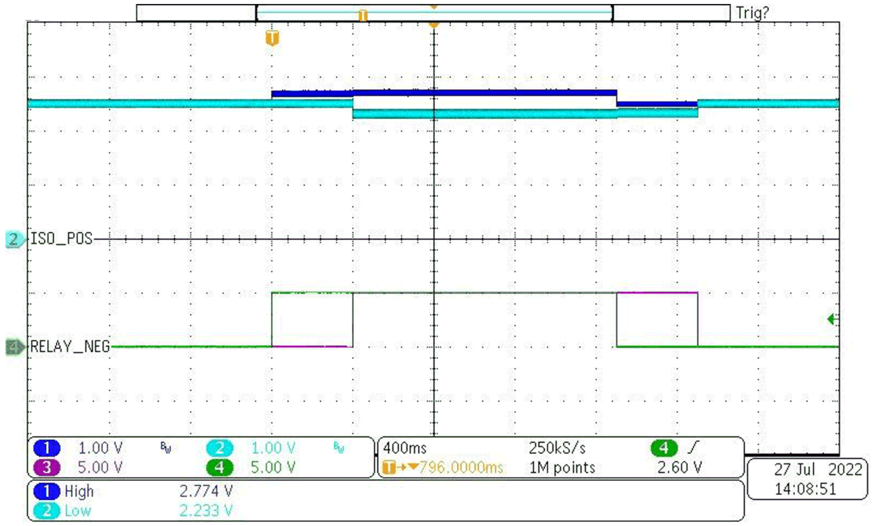


Figure 3-34. Isolation Error at 50 V for 100 V Battery

Table 3-14. Measurements at Middle of HV Battery Voltage

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	MEASURED REFERENCE VOLTAGE	PEAK ISO_POS VOLTAGE	PEAK ISO_NEG VOLTAGE
100	2.499	2.329	2.7545
200	2.499	2.118	2.9658
300	2.499	1.907	3.1768
400	2.499	1.696	3.883

3.2.4 High Voltage Measurements

High-voltage measurements are done by populating R1, R2, R3, R4, R5, and R6. The total resistance measured from HV POS to HV NEG is 801 kΩ; this result includes a shunt resistance of 488 Ω. The typical gain stage of the AMC1301-Q1 is 8.1517.

$$V_{ADC1} = V_{RDIV3} = -V_{PACK} \frac{(R_{ISON}||(R_{DIV3} + R_{DIV4}))}{(R_{ISON}||(R_{DIV3} + R_{DIV4})) + R_{ISOP})} \times \frac{R_{DIV3}}{R_{DIV3} + R_{DIV4}} \quad (6)$$

$$\text{Expected output OPA320} = \left(\frac{HV\_BATT \times Rsh}{Rsx} \pm offset\_AMC1301Q1 \right) \times Gain\_AMC1301 \times Gain\_OPA320 \quad (7)$$

Table 3-15. High-Voltage Measurements

HV BATTERY VOLTAGE (SUPPLIED AND MEASURED)	EXPECTED OUTPUT OF OPA320-Q1	MEASURED OUTPUT OF OPA320-Q1	ERROR (%)
99.98	0.9947	0.9885	0.624
149.99	1.4926	1.4856	0.473
200.003	1.9905	1.9825	0.403
250	2.4884	2.4795	0.361
300	2.9863	2.9762	0.340
350	3.4842	3.473	0.322
400	3.9820	3.97	0.303
450	4.4799	4.4668	0.293
500	4.9777	4.948	0.598

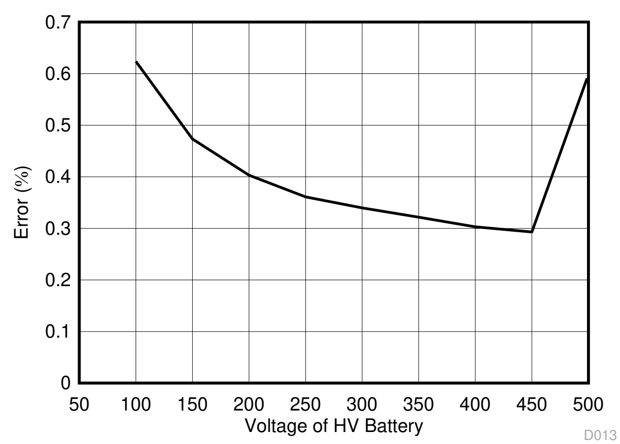


Figure 3-35. Behavior for Isolation Error at Middle of HV Battery

Multiple factors influence the calculations of high voltage. MELF resistors tolerance, bias currents, and offset voltages of analog components are important sources for the error. Consider the same for lifetime error calculations and design accordingly. MELF resistors must be chosen for low drift in resistance for temperature and aging factors.

3.2.5 Isolation Measurement Analysis

Figure 3-36 remains true if there are no capacitors between high-voltage lines to chassis ground.

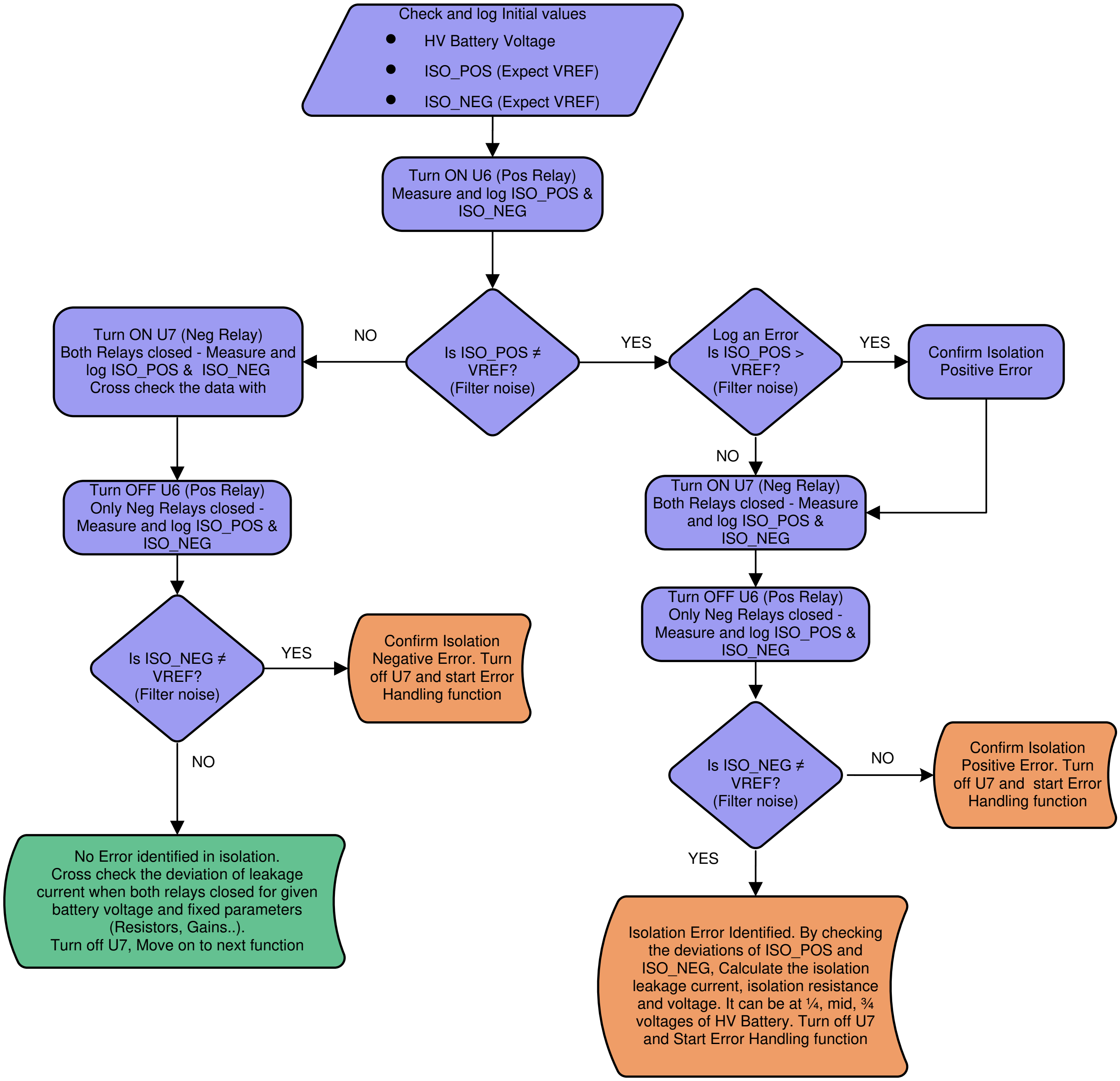


Figure 3-36. Flow Chart of Isolation Leakage Detection

By using Figure 3-36, the designer can identify the type of isolation error in the HEV or EV system. First, identify the isolation error. To classify the severity of the error, perform an analysis to implement the prevention mechanisms. Calculating the isolation leakage current can be complex if using capacitors from high-voltage lines to the chassis ground, which is a step to improve the electromagnetic compatibility (EMC) of the system. Maintain the look-up table or equations for the expected isolation voltages and leakage currents, which change to temperature. Highly precise analog components must be used for measurement circuits to identify and analyze isolation errors.

3.2.6 Error Analysis

Isolation error analysis is done based on the requirements from original equipment manufacturers (OEMs), safety goals, and algorithms. This design guide is limited in analyzing the circuit and explaining the error calculations. The error handling part is left to the manufacturers.

The following measurements were taken with this reference design at various high voltages and under different error conditions:

- Feedback resistor R9, R12 = 5 kΩ
- Series resistance (Pin 3 of relay to input of POS/NEG op amp) = 10 kΩ
- Series resistance (Pin 5 of relay to input of HV POS/HV NEG) = 1.18 MΩ
- Reference voltage (VREF2.5V) = 2.504 V
- C17 and C22 are not populated

Table 3-16. Isolation Error Analysis

HIGH VOLTAGE	CALCULATED / EXPECTED			MEASURED			ACCURACY		
	ISO_POS (V)	ISO_NEG (V)	LEAKAGE CURRENT (mA)	ISO_POS (V)	ISO_NEG (V)	LEAKAGE CURRENT (mA)	ISO_POS (%)	ISO_NEG (%)	LEAKAGE CURRENT (%)
100.006	2.293	2.714	0.042	2.295	2.714	0.0419	-0.087	0.000	0.238
150.008	2.188	2.819	0.063	2.19	2.819	0.0629	-0.091	0.000	0.159
200.003	2.083	2.924	0.084	2.086	2.923	0.0837	-0.144	0.034	0.357
250.004	1.978	3.029	0.105	1.982	3.027	0.104	-0.202	0.066	0.476
300.004	1.873	3.134	0.126	1.878	3.131	0.125	-0.267	0.096	0.556
350.004	1.768	3.239	0.147	1.774	3.235	0.146	-0.339	0.123	0.612
400.006	1.663	3.344	0.168	1.669	3.34	0.167	-0.361	0.120	0.536
450.007	1.558	3.449	0.189	1.565	3.444	0.1879	-0.449	0.145	0.582

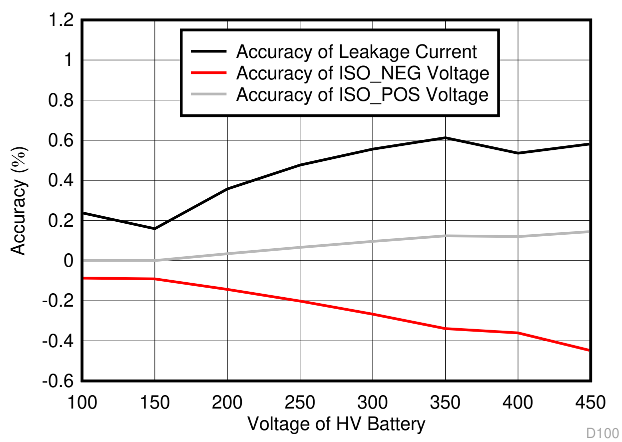


Figure 3-37. Accuracy of Isolation Measurements

As per Figure 3-36 and measurements, the isolation leakage identification is quite straightforward with the isolation error at HV positive or HV negative. Complexity arises when an isolation error is in between the high-voltage positive and negative lines. For the sake of testing this reference design, a potential divider load card is used for isolation error in between battery voltages. The performance of the results shown for these tests may differ to the actual tests for the middle-voltage isolation error, which is one of the less probable errors. The following analysis in Figure 3-38 helps to find the leakage current if there is an isolation error in the middle of the battery.

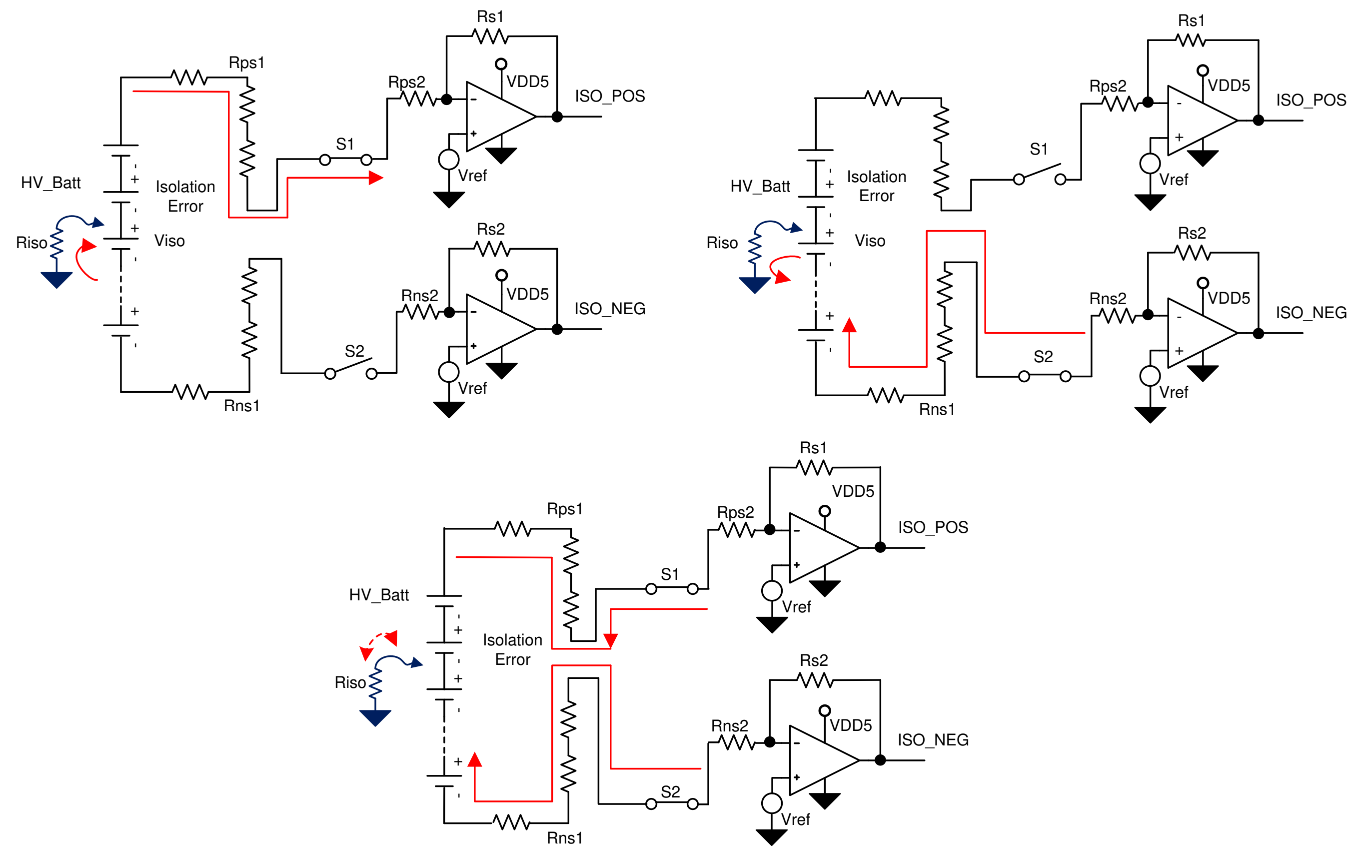


Figure 3-38. Isolation Error at Middle of Battery

Isolation resistance (Riso) and isolation voltage (Viso) can be calculated easily by using the voltages measured before and after closing the switches S1 and S2. Leakage current can be calculated with both isolation error voltage and resistance. When only S1 is closed, the HV_Batt - Vref - Viso voltage is confirmed to be across resistors Riso , Rps1, and Rps2 (neglect bias currents); leakage current can be measured from ISO_POS. When only S2 is closed, the Viso-Vref voltage is confirmed to be across Rns1, Rns2, and Riso, which can be measured from ISO_NEG. By design, resistors Rps1 and Rps2 are the same as Rns1 and Rns2. By using both equations, Riso and Viso can be calculated easily.

In summary, this reference provides a flow chart to monitor the isolation leakage from high voltage to chassis grounds in HEV and EV motors. If the error condition is identified, equations provided in this design guide support the diagnoses of the isolation voltage, isolation resistance, and isolation leakage currents.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01513.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01513.

4.3 PCB Layout Recommendations

The PCB layout for isolation leakage current measurements must be based on the requirements and components selected for the design.

- The high-voltage section of the system must not have any polygons to HV positive, HV negative, or chassis ground.
- Place MELF resistors in series or a series parallel combination that maintains the isolation and does not allow any low-ohmic paths due to PCB, humidity, or liquids, which are all probable occurrences on the PCB.

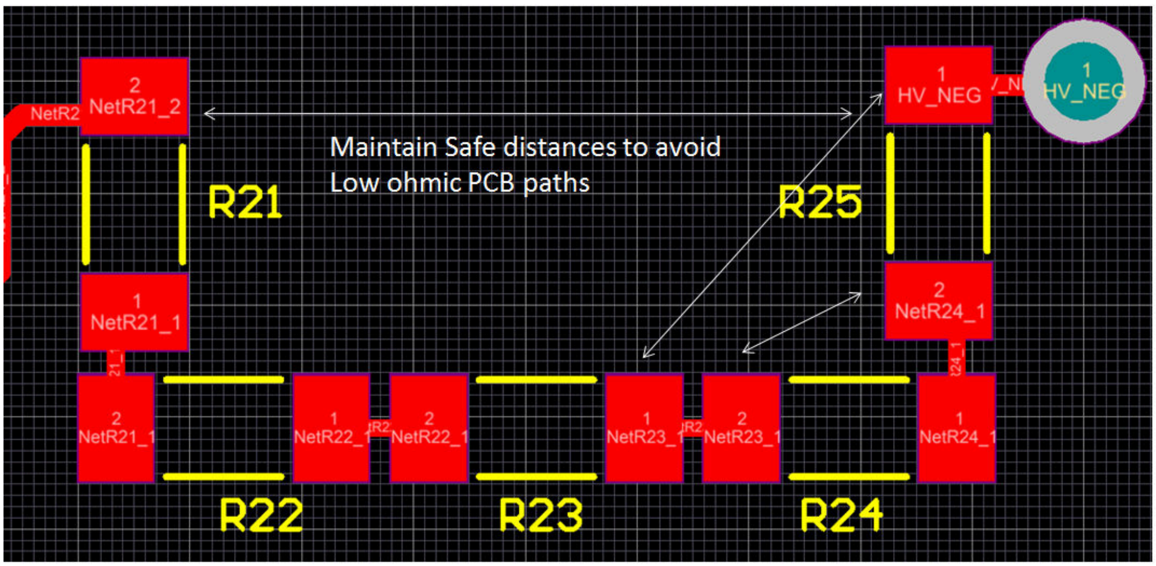


Figure 4-1. Placing MELF Resistors

- Maintain creepage and clearance distances required for isolation components (AMC1301-Q1) as explained in the device data sheet.
- To minimize noise, take care when placing analog lines to avoid noise from relays and power switching components.
- Follow the component data sheet to minimize the EMC issues on layout.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01513.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01513.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01513.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01513.

5 Software Files

To download the software files, see the design files at TIDA-01513.

6 Related Documentation

1. Texas Instruments, *TI Precision Labs - Op Amps TI Training*
2. Texas Instruments, *High-voltage isolation quality and reliability for AMC130x Marketing White Paper*
3. Texas Instruments, *High-voltage reinforced isolation: Definitions and test methodologies Marketing White Paper*

7 Trademarks

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8 Revision History

Changes from Revision A (August 2022) to Revision B (January 2023) **Page**

Changes from Revision * (April 2018) to Revision A (August 2022) **Page**

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