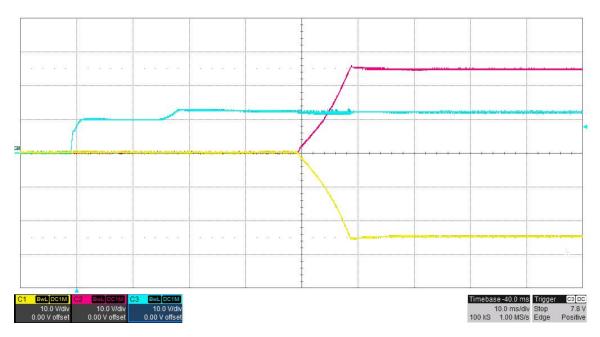


1 Startup

The photo below shows the output voltage startup waveform after the application of 12V in. The +25V/-25V outputs were loaded to 0.01A. (10V/DIV, 10mS/DIV)



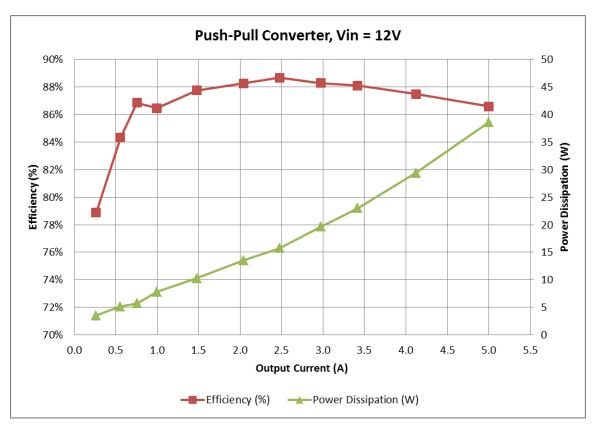
The photo below shows the output voltage startup waveform after the application of 12V in. The +25V/-25V outputs were loaded differentially with 10 ohms (5A). (10V/DIV, 10mS/DIV)

				-				
					/			
			 	/				
				-				
1 BwL DC1M 10.0 V/div 0.00 V offse	v 10.0 V/div	C3 BwL DC1M 10.0 V/div 0.00 V offset				1	Timebase -40.0 ms 10.0 ms/div 100 kS 1.00 MS/s	Stop 7



2 Efficiency

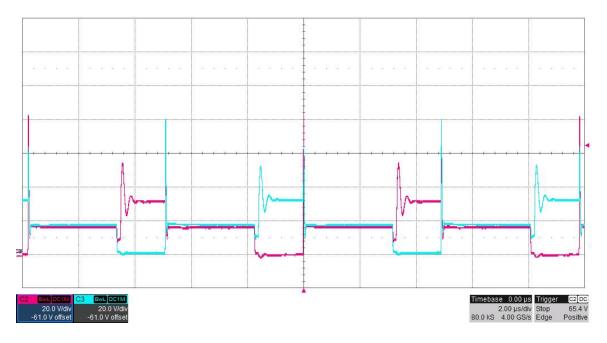
The converter efficiency and power dissipation is shown below for Vin = 12V.



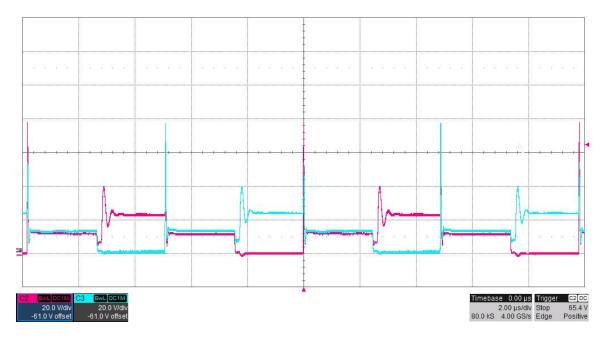


3 Switch Node Waveforms

The photo below shows the FET switching voltages for an input voltage of 16V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 2uS/DIV)

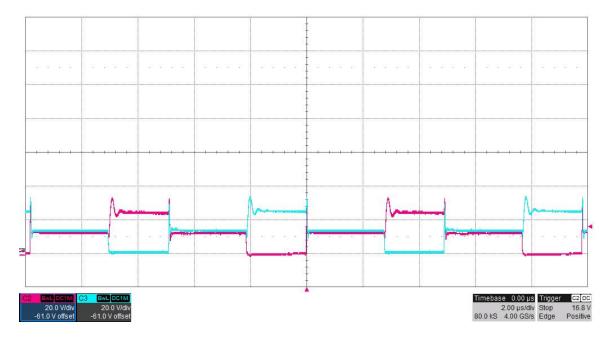


The photo below shows the FET switching voltages for an input voltage of 12V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 2uS/DIV)

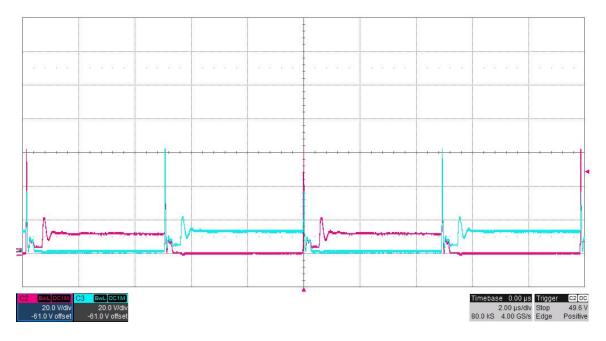




The photo below shows the FET switching voltages for an input voltage of 12V. The outputs were loaded differentially with 50 ohms (1A). (20V/DIV, 2uS/DIV)



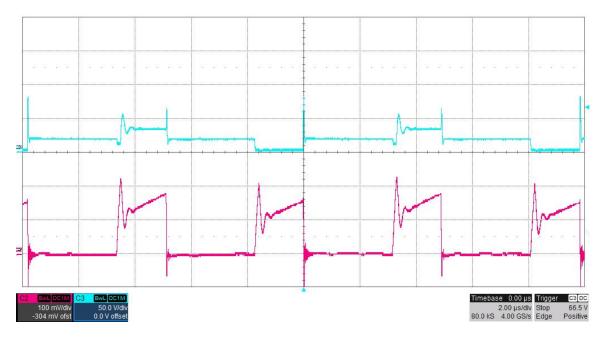
The photo below shows the FET switching voltages for an input voltage of 6V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 2uS/DIV)



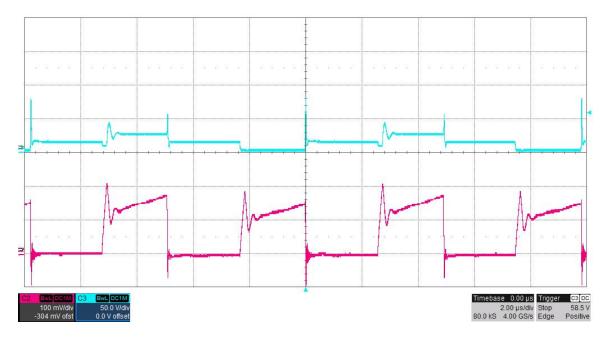


4 Current Sense resistor (R7) pin Waveforms

The photo below shows the FET switching voltage and the voltage across R7 for an input voltage of 16V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

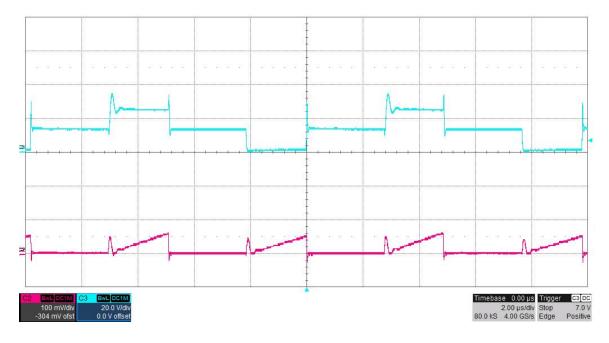


The photo below shows the FET switching voltage and the voltage across R7 for an input voltage of 12V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

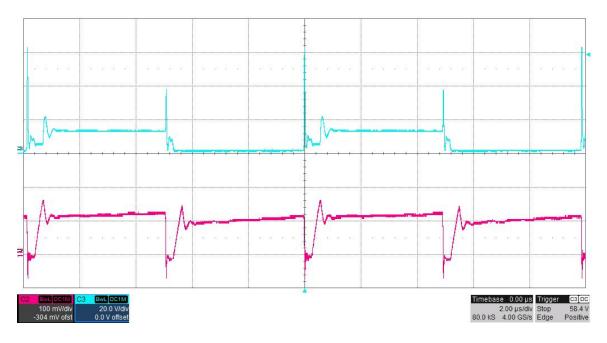




The photo below shows the FET switching voltage and the voltage across R7 for an input voltage of 12V. The outputs were loaded differentially with 50 ohms (1A). (20V/DIV, 100mV/DIV, 2uS/DIV)



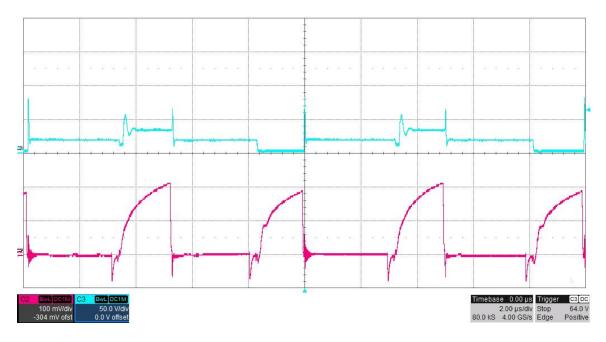
The photo below shows the FET switching voltage and the voltage across R7 for an input voltage of 6V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 100mV/DIV, 2uS/DIV)



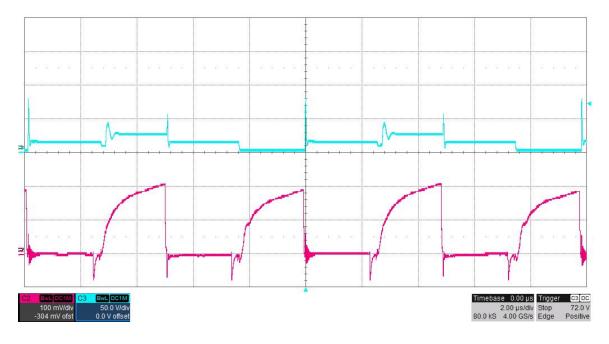


5 CS pin Waveforms

The photo below shows the FET switching voltage and the controller CS pin voltage for an input voltage of 16V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

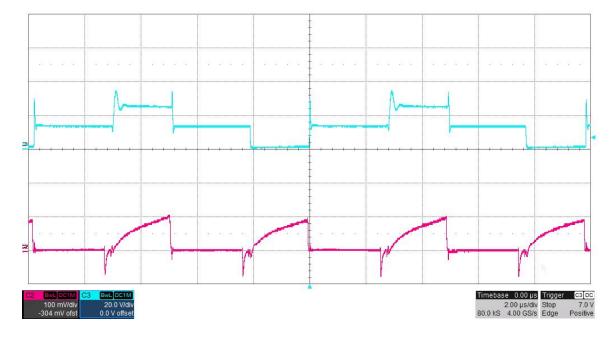


The photo below shows the FET switching voltage and the controller CS pin voltage for an input voltage of 12V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

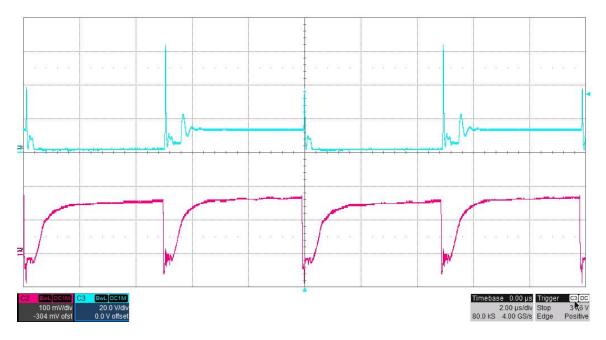




The photo below shows the FET switching voltage and the controller CS pin voltage for an input voltage of 12V. The outputs were loaded differentially with 50 ohms (1A). (20V/DIV, 100mV/DIV, 2uS/DIV)



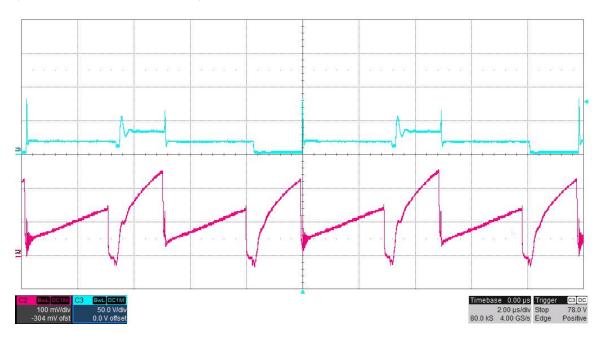
The photo below shows the FET switching voltage and the controller CS pin voltage for an input voltage of 6V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 100mV/DIV, 2uS/DIV)



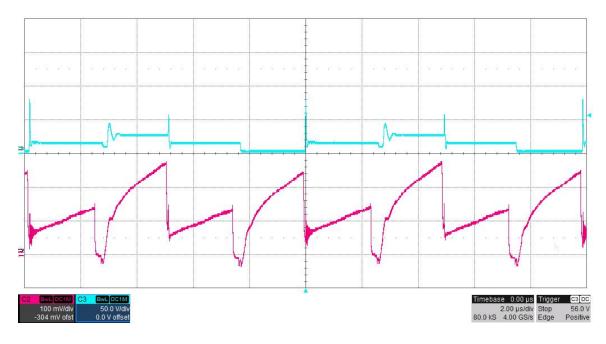


6 RAMP pin Waveforms

The photo below shows the FET switching voltage and the controller RAMP pin voltage for an input voltage of 16V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

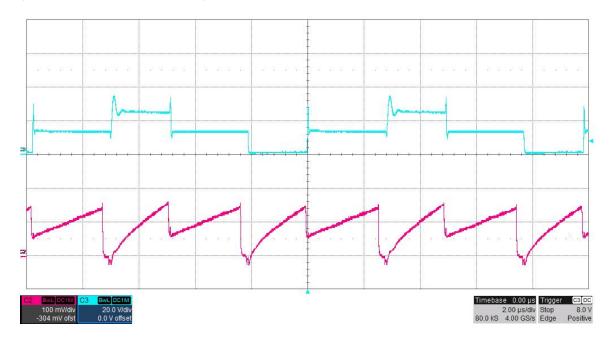


The photo below shows the FET switching voltage and the controller RAMP pin voltage for an input voltage of 12V. The outputs were loaded differentially with 10 ohms (5A). (50V/DIV, 100mV/DIV, 2uS/DIV)

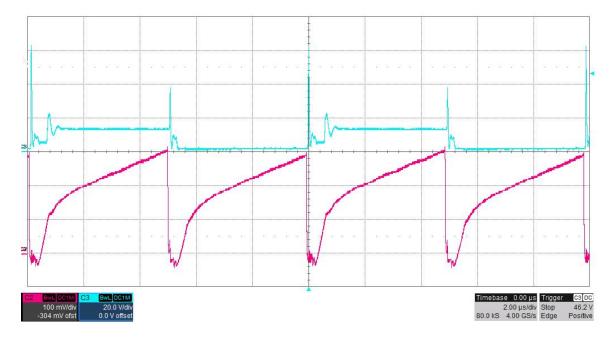




The photo below shows the FET switching voltage and the controller RAMP pin voltage for an input voltage of 12V. The outputs were loaded differentially with 50 ohms (1A). (20V/DIV, 100mV/DIV, 2uS/DIV)



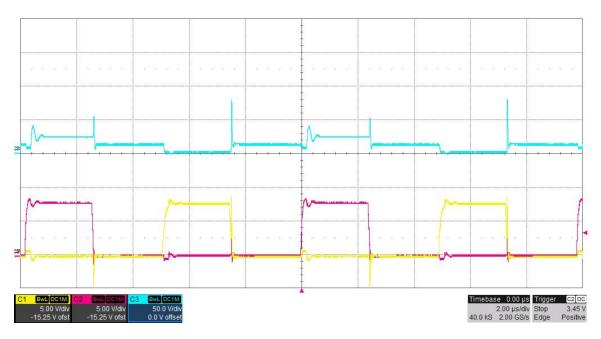
The photo below shows the FET switching voltage and the controller RAMP pin voltage for an input voltage of 6V. The outputs were loaded differentially with 10 ohms (5A). (20V/DIV, 100mV/DIV, 2uS/DIV)



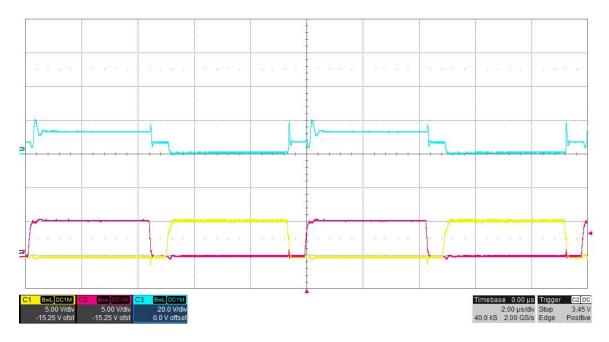


7 Gate drive Waveforms

The photo below shows the FET switching voltage and the OUTA and OUTB FET gate driver voltages for an input voltage of 12V. The outputs were loaded differentially with 10 ohms (5A). (5V/DIV, 2uS/DIV)



The photo below shows the FET switching voltage and the OUTA and OUTB FET gate driver voltages for an input voltage of 6V. The outputs were loaded differentially with 10 ohms (1A). (5V/DIV, 2uS/DIV)





8 Photo

The photo below shows the PMP11186 REVB assembly modified with the G154054ALF transformer and snubber clamp resistors R8, R9 removed.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https://www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2021, Texas Instruments Incorporated