TI Designs: TIDA-01630

High EMC Immunity RS485 Interface Reference Design for Tamagawa Encoders

Description

EMC immunity, especially immunity against inverter switching noise, is important for positioning encoder feedback systems of industrial drives. This design demonstrates a high EMC immunity RS485 transceiver solution which can be used on both the drive and encoder, such as Tamagawa™, EnDat 2.2, BiSS®, and so forth. The design supports a wide input voltage of 5 V. A connector with 3.3-V logic I/O signals and a 3.3-V power supply allows direct interface with the host processor to run the master protocol and power the processor. To meet the supply range of the selected encoder, the design offers an output voltage to the encoder equal to the Vin. This design's power supply offers protection against overvoltage and short circuit, according to the selected encoder's voltage range, to prevent damage during a cable short. The design has been tested for up to a 50-m cable length with the Tamagawa encoder.

Resources

TIDA-01630	Design Folder
THVD1550	Product Folder
SN74LVC2T45	Product Folder
TPS62162	Product Folder
TPS61240	Product Folder
TPS22810	Product Folder
Launchxl-f28379d	Tool Folder

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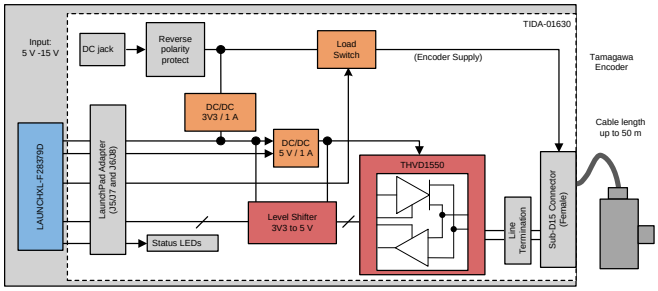
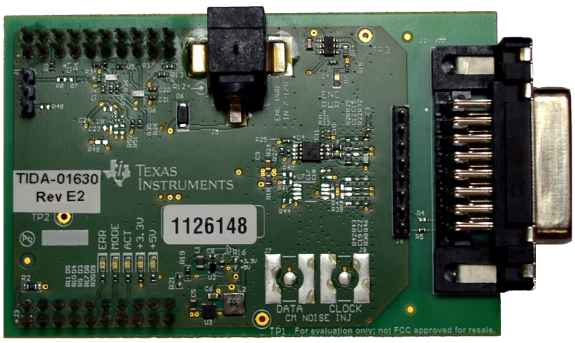
Features

- 5-V half-duplex RS485 transceiver with up to 50-Mbps baud rate and improved EMC immunity against IEC61000-4-4
- Hardware supports 2-wire interfaces standards, such as Tamagawa, or 4-wire RS485 interface standards, such as EnDat2.2 and BiSS
- 5-V supply half-duplex RS485 transceiver THVD1550 with 16-kV IEC-ESD and 4-kV EFT eliminates cost for external ESD components.
- Highest immunity against IEC61000-4-4 fast electrical transients versus other industry standard RS485 transceivers, validated in system tests
- Designed to meet IEC61800-3 EMC immunity for variable-speed drives without the need for additional protection devices, such as TVS diodes, when used in applications with encoders using shielded cables
- The design is in BoosterPack™ plug-in module form factor, with a connector compatible to the TI LaunchPad™ Development Kit for easy evaluation of Tamagawa with a C2000™ MCU

Applications

- Servo CNC and Robotics
- AC Inverter and VF Drives
- Position Sensor (Encoders)
- Industrial Robots





1 System Description

Absolute digital encoders acquire absolute position or rotary angle and feedback, typically in industrial drives, such as servo drives, CNC, and robotics EE.

Multiple protocol standards are based on RS485/RS422, with synchronous or asynchronous communication and a protocol-specific encoder supply voltage range. Drive customers are looking for a universal RS485 digital interface to enable their drive to support the absolute encoder which best fits their system.

The trend is for more precise and robust control of motors, additional safety features, and predictive maintenance for lesser or complete avoidance of shut-down time.

Devices able to withstand harsh industrial environments yield higher reliability and less down-time

- In real drives, the most critical noise is the PWM switching noise, coupled into the shield of the power cable during the high-voltage PWM switching transients. These transients can be 10 kV/µs with IGBT, and up to 50-100 kV/µs with SiC in the future. These transients can couple typically as AC common-mode transients into the RS485 differential signals. EFT and INS common-mode noise are closest to the real impulse noise in drives.
- Corrupt communication (bit errors), even when detected with a CRC error, make the current position or angle read data invalid, and can impact the performance of the drive. In a worst case scenario, the drive must shut down due to lack of angle correct information.

The EMEA/U.S. drive and encoder customers focus on RS485 immunity against ESD, surge, and EFT/INS. The trend to faster switching GaN and SiC with higher impulse noise than today's IGBT further increases the importance of an RS485 transceiver with high EMC (EFT) immunity.

Figure 1 shows a simplified system block of a hardware interface module supporting digital absolute position encoders. The design is shown as a subsystem of an industrial servo drive connected to the absolute position encoder; the RS485 transceiver is needed in both the encoder and the drive.

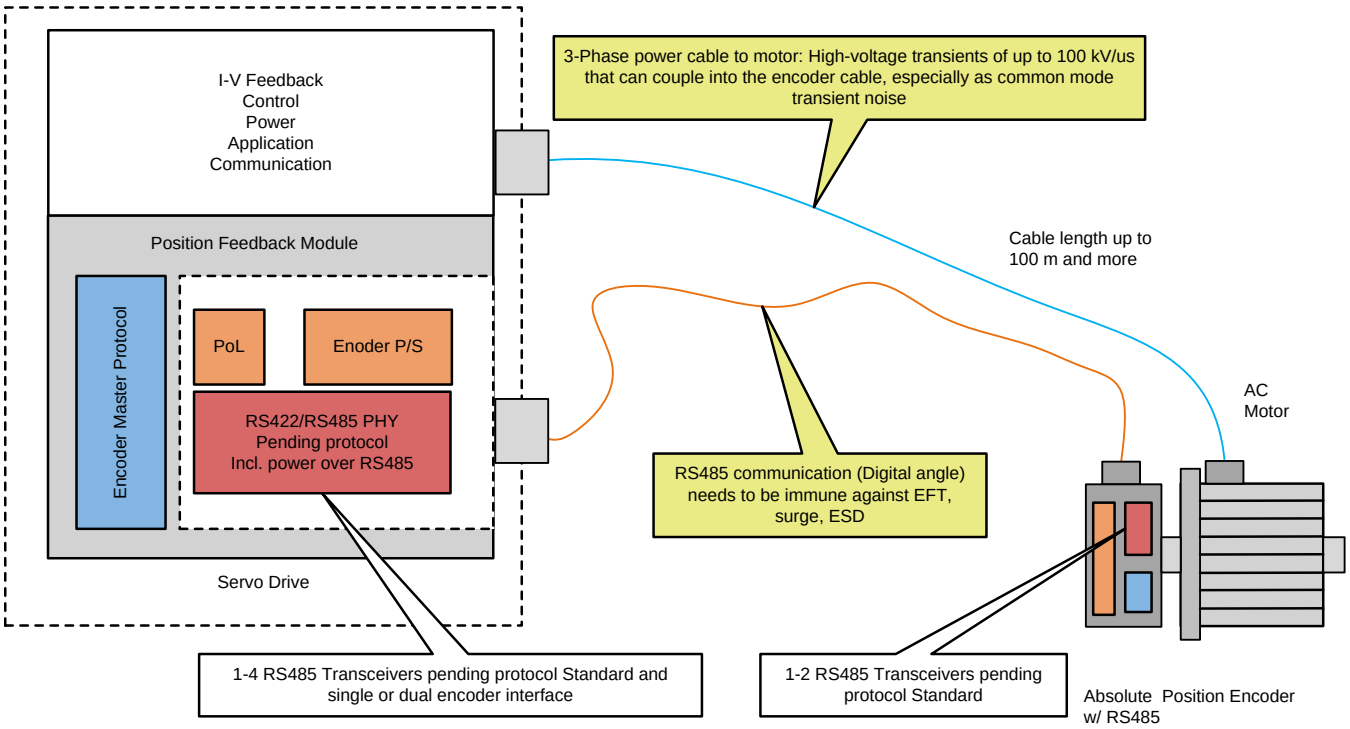


Figure 1. Industrial Drive with Digital Interface to Absolute Position Encoders

1.1 EC61800-3 EMC Immunity Standard

When building an industrial drive, the customer must pass the compliance test of the IEC61800-3 EMC standards.

For more details on the IEC61800-3 standard, see the blog , or the video .

The blog shows that there are several interfaces which must be tested.

For this design, the signal interface is tested; this focus is on surge and EFT immunity.

Table 1. IEC618000-3 EMC EFT Immunity Requirements for Second Environment, Measured Voltage Levels, and Class

Requirements				
Port	**Phenomenon**	**Basic Standard**	**Level**	**Performance (Acceptance) Criterion**
Ports for control lines and DC auxiliary supplies <60 V	Fast transient Burst (EFT)	IEC61000-4-4	±2 kV / (5 kHz or 100 kHz), capacitive clamp	B
Ports for control lines and DC auxiliary supplies <60 V	Surge 1, 2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV. Because the shielded cable >20 m, direct coupling to shield (2 Ω / 500 A)	B

The performance (acceptance) criterion is defined, as follows:

Performance (Acceptance) Criterion	Description
A	The module continues to operate as intended. No loss of function or performance, including the duration of the test.
B	Temporary degradation of performance is accepted. After the test, the module continues to operate as intended, without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module continues to operate as intended automatically, after manual restart, or power off, or power on.

Depending on the geographic location where the drive is EMC tested, there are other IEC standards for electrical fast transients.

For example, Japan specifies an additional standard: the NECA TR-28 for impulse noise (INS). This design was tested against IEC61000-4-4.

1.2 TI Design Overview

This TI design implements a high EMC immunity RS485 digital interface for absolute position encoders, using Tamagawa T-Format.

The major building blocks of this TI hardware design are the bidirectional 2-wire RS485 interface, the encoder power supply protected by a load switch, and a 3.3-V digital interface to a host processor to run the corresponding encoder standard protocol. The host processor that runs the corresponding encoder master protocol is not part of this design.

The absolute position encoder can be connected to the reference design, either through a SubD-15 connector or a 10-pin header. The connector has dedicated pins needed for the data lines and the encoder power supply. This design supports cable lengths of up to at least 50 m. For cable specifications, refer to the recommendations of the corresponding encoder vendor.

A block diagram is shown in Figure 2.

The design has been tested for EMC immunity against fast transient burst (EFT), with levels specified per IEC61800-3 and above standard. For details on the EFT, see the section below. There are multiple absolute position encoder protocol standards that use RS-485 or RS-422-based serial digital interfaces, such as EnDat 2.2, BiSS, or HIPERFACE DSL. Further interface standards include PROFIBUS® DP and PROFIBUS IO, as well as CAN or Ethernet-based interfaces. Additional standards include proprietary, drive vendor-specific standards, such as Tamagawa, Fanuc Serial Interface, Mitsubishi™ High-Speed Serial Interface, and this TI design supports the Tamagawa T-format serial interface.

For more details on the different standards, see the following TI designs listed in Table 2, listed per protocol.

Table 2. Absolute Position Encoder Digital Interface TI Designs

Encoder Protocol	TI Design
Endat2.2	TIDA-00172, TIDA-00179, TIDA-01401, TIDM-1008
BiSS	TIDA-00175, TIDA-00179, TIDA-01401
HiperfaceDSL	TIDA-00177, TIDA-00179
Hiperface	TIDA-00202
Tamagawa	TIDA-01630, TIDA-00179

1.3 Key System Specifications

Table 3. TIDA-01630 Specifications

Parameter	Value	Comment
DC input voltage	5 V	2.1-mm ID / 5.5-mm ODM barrel DC jack. 5-V input to supply the board.
RS485 interface	1 channel half duplex 5-V RS485 transceiver	Can be configured for use in both encoder and drive interface.
Encoder power supply	DC input voltage	Same as DC input voltage, can be turned controlled using a load switch using I/O interface
I/O interface signaling voltage	3.3 V	BoosterPack for launchxl-f28379d, for pin assignment; see Table 8
RS485 transceiver power supply	3.3 V or 5 V	Flexible power supply for 3.3-V or 5-V versions of RS485 transceivers. Default 5 V.
RS485 transfer rate	50 MBaud	Supports all standard encoder protocols. 50 MBaud improves rate reach.
Temperature range	-40 to 85°C	Industrial temperature range -40 to 85°C. No heat sink required.
Electromagnetic compatibility (EMC)	According to IEC61800-3	Designed to exceed IEC61800-3 EMC levels and pass criterion for ESD, EFT and surge according to test method described in: • IEC61000-4-4 • IEC61000-4-5
Encoder connector	Sub D-15 or 10-pin header	See section Section 3.1.1.4 for pinout
Encoder standard	Tamagawa	Pending SW for C2000. For further details, refer to the forum e2e.ti.com
Indicator LEDs	Power rails, 3 I/O controlled	3.3 V, 5 V, and Encoder PS and LaunchPad LEDs for test and debug option

2 System Overview

2.1 Block Diagram

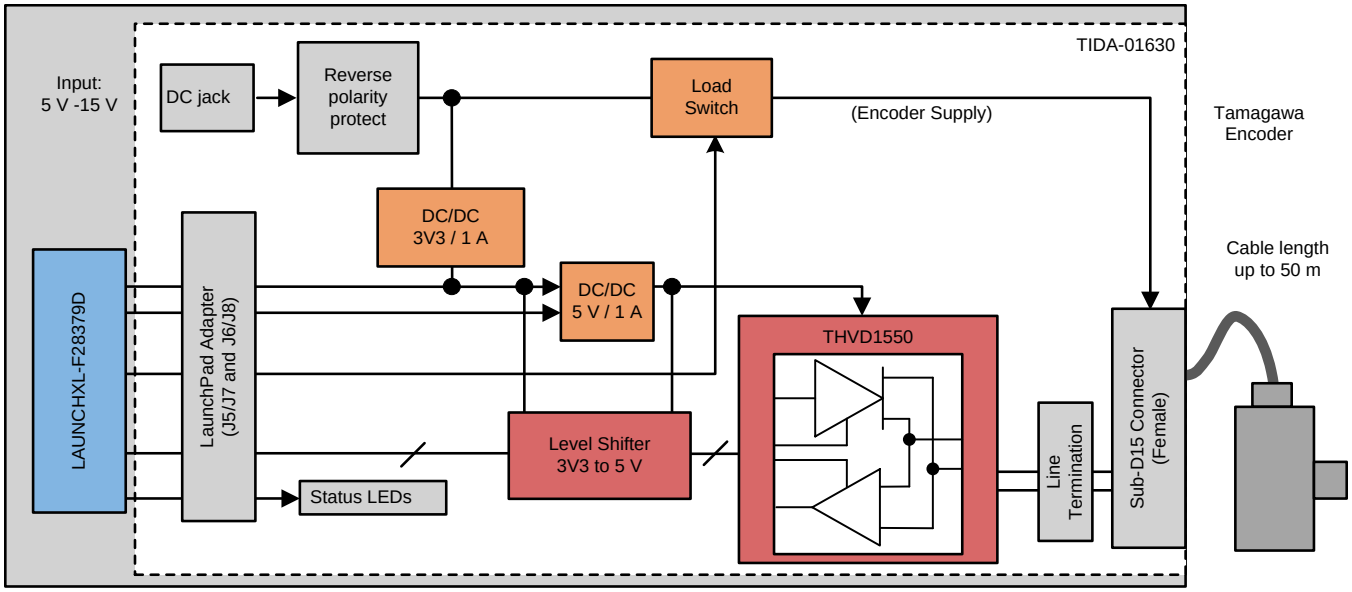


Figure 2. System Block Diagram of TIDA-01630

2.2 Design Considerations

This design has three major hardware blocks: the digital interface, the power supply for the digital interface, and the power supply for the encoder.

These three blocks are explained in the hardware design section.

A brief overview of the software required to use the TI Design is also given.

2.2.1 Hardware Design

2.2.1.1 Digital Interface

RS-485 Transceiver Circuits

The Tamagawa T-format protocol is an asynchronous communication which runs up to a maximum of 2.5-MHz frequency on the data communication path.

Parameters with regards to RS-485 transceivers taken into consideration are listed in Table 4.

Table 4. RS-485 Parameters From Corresponding Datasheets (SLLSEV1)

PARAMETER	THVD1550
Supply voltage (recommended)	5 V
Baud rate (maximum)	50 Mbps
Receiver propagation delay (maximum)	40 ns
Driver propagation delay (maximum)	16 ns
Receiver rise/fall time (maximum)	6 ns
Driver rise/fall time (maximum)	6 ns
Supply current (quiescent) driver and receiver enabled	700 µA
IEC61000-4-4 EFT (absolute maximum ratings)	±4 kV

With that information, the RS-485 device chosen for the design is the THVD1550.

RS-485 Termination and Transient Protection

Instead of single 220-Ω / 0.1-W resistors, two smaller resistors 0603 in series 0.1 W each have been chosen. A pulse-proof resistor is added to the A and B bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver, and prevent it from latching up. In data receive mode, due to the low input current of typical 240 μA, the voltage drop across the 10-Ω resistors is negligible. In the clock and data transmit direction, the voltage drop across both 10-Ω resistors is around 15%, which results in a slightly lower transmit differential voltage.

To further improve immunity against common-mode noise, two different circuits choice are shown.

Option 1: 220-pF bypass capacitors are added from each of the differential RS-485 outputs A and B, to GND. See C19 and C22 in Figure 9; these capacitors must be high quality capacitors (NP0/C0G).

Option 2: A 470-pF bypass capacitor is added at the center point of the termination resistors R42 and R43. This bypass capacitor removes the need to match the capacitors to have the same effect on the common mode during an event. The difference in the resistor values affects the equal distribution of an event. The capacitor must be a high quality capacitor (NP0/C0G).

The bus terminals of the THVD15xx transceiver family possess on-chip ESD protection against ±30-kV human body model (HBM), ±16-kV IEC61000-4-2 contact discharge, and ±4-kV IEC61000-4-4 Fast Transient Burst, meaning no further protection is required.

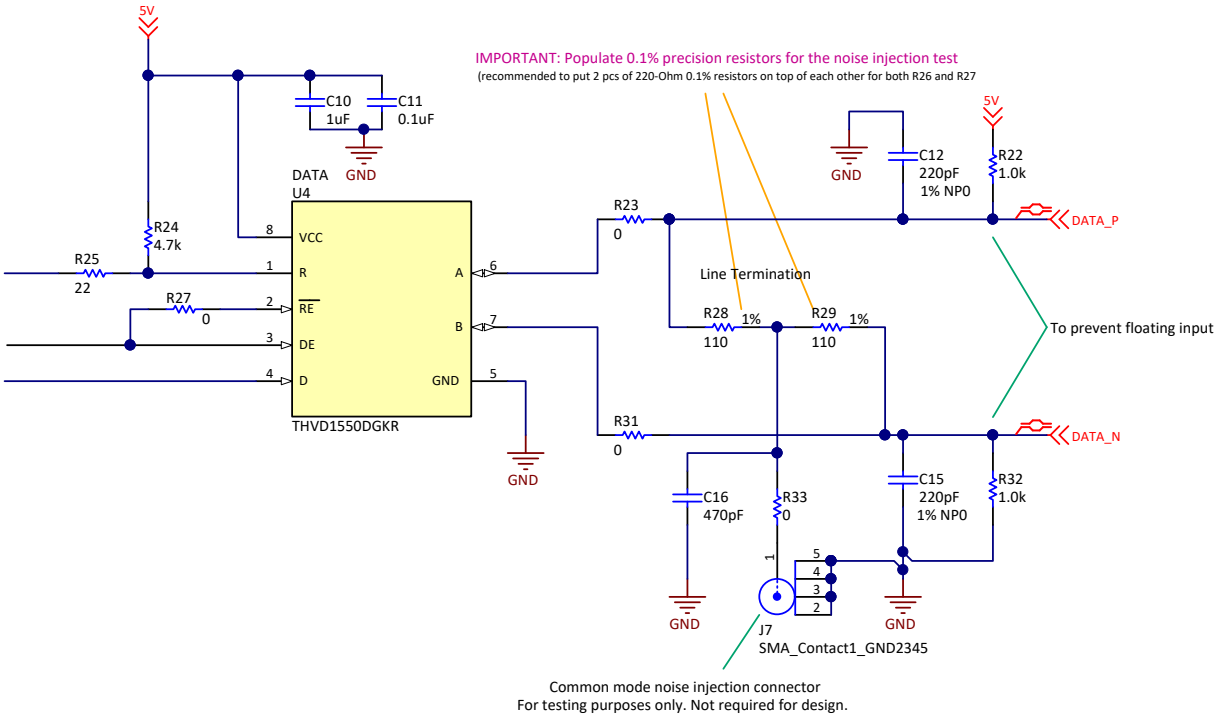


Figure 3. Image of Data Transceiver Circuit

For the data circuit, the resistors mentioned are R28, R29, and R33, and the capacitors are C12, C15, and C16.

Common Mode Noise Injection Circuit

Figure 3 shows that R33 and C16 and the J7 connector define this test circuit, which can be used to test how well the RS485 transceiver works with common-mode noise. J7 and R33 of this circuit are used for test purposes only. This circuit is only needed for test and debug, and should be removed for a final design.

5-V to 3.3-V Level Shifter

As the THVD1550 is a 5-V RS485 transceiver, level translation between 5 V and 3.3 V is typically needed. This level shifter must have low propagation delay, as this affects the system performance at long cable lengths. For this design, the SN74LVC2T45 was chosen; with this device, 3 IC's are needed, using two for transmitting data and one for receiving data. The VCCB was always chosen as input and VCCA always as output of the level shifter. With this configuration and the voltage levels used, the data sheet shows that the propagation delay is similar, as shown in Table 5.

Table 5. Maximum Propagation Delay From Corresponding Data Sheets (SCES516)

VCCA	VCCB	Direction	Propagation Delay tPLH / tPHL
3.3 V	5 V	B to A	5.4 ns / 4.5 ns
5 V	3.3 V	B to A	3.9 ns / 3.5 ns

2.2.1.2 Power Supply for Digital Interface

The design requires two voltage rails, one 3v3 rail and one 5-V rail; in this design, the 3v3 voltage rail was selected, using a buck controller, with the 3v3 rail generating the 5-V rail using a boost controller.

The 3v3 rail has a power requirement of approximately 1 A; this includes the transceivers and the option of powering the LaunchPad from the 3v3 rail. The second requirement is what input voltage range could be used. As described in the TIDA-00179 design guide, the typical voltage rail of an encoder is either a 5-V rail or an 8-V to 20-V rail. Thus, the input voltage of the design was chosen to be 5 V to 15 V. Choose an encoder which can support the chosen input voltage of the design.

The TPS62162 has an input voltage range of 3 V to 17 V providing 1-A current. This device comes in a fixed output voltage or adjustable output voltage range; a fixed output voltage was chosen to minimize external components and PCB size.

In section 9.3.1 of the TPS6216x data sheet, a schematic example is shown how to build a 3v3 voltage rail; one input capacitor, one output capacitor, and an inductor are needed as external components. In Table 3 of the TPS62162 data sheet, inductors that have already been tested can be found. For the two capacitors X5R or X7R, TI recommends ceramic capacitors.

To generate the 5-V rail, a boost converter which boosts from the 3v3 rail was chosen; this is done to be able to have Vin down to 5 V without special considerations of generating the 5-V rail.

The TPS61240 has an input voltage range of 2.3 V to 5.5 V, providing 600-mA current. This device comes with a fixed output voltage; this minimizes external components and PCB size.

In section 10.2 of the TPS61240 data sheet, a schematic example shows how to build a 3v3 to 5-V rail; one input capacitor, one output capacitor, and an inductor are needed as external components.

Additionally, for this design a turn off option of the 5-V rail is provided. This is done by adding a two resistors on the enable pin: one to GND and one to Vin of the TPS61240. With this circuit, it is possible to test transceivers with both 5-V and 3V3 Vcc requirement.

2.2.1.3 Power Supply for the Encoder

To power the encoder, the Vin voltage level was selected to provide the encoder rail. This must be remembered when connecting an encoder to the board. To protect the encoder and the board input voltage, a load switch is added to provide a UVLO and a thermal protection, which can be translated into an approximately 2-A current limit before the thermal protection shuts off the switch. This current limit is dependent on the package choice. To calculate the current limit, use equation 9 of the TPS62162 data sheet. For an IINRUSH, 200 mA is needed to supply the encoder; the rise time defined on the CL pin must be smaller. The choice of CL defines how fast the rise time must be.

$dt = C_L \times dVout / I_{INRUSH} = 2.2\ \mu F \times 9.6\ V / 200mA = 106\ \mu s$

With dVout defined to 9.6 V, see section 10.2.2.3 of the TPS62162 data sheet.

To see what time must be set on the CT pin, see table 2 in the data sheet.

A 470-pF capacitor is needed, which gives a rise time of 96 µs; with the smaller rise time, the IINRUSH is 225 mA.

For this design, the device TPS22810 was chosen; this device fits the voltage range of the TPS62162.

2.2.2 Hardware Updates

- Change the direction of the level shifters so the propagation delay of the level shifters are the same; this can be accomplished, as the level shifters are used in only one communication direction.
- Add resistors between the LaunchPad connector and level shifter to enable slave and master operation of the SPI peripheral of the C2000 microcontroller.

2.2.3 Software Design

To test this design, the C2000 microcontroller was chosen. This test uses the software library Position manager, which enables the use of the Tamagawa T-format protocol.

To generate this example software, use the software package ControlSuite.

The position manager libraries enable many different digital and analog encoder interfaces; for more information on the position manager from the C2000, refer to the following link: www.ti.com/C2000Drives

For the tests of this design two types of software was built one needed to test a Tamagawa interface and one software which is used to generate eye diagrams and bit error tests.

The Tamagawa software example can be found in ControlSuite.

Download Controlsuite here: www.ti.com/ControlSuite.

The software used for the tests is a demo version showing a Tamagawa connection, giving the result back in a virtual com port.

This combines two examples from ControlSuite; the first example shows the Tamagawa protocol, and the second software shows a UART implementation using the C2000. For questions on ControlSuite, visit the e2e forum: https://e2e.ti.com/support/microcontrollers/c2000/

For Tamagawa documentation for the C2000, see the *C2000 Position Manager T-Format Library Module User's Guide* (SPRUI71).

2.3 Highlighted Products

2.3.1 THVD1550

These devices have robust drivers and receivers for demanding industrial applications. The bus pins are robust to high levels of IEC contact discharge ESD events, eliminating the need for additional system-level protection components.

Each of these devices operates from a single 5-V supply. The devices in this family feature a wide common-mode voltage range, which makes them suitable for multi-point applications over long cable runs.

The THVD15xx family of devices is available in small VSSOP packages for space-constrained applications.

These devices are characterized from –40°C to 125°C. Features:

- 4.5-V to 5.5-V Supply Voltage
- Bus I/O Protection
  - ±30-kV HBM
  - ±16-kV IEC61000-4-2 Contact Discharge
  - ±4-kV IEC61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range: –40°C to 125°C
- Large Receiver Hysteresis (80 mV) for Noise Rejection
- Low Power Consumption
  - Low Standby Supply Current: < 1 μA
  - ICC < 700 μA Quiescent During Operation

- Glitch-Free Power-Up/Down for Hot Plug-in Capability
- Open, Short, and Idle Bus Failsafe
- 1/8 Unit Load Options (Up to 256 Bus Nodes)
- Small-Size VSSOP Packages Save Board Space or SOIC for Drop-in Compatibility
- Low EMI 500-kbps 50-Mbps Data Rates

2.3.2 TPS62162

The TPS6216x device family are easy to use synchronous step-down DC/DC converters, optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors, and provides fast transient response and high output voltage accuracy by using the DCS-Control™ topology.

With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery, as well as from 12-V intermediate power rails. It supports up to 1-A continuous output current, at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

Power sequencing is also possible by configuring the enable and open-drain power good pins.

In power save mode, the devices show quiescent current of about 17 µA from VIN. Power save mode, entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 µA.

The device, available in adjustable and fixed output voltage versions, is packaged in an 8-pin WSON package measuring 2.00 mm × 2.00 mm (DSG), or 8-pin VSSOP package measuring 3.00 mm × 3.00 mm (DGK).

2.3.3 TPS22810

The TPS22810 is a single-channel load switch with configurable rise time, and with an integrated quick output discharge (QOD). In addition, the device features thermal shutdown to protect the device against high junction temperature. This ensures a safe operating area for the device. The device contains an N-channel MOSFET that can operate over an input voltage range of 2.7 V to 18 V. The SOT23-5 (DBV) package can support a maximum current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

The configurable rise time of the device greatly reduces the inrush current caused by large bulk load capacitances, thus reducing or eliminating power supply droop. Undervoltage lock-out is used to turn off the device if the VIN voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged when supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device, to allow design flexibility for power down.

The TPS22810 is available in a leaded, SOT-23 package (DBV), which lets the user visually inspect the solder joints. The device is characterized for operation over the free-air temperature range of –40˚C to +105˚C.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 PCB Overview

Figure 4 shows a photo of the top side of the TIDA-01630 PCB with the Launchxl-f28379d. The headers and default jumper settings are explained in Section 3.1.1.3.

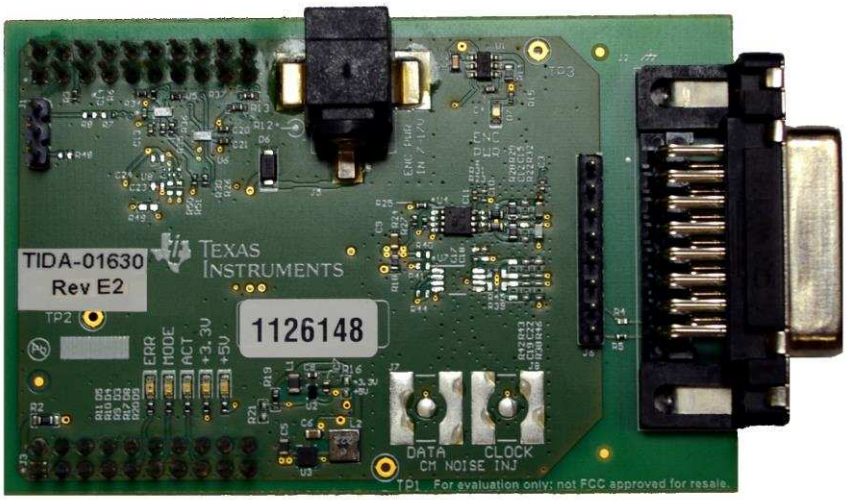


Figure 4. Board Picture (Top View)

3.1.1 Hardware

3.1.1.1 Prerequisites

The following hardware equipment and software is required for the evaluation of the TIDA-01630 TI Design.

Table 6. Pinout of J3 and J4 host processor Interface

Equipment	Comment
5-V DC power supply	5-V output power brick with at least 2-A output current capability using 2.1-mm ID / 5.5-mm OD mating barrel connector
TIDA-01630 hardware	With the default jumper settings per Section 3.1.1.3.
TIDA-01630 firmware	Download ControlSuite
F28379D Launchpad(Launchxl-f28379d)	Available through TI eStore
Code Composer Studio™ 6	Download from https://www.ti.com
Encoder cables	ÖLFLEX® SERVO FD 798 CP - 0036910
Connector	Wurth – 618 015 248 23 and 618 015 249 23
Connector housing	Wurth – 618 015 253 11
Encoder	TS5667N422

3.1.1.2 Connector

The connector assignment and jumper settings are outlined in Table 7 through Table 8.

The 5-V nominal input voltage can be supplied through the connector J8, the chosen connector is a RAPC722X from the company Switchcraft.

This connector is expecting a 2.1-mm ID / 5.5-mm OD mating barrel connector.

CAUTION

The input voltage of the board is directly connected to the encoder; ensure that the encoder supports the applied voltage.

3.1.1.3 Default Resistor Configuration

Before working with the TIDA-01630 board, apply the correct resistor settings. The default jumper configuration is shown on the board picture in Figure 4.

Table 7. Default Resistor Settings

Header	Jumper Setting
R2	Enables the 3.3-V intermediate rail connect to power the LaunchPad
R4 and R5	Configuration to remove the clock lines from the SUB-D connector. For test and debug.

3.1.1.4 Host Processor Interface

The signals the TIDA-01630 BoosterPack uses to communicate with the C2000 LaunchPad are shown in Table 8.

Table 8. Pinout of J3 and J4 Host Processor Interface

LAUNCHXL-F28379D				TIDA-01630 rev E2			
J5	J7	J8	J6	J3		J4	
3V3	5V	GPIO6	GND	3V3	NC	TX_CLK(Not Used)	GND
GPIO95	GND	GPIO7	SPIBCS/GPIO 66	NC	GND	SPICLK(Not Used)	GND
GPIO139	ADCIN15	GPIO8	GPIO131	NC	NC	NC	NC
GPIO56	ADCINC5	GPIO9	GPIO130	NC	NC	Data TX Enable	NC
GPIO97	ADCINB5	GPIO10	RESETn	LED	NC	NC	NC
GPIO94	ADCINA5	GPIO11	SPIBSIMO/GPIO63	LED	NC	NC	Data RX
SPIBCLK/GPIO65	ADCINC4	GPIO14	SPIBSOMI/GPIO64	CLK(Not Used)	NC	NC	Data TX
GPIO52	ADCINB4	GPIO15	GPIO26	LED	NC	NC	NC
GPIO41	ADCINA4	DAC3	GPIO27	EN_CLK(Not Used)	NC	NC	Enc_PS_Enable
GPIO40	ADCINA1	DAC4	GPIO25	NC	NC	NC	NC

3.1.2 Software

Use the ControlSuite Position Manager software framework for the LaunchPad Launchxl-f28379d. Select the software library for Tamagawa, working on the connectors J5 to J8 of the LaunchPad.

Follow the example as described in ControlSuite; this compiles and runs the code on the LaunchPad with the TIDA-01630 connected, as seen in Figure 4.

For more information on the Tamagawa library, see the *C2000 Position Manager T-Format Library Module User's Guide* (SPRUI71).

For a user example, see the *DesignDRIVE Development Kit IDDK v2.2.1 - User's Guide* (SPRUI44); this document shows how to use the Tamagawa software on the IDDK hardware platform.

The user interface of the standard example would be the debug window of Code Composer Studio.

To find this software, go to www.ti.com/ControlSuite.

3.2 Testing and Results

Tests were done to characterize each individual functional block and the entire board. In particular, the following tests were conducted:

- Power management
- Digital interface signal tests
- System performance

Tests were done at room temperature at approximately 22°C.

3.2.1 Test Setup

The following equipment has been used for the TIDA-01630 testing session:

Table 9. Test Equipment for TIDA-01630 Performance Tests

Test Equipment	Part #
High-speed oscilloscope	Tektronix TDS784C
Differential probes	Tektronix P6630
Single-ended probes	Tektronix P6139A
Power supply (5 V)	Agilent™ E3648A with 2.1-mm ID and 5.5-mm OD mating barrel connector cable
Power supply AC mains to 24 V	Siemens LOGO!Power 6EP1331-1SH03
Power supply 24 V to 5 V	LMR23625C EVM (5-V configuration)
Power supply multi rail	EA-PS 2342-10B
True RMS multimeter	Fluke 179
Encoder cable with sub d-15 connector and housing(	ÖLFLEX® SERVO FD 798 CP - 0036910
	Wurth – 618 015 248 23 and 618 015 248 23
	Wurth – 618 015 253 11
Encoder	Tamagawa - TS5667N422
Burst generator	Schaffner Elektrotest - NSG 2025
Coupling clamp	Schaffner Elektrotest - CDN 8014
EMC software	Schaffner Elektrotest - WIN 2025 V 5.00
Surge generator	Schaffner Elektrotest - NSG 2050
EMC software	Schaffner Elektrotest - WIN 2050 V 6.00

For the different tests, some of the equipment was used as described above. A test setup used for system tests is shown in Figure 5.

Figure 5. Picture of Test Setup for System Tests

Per test section, different setups were used and are described with a diagram in each test section.

3.2.2 Test Results

3.2.2.1 RS485 Transceiver and Level Shifter Tests

Understanding the system specification for the data protocol, the user must understand the system propagation delay of the signal chain. There are two contributors to this delay: the RS-485 transceiver and the level shifter. To measure this system delay, the TIDA-01630 board is measured from logic input to differential output for the driver, and in the opposite order for the receiver.

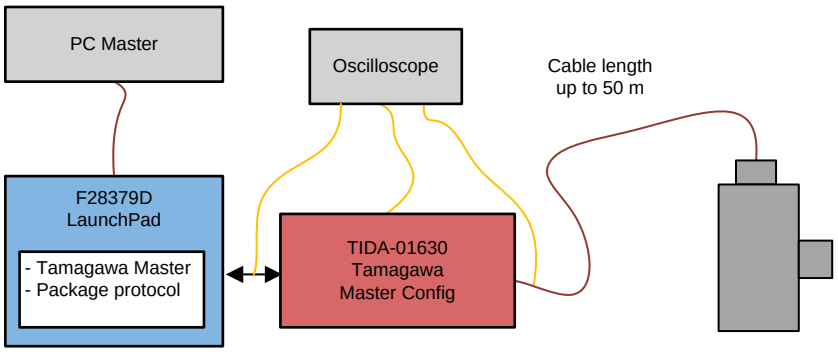


Figure 6. Block Diagram of Test Setup Used for Propagation Delay Measurements

The oscilloscope is connected on the connecter J6 for the differential data, and J4 for the single-ended data signal.

With this test setup, the following results were achieved.

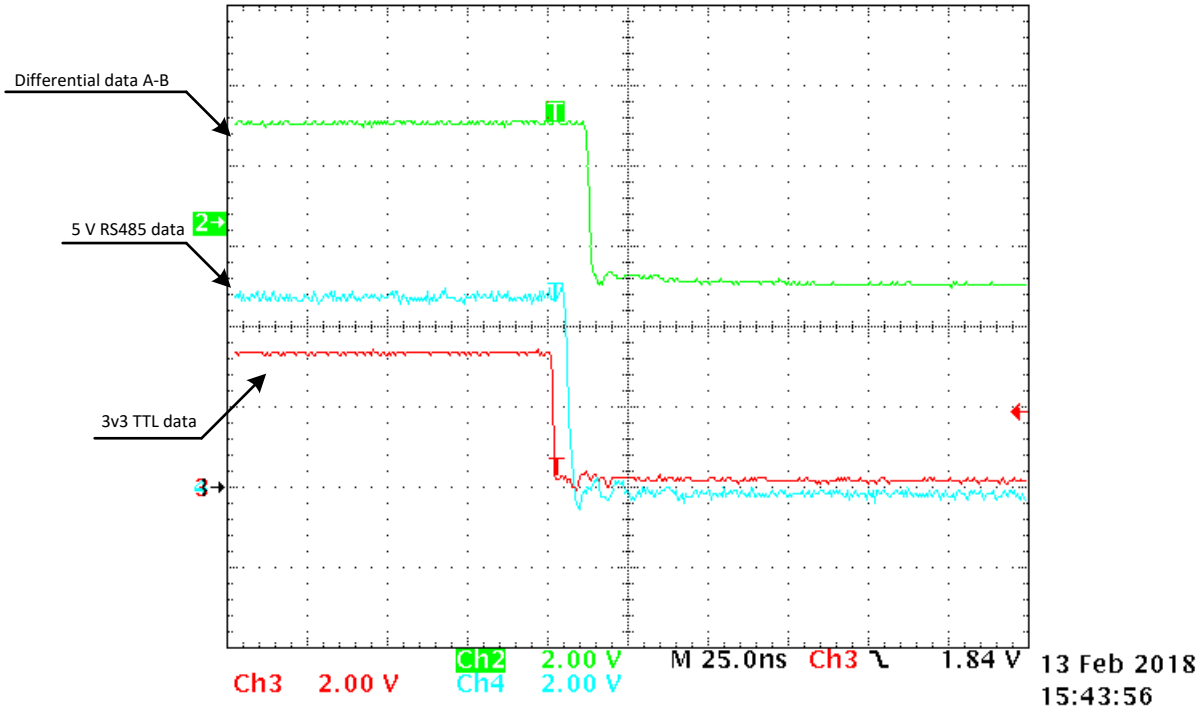


Figure 7. THVD1550 Receiver Propagation Delay with 20-m Cable

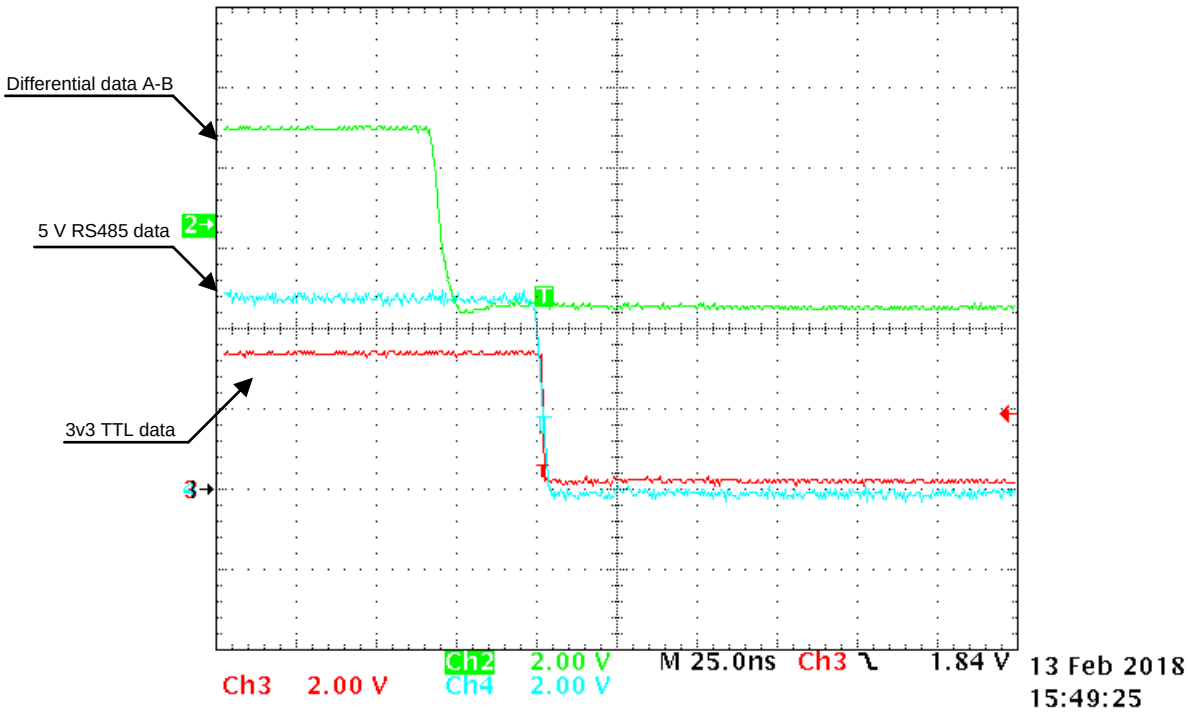


Figure 8. THVD1550 Propagation Delay Driver with 20-m Cable

There is a different time scale for driver and receiver measurement. The driver propagation delay measured is approximately 10 ns, and the receiver propagation delay is approximately 35 ns. The RS-485 master transceiver only contributes to 45 ns to the overall loop delay, which is well below the critical threshold for the configuration without delay compensation.

The propagation delay of the cable must also be considered. The cable propagation delay (around 5 m) is already dominant versus the RS-485 transceiver. For a 2.5-MHz data transfer frequency, the entire loop delay is approximately 0.6 µs. At 2.5-MHz data rates, the data is delayed by 1.5-bits at the master receiver side.

For more details on the cable delay, refer to the TIDA-00179 design guide.

Considering the cable propagation delay, the delay caused by the TIDA-01630 board is small compared to the cable.

3.2.2.2 Test Results

The data and clock signal is measured at a 220-Ω termination at 200m cable. The measurement done is an eye diagram where an SPI interface is required, which can generate a continuous random number generation bit pattern. This pattern can be used to emulate the asynchronous Tamagawa data transfer, which is sampled at the falling edge of the SPI clock signal.

The test setup was done as shown in Figure 9.

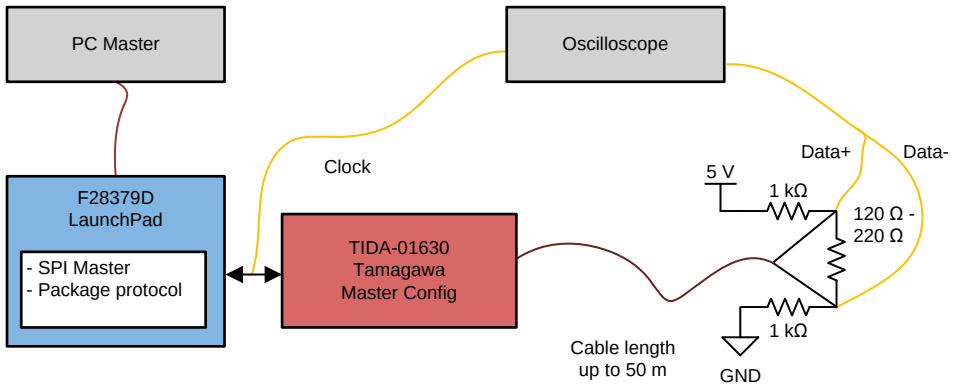


Figure 9. Block Diagram of Test Setup Used for Eye Diagram Generation Tests

The test setup gives a termination of the cable equal to 96.77 Ω at 120 Ω, or 152.77 Ω at 220 Ω.

The oscilloscope is connected to the resistor for the differential data, and J3 for the single-ended clock signal.

The eye diagram can be seen for both termination options using a 20-m cable.

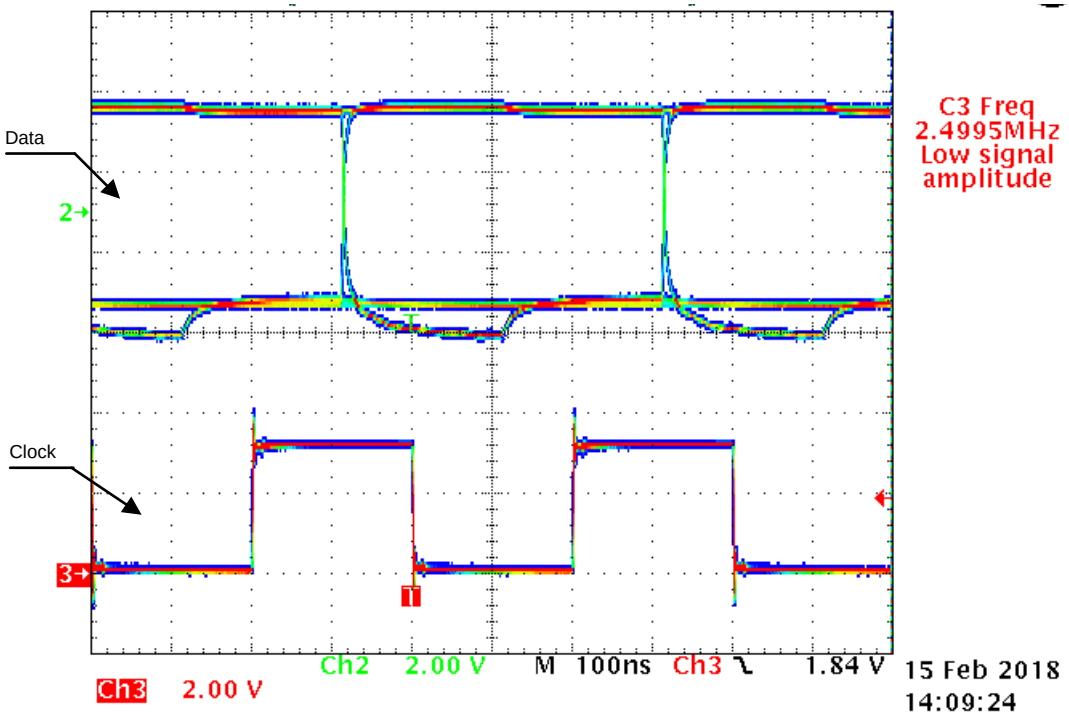


Figure 10. Eye Diagram of the THVD1550 at Master Transmit, 20-m Cable Data Rate 2.5 MHz With 220-Ω Termination

During these tests, it was seen that the choice of 220-Ω termination gives a poor eye diagram for industrial grade cables; the use of a 120-Ω termination on the drive side gives a better eye while using the cable in this report. The eye performance can be accepted if the cable length is limited in such a way that the termination ringing does not effect the measurement point. If this is done, this increases the common-mode voltage of the receiver signal. This gives the receiver a larger voltage difference to detect the measured signal.

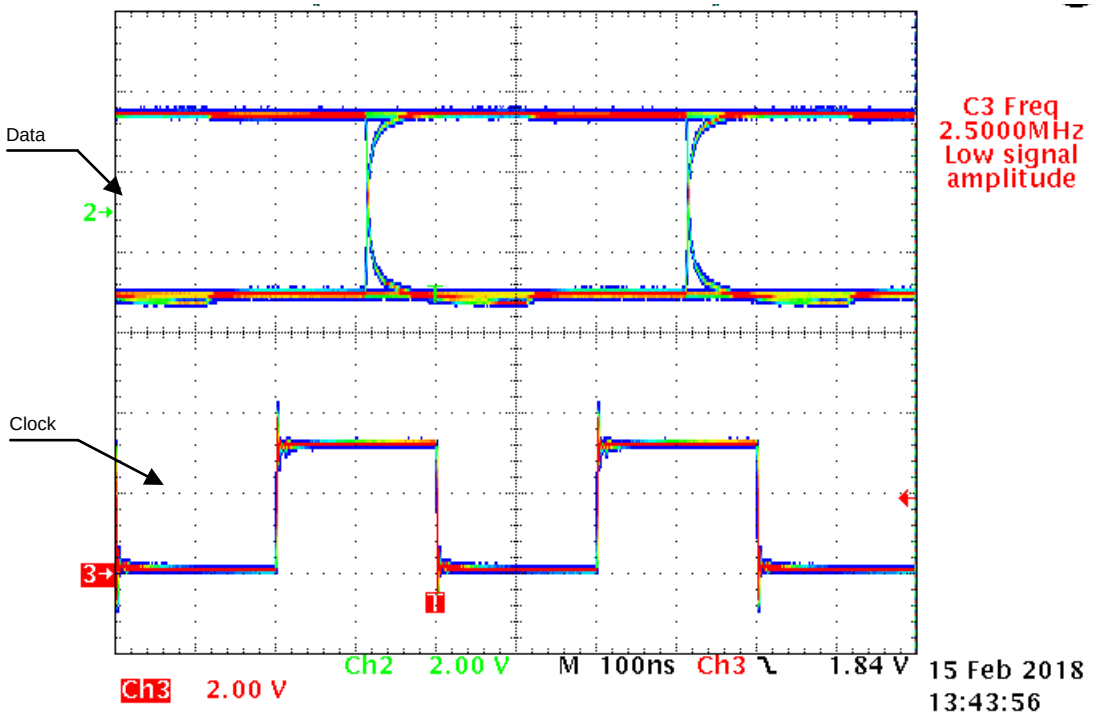


Figure 11. Eye Diagram of the THVD1550 at Master Transmit, 20-m Cable Data Rate 2.5 MHz with 120-Ω Termination

The jitter of the received differential data at the cable with a 120-Ω termination at the Tamagawa frequency is around 5% (0.95 UI-open). The steady state differential voltage is around ±2.5 V (5.0 Vpp). However, the rise or fall time from 10% to 90% is half a clock cycle. Taking into account that the receive data is sampled at the falling clock edge (in the center of the clock cycle), the effective worst case differential voltage is approximately ±2.3 V. Because Tamagawa specifies the data frequency based on a 50% duty cycle, the data frequency can be supported.

3.2.2.3 System Performance

Tests are done using the interface as an encoder interface; in this case, the Tamagawa T-Format protocol is used combined with an Tamagawa encoder.

The T-Format master interface is a known RS485 transceiver, and Tamagawa Slave (Encoder) is an unknown transceiver.

3.2.2.3.1 Tamagawa Tests

The test uses the TS5667N422 encoder. Figure 12 shows the block diagram of the test setup.

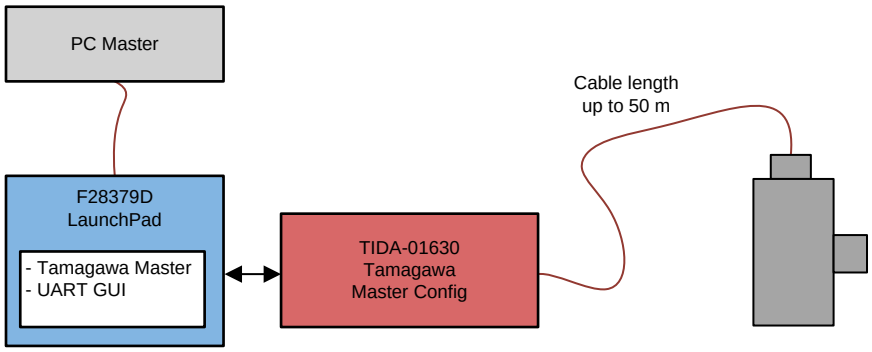


Figure 12. Block Diagram of Test Setup Used for System Performance Tests

The results of the performance tests can be seen in Figure 13. The result is compared with the Tamagawa length standards.

These tests show that the solution works for Tamagawa encoders using 2.5-MHz frequency.

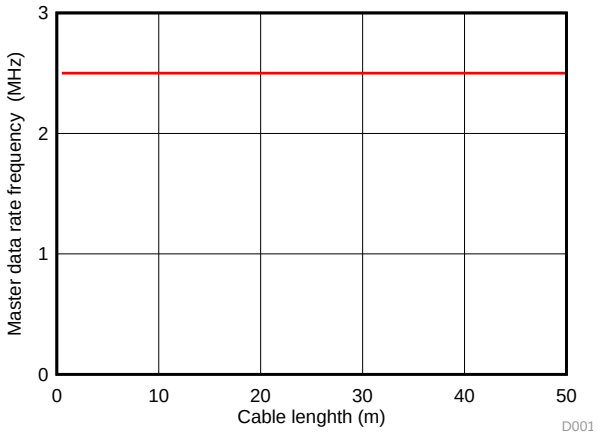


Figure 13. Tamagawa Cable Length Tests at 2.5 MHz

The THVD1550 can run the Tamagawa protocol from 0 up to 50 m, as the protocol states.

3.2.2.4 Power Management

For the power management subsystem of the TIDA-01630 board, the following tests were done:

- Testing the power-up sequence of the power rails
- Testing the power-down sequence
- Testing the current consumption on each power rail

Tests were performed with the test setup shown in the different test sections.

3.2.2.4.1 Power-up Behavior of the On-board Supply Rails

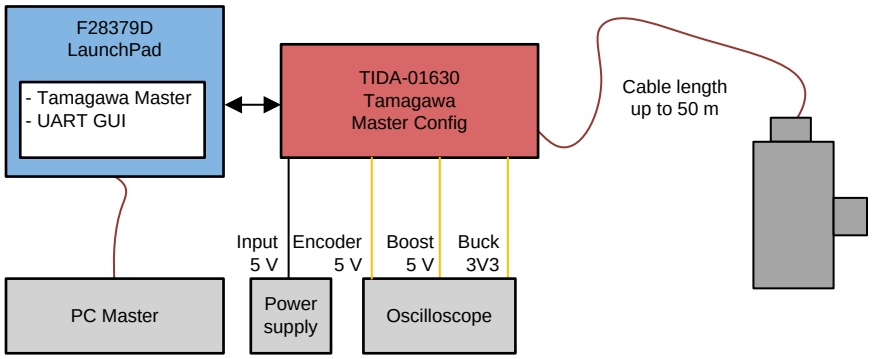


Figure 14. Block Diagram of Test Setup for the Power Sequence Tests of the TIDA-01630 Design

The oscilloscope is connected on the connecter J6 for the 5-V encoder rail, J3 for the 3v3 rail, and on the 5-V rail of the board by hand.

As expected, the 5-V rail starts after the 3v3 rail is supplied. The 3v3 rail starts as soon as the input gets to 3 V.

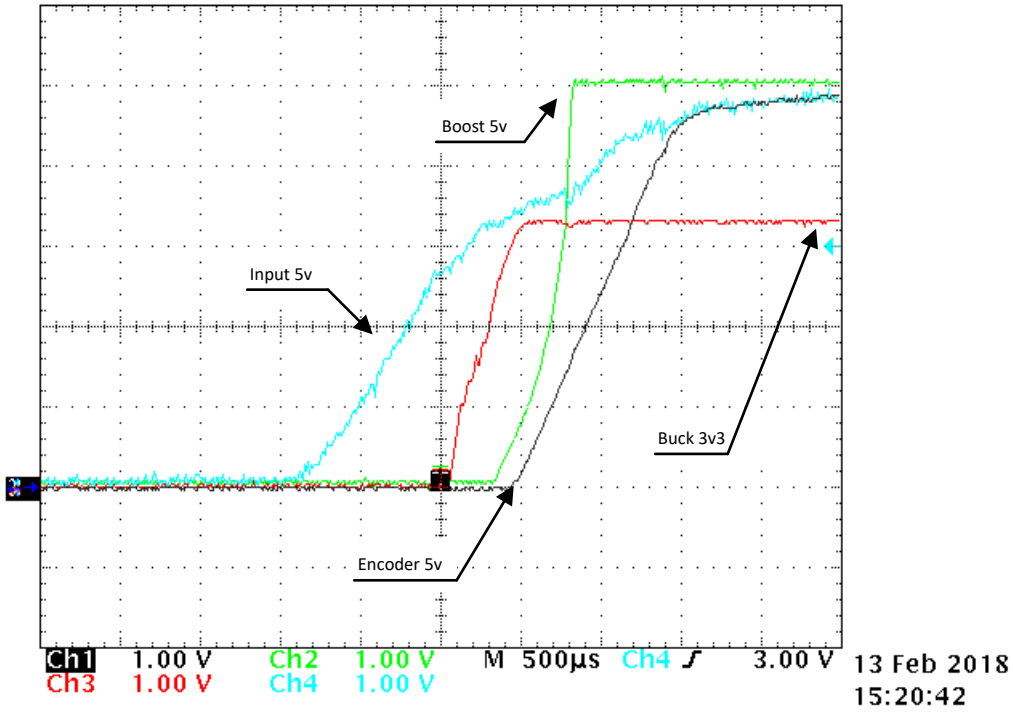


Figure 15. Power Up Sequence of the TIDA-01630

3.2.2.4.2 Power-down Behavior of the On-board Supply

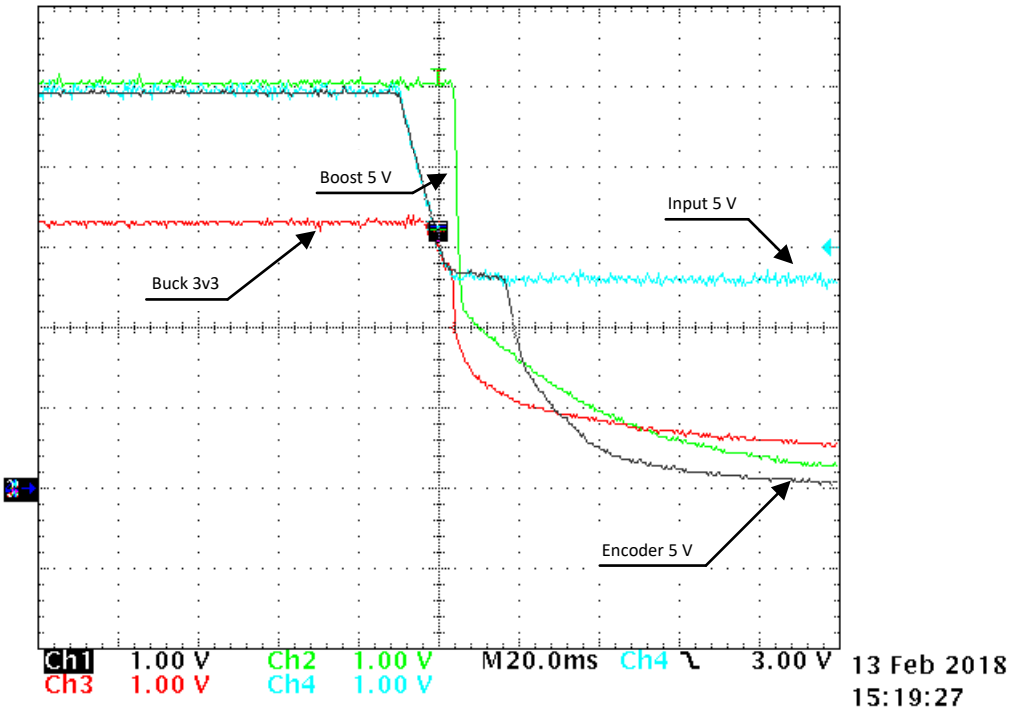


Figure 16. Power Down Sequence of the TIDA-01630

During power down, the 5-V rail and the encoder voltage start ramping down as the 3v3 rail gets below 2.7 V, as expected.

3.2.2.4.3 Power Consumption of the System

For the test of the power consumption measurement, the following test setup was done. Power to the LaunchPad was provided over the USB connection from the PC master.

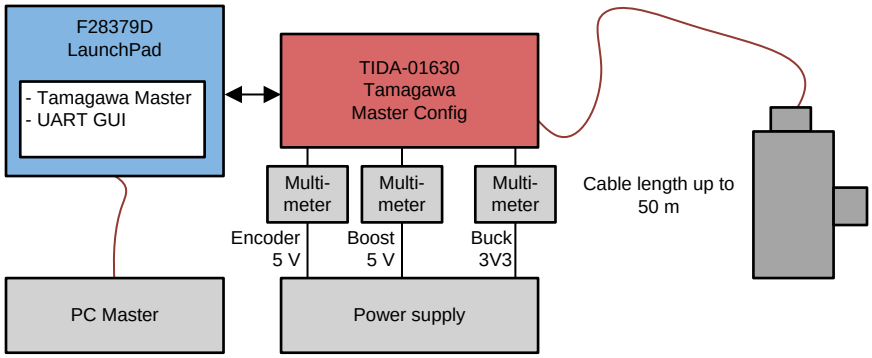


Figure 17. Block Diagram of Test Setup for the Power Consumption Tests

For this measurement, current was measured after disabling the 5-V boost and converted pulling the enable pin to ground, removing the resistor R2 externally powering the LaunchPad.

The power consumption is measured with the TIDA-01630 running a Tamagawa encoder at 2.5-MHz clock frequency, with a communication repetition of 16 kHz. The termination is 120 Ω with 1k parallel and a 20-m cable.

Table 10. Power Consumption for 5 V and 3v3 Rail at 220-Ω Termination

Measurement	Task	5-V Boost	3v3 Buck	5-V Encoder
Current[mA]	Idle	3.33 mA	0.51 mA	67.3 mA
Current[mA]	Tamagawa at 2.5 MHz	7.38 mA	0.54 mA	80.6 mA

3.2.2.5 EMC Immunity Test Results

The TIDA-01630 TI design has been tested for IEC61000-4-4 and 4-5 (EFT and Surge), with test levels and performance criterion specified in the standard IEC 61800-3 “EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems”.

The design meets these standards and exceeds the voltage levels.

Table 11. IEC618000-3 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

Requirements					TIDA-01630 Measurements		
Port	**Phenomenon**	**Basic Standard**	**Level**	**Performance (Acceptance) Criterion**	**Level**	**Performance (Achieved) Criterion (1)**	**Test**
Ports for control lines and DC auxiliary supplies < 60 V	Fast transient Burst (EFT)	IEC61000-4-4	±2 kV / 5 kHz or 100 kHz, capacitive clamp	B	±4 kV	B	PASS (EXCEED)
	Fast transient Burst (EFT)	IEC61000-4-4	±2 kV / 5 kHz or 100 kHz, power port	B	±4 kV	B	PASS (EXCEED)
	Surge 1,2 / 50 µs, 8 / 20 µs	IEC61000-4-5	±1 kV. Because shielded cable > 20 m, direct coupling to shield (2 Ω / 500 A)	B	±2 kV	A	PASS (EXCEED)

3.2.2.5.1 IEC-61000-4-4 Electrical Fast Transient (EFT) Test Results

A diagram and a picture of the EFT test setup for TIDA-01630 is shown in Figure 18 and Figure 19. During the test, the SubD-15 female connector is connected to the encoder by using a 20-m cable.

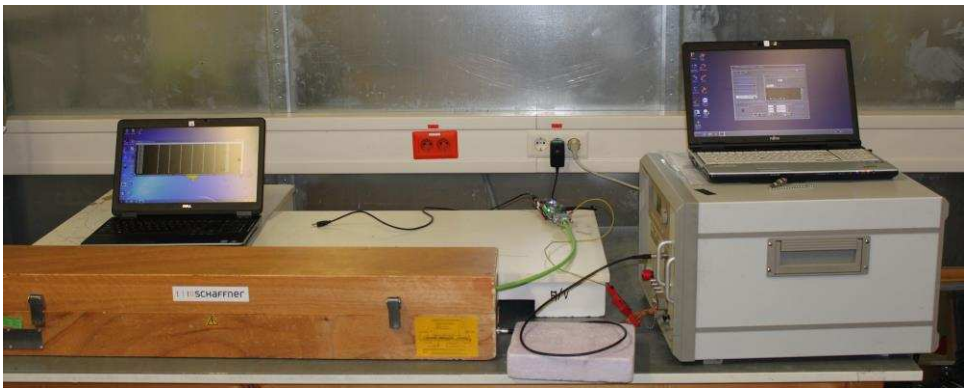


Figure 18. Picture of EFT Test Setup for Data Line of the TIDA-01630

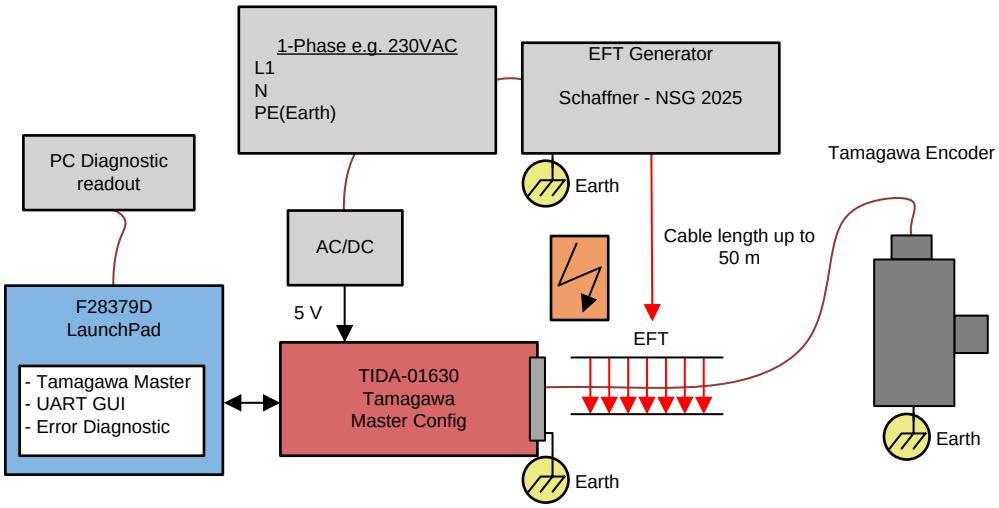


Figure 19. Block Diagram of EFT Test Setup Using the Data Line of the TIDA-01630

Table 12. EFT Test Results for TIDA-01630 on Data Lines

Phenomenon	Basic Standard	Level	TIDA-01630 Connector	Achieved Performance Criterion	Comment
EFT	IEC61000-4-4	±1 kV / 5 kHz, capacitive clamp	SubD-15	A	Criterion B required per IEC61800-3
EFT	IEC61000-4-4	±2 kV / 5 kHz, capacitive clamp	SubD-15	B	
EFT	IEC61000-4-4	±3 kV / 5 kHz, capacitive clamp	SubD-15	B	Not required per IEC61800-3
EFT	IEC61000-4-4	±4 kV / 5 kHz, capacitive clamp	SubD-15	B	Not required per IEC61800-3
EFT	IEC61000-4-4	±1 kV / 100 kHz, capacitive clamp	SubD-15	A	Criterion B required per IEC61800-3
EFT	IEC61000-4-4	±2 kV / 100 kHz, capacitive clamp	SubD-15	B	
EFT	IEC61000-4-4	±3 kV / 100 kHz, capacitive clamp	SubD-15	B	Not required per IEC61800-3
EFT	IEC61000-4-4	±4 kV / 100 kHz, capacitive clamp	SubD-15	B	Not required per IEC61800-3

Table 13 shows a more detailed test result, illustrating how many errors were seen during the 2 minute EFT test on the data lines.

Table 13. Communication Errors During the EFT Test on Data Lines

CRC Errors	Occurrence at 1-kV EFT	Occurrence at 2-kV EFT	Occurrence at 3-kV EFT	Occurrence at 4-kV EFT
Number of CRC errors at 5 kHz	0 errors in 1.92M packets transmissions	3 errors in 1.92M packets transmissions	102 errors in 1.92M packets transmissions	770 errors in 1.92M packets transmissions
Lost frames at 5 kHz	0 lost frames in 1.92M packets transmissions	0 lost frames in 1.92M packets transmissions	0 lost frames in 1.92M packets transmissions	1 lost frames in 1.92M packets transmissions
Number of CRC errors at 100 kHz	0 errors in 1.92M packets transmissions	1 errors in 1.92M packets transmissions	80 errors in 1.92M packets transmissions	1109 errors in 1.92M packets transmissions
Lost frames at 100 kHz	0 lost frames in 1.92M packets transmissions	0 lost frames in 1.92M packets transmissions	0 lost frames in 1.92M packets transmissions	1 lost frames in 1.92M packets transmissions

The position angle before and after the EFT tests is the same value within the standard angle distribution.

3.2.2.5.2 IEC-61000-4-5 Surge Test Results

A diagram and a picture of the EFT test setup for the TIDA-01630 is shown in Figure 21 and Figure 20. During the test, the SubD-15 female connector is connected to the encoder by using a 20-m cable.

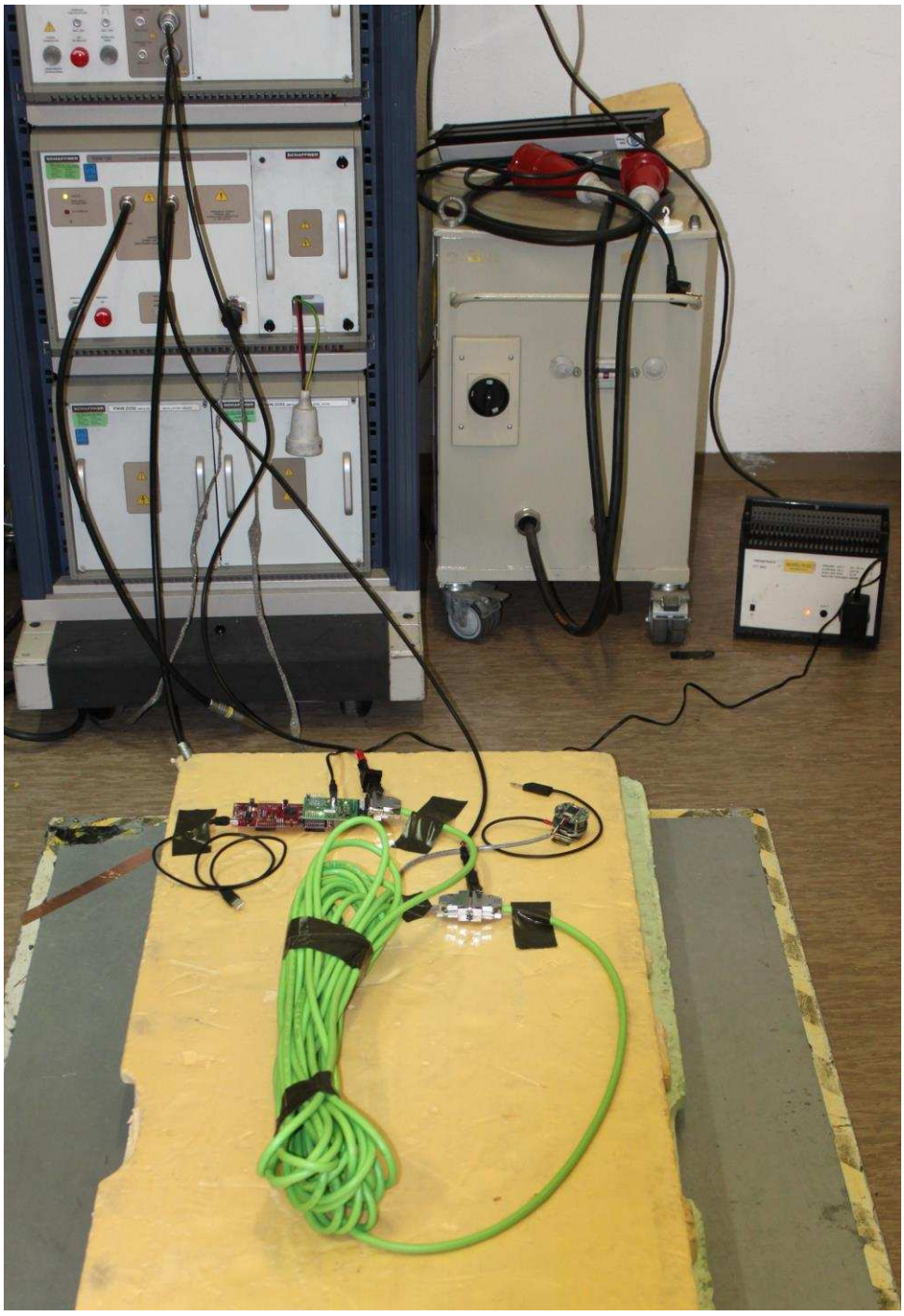


Figure 20. Picture of Surge Test Setup for TIDA-01630

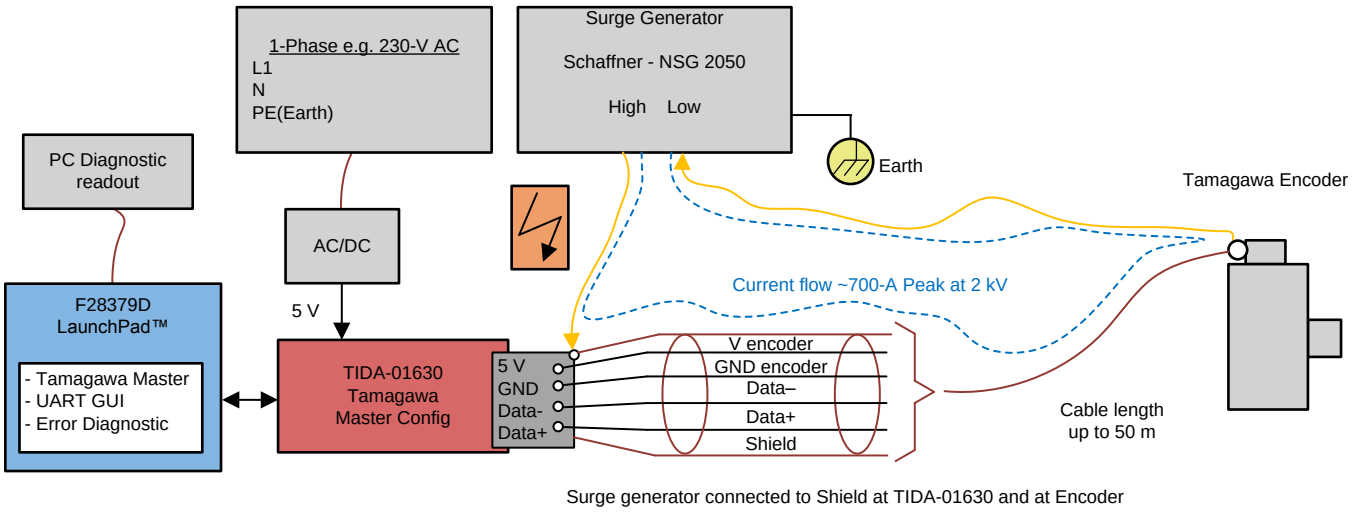


Figure 21. Block Diagram of Surge Test Setup for Data Line of the TIDA-01630

Table 14. EFT Test Results for TIDA-01630 on Data Lines

Phenomenon	Basic Standard	Level	TIDA-01630 Connector	Achieved Performance Criterion	Comment
Surge	IEC61000-4-5	±0.5 kV / 2 Ω (20-m shielded cable)	SubD-15	A	Criterion B required per IEC61800-3
Surge	IEC61000-4-5	±1 kV / 2 Ω (20-m shielded cable)	SubD-15	A	Criterion B required per IEC61800-3
Surge	IEC61000-4-5	±2 kV / 2 Ω (20-m shielded cable)	SubD-15	A	Criterion B required per IEC61800-3

No communication error occurred during the surge tests; neither the angle before and after the tests changed.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01630 .

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01630 .

4.3 PCB Layout

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01630 .

4.3.2 Layout Guidelines

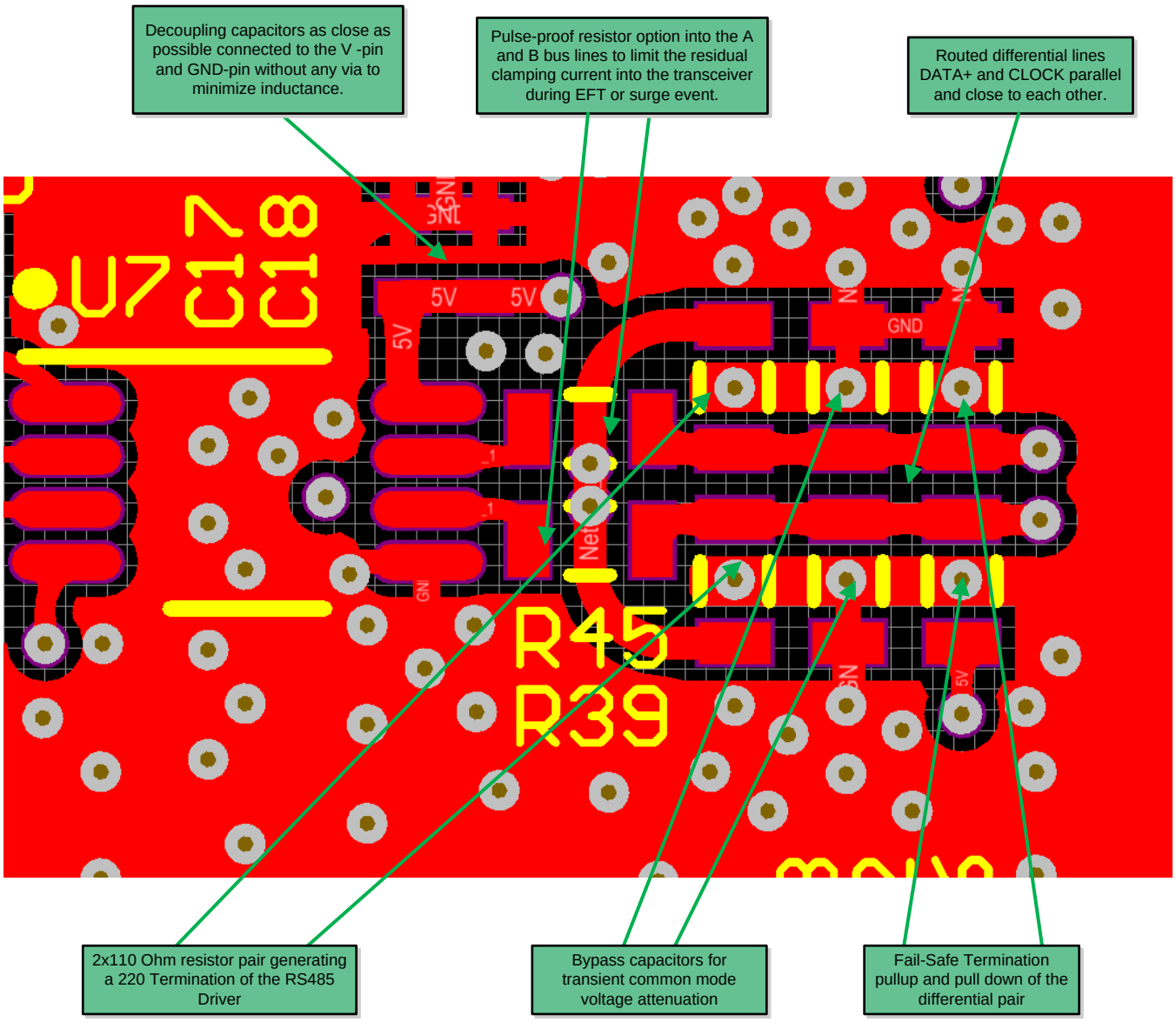


Figure 22. Transceiver Layout Guide Lines

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01630 .

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01630 .

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01630 .

5 Software Files

To download the software files, see the design files at ControlSuite .

6 Related Documentation

1. *Universal Digital Interface to Absolute Position Encoders Reference Design*
2. *C2000™ Position Manager T-Format Library Module*
3. *DesignDRIVE Development Kit IDDK v2.2.1*

6.1 Trademarks

7 Terminology

EFT - Electrical Fast Transient

8 About the Author

KRISTEN MOGENSEN is a system engineer in the Industrial Systems-Motor Drive team at Texas Instruments, responsible for developing reference designs for industrial drives.

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