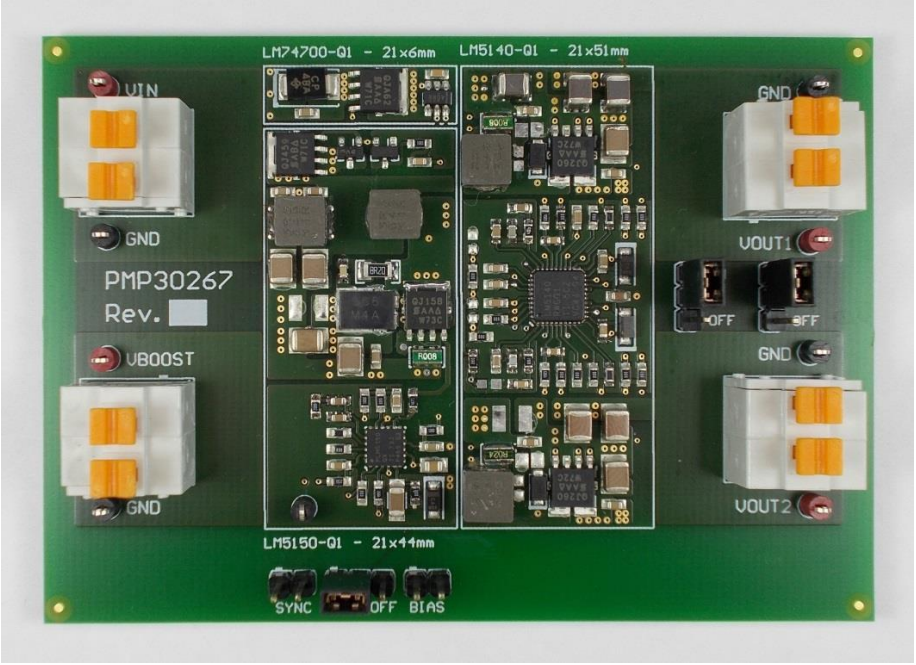
Test Report: PMP30267
Automotive Power Reference Design for Infotainment Systems

Description

This reference design shows a complete power tree for automotive infotainment systems. The LM74700-Q1 provides reverse battery protection to the system and provides immunity to automotive transients specified in ISO 7637-2 and ISO 16750-2. The pre-booster with LM5150-Q1 provides a stable supply voltage of 10.5 V during cranking for the dual-synchronous buck converter with LM5140-Q1 that provides an output voltage of 3.3 V for a load current of 6.0 A and an output voltage of 7.5 V for a load current of 2.5 A.

Automotive Power Solution

- Input 3.2 .. 16.0V / 40.0V peak
- LM74700 Smart Diode Controller
- LM5150-Q1 Pre-Booster
  - Output 10.5V @ 1.5A
  - Free-Running Switching Frequency of 400 kHz
- LM5140-Q1 Dual Synchronous Buck
  - Output 1 3.3V @ 3.0A / 6.0A peak
  - Output 2 7.5V @ 1.5A / 2.5A peak
  - Free-Running Switching Frequency of 440 kHz



1. LM5150 – Startup

The startup waveform at 6.0V input voltage and no load on the 10.5V output is shown in Figure 1.

Channel C1 **6.0V Input Voltage**
2V/div, 2ms/div

Channel C2 **10.5V Output Voltage**
2V/div, 2ms/div

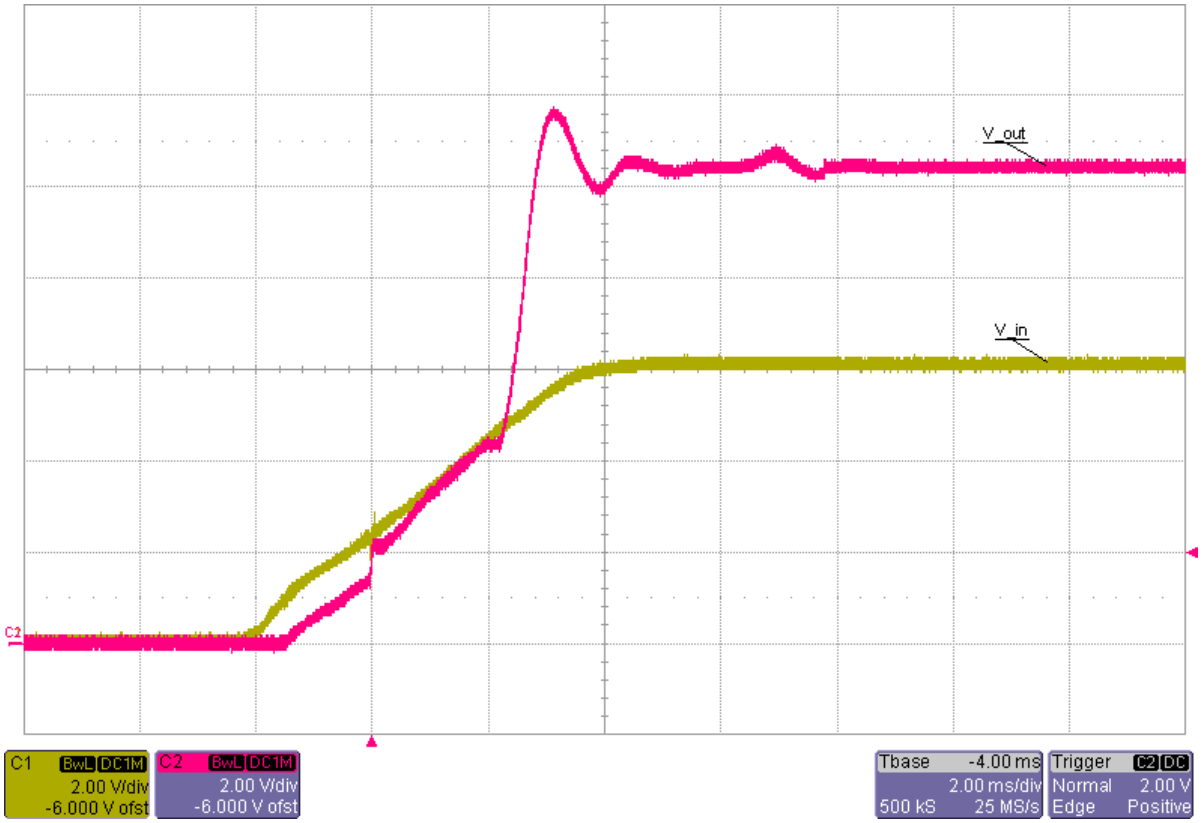


Figure 1

2. LM5150 – Shutdown

The shutdown waveform at 6.0V input voltage and 1.5A load at 10.5V output voltage is shown in Figure 2.

Channel C1 **6.0V Input Voltage**
2V/div, 2ms/div

Channel C1 **10.5V Output Voltage**
2V/div, 2ms/div

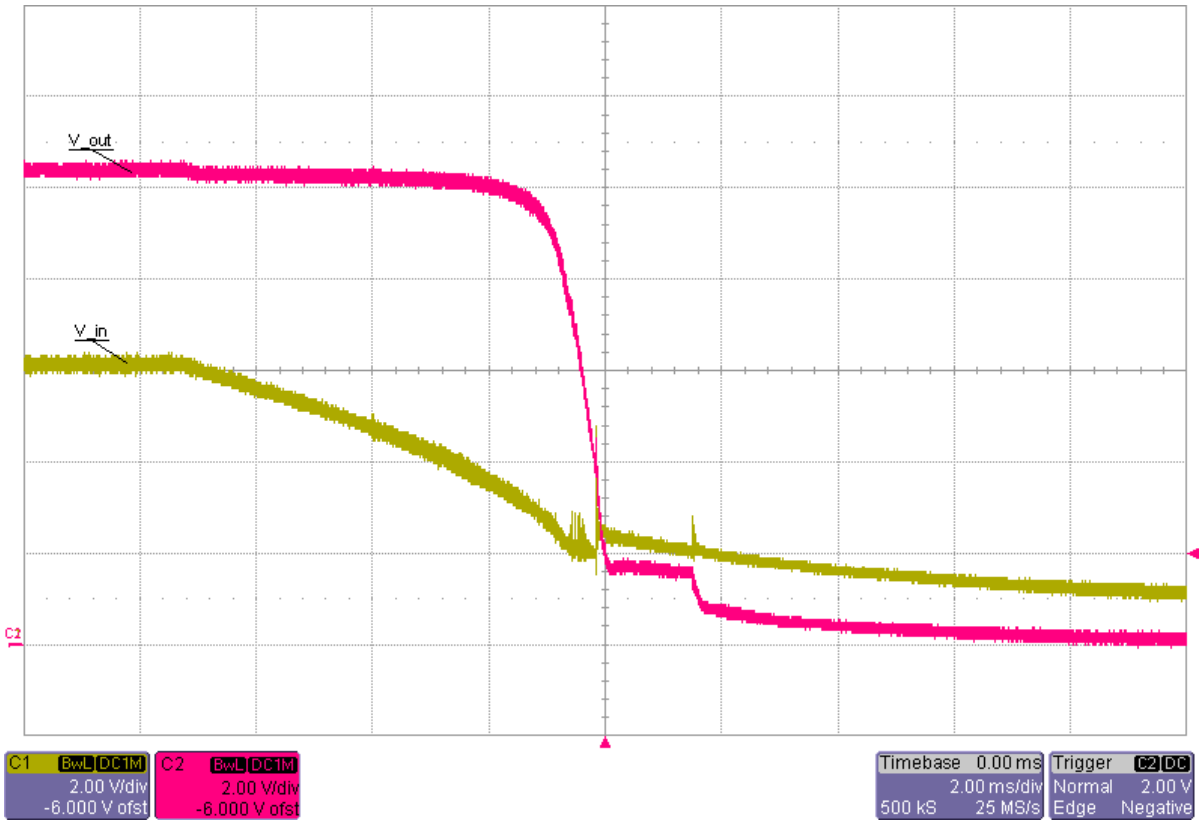


Figure 2

3. LM5150 – Efficiency

The efficiency and load regulation are shown in Figure 3 and Figure 4.

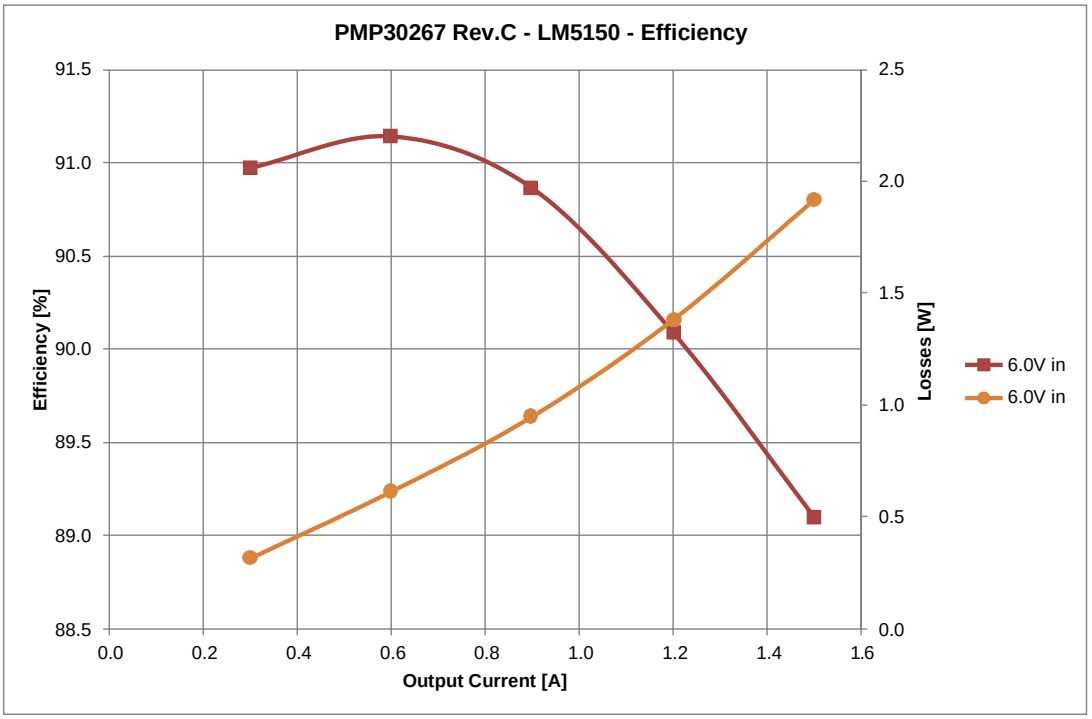


Figure 3

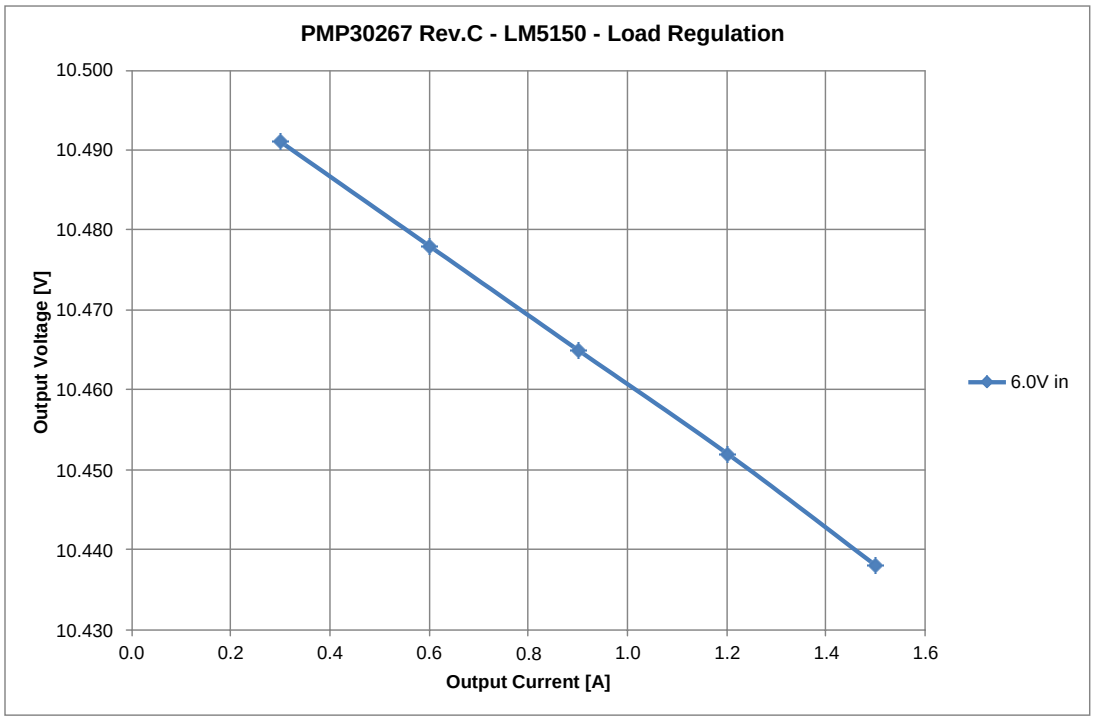


Figure 4

4. LM5150 – Transient Response

The response to a load step at 6.0V input voltage is shown in Figure 5.

Channel C1 **Output Current**, Load Step 1.25A to 2.5A
1A/div, 1ms/div

Channel C2 **Output Voltage**, -1.3V undershoot (12.4%), 1.4V overshoot (13.3%)
1V/div, 1ms/div, AC coupled

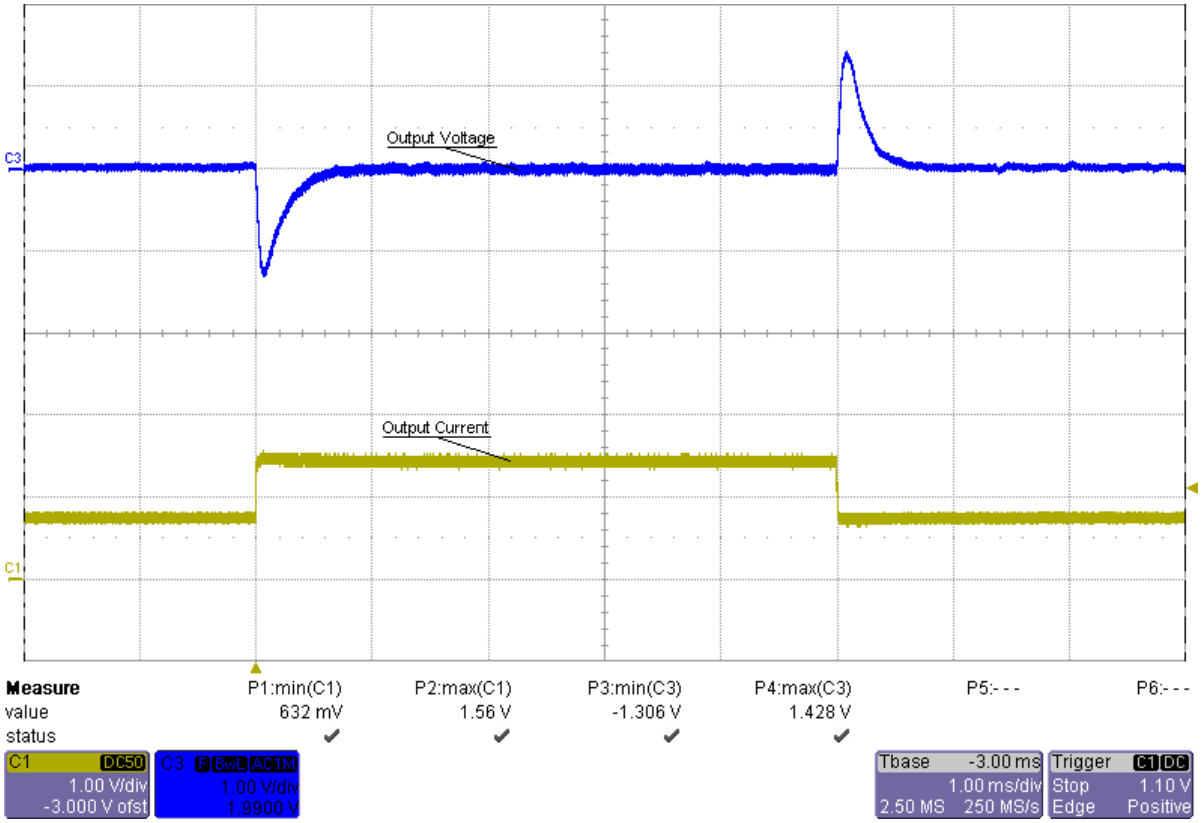


Figure 5

5. LM5150 – Frequency Response

The frequency response is shown in Figure 6.

3.2V Input, 1.5A Load	406 Hz Bandwidth, 62 deg Phase Margin, -19 dB Gain Margin
6.0V Input, 1.5A Load	1.1 kHz Bandwidth, 100 deg Phase Margin, -27 dB Gain Margin
8.0V Input, 1.5A Load	1.1 kHz Bandwidth, 106 deg Phase Margin, -24 dB Gain Margin

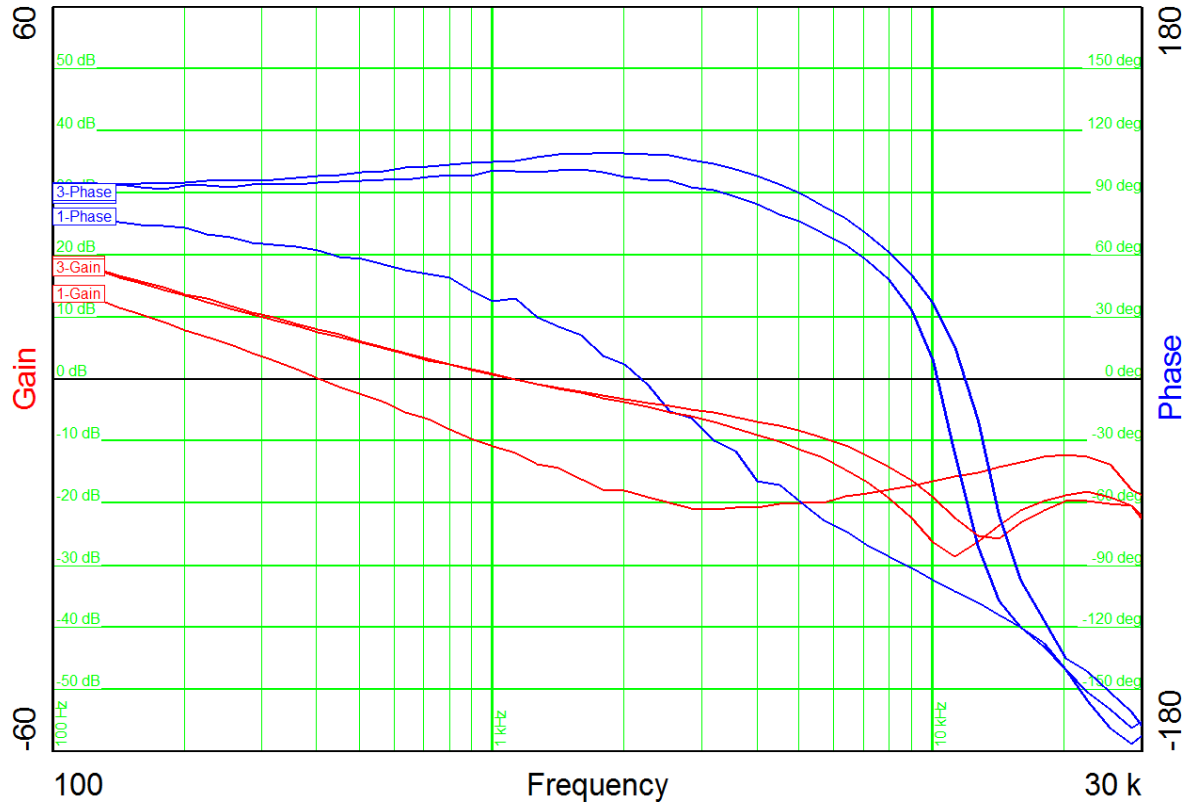


Figure 6

6. LM5150 – Output Ripple

The output ripple voltage is shown in Figure 7.

Channel M1 **Output Voltage @ 3.2V Input / 1.5A Load**, 202mV peak-peak (1.9%)
100mV/div, 1us/div

Channel M2 **Output Voltage @ 6.0V Input / 1.5A Load**, 107mV peak-peak (1.0%)
100mV/div, 1us/div

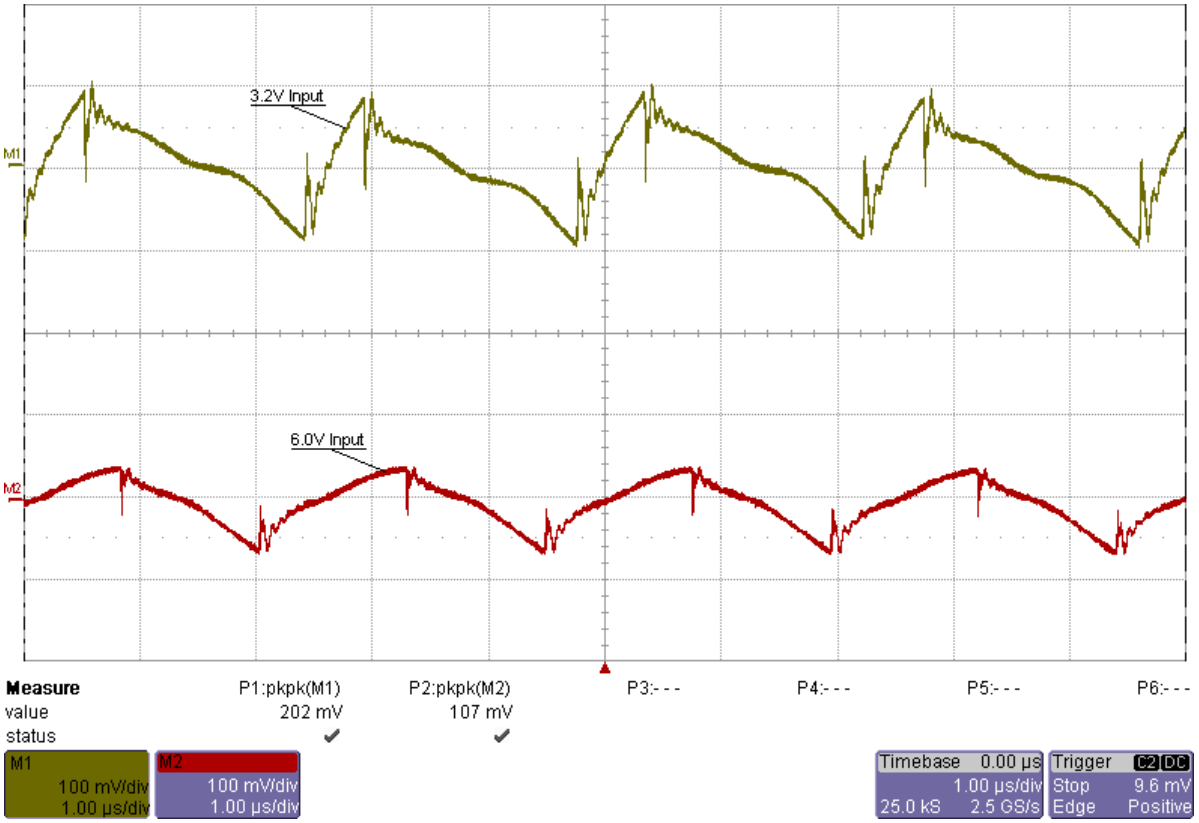


Figure 7

7. LM5150 – Low-Side FET (Switching Node)

The drain-source voltage of the low-side FET at 3.2V input voltage and 1.5A load on the output is shown in Figure 8.

Channel C1 **Drain-Source Voltage**, -1.0V minimum, 20.7V maximum
5V/div, 1us/div

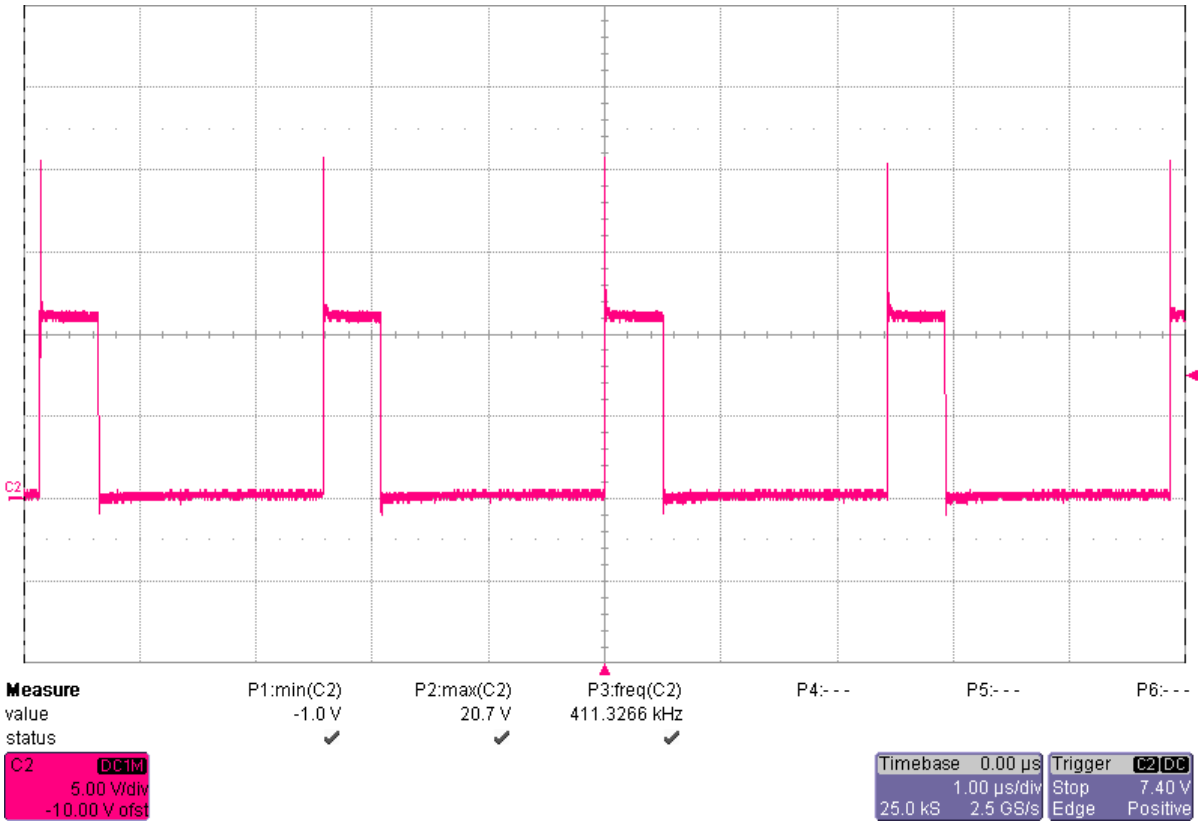


Figure 8

9. LM5150 – Diode Voltage

The voltage of the diode at 3.2V input voltage and 1.5A load on the output is shown in Figure 9.

Channel C1 **Drain-Source Voltage**, -1.7V minimum, 15.1V maximum
5V/div, 1us/div

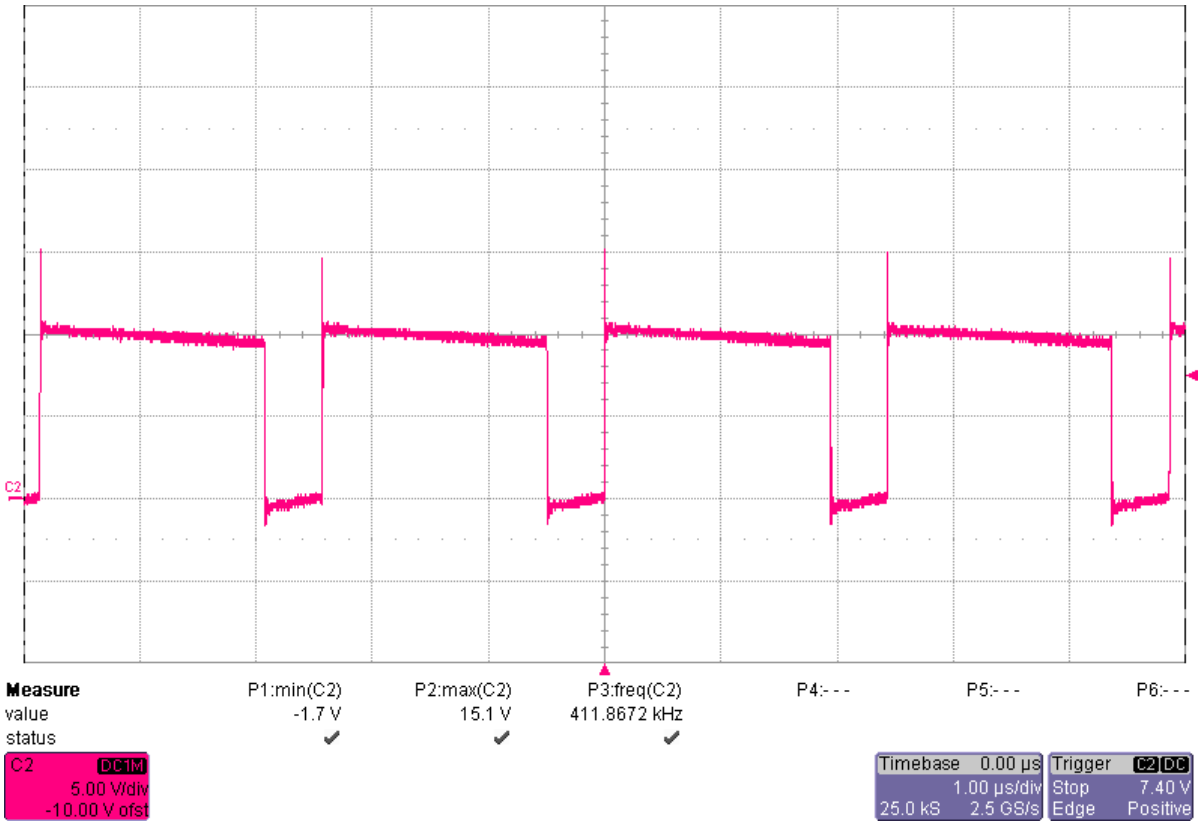


Figure 9

10.LM5150 – Cranking Pulse 1

The response on a cranking pulse (test pulse “severe”, VW 80000) at 1.5A load and 500ms/div is shown in Figure 10.

Channel C1 **Input Voltage**
2V/div, 500ms/div

Channel C2 **10.5V Output Voltage**
2V/div, 500ms/div

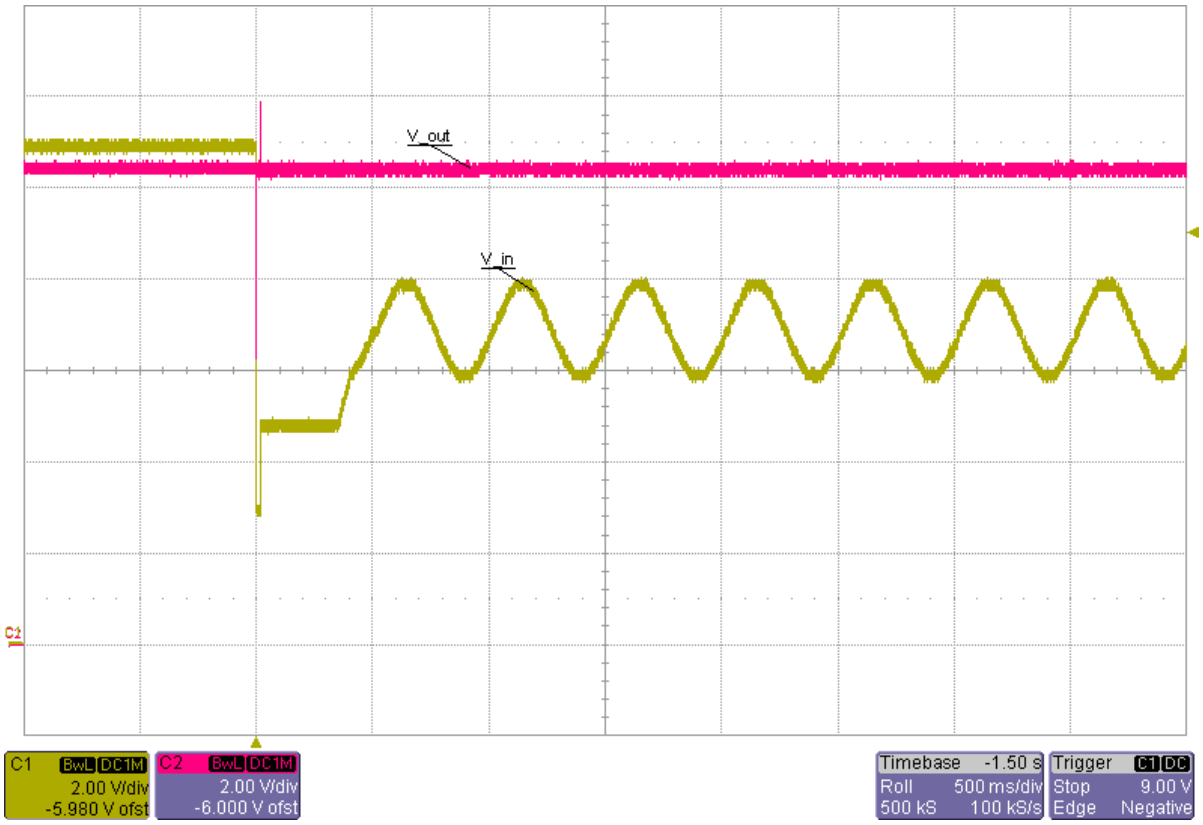


Figure 10

Figure 11 shows a zoom of the most critical point right at the beginning when the input voltage falls from 11.0V to 3.2V within less than 1ms Figure 10.

The output voltage drops down to 6.5V due to very low output capacitance of the boost converter before it recovers and maintains 10.5V.
If this voltage dip is not acceptable, the output capacitance of the boost converter has to be increased.

Channel C1 **Input Voltage**
2V/div, 5ms/div

Channel C2 **10.5V Output Voltage**
2V/div, 5ms/div

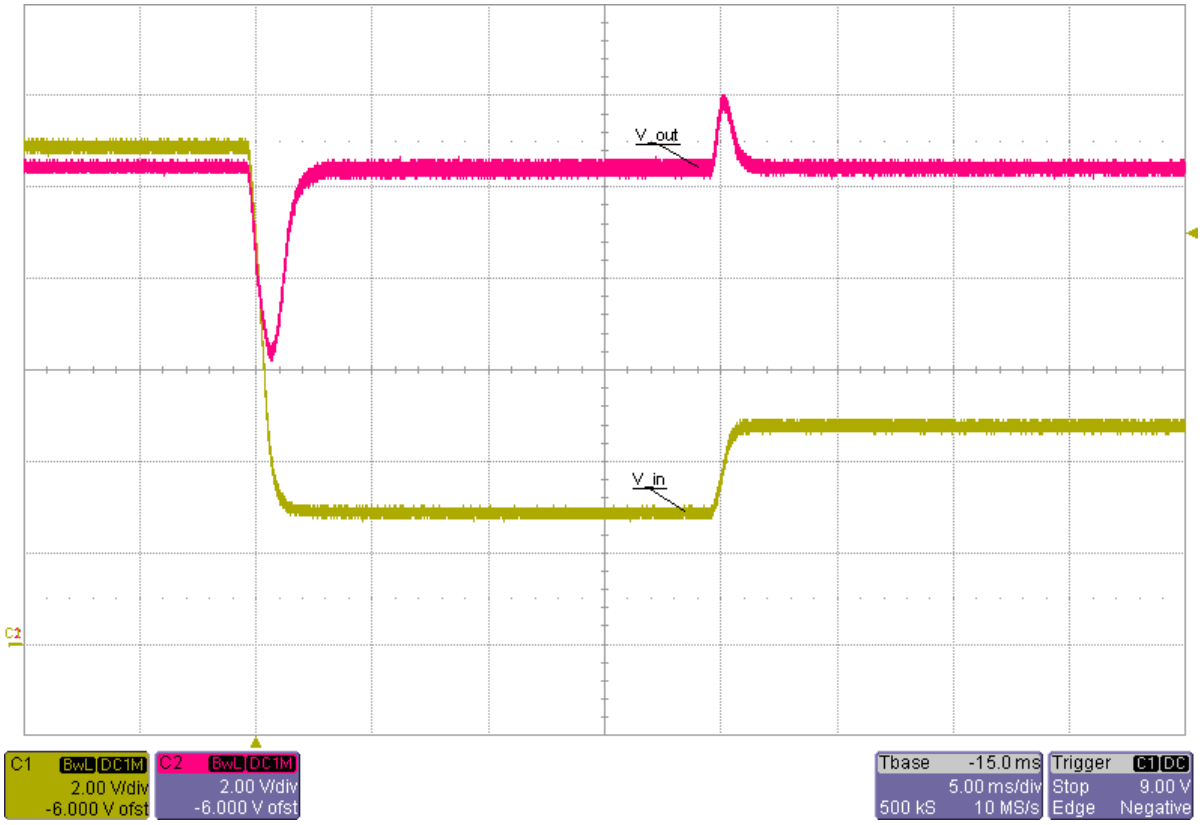


Figure 11

11.LM5150 – Thermal Image

The thermal image (Figure 12Figure 12) shows the circuit at an ambient temperature of 20°C with an input voltage of 6.0V and 1.0A load on the output.

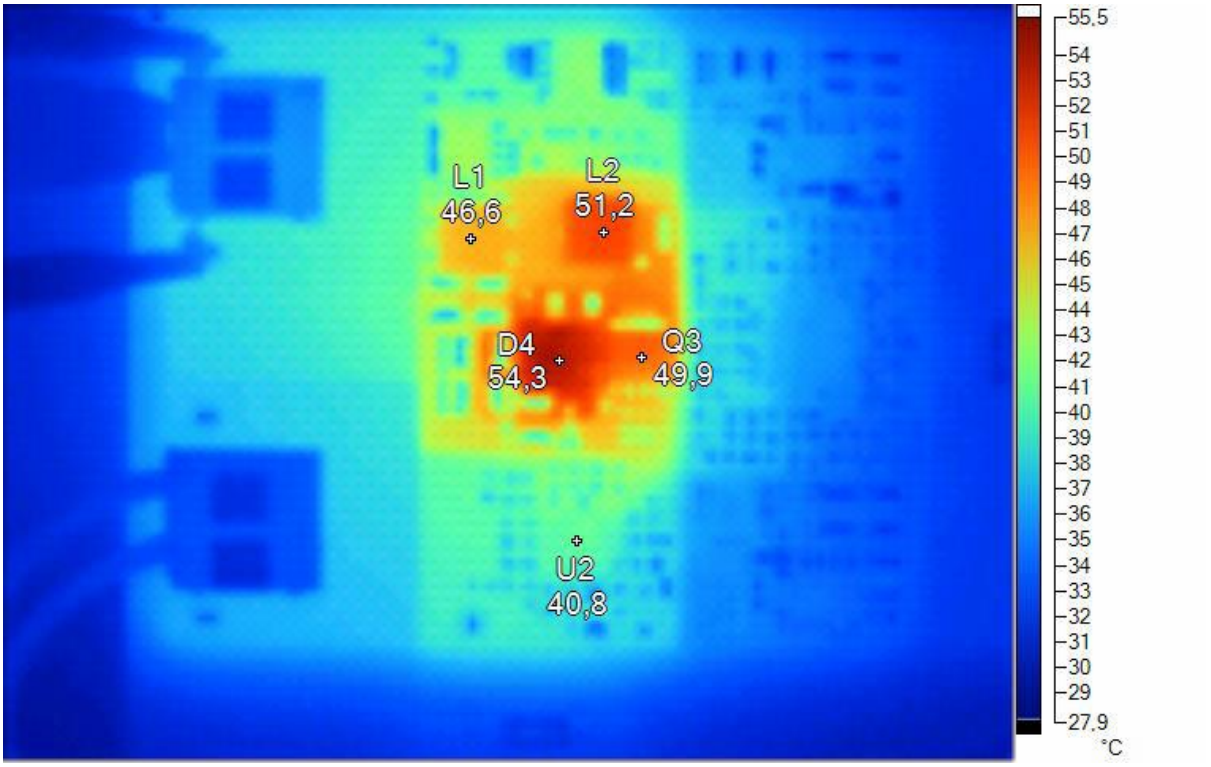


Figure 12

Name	Temperature	Emissivity	Background
D4	54.3°C	0.95	20.0°C
L1	46.6°C	0.95	20.0°C
L2	51.2°C	0.95	20.0°C
Q3	49.9°C	0.95	20.0°C
U2	40.8°C	0.95	20.0°C

12.LM5140 – 3.3V Output – Startup

The startup waveform at 12.0V input voltage and no load on the 3.3V output is shown in Figure 13Figure 1.

Channel C1 **12.0V Input Voltage**
2V/div, 2ms/div

Channel C2 **3.3V Output Voltage**
2V/div, 2ms/div

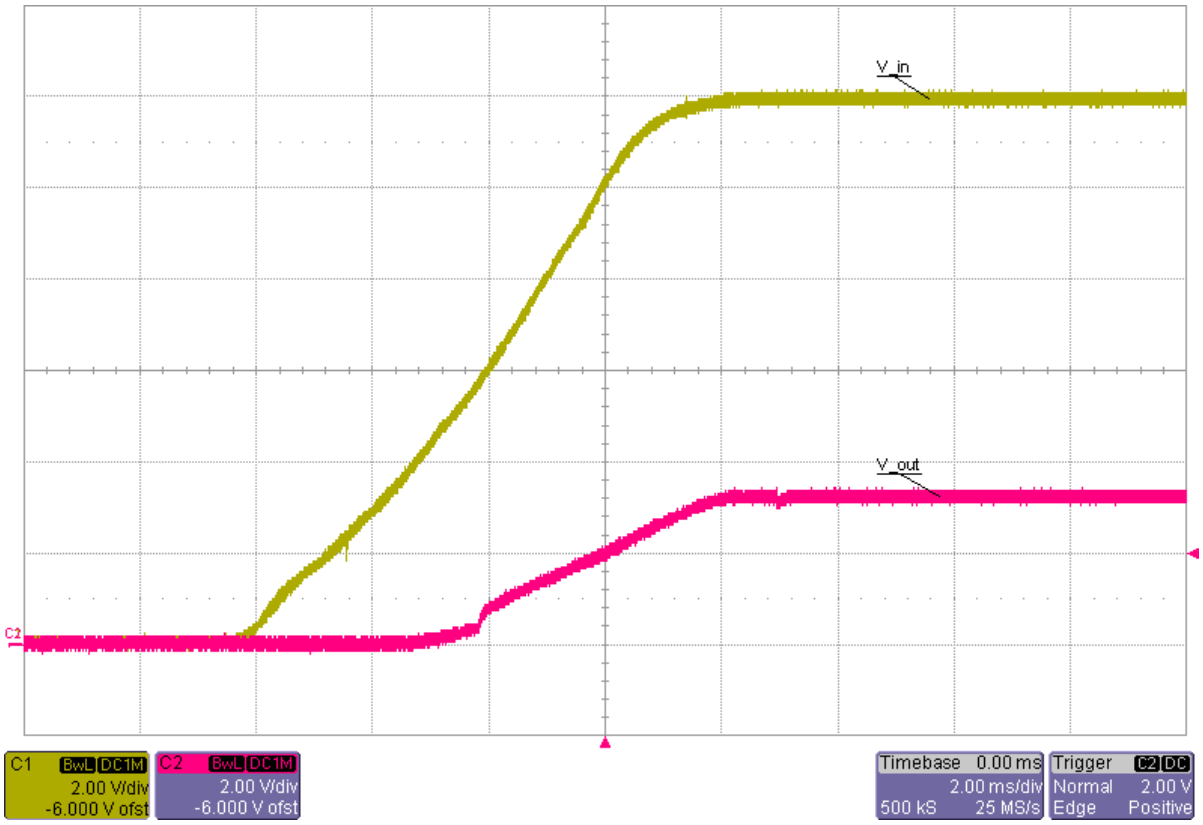


Figure 13

13.LM5140 – 3.3V Output – Shutdown

The shutdown waveform at 12.0V input voltage and 6.0A load at 3.3V output voltage is shown in Figure 14Figure 2.

Channel C1 **12.0V Input Voltage**
2V/div, 1ms/div

Channel C1 **3.3V Output Voltage**
2V/div, 1ms/div

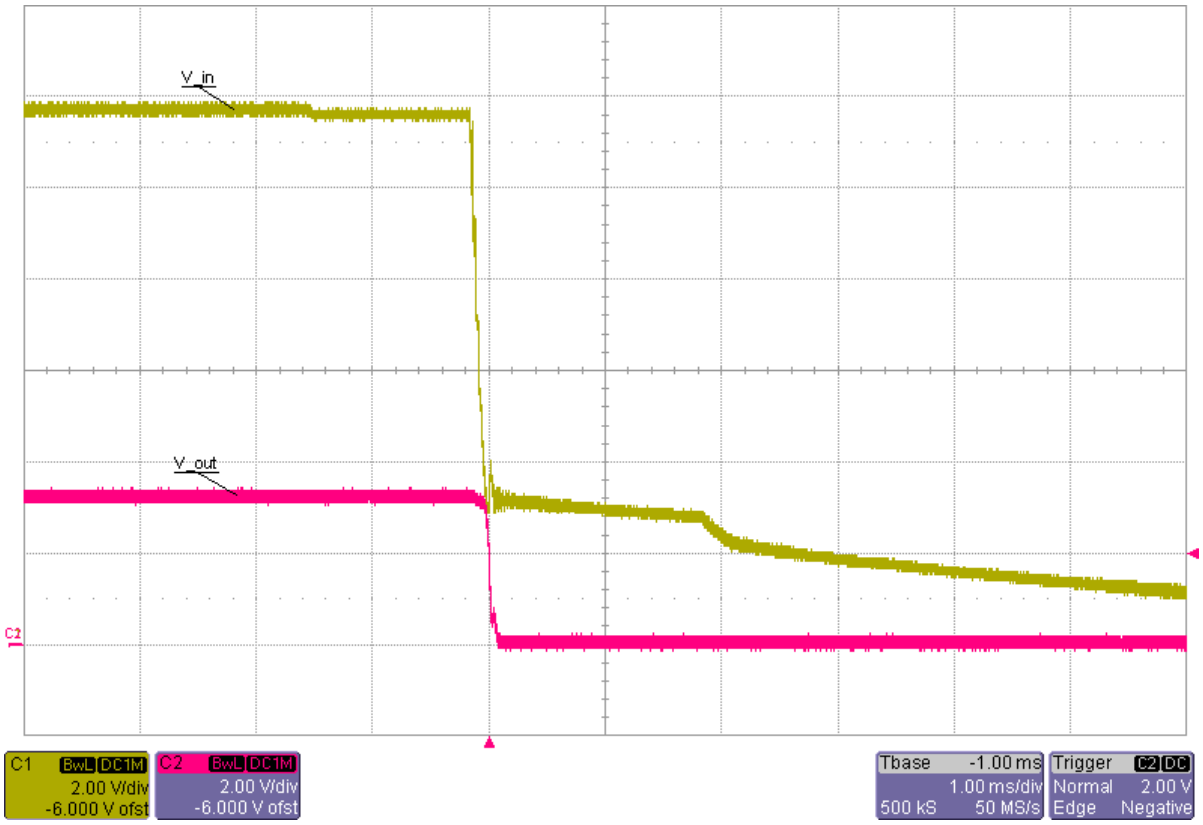


Figure 14

14.LM5140 – 3.3V Output – Efficiency

The efficiency and load regulation are shown in Figure 15Figure 3 and Figure 16Figure 4.

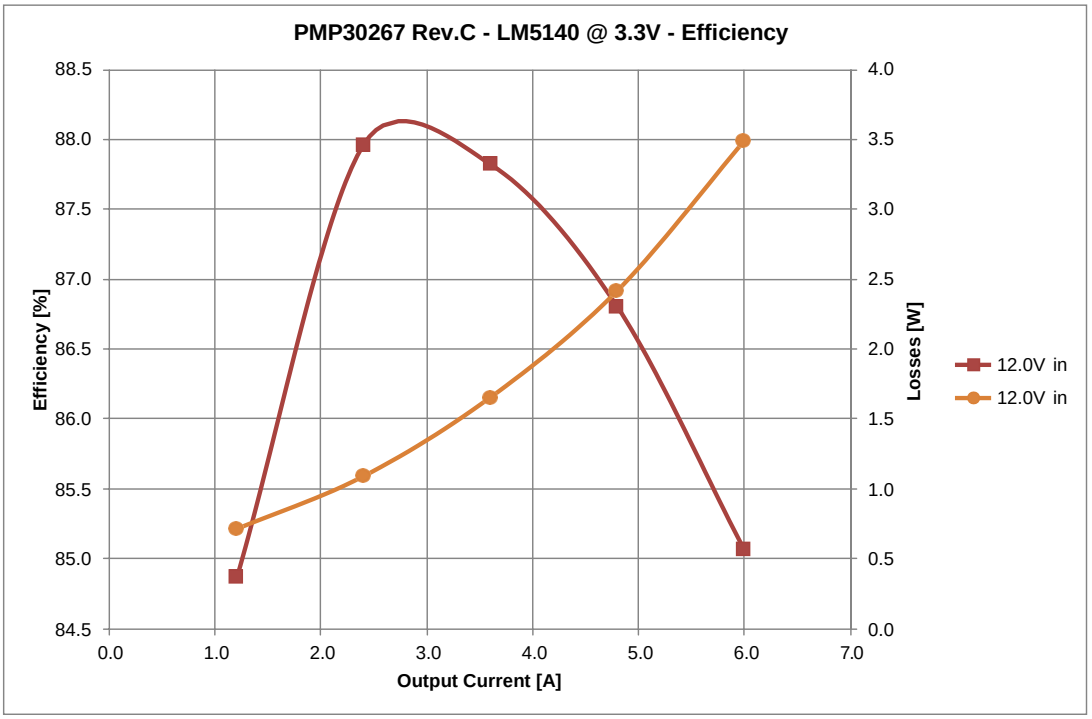


Figure 15

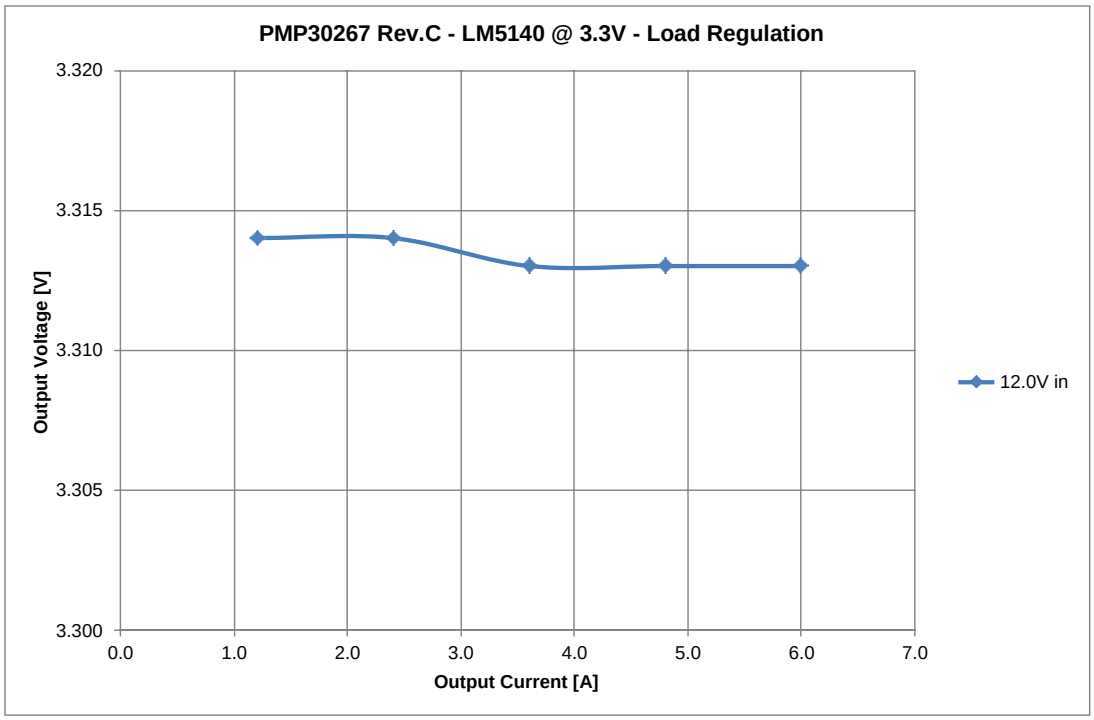


Figure 16

15.LM5140 – 3.3V Output – Transient Response

The response to a load step at 12.0V input voltage is shown in Figure 17Figure 5.

Channel C1 **Output Current**, Load Step 2.0A to 4.0A
2A/div, 1ms/div

Channel C2 **Output Voltage**, -93mV undershoot (2.8%), 85mV overshoot (2.6%)
50mV/div, 1ms/div, AC coupled

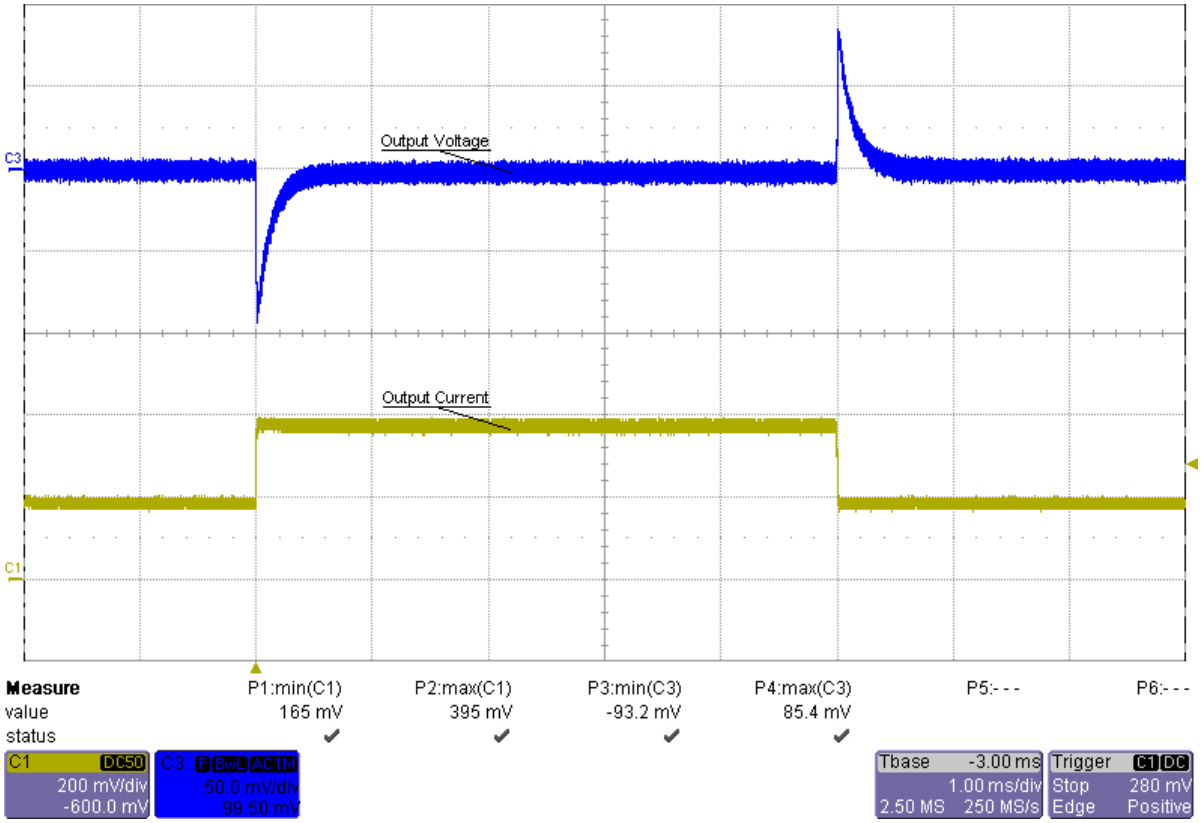


Figure 17

16.LM5140 – 3.3V Output – Frequency Response

The frequency response is shown in Figure 18Figure 17Figure 6.

12.0V Input, 6.0A Load 32.4 kHz Bandwidth, 64 deg Phase Margin, -13 dB Gain Margin

16.0V Input, 6.0A Load 32.5 kHz Bandwidth, 66 deg Phase Margin, -13 dB Gain Margin

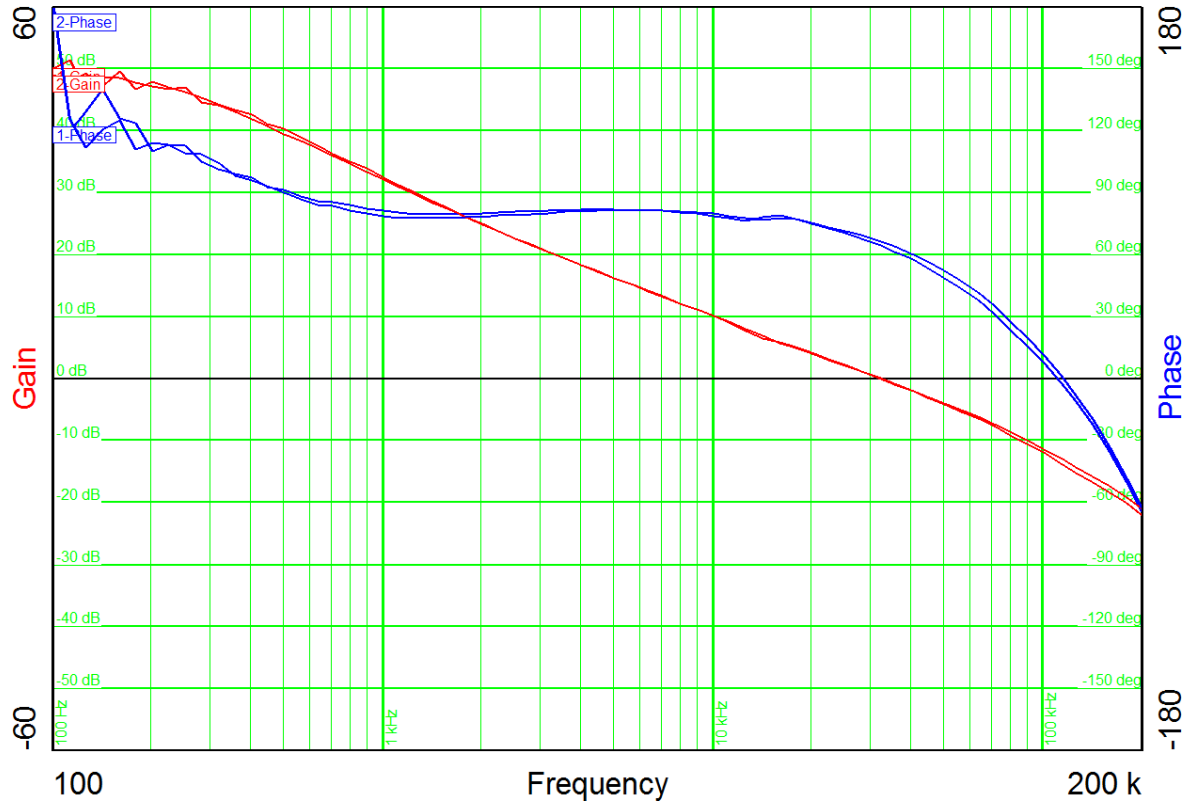


Figure 18

17.LM5140 – 3.3V Output – Output Ripple

The output ripple voltage is shown in Figure 19Figure 7.

Channel M1 **Output Voltage @ 12.0V Input / 6.0A Load**, 77mV peak-peak (2.3%) spikes 50mV/div, 1us/div

Channel M2 **Output Voltage @ 16.0V Input / 6.0A Load**, 80mV peak-peak (2.4%) spikes 50mV/div, 1us/div

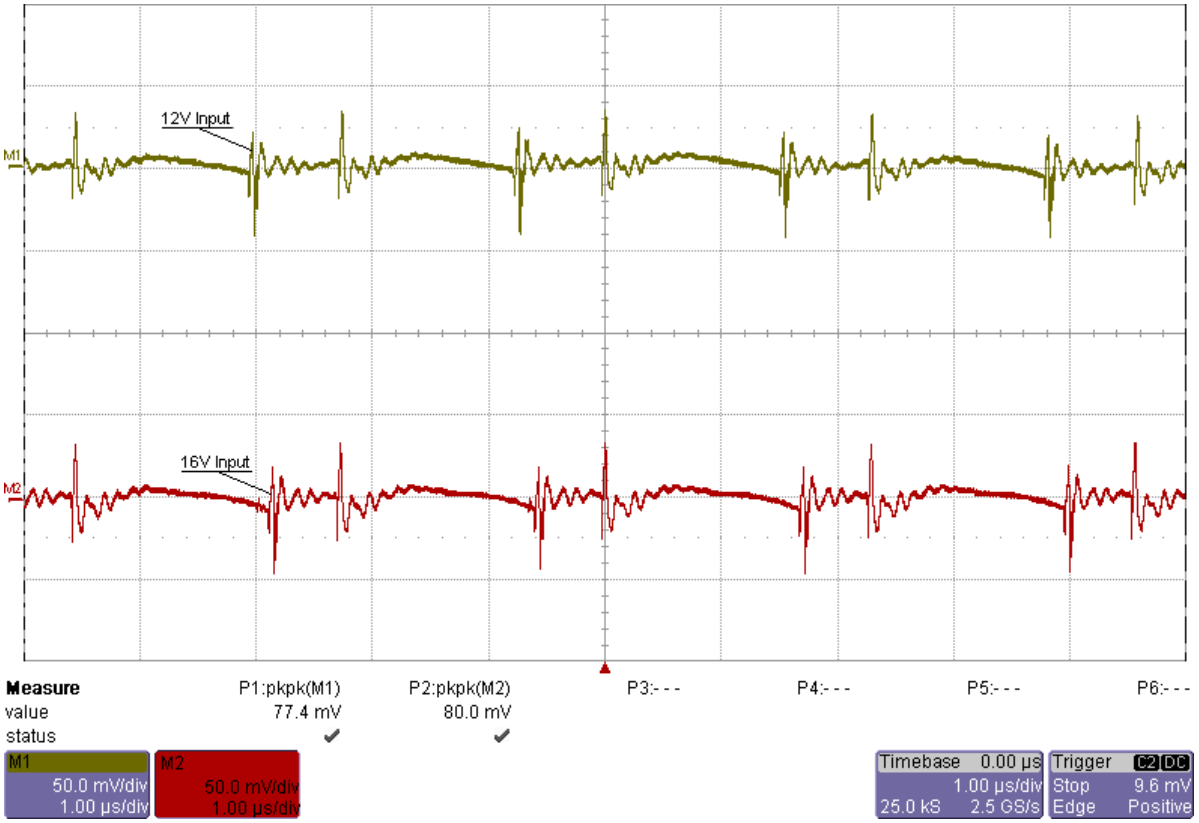


Figure 19

18.LM5140 – 3.3V Output – Low-Side FET (Switching Node)

The drain-source voltage of the low-side FET at 12.0V input voltage and 6.0A load on the output is shown in Figure 20Figure 8.

Channel C1 **Drain-Source Voltage**, -1.2V minimum, 17.9V maximum
5V/div, 1us/div

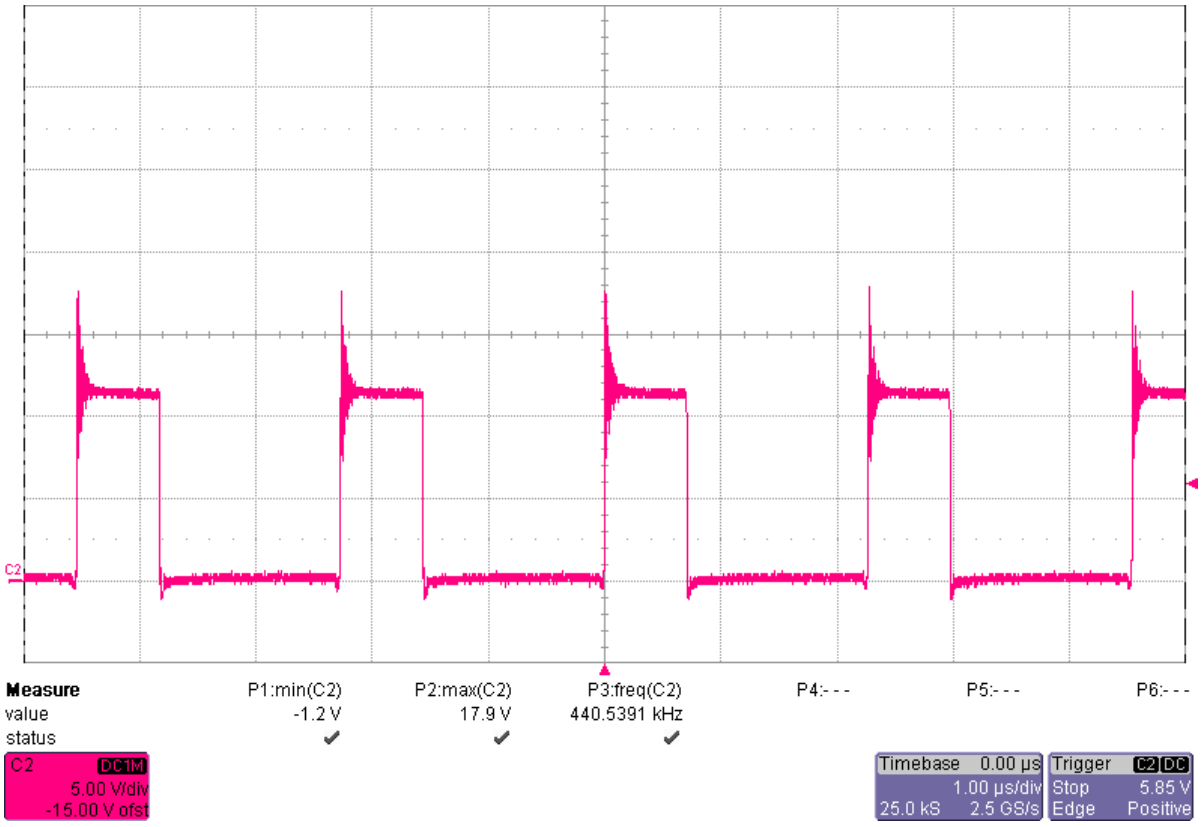


Figure 20

20. LM5140 – 7.5V Output – Startup

The startup waveform at 12.0V input voltage and no load on the 7.5V output is shown in Figure 21Figure 13Figure 1.

Channel C1 **12.0V Input Voltage**
2V/div, 2ms/div

Channel C2 **7.5V Output Voltage**
2V/div, 2ms/div

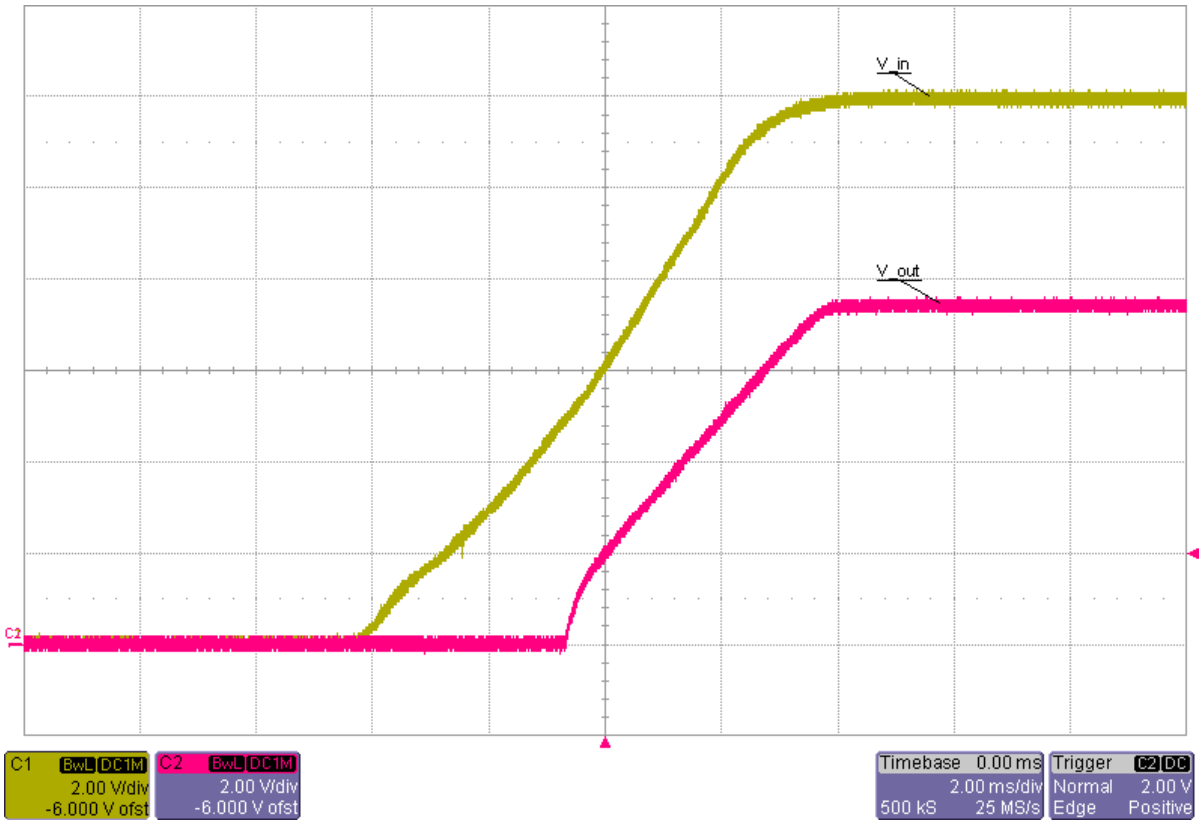


Figure 21

21. LM5140 – 7.5V Output – Shutdown

The shutdown waveform at 12.0V input voltage and 2.5A load at 7.5V output voltage is shown in Figure 22Figure 2.

Channel C1 **12.0V Input Voltage**
2V/div, 1ms/div

Channel C1 **7.5V Output Voltage**
2V/div, 1ms/div

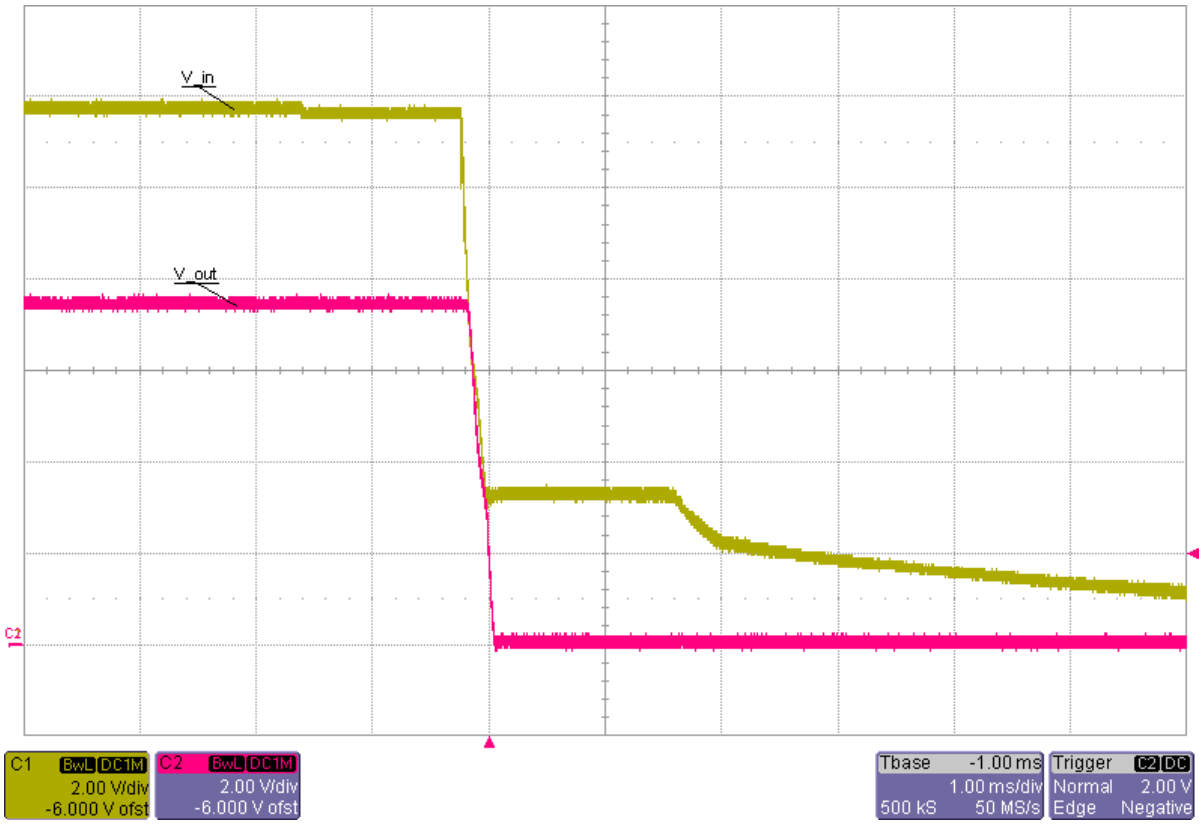


Figure 22

22. LM5140 – 7.5V Output – Efficiency

The efficiency and load regulation are shown in Figure 23Figure 15Figure 3 and Figure 24Figure 16Figure 4.

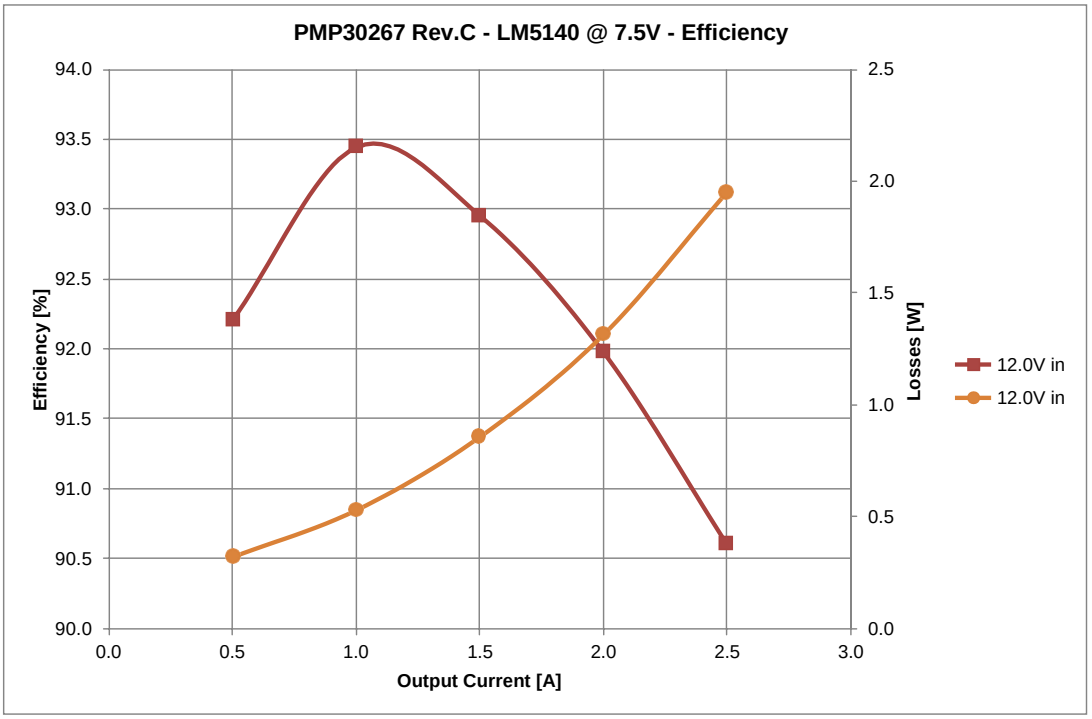


Figure 23

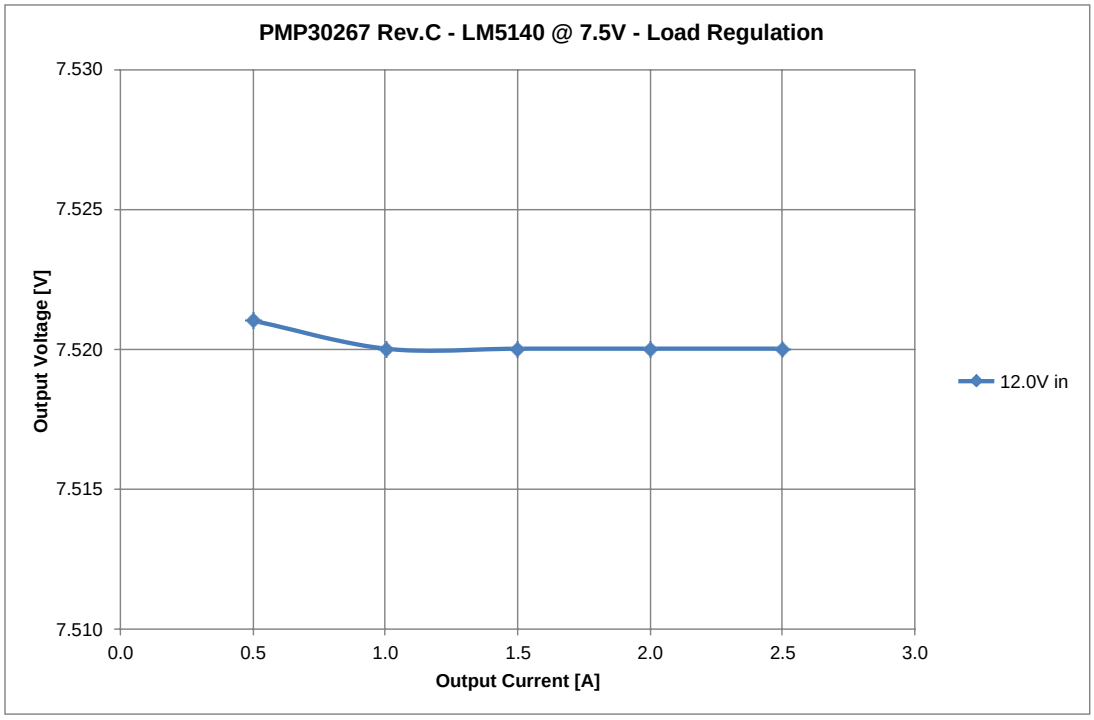


Figure 24

23. LM5140 – 7.5V Output – Transient Response

The response to a load step at 12.0V input voltage is shown in Figure 25Figure 17Figure 5.

Channel C1 **Output Current**, Load Step 1.25A to 2.5A
1A/div, 1ms/div

Channel C2 **Output Voltage**, -137mV undershoot (1.8%), 150mV overshoot (2.0%)
100mV/div, 1ms/div, AC coupled

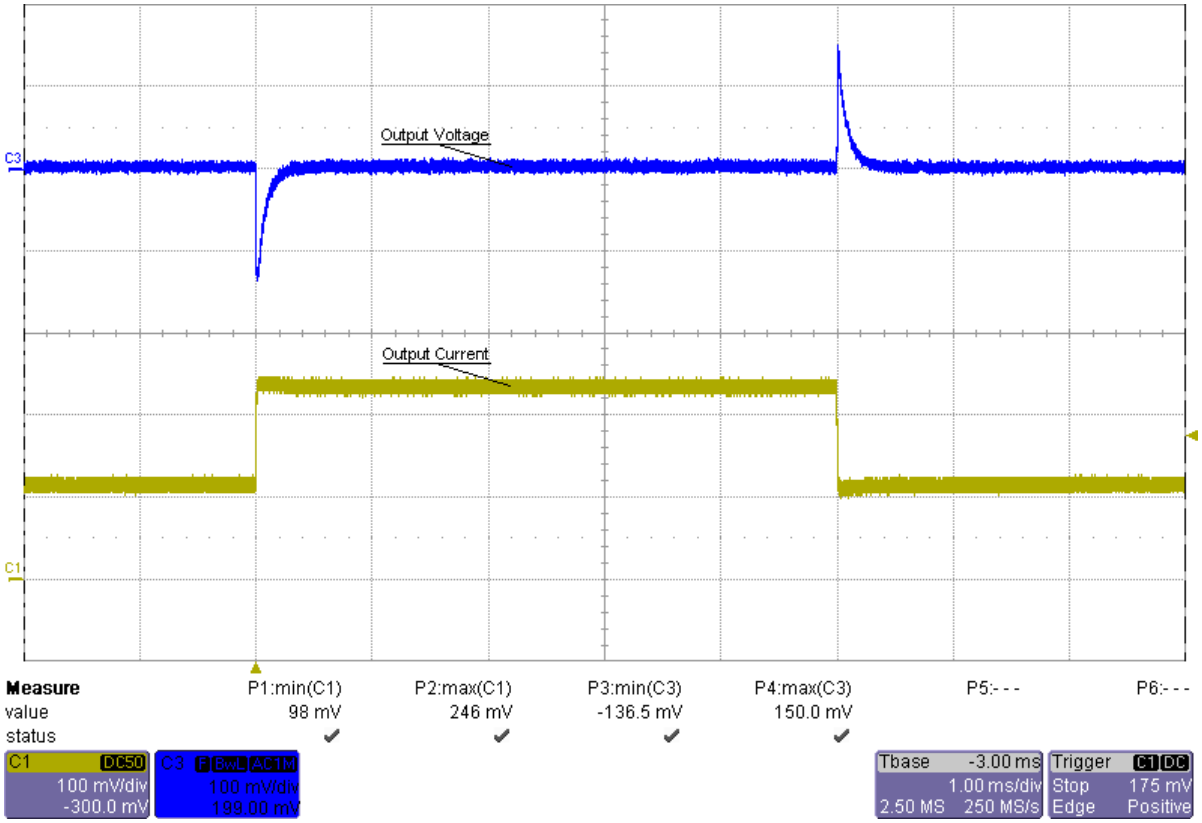


Figure 25

24. LM5140 – 7.5V Output – Frequency Response

The frequency response is shown in Figure 26Figure 18Figure 17Figure 6.

12.0V Input, 2.5A Load	40.5 kHz Bandwidth, 59 deg Phase Margin, -13 dB Gain Margin
16.0V Input, 2.5A Load	36.7 kHz Bandwidth, 52 deg Phase Margin, -15 dB Gain Margin

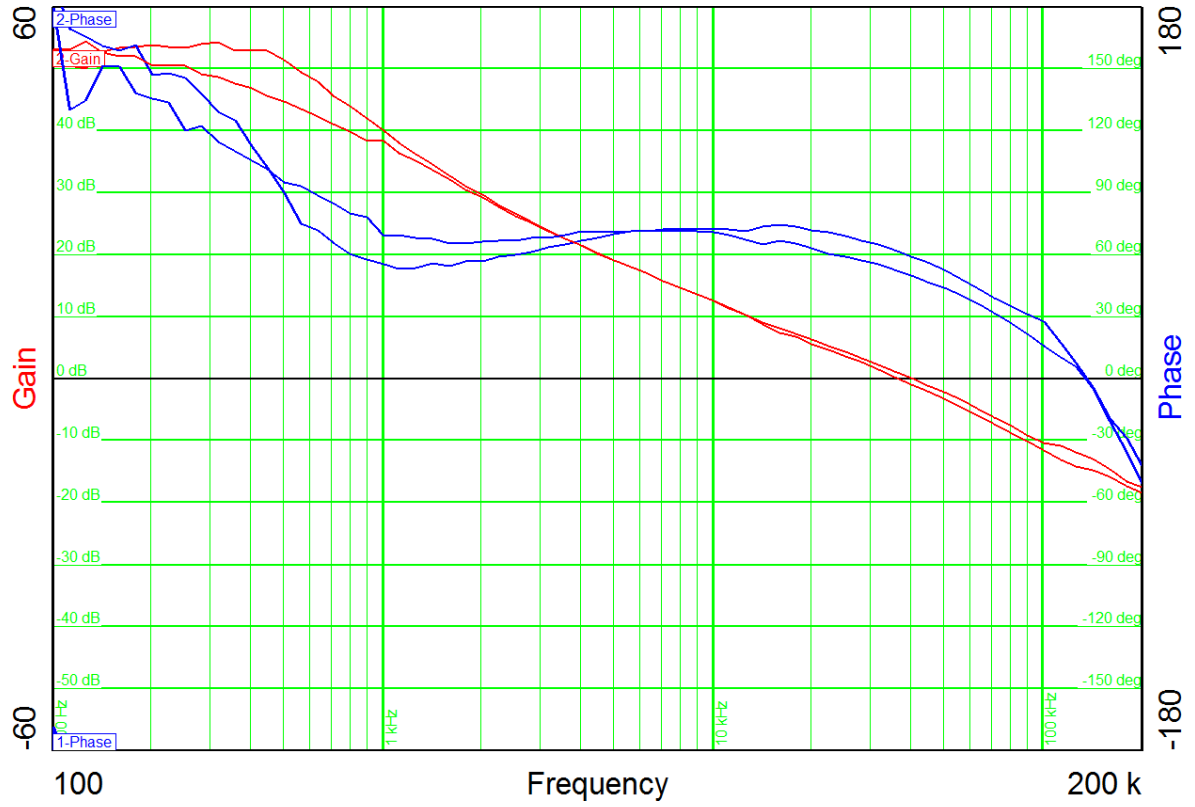


Figure 26

25. LM5140 – 7.5V Output – Output Ripple

The output ripple voltage is shown in Figure 27Figure 19Figure 7.

Channel M1 **Output Voltage @ 12.0V Input / 2.5A Load**, 83mV peak-peak (1.1%) spikes 50mV/div, 1us/div

Channel M2 **Output Voltage @ 16.0V Input / 2.5A Load**, 85mV peak-peak (1.1%) spikes 50mV/div, 1us/div

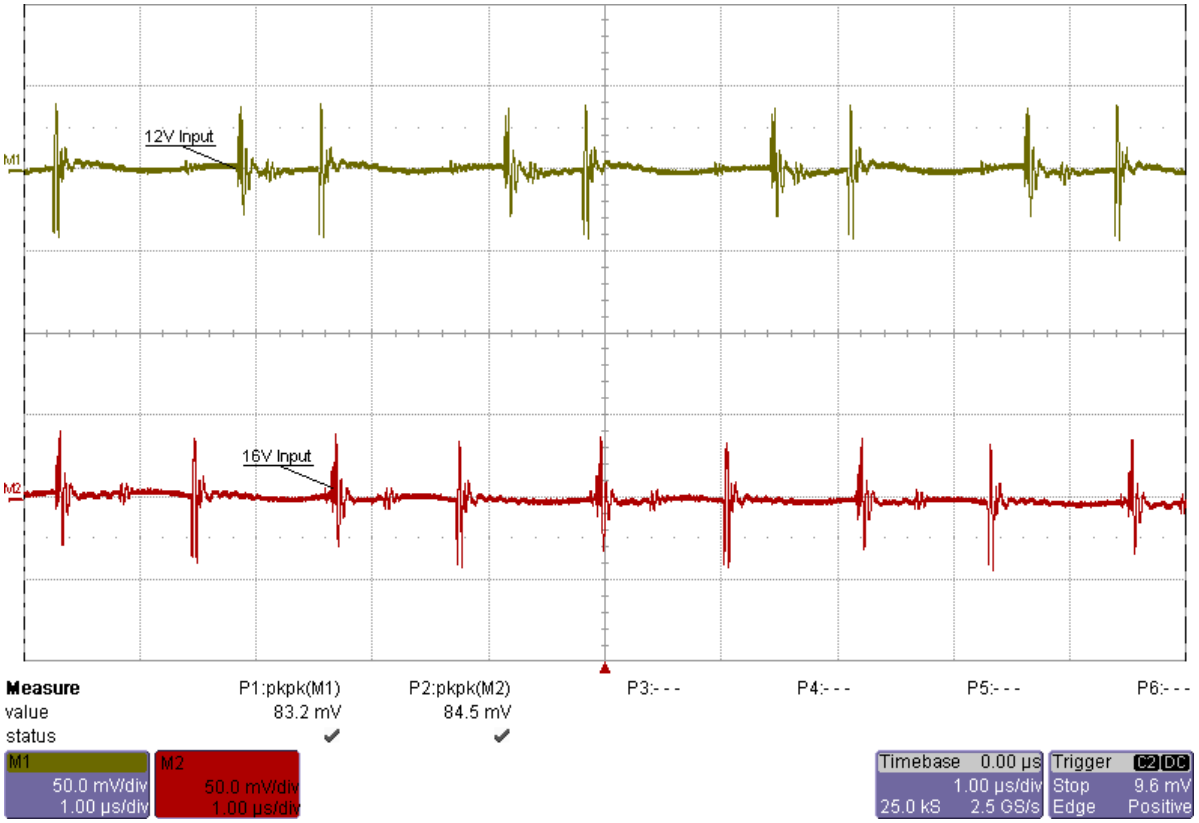


Figure 27

26. LM5140 – 7.5V Output – Low-Side FET (Switching Node)

The drain-source voltage of the low-side FET at 12.0V input voltage and 2.5A load on the output is shown in Figure 28Figure 20Figure 8.

Channel C1 **Drain-Source Voltage**, -1.0V minimum, 20.9V maximum
5V/div, 1us/div

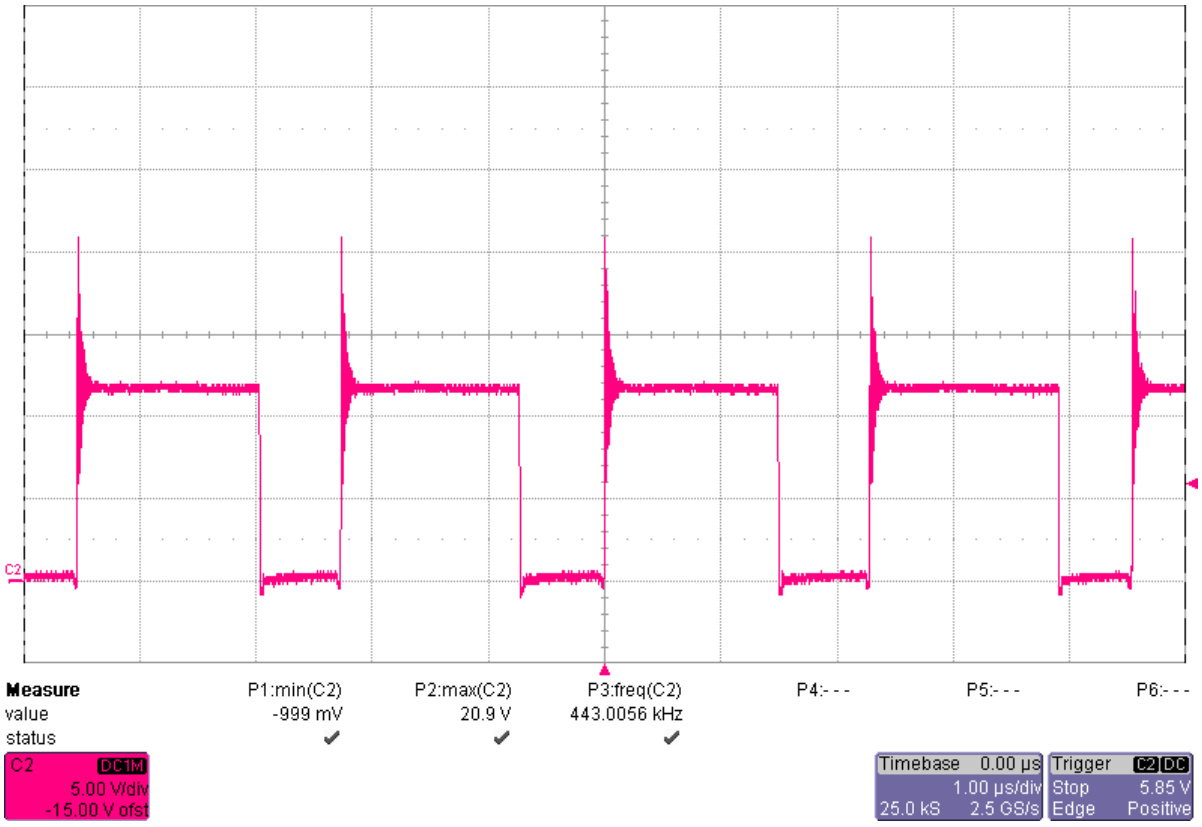


Figure 28

28. LM5140 – Thermal Image

The thermal image (Figure 12Figure 29) shows the circuit at an ambient temperature of 20°C with an input voltage of 12.0V, 3.0A load on the 3.3V output and 1.5A load on the 7.5V output.

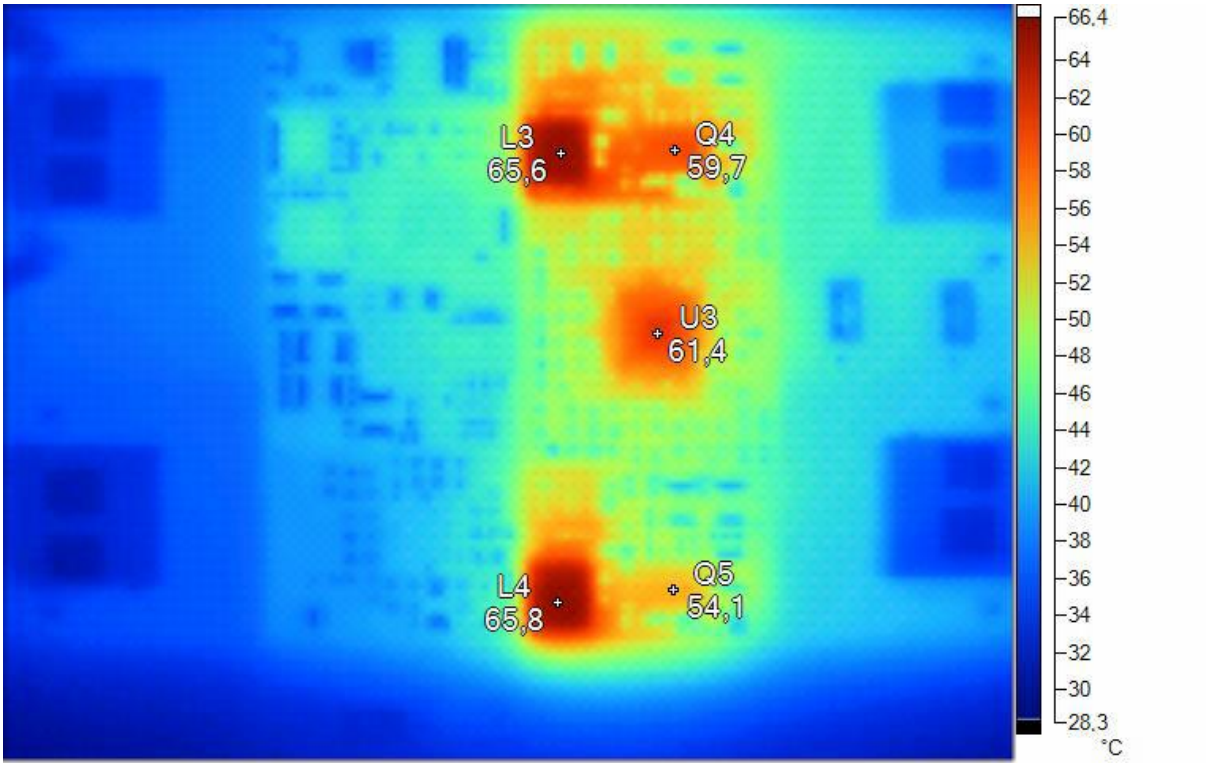


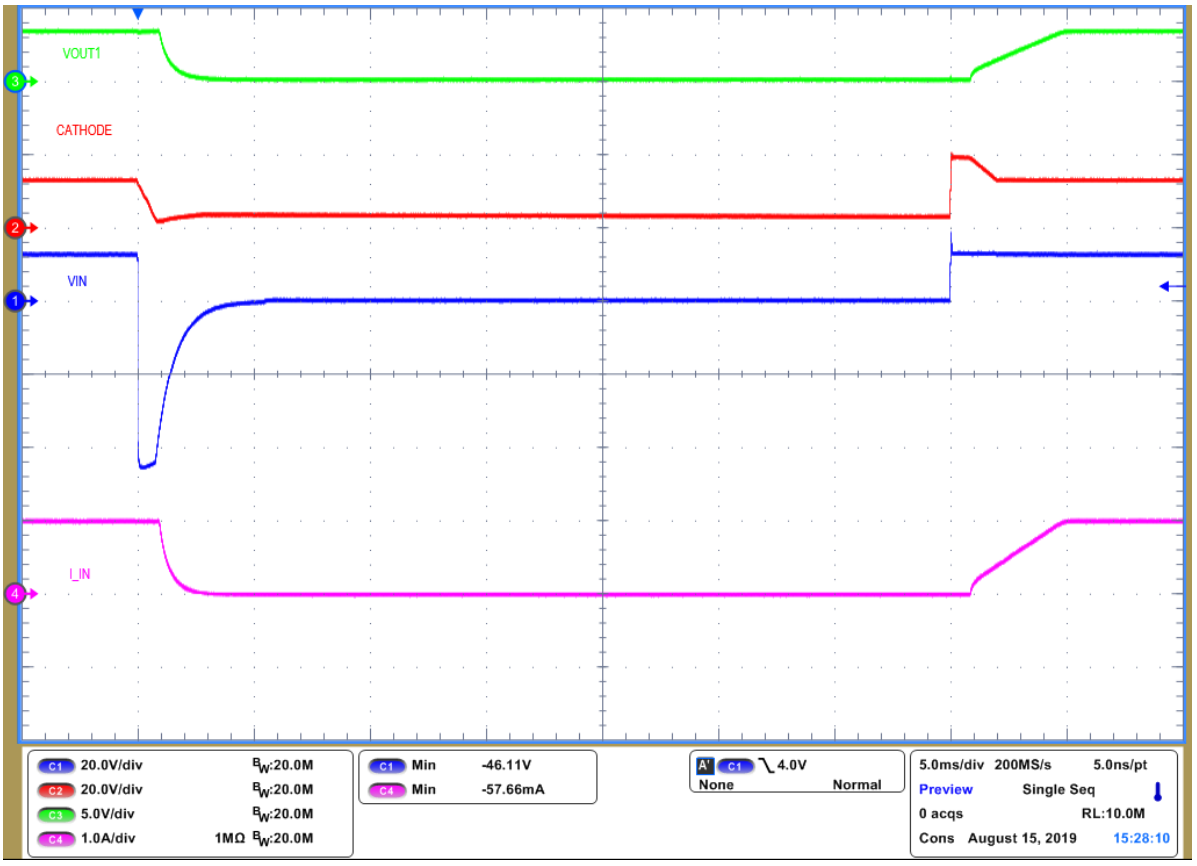
Figure 29

Name	Temperature	Emissivity	Background
L3	65.6°C	0.95	20.0°C
L4	65.8°C	0.95	20.0°C
Q4	59.7°C	0.95	20.0°C
Q5	54.1°C	0.95	20.0°C
U3	61.4°C	0.95	20.0°C

29. LM74700-Q1 ISO 7637-2 Pulse 1 Response: VOUT1

Response to ISO 7637-2 Pulse 1 applied at the input connector J1 is captured in Figure 29. LM74700-Q1 turns off Q2 as input voltage swings negative and clamped by SMBJ36CA TVS diode D2. The 3.3V output of LM5140-Q1 turns off and recovers when the input voltage returns to 12V.

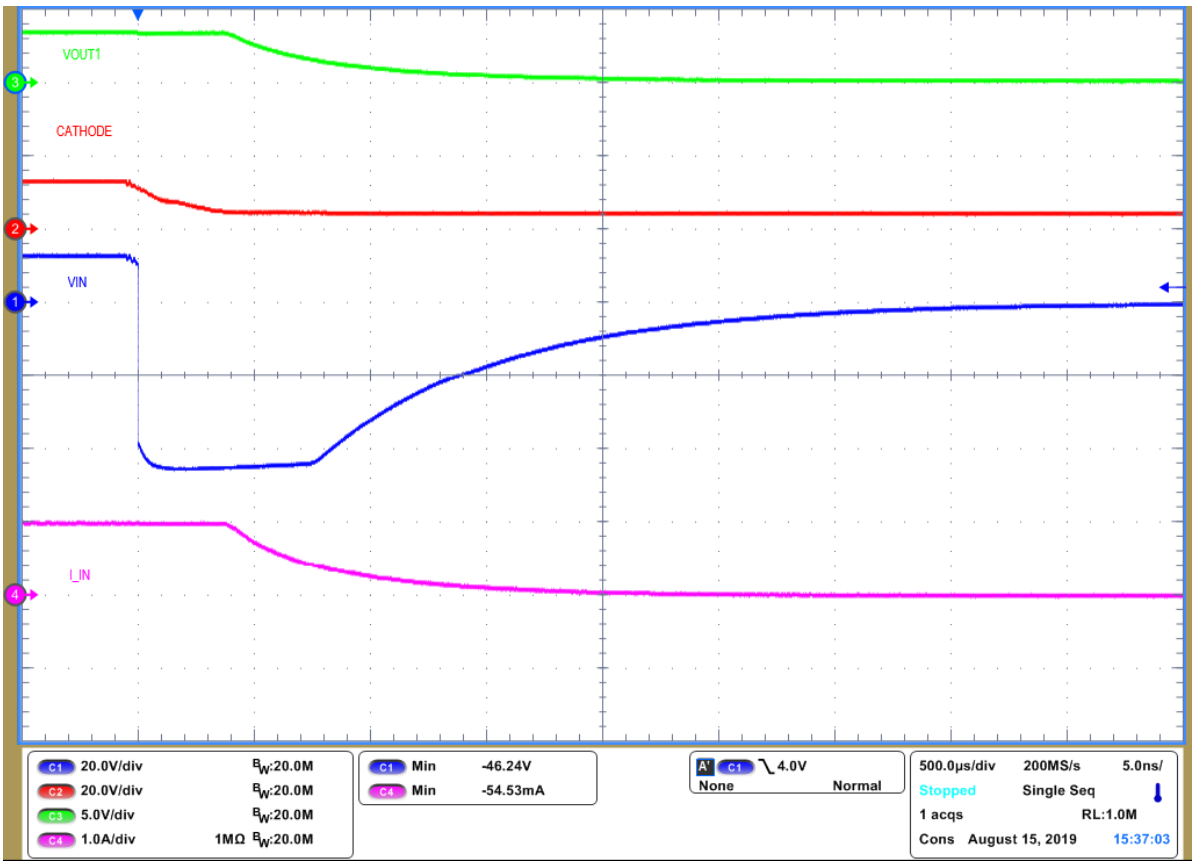
Channel 1	**12.0V Input Voltage @ J1**
	5.0ms/div
Channel 2	**12.0V Cathode Voltage of LM74700-Q1**
	5.0ms/div
Channel 3	**3.3V Output Voltage of LM5140-Q1 @ VOUT1**
	5.0ms/div
Channel 4	**Load Current @ 3.3V VOUT1**
	5.0ms/div



30. LM74700-Q1 ISO 7637-2 Pulse 1 Response: VOUT1 Zoomed

Response to ISO 7637-2 Pulse 1 applied at the input connector J1 is captured in Figure 30 at a smaller time scale. LM74700-Q1 turns off Q2 and cuts off downstream circuits from negative voltage. VOUT1 turns off as the cathode voltage of LM74700-Q1 ramps down.

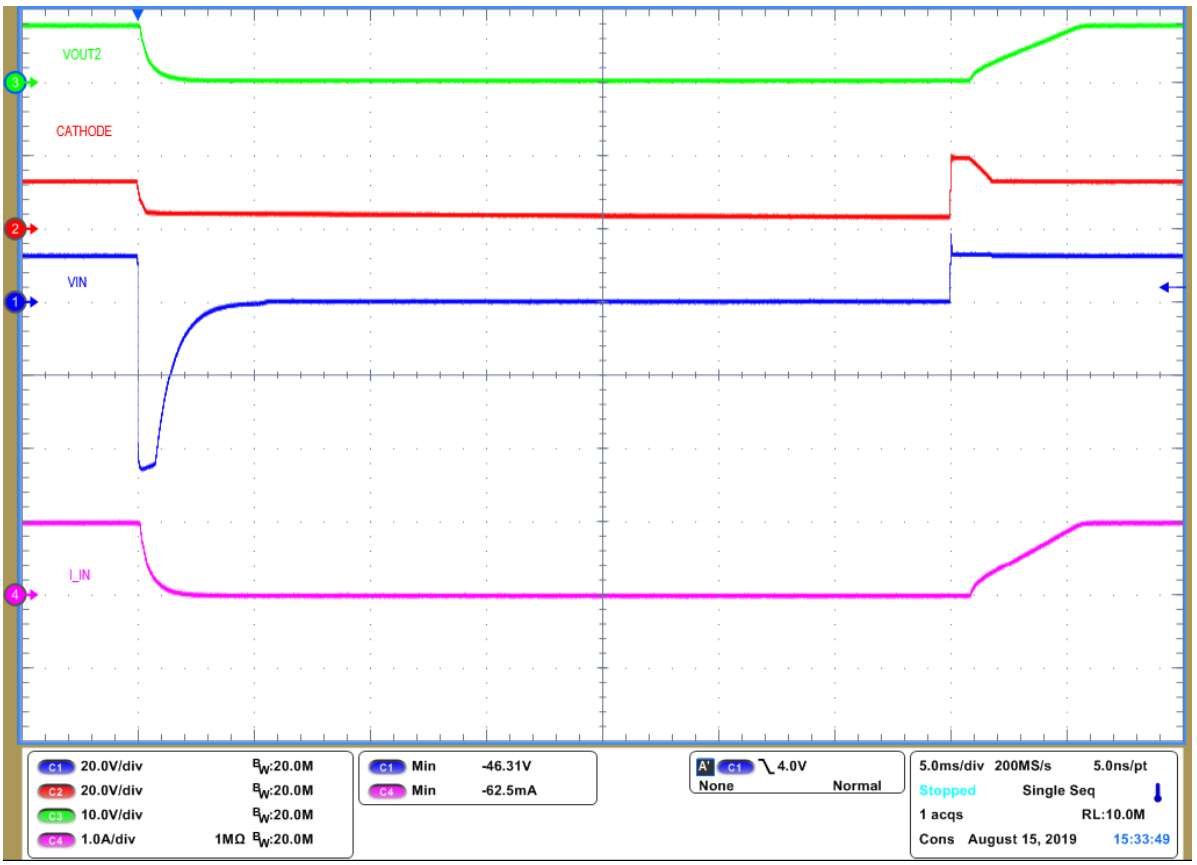
Channel 1 **12.0V Input Voltage @ J1**
500.0µs/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
500.0µs/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
500.0µs/div
Channel 4 **Load Current @ 3.3V VOUT1**
500.0µs/div



31. LM74700-Q1 ISO 7637-2 Pulse 1 Response: VOUT2

Response to ISO 7637-2 Pulse 1 applied at the input connector J1 is captured in Figure 31. LM74700-Q1 turns off Q2 and cuts off downstream circuits from negative voltage. The 7.5V output of LM5140-Q1 turns off and recovers when the input voltage returns to 12V.

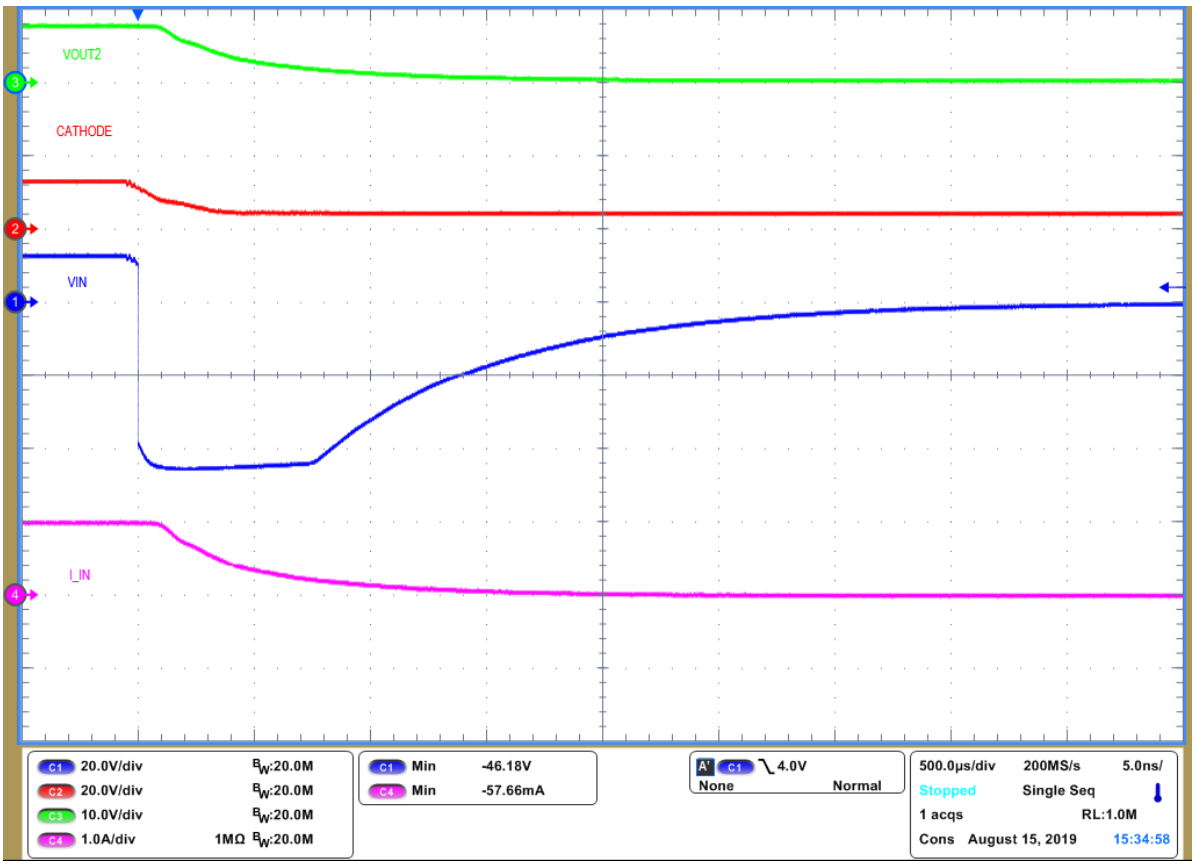
Channel 1 **12.0V Input Voltage @ J1**
5.0ms/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
5.0ms/div
Channel 3 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
5.0ms/div
Channel 4 **Load Current @ 7.5V VOUT2**
5.0ms/div



32. LM74700-Q1 ISO 7637-2 Pulse 1 Response: VOUT2 Zoomed

Response to ISO 7637-2 Pulse 1 applied at the input connector J1 is captured in Figure 32 at smaller time scale. LM74700-Q1 turns off Q2 and cuts off downstream circuits from negative voltage. VOUT2 turns off as the cathode voltage of LM74700-Q1 ramps down.

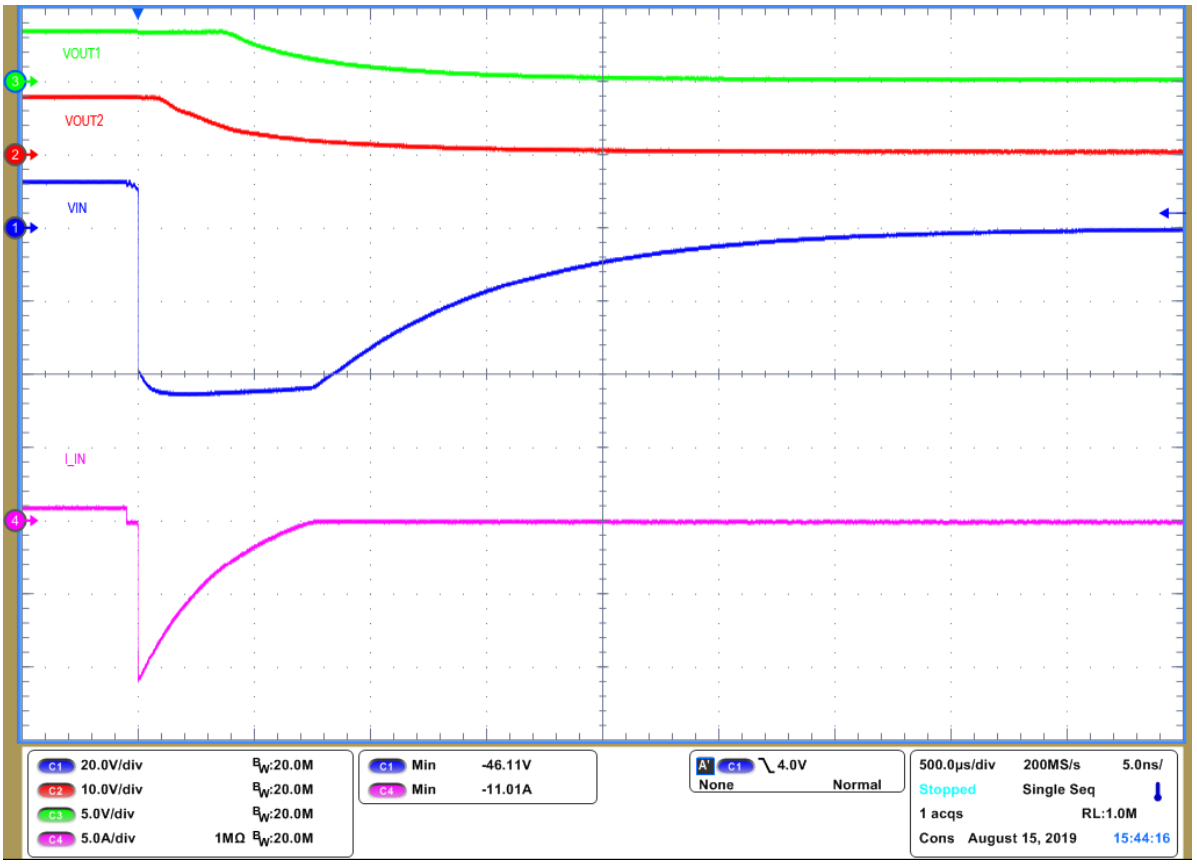
Channel 1 **12.0V Input Voltage @ J1**
500.0µs/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
500.0µs/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
500.0µs/div
Channel 4 **Load Current @ 7.5V VOUT2**
500.0µs/div



33. LM74700-Q1 ISO 7637-2 Pulse 1 Response: Input Current

Response to ISO 7637-2 Pulse 1 applied at the input connector J1 is captured in Figure 33 showing the input current. Input current reaches peak value of -11A during the pulse because the input TVS D2 clamps and absorbs the input transient energy. TVS D2 clamps -150V transient applied with a generator impedance of 10Ω to -42V. This results in -(150-42)V / 10Ω = 10.8A of peak current through the input TVS D2. Measured peak current is -11.01A.

Channel 1 **12.0V Input Voltage @ J1**
500.0µs/div
Channel 2 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
500.0µs/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
500.0µs/div
Channel 4 **Input Current @ J1**
500.0µs/div



34. LM74700-Q1 ISO 7637-2 Pulse 2a Response: VOUT1

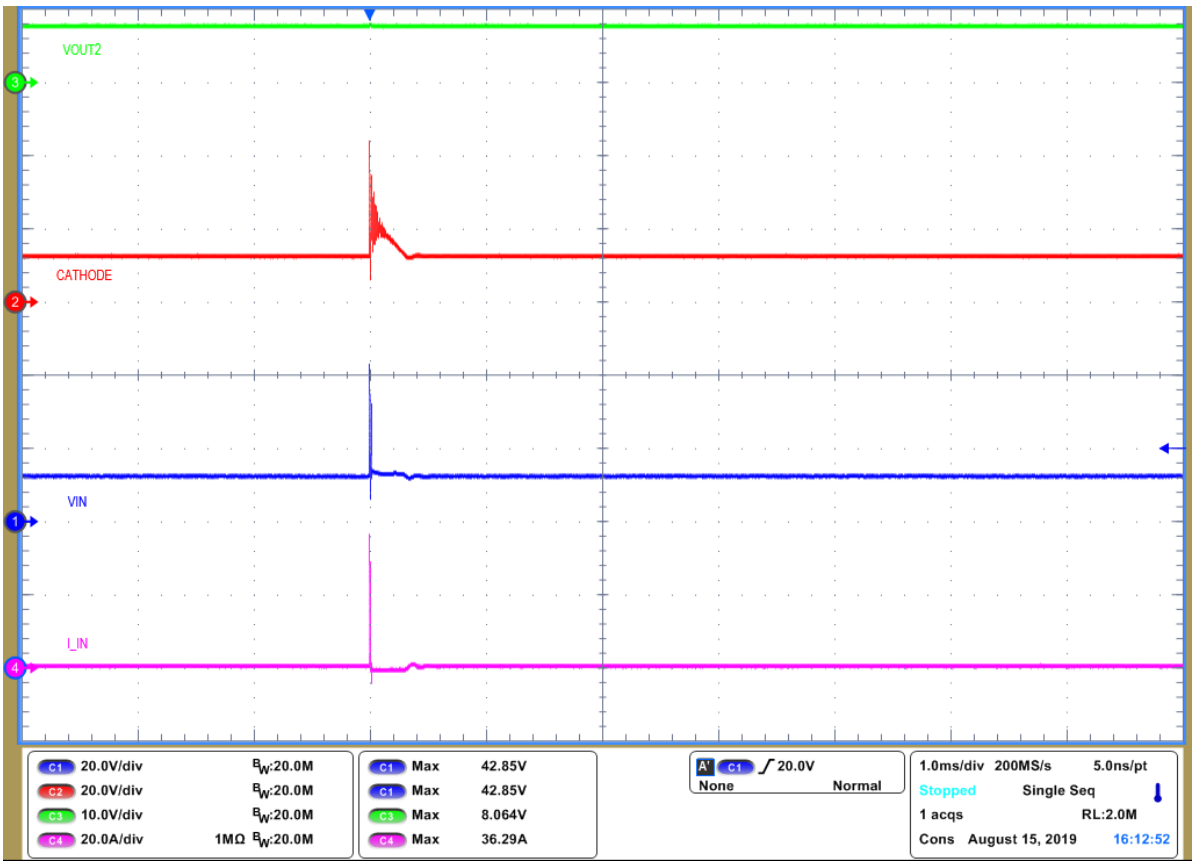
Response to Pulse 2a is captured in Figure 34. Positive pulse applied at the input is clamped by the TVS D2 and 3.3V output of LM5140-Q1 VOUT1 remains unperturbed during the test.

Channel 1 **12.0V Input Voltage @ J1**
1ms/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
1ms/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
1ms/div
Channel 4 **Input Current @ J1**
1ms/div

35. LM74700-Q1 ISO 7637-2 Pulse 2a Response: VOUT2

Response to Pulse 2a is captured in Figure 35. Positive pulse applied at the input is clamped by the TVS D2 and 7.5V output of LM5140-Q1 VOUT2 remains unperturbed during the test.

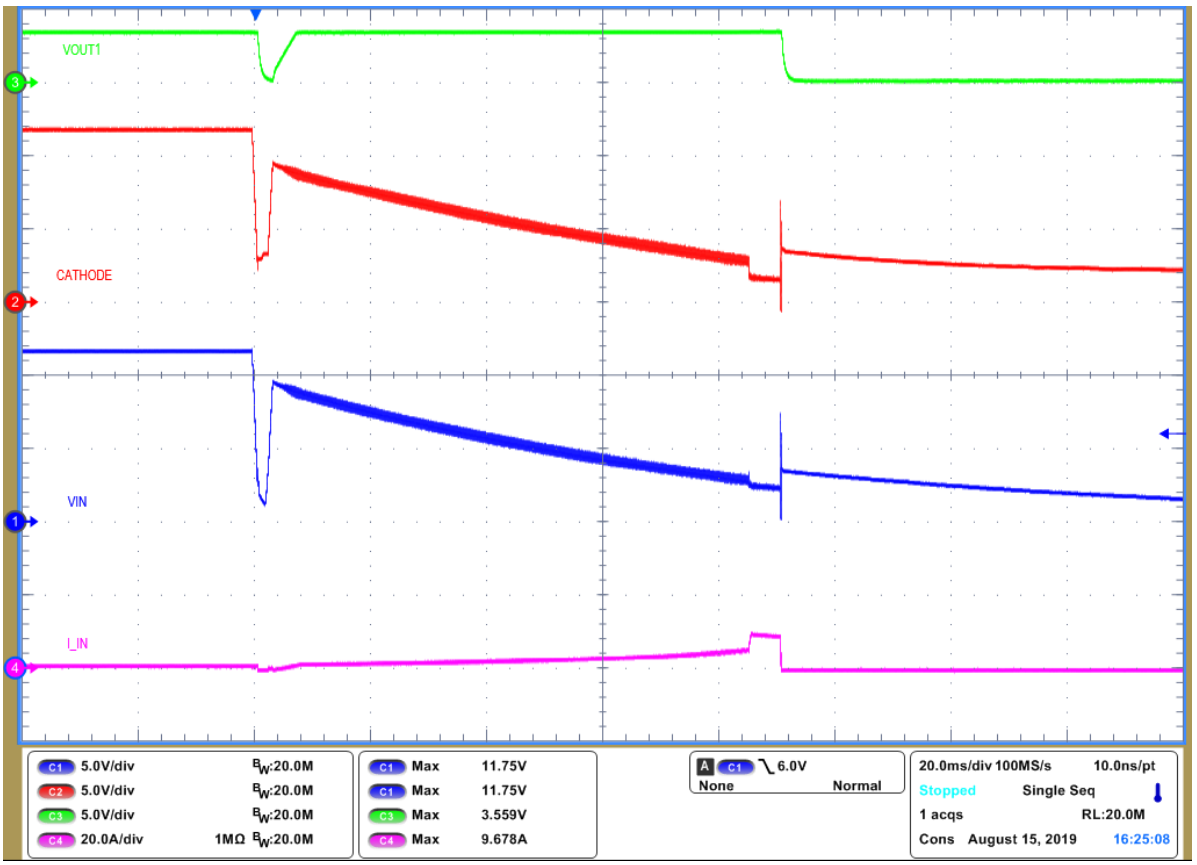
Channel 1 **12.0V Input Voltage @ J1**
1ms/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
1ms/div
Channel 3 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
1ms/div
Channel 4 **Input Current @ J1**
1ms/div



36. LM74700-Q1 ISO 7637-2 Pulse 2b Response: VOUT1

LM5140-Q1 3.3V Output response to Pulse 2b is captured in Figure 36.

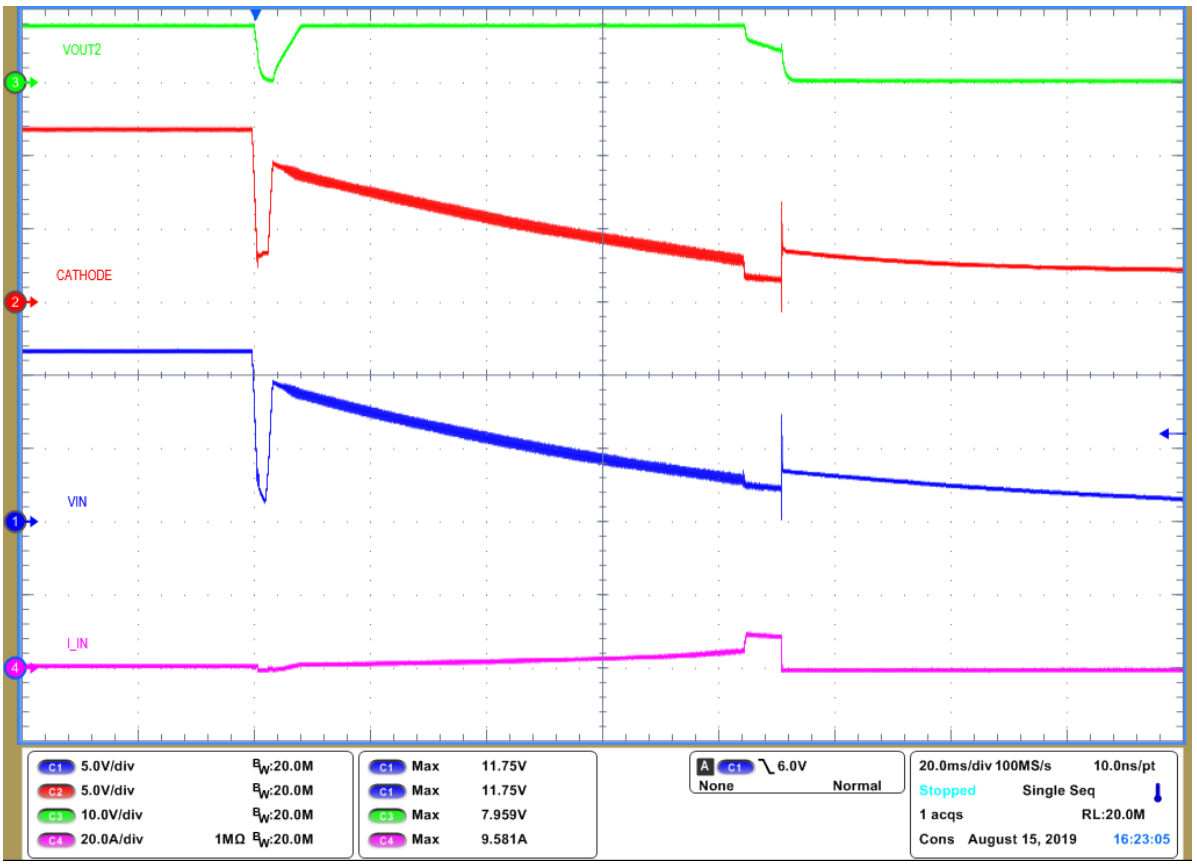
Channel 1	**12.0V Input Voltage @ J1**
	20ms/div
Channel 2	**12.0V Cathode Voltage of LM74700-Q1**
	20ms/div
Channel 3	**3.3V Output Voltage of LM5140-Q1 @ VOUT1**
	20ms/div
Channel 4	**Input Current @ J1**
	20ms/div



37. LM74700-Q1 ISO 7637-2 Pulse 2b Response: VOUT2

LM5140-Q1 7.5V Output response to Pulse 2b is captured in Figure 37.

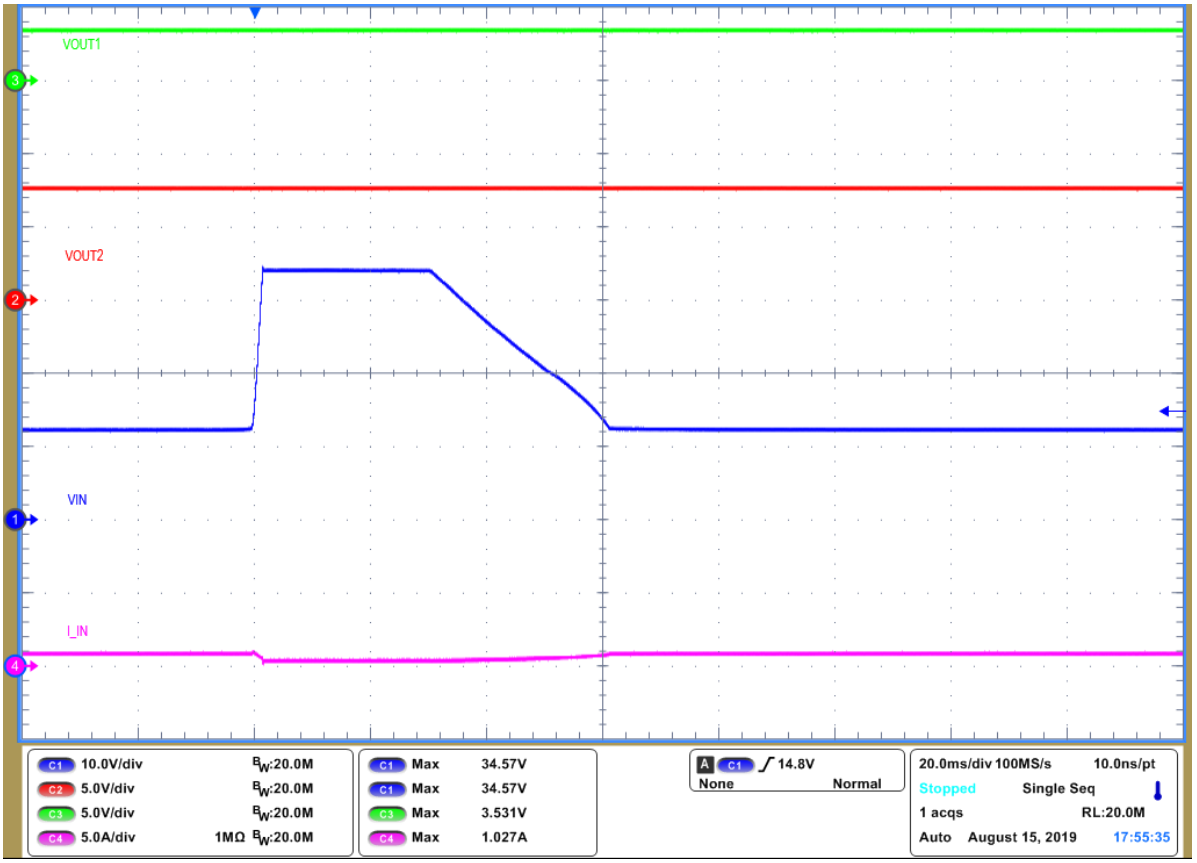
Channel 1 **12.0V Input Voltage @ J1**
20ms/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
20ms/div
Channel 3 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
20ms/div
Channel 4 **Input Current @ J1**
20ms/div



38. LM74700-Q1 ISO 16750-2 Suppressed Load Dump: VOUT1 & VOUT2

LM74700-Q1 allows suppressed load dump voltage 35V to pass through to downstream. Boost controller LM5150-Q1 and dual buck controller are rated for 42V and 65V maximum opertation respectively. This allows VOUT1 and VOUT to operate without any issues during supressed load dump. Figure 38 captures the suppressed load dump resoponse.

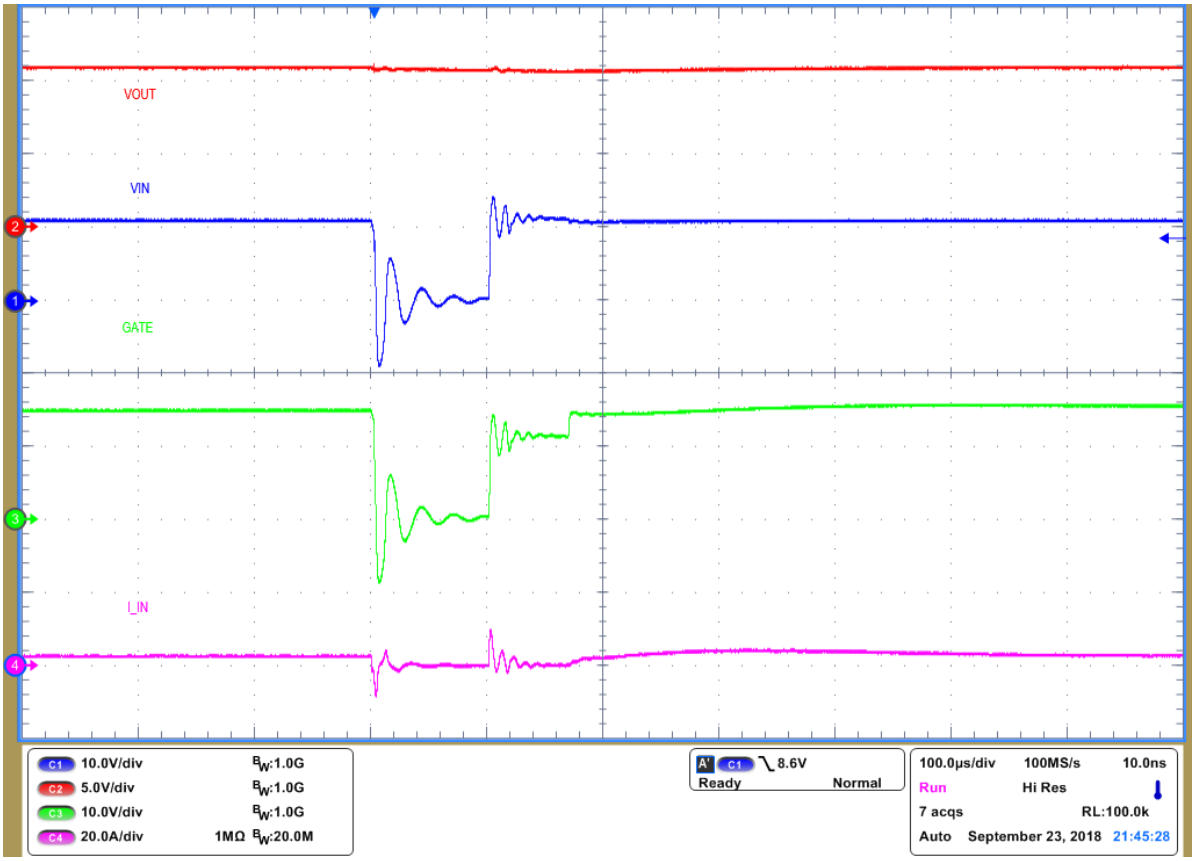
Channel 1 **12.0V Input Voltage @ J1**
20ms/div
Channel 2 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
20ms/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
20ms/div
Channel 4 **Input Current @ J1**
20ms/div



39. LM74700-Q1 LV-124 Input Micro-short: E-10 Test Case 2

Figure 39 captures the LM74700-Q1 response to input micro-short on the 12V for 100us as specified by LV124 E-10 Test Case 2. A very fast reverse current blocking comparator allows LM74700-Q1 to turn off Q2 within 1µs and blocking reverse current completely.

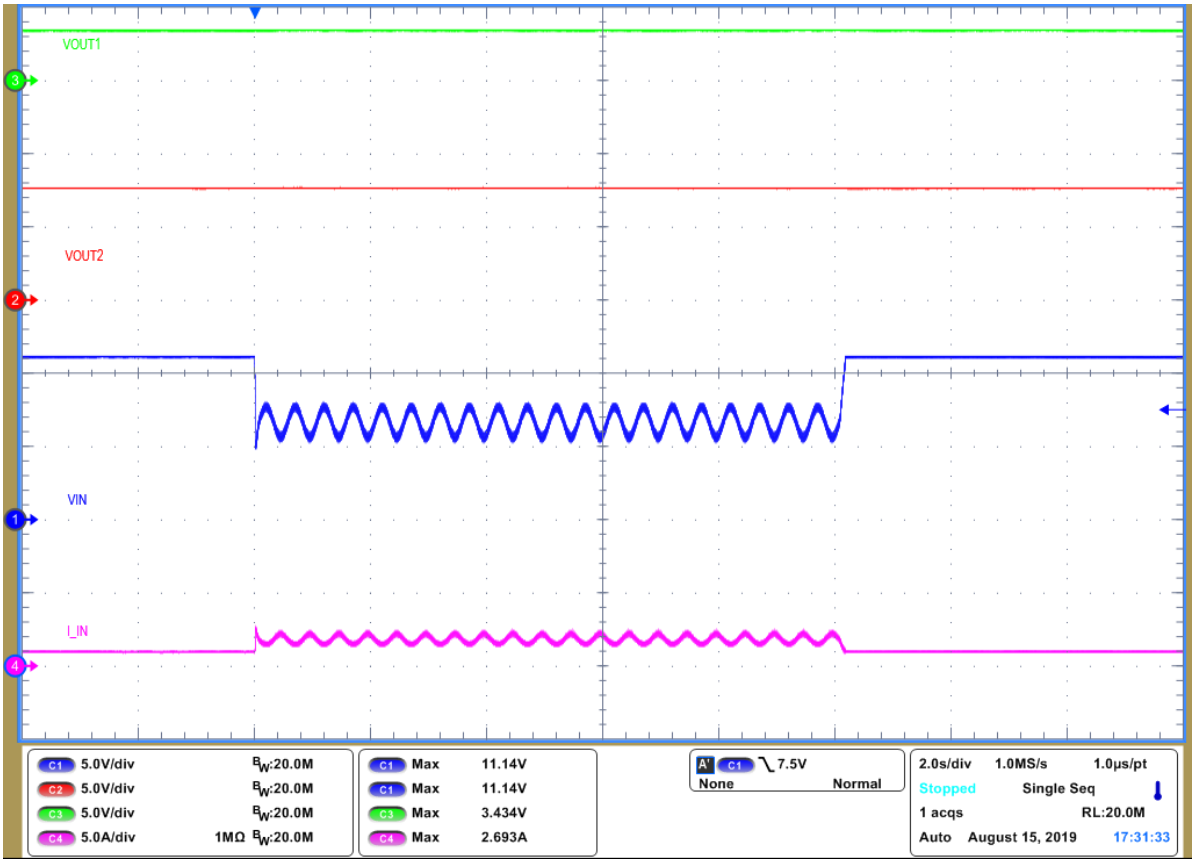
Channel 1 **12.0V Input Voltage @ J1**
100µs/div
Channel 2 **12V Cathode Voltage of LM74700-Q1**
100µs/div
Channel 3 **Gate Voltage of LM74700-Q1**
100µs/div
Channel 4 **Input Current @ J1**
100µs/div



40. LM74700-Q1 ISO 16750-2 Starting Profile: VOUT1 and VOUT2

Response to cranking or starting profile is captured in Figure 40. VOUT1 and VOUT2 of LM5140-Q1 remain unperturbed during the cranking profile test.

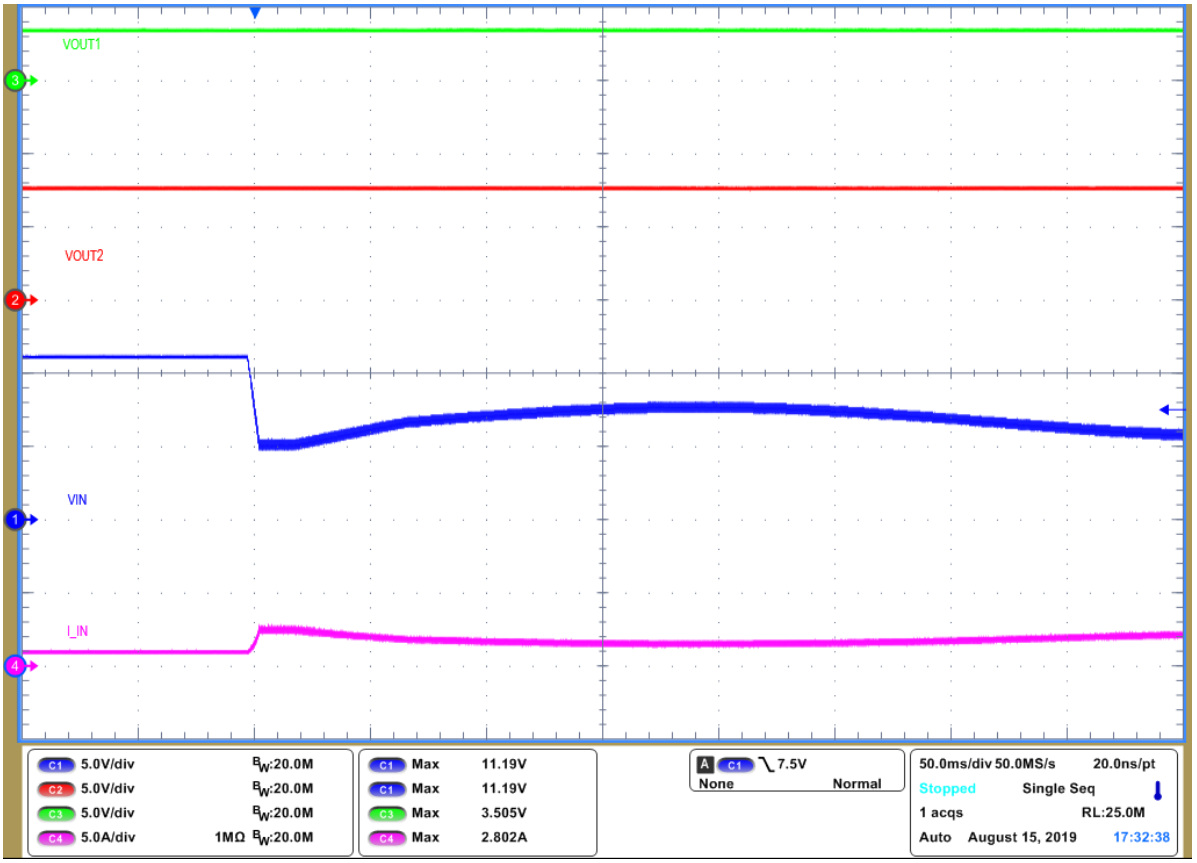
Channel 1 **12.0V Input Voltage @ J1**
2s/div
Channel 2 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
2s/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
2s/div
Channel 4 **Input Current @ J1**
2s/div



41. LM74700-Q1 ISO 16750-2 Starting Profile: Zoomed

Response to cranking or starting profile is captured in Figure 41 in smaller time scale. VOUT1 and VOUT2 of LM5140-Q1 remain unperturbed during the cranking profile test.

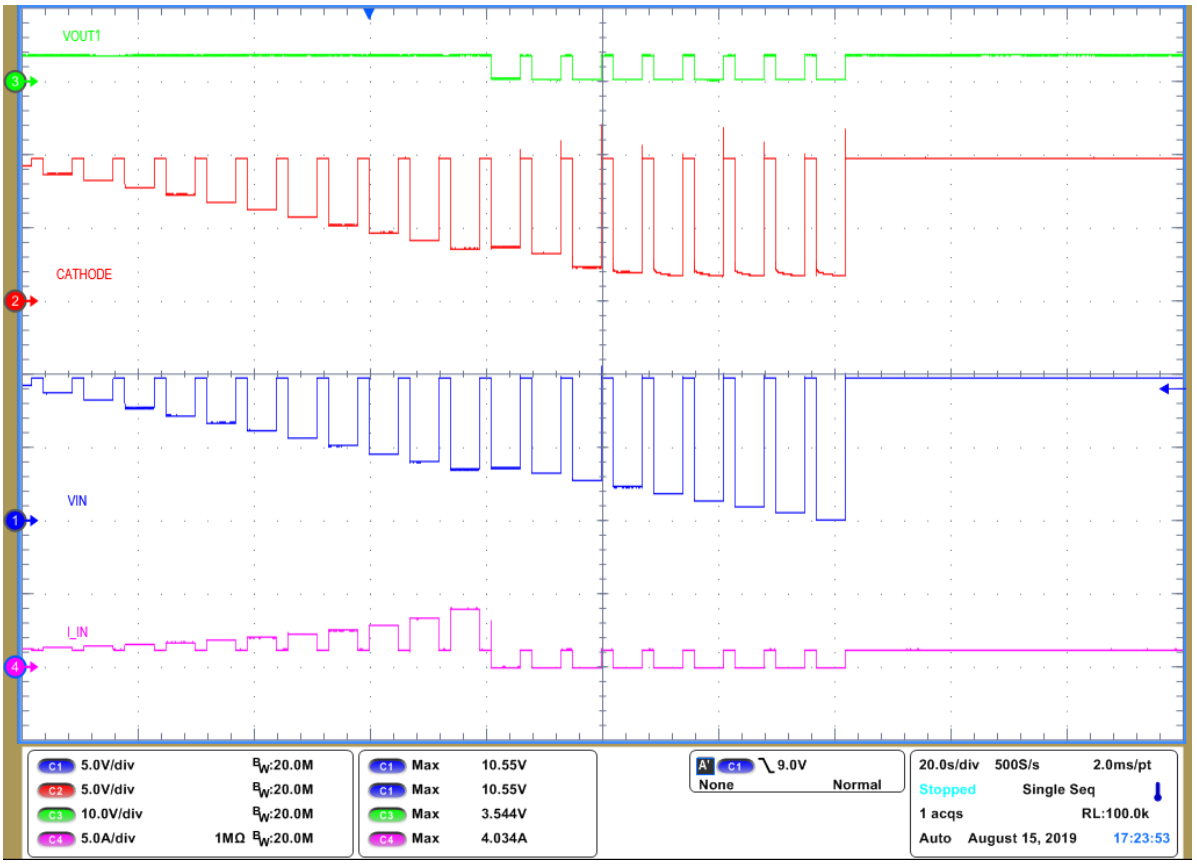
Channel 1 **12.0V Input Voltage @ J1**
50ms/div
Channel 2 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
50ms/div
Channel 3 **3.3V Output Voltage of LM5140-Q1 @ VOUT1**
50ms/div
Channel 4 **Input Current @ J1**
50ms/div



42. LM74700-Q1 ISO 16750-2 Reset Behavior: VOUT1

Response to reset behavior at voltage drop is captured in Figure 42. VOUT1 of LM5140-Q1 remain unperturbed until the input voltage drop to 3.5V and from then it follows the input reset pulse.

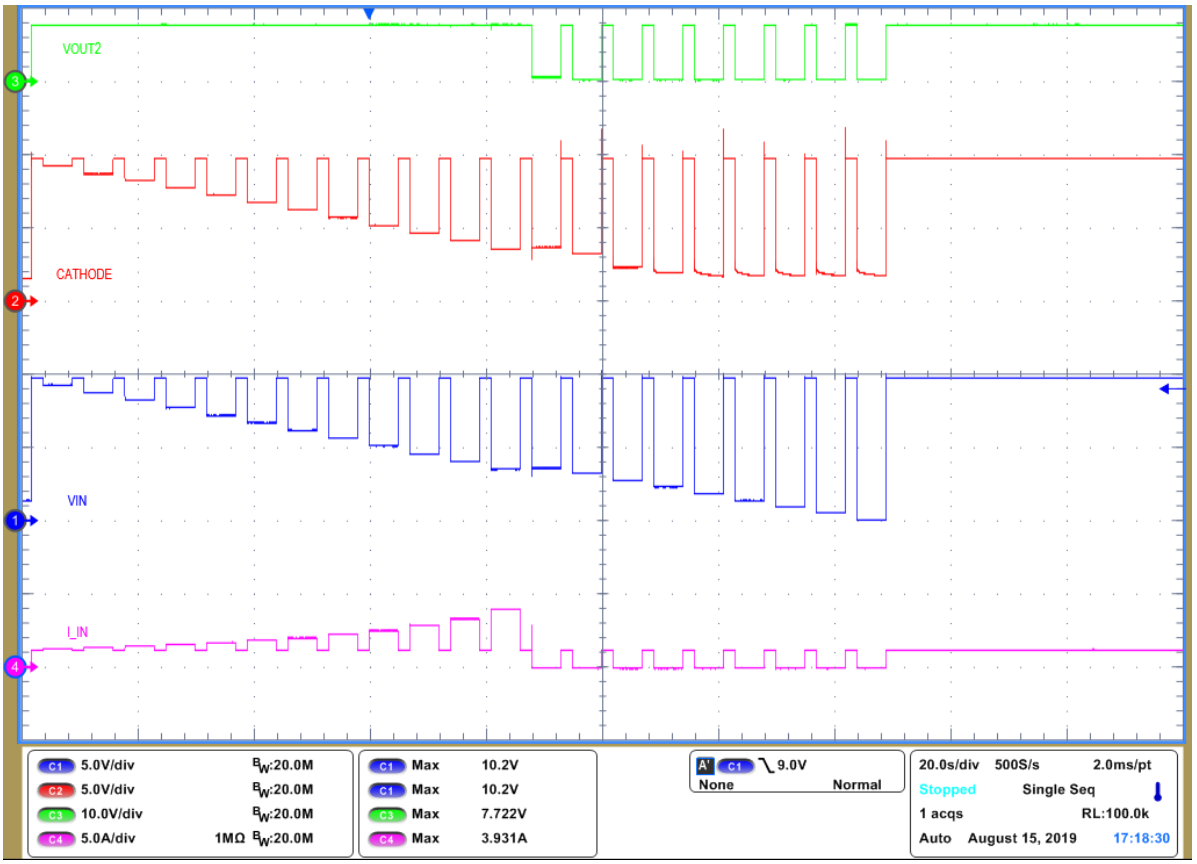
Channel 1	**12.0V Input Voltage @ J1**
	20s/div
Channel 2	**12.0V Cathode Voltage of LM74700-Q1**
	20s/div
Channel 3	**3.3V Output Voltage of LM5140-Q1 @ VOUT1**
	20s/div
Channel 4	**Input Current @ J1**
	20s/div



43. LM74700-Q1 ISO 16750-2 Reset Behavior: VOUT2

Response to reset behavior at voltage drop is captured in Figure 42. VOUT2 of LM5140-Q1 remain unperturbed until the input voltage drop to 3.5V and from then it follows the input reset pulse.

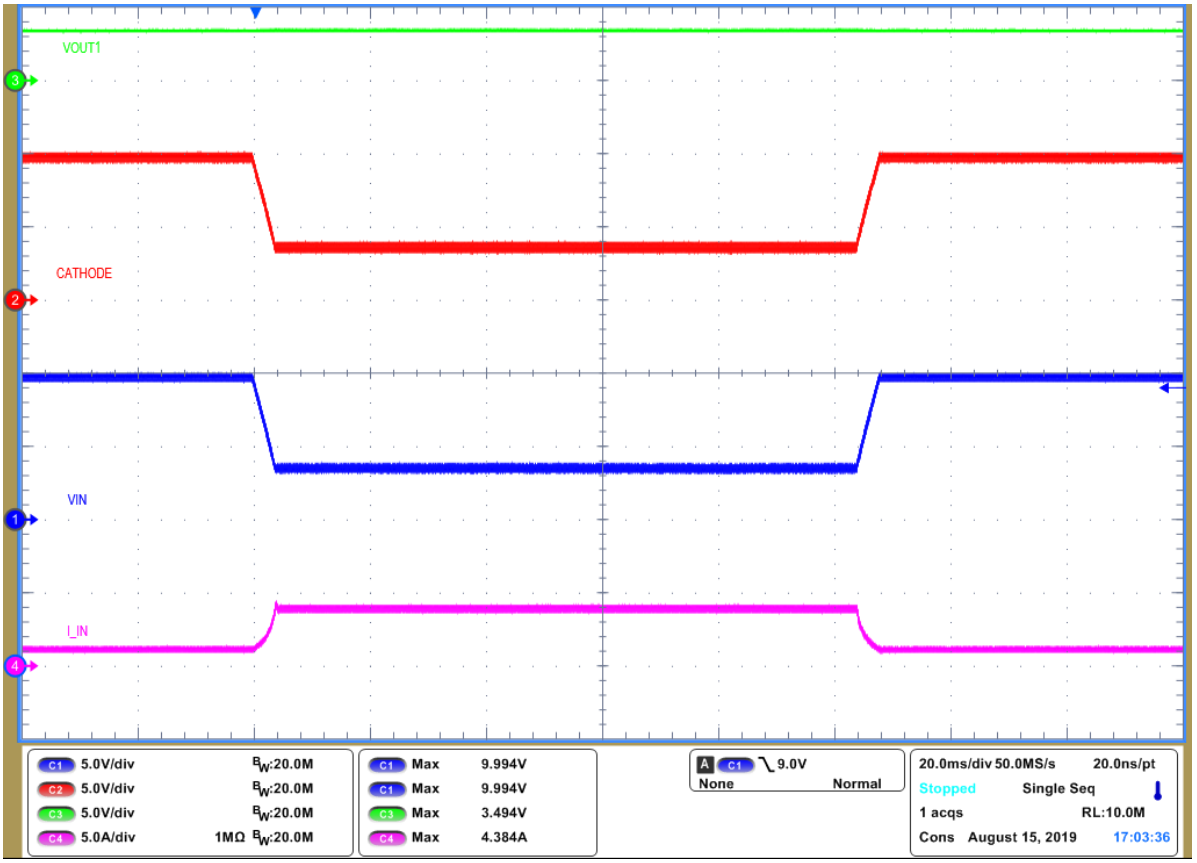
Channel 1 **12.0V Input Voltage @ J1**
20s/div
Channel 2 **12.0V Cathode Voltage of LM74700-Q1**
20s/div
Channel 3 **7.5V Output Voltage of LM5140-Q1 @ VOUT2**
20s/div
Channel 4 **Input Current @ J1**
20s/div



44. LM74700-Q1 ISO 16750-2 Reset Behavior: VOUT1

Response to momentary drop in input voltage is captured in Figure 44. VOUT1 of LM5140-Q1 remain unperturbed during the momentary drop in input voltage.

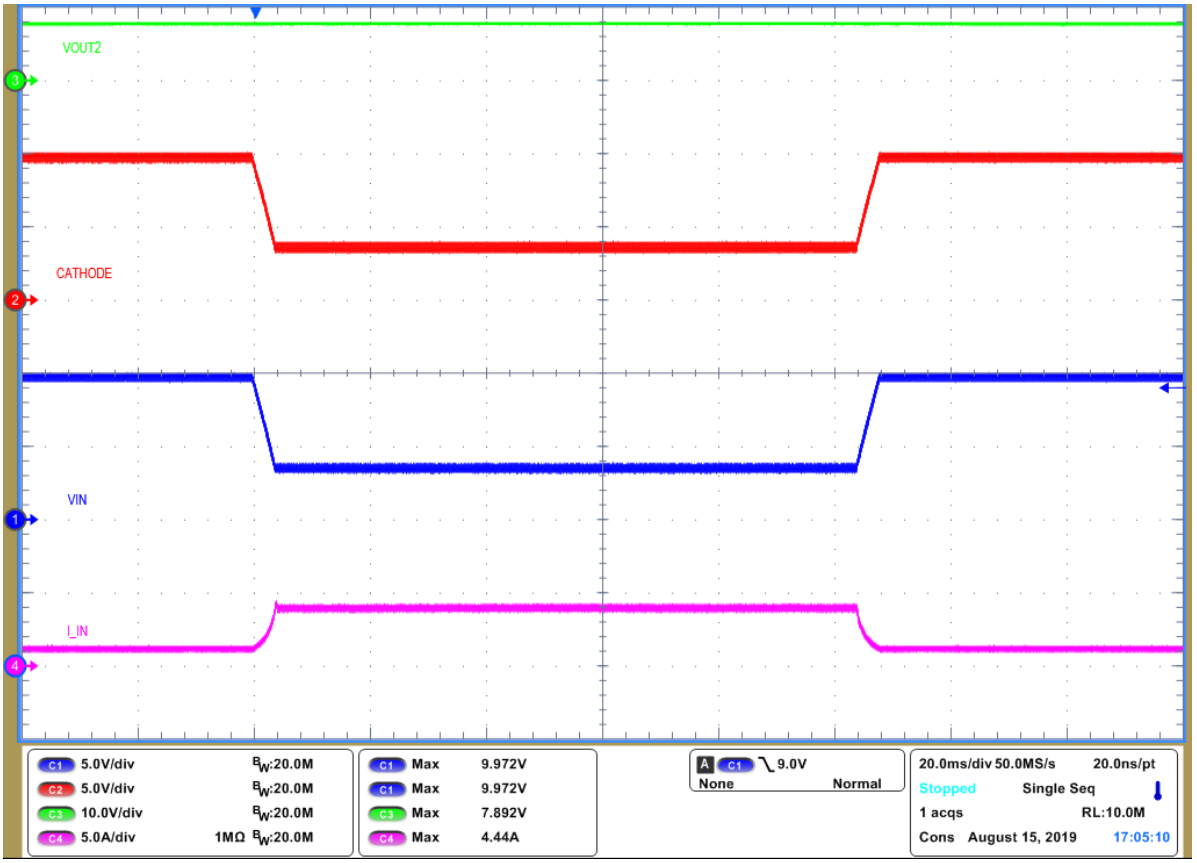
Channel 1	**12.0V Input Voltage @ J1** 20ms/div
Channel 2	**12.0V Cathode Voltage of LM74700-Q1** 20ms/div
Channel 3	**3.3V Output Voltage of LM5140-Q1 @ VOUT1** 20ms/div
Channel 4	**Input Current @ J1** 20ms/div



45. LM74700-Q1 ISO 16750-2 Reset Behavior: VOUT1

Response to momentary drop in input voltage is captured in Figure 45. VOUT1 of LM5140-Q1 remain unperturbed during the momentary drop in input voltage.

Channel 1	**12.0V Input Voltage @ J1** 20ms/div
Channel 2	**12.0V Cathode Voltage of LM74700-Q1** 20ms/div
Channel 3	**7.5V Output Voltage of LM5140-Q1 @ VOUT2** 20ms/div
Channel 4	**Input Current @ J1** 20ms/div



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