TI Designs: TIDA-010006

Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller

Description

This reference design provides the isolated positive and negative voltage rails required for *Insulated Gate Bipolar Transistor* (IGBT) gate drivers from 24-V DC input supply. This design uses a flyback power-supply topology with the LM5180 device with primary-side regulation. It uses a single transformer to generate four pairs of 15-V and –5-V outputs suitable for powering six IGBT gate drivers of 1 W each. The integration of the 100-V rated primary side switch within the flyback controller LM5180 together with the elimination of an auxiliary transformer winding enables a compact solution. While this design generates 20-V on its output rails, by changing only the feedback resistor it can be scaled to generate 24 V (15 V and –8 V).

Resources

TIDA-010006	Design Folder
LM5180-Q1	Product Folder

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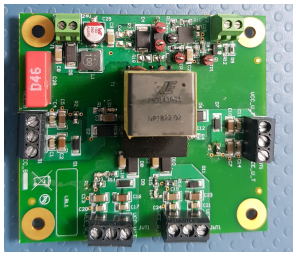
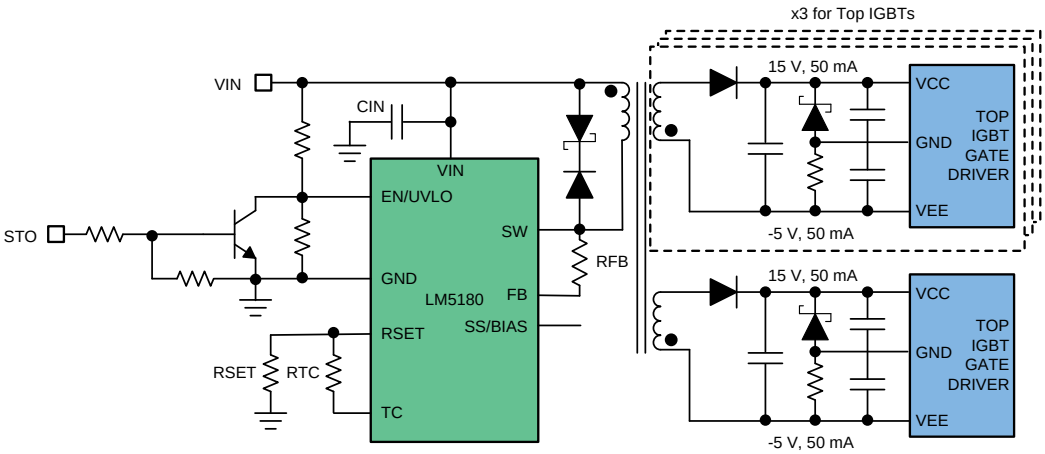
Features

- Isolated power supply supporting six IGBT gate drivers of the three-phase inverter
- Quasi-resonant boundary conduction mode along with frequency modulation provides peak efficiency of 90% at balanced full load
- Supplies output power up to 1.2 W per IGBT driver
- Provides compact and cost-effective solution due to elimination of opto-coupler and transformer auxiliary winding
- Provision to turn the power supply on and off through the EN pin
- Programmable soft start limits the inrush current drawn by the power supply

Applications

- Variable Speed AC and Servo Drives
- Industrial and Solar Inverter
- IGBT-Based HVDC Systems





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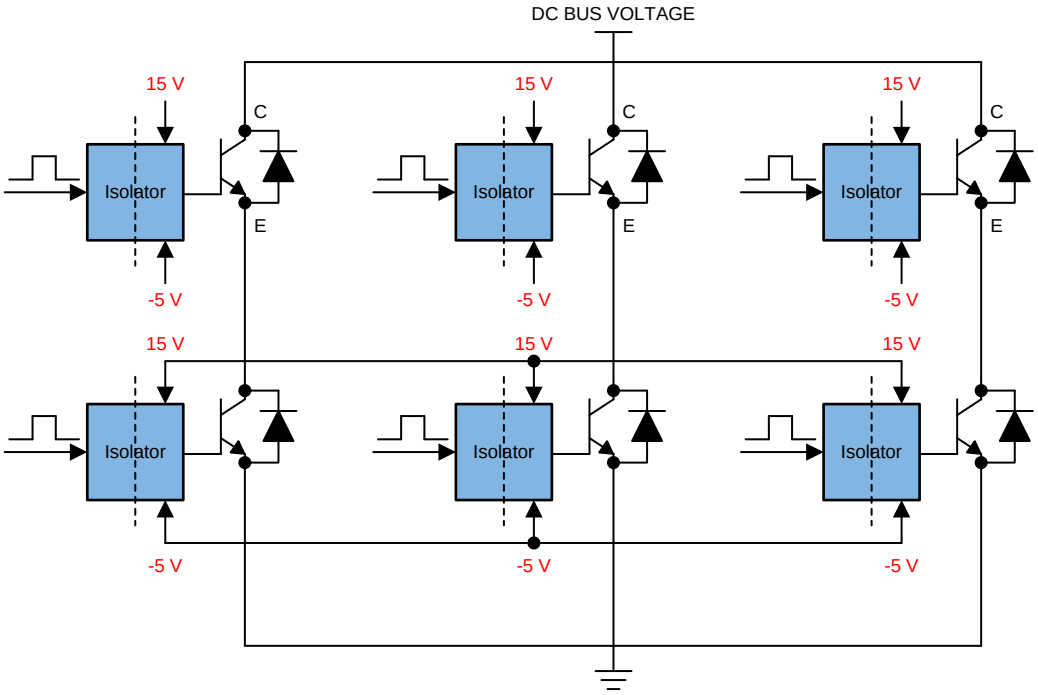
1 System Description

Three-phase inverter power stages are the fundamental block of servo drives, solar inverters, and variable frequency drives. Three-phase inverters convert the DC bus voltage to three-phase AC voltage with adjustable magnitude and frequency depending on the application. The three-phase inverters use IGBTs as semiconductor switches. The fundamental frequency of the three-phase output generated by the inverter is controlled by the PWM signals generated by the MCU. These PWM signals generated from the MCU, however, control these six IGBT switches through isolated gate drivers that galvanically isolate the high-voltage gate-driver outputs from the low-voltage control signals. Each IGBT is driven by a single isolated gate driver. The emitters of each of the top IGBTs float, which necessitates using isolated gate-driver for each of the top IGBTs. These isolated gate drivers require isolated power supply, which is provided by this reference design. Thus, this design generates four isolated power rails: one combined power supply rail for the three bottom IGBTs, and three isolated rails for each of the top IGBTs. Figure 1 shows the system-level block diagram. The output voltages supplied by this reference design to the gate-drivers is decided by considering the switching and conduction characteristics of the IGBT.

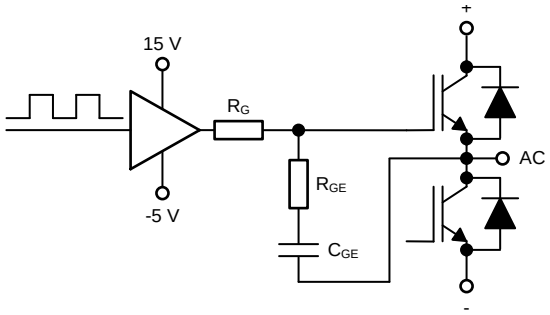
Figure 1. Three-Phase Inverter Power Stage With Gate Driver



Assuming identical conditions, IGBTs and MOSFETs behave identically when turned on, and both have similar current rise and voltage fall times. Gate drivers must provide sufficient drive current to ensure fast charging and discharging of the power switch which is capacitive in nature (gate capacitance of the IGBT), reducing switching power loss. Once turned on, to reduce conduction losses, the gates of the IGBTs are supplied with a much higher voltage than the actual gate-threshold voltages. Typically, 15-V to 18-V is applied at the gate to reduce VCE(on), reducing the conduction loss. Thus, gate drivers are necessary to level shift the output voltages produced by the MCU (3.3-V or 5-V) and provide the necessary current to decrease or increase the charging time of the IGBT gate capacitance. The turn-off characteristics of the IGBT differ slightly from the MOSFET. At the end of the switching event, the IGBT has a tail current, which does not exist for the MOSFET. This tail is caused by minority carriers trapped in the base of the bipolar output section of the IGBT, which causes the device to remain turned on. Unlike a bipolar transistor, it is not possible to extract these carriers to speed up switching, since there is no external connection to the base. Therefore, the device remains turned on until the carriers recombine. This tail current increases the turn-off losses. To reduce the turn-off time, and hence turn-off losses, a negative voltage (–5 V to –10 V) is applied at the gate. A negative voltage also prevents spurious IGBT turn on. For example, when the top IGBT is turned on, some voltage spikes are generated on the gate terminal, due to the high dV/dt and parasitic capacitance between the gate and emitter. The voltage spikes can cause a false turn-on for the

bottom IGBT. A negative voltage at the gate helps to avoid this false turn-on trigger. The power (gate voltage and current) required to switch each IGBT on and off determines the output power of the gate-driver power supply. In the process of switching the IGBT on and off , power is dissipated in the gate-driver IC, IGBT gate, and the RC circuits in the gate-drive path as Figure 2 shows. The total gate power dissipation is given by Equation 1:

Figure 2. IGBTs With Gate-Driver Circuitry for Gate-Power Calculation



$$P_{gate} = P_{driver} + \left(Q_{gate} \times f_{SW} \times \Delta V_{gate}\right) + \left(C_{ge} \times f_{SW} \times \Delta V_{gate}^2\right) \quad (1)$$

where

- Q_{gate} = total gate charge
- f_{SW} = switching frequency of the controller
- ΔV_{gate} = gate driver output voltage swing

NOTE: The second term in Equation 1 reflects the power requirement for IGBT gate capacitance and the third term reflects the power requirement for an additional external capacitance, as Figure 2 shows.

Consider the following example:

- An IGBT module with 1200-V, 100-A capability (applicable for <100-kW drives) with Q_{gate} = 250 nC
- Switching frequency of 16 kHz (which is on the higher side for typical high-power drives)
- A gate voltage, swinging from –5 V to 15 V
- C_{ge} = 20 nF (typical value ranges between 1 nF and 20 nF)
- P_{driver} = approximately 600 mW (estimated using the typical data sheet of an isolated IGBT gate-driver)

Using the previous values:

$$P_{gate} = 0.6\ W + 0.08\ W + 0.128\ W = 0.808\ W \quad (2)$$

Considering the de-rating, the power in Equation 2 must be rounded up to 1 W / IGBT.

With de-rating, Equation 2 comes to 1 W / IGBT. Thus, this reference design provides 20-V (15 V and –5 V) output voltage and 0.050-A output current, per IGBT. The gate-drive supply for the three bottom IGBTs is combined. Hence, this design provides four isolated output power rails: one rail supplying 3 W for all three bottom IGBTs and three rails, each supplying 1 W to each of the top IGBTs. This design can also be scaled to provide an output of 1.2 W per IGBT by changing the output voltages of each rail to 15 V and –8 V.

1.1 Key System Specifications

Table 1. Key System Specifications

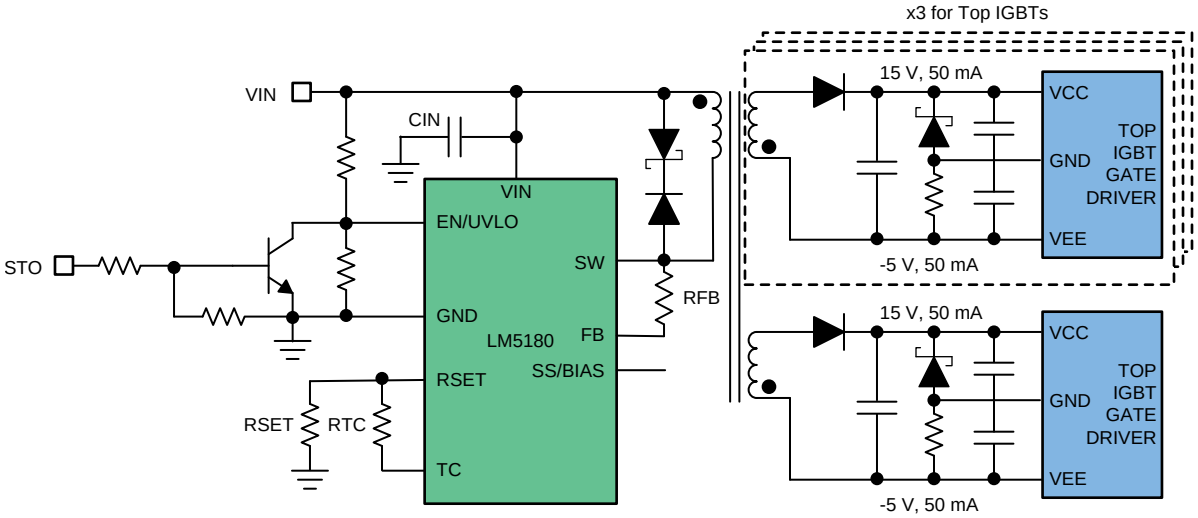
SNo.	SPECIFICATIONS	DETAILS
1	Input voltage to IGBT gate-drive power supply	24 V ±20%
2	Output voltage rails	4 Bipolar rails (15-V and –5-V)
3	Continuous output current	50 mA / IGBT driver
4	Switching frequency	Up to 350 kHz
5	Configuration	Closed loop regulation
6	Efficiency	Approximately 85–90%
7	Ambient temperature	85°C

2 System Overview

2.1 Block Diagram

Figure 3 shows the block diagram of TIDA-010006 which uses the LM5180 device as flyback controller.

Figure 3. TIDA-010006 Block Diagram

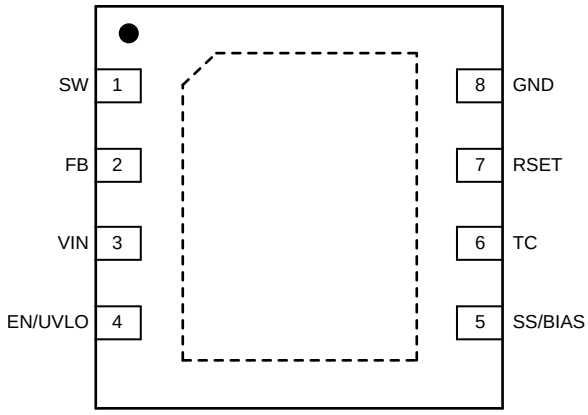


2.2 Highlighted Products

2.2.1 LM5180

Figure 4 shows the pin diagram of the LM5180 device.

Figure 4. LM5180 Pin Diagram



The LM5180 device is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 70 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results is a simple, reliable and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1% load and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

2.3 System Design Theory

2.3.1 Selection of Flyback Topology With LM5180

There exist many standard converter topologies, such as push-pull, flybuck, and flyback converters, used for the gate-drive bias supply. Factors such as input supply regulation, isolation, cost, power, target load regulation, and efficiency decide the topology for a power supply.

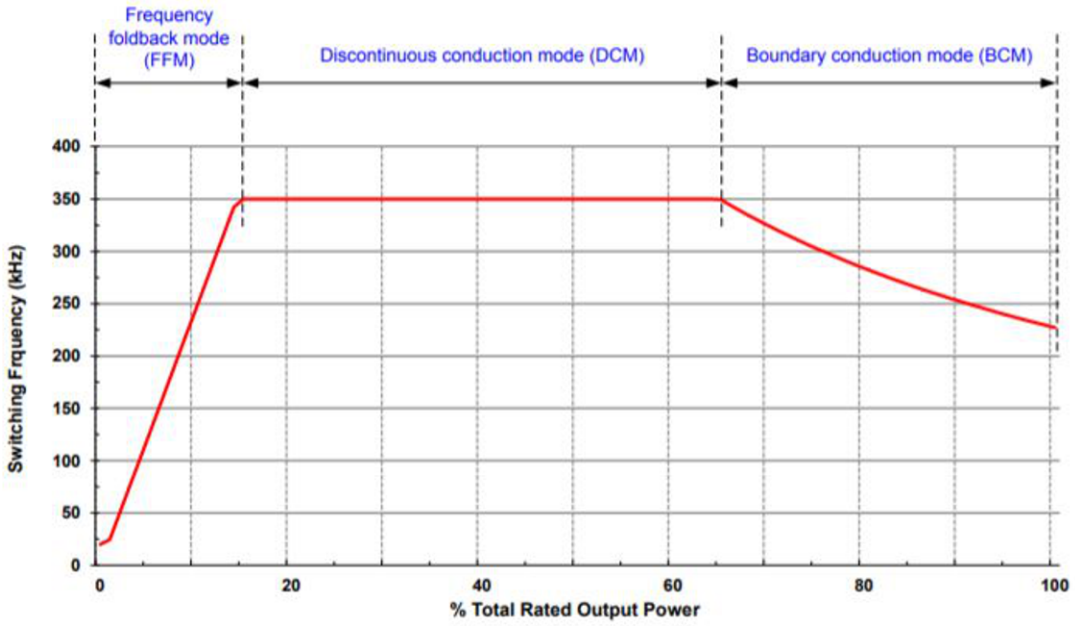
The regulation of the input supply to the gate-drive supply decides the necessity of having feedback – if the input supply is regulated then an open-loop topology can provide reasonable regulated output; however, if the input source is not regulated (or coming from an external source whose regulation is not known), a closed-loop topology is preferred. A push-pull converter operates as an interleaved forward converter and is ideal for higher power designs above 200 W. Compared to the flybuck topology (TIDA-00199), the flyback topology using the LM5180 device has a smaller component count, tighter load regulation, and higher efficiency at light loads.

The LM5180 device uses primary-side regulation (PSR), which is advantageous compared to the auxiliary winding feedback method. PSR offers better cross-regulation between the multiple outputs when compared with the auxiliary winding feedback method. Moreover, this also eliminates the need for an additional transformer winding or opto-isolator, reducing the cost and solution size. The primary-side N-channel power MOSFET used in the flyback topology is integrated in the LM5180 itself, making the design more compact. These factors render the LM5180 device as an optimal solution to implement the flyback topology required by this design. The LM5180 device operates in 3 different modes (explained in Section 2.3.2), according to the variation in load current.

2.3.2 LM5180 Operation

The LM5180 flyback controller works in three different modes depending on the load as Figure 5 shows.

Figure 5. Three Modes of Operation Illustrated by Variation of Switching Frequency With Load



At high loads, the LM5180 device operates in *Quasi-Resonant Boundary Conduction Mode*. The power MOSFET turns on when the current in the secondary winding reaches zero at the first valley on the SW node, to minimize switch-on losses. The MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the peak current decreases and the frequency increases to maintain BCM operation. The duty cycle (D) remains constant with the load in this mode, and is determined by Equation 3. The peak current I_{SW-PK} for a given load can be estimated using Equation 4.

$$D = \frac{(V_O + V_{FWD}) \times N_{PS}}{(V_O + V_{FWD}) \times N_{PS} + V_{IN}} = \frac{(20 + 0.7) \times 1}{(20 + 0.7) \times 1 + 24} = 0.46$$
$$I_{SW-PK} = \frac{2 \times I_{OUT} \times V_{OUT}}{V_{IN} \times D \times \eta} = \frac{2 \times 0.3 \times 20}{24 \times 0.46 \times 0.85} = 1.27 \text{ A} \quad (3)$$

where

- N_{PS} is the primary-to-secondary turns ratio, which is 1:1 in this reference design (explained in Section 2.3.3.
- V_{OUT} is the output voltage, 20 V for this design
- I_{OUT} is the output current, 300 mA for this design
- V_{FWD} is the forward voltage drop of the flyback secondary diode, which is 0.7 V for the diode used in this reference design
- η is the efficiency which is estimated as 85% at full load for calculations (4)

At medium loads, the LM5180 device operates in *Discontinuous Conduction Mode* (DCM), where it clamps the maximum switching frequency to 350 kHz and as the load decreases, the peak current reduces to maintain regulation at 350 kHz.

At even lighter loads, the system operates in *Frequency Fold-Back Mode* (FFM), and the switching frequency decreases as the load current is reduced. The primary-side peak current fixed by the internal error amplifier decreases to a minimum level of 0.27 A and the MOSFET off-time extends to maintain the output load requirement. The LM5180 device has a minimum frequency of operation at 12 kHz.

2.3.3 Transformer Design

The transformer design includes making key decisions on the turns ratio and primary inductance. Further specifications like the switching frequency, saturation current, leakage inductance, isolation, primary and secondary DCRs, and mechanicals – pinout, footprint, and height also need to be optimized to minimize losses, size, and cost.

The constraint on the minimum value of the turns ratio (primary to secondary) is set by the maximum output power yielded by a particular turns ratio to be greater than 6 W. Whereas, the maximum possible value of the turns ratio is constrained by the voltage rating of the built-in MOSFET in the LM5180 device. The initial estimate of turns ratio can be calculated according to Equation 5:

$$N_{PS} = \frac{N_P}{N_S} = \frac{D}{1-D} \times \frac{V_{IN(MIN)}}{V_{OUT} + V_D} = \frac{0.46}{1-0.46} \times \frac{22}{20 + 0.7} \sim 1 \quad (5)$$

The built-in MOSFET is rated at 100 V. In the off cycle, when the secondary (flyback) diode is on, the voltage on the drain (V_{DS}) is as Equation 6 shows.

$$V_{DS} = V_{IN(MAX)} + V_{REF} + V_{RING} = 28 + 20.7 + 20 = 68.7 \text{ V} \quad (6)$$

Also, the voltage across the secondary diode when the switch is on can be calculated as Equation 7 shows.

$$V_{Diode} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}} + V_{D-SPIKE} = 20 + 28 + 20 = 68 \text{ V}$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- $V_{REF} = N_{PS} \times (V_{OUT} + V_{FWD}) = 1 \times 20.7$ is the primary voltage reflected across the transformer.
- V_{OUT} is the output voltage, specified as 20 V
- V_{RING} and $V_{D-SPIKE}$ is the spike in voltage due to resonance (assumed to be 20 V) (7)

To provide the maximum possible output power for a given turns ratio, the controller will work in the BCM with the maximum possible $I_{PK,PRI(MAX)}$ that can be withstood by the primary MOSFET (1.45 A). As the primary-to-secondary turns ratio is increased, the duty cycle increases according to Equation 3. In BCM, the output power can be estimated with Equation 8.

$$P_{OUT\_max} = \frac{I_{SW-PK}}{2 \times \left(\frac{1}{V_{IN(MAX)}} + \frac{1}{N_{PS} \times (V_O + V_{FWD})} \right)} = 11\,W \quad (8)$$

Thus, this reference design uses a transformer of primary-to-secondary turns ratio of 1:1.

The inductance of the transformer primarily determines the modes of operation in the LM5180 device as the load is varied from the minimum load to full load. An increase in the magnetic inductance generally leads to an increase in the leakage inductance of the transformer. The LM5180 device has a minimum off-time ($T_{OFF(MIN)}$) of 500 ns: the magnetizing current should not decrease to zero in less than 500 ns. Equation 9 calculates the minimum inductance value (L_{PRI}) as 38 µH.

$$L_{PRI} \geq \frac{(V_O + V_{FWD}) \times T_{OFF(MIN)} \times N_{PS}^2}{\left(I_{SW-PK(MIN)} \times N_{PS}\right)} \quad (9)$$

where

- Output voltage (V_O) is taken as 24 V, since this reference design should be scalable to generate 24-V output at the four rails
- The minimum peak primary current ($I_{PK,PRI(MIN)}$) is 0.27 A for the LM5180 device
- The primary to secondary turns ratio is (N_{PS}) is 1

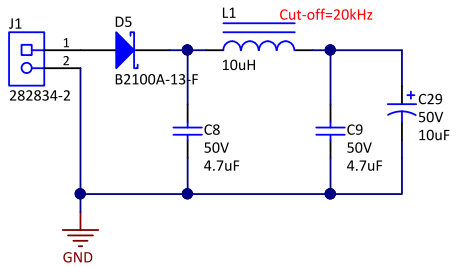
Thus, this reference design uses a transformer with primary magnetic inductance of 47 µH.

2.3.4 Input Section of Flyback

2.3.4.1 Input Filter

The 24-V input supply is given to the transformer and the VIN pin of the controller through a ∏-LC filter. The advantage of this type of filter is two-fold. First, the filter has two-poles at its cutoff frequency, resulting in a slope of –40 dB/decade, giving rise to a steeper roll cutoff. Second, owing to its bidirectional nature, this not only filters out high-frequency noise from entering the system, but also protects the line from EMI noise generated in the system. The ∏-LC (C8, L1, and C9) filter used in this reference design uses ceramic capacitors of 4.7 µF, 50-V, X7R and an inductor with an inductance value of 10 µH. The diode D5 at the input provides reverse-polarity protection to the power supply.

Figure 6. Schematics of the Input Filter Section



The ceramic capacitors are used in this filter because they have far less ESR and ESL values. For further input filtering and damping, an electrolytic capacitor, C29 of 10 µF, and 50 V is added in parallel to the already existing ceramic capacitors. This is a much cheaper and compact solution than using only ceramic capacitors with large capacitance values to construct a low cutoff frequency filter.

2.3.4.2 Input Capacitor

Without input capacitors, the high ripple current in the converter is supplied by the unregulated power source. Stray inductance and resistance causes high-voltage ripple. Input capacitors provide a bypass for this ripple current and stabilize the supply bus voltage during a transient event.

This design uses a ceramic capacitor at the input, since the ESR of aluminum electrolytics and most tantalums is too high to allow for effective ripple reduction and causes excessive power dissipation in the ESR parasitic. The capacitance value can be calculated with Equation 10:

$$C_{in} > \frac{I_{SW-PK} \times D \times (1-D)^2}{2 \times f_{SW} \times \Delta V_{in}}$$

where

- I_{SW-PK} is the peak primary current
- ΔVin is variation in the input voltage (10)

2.3.5 Setting LM5180

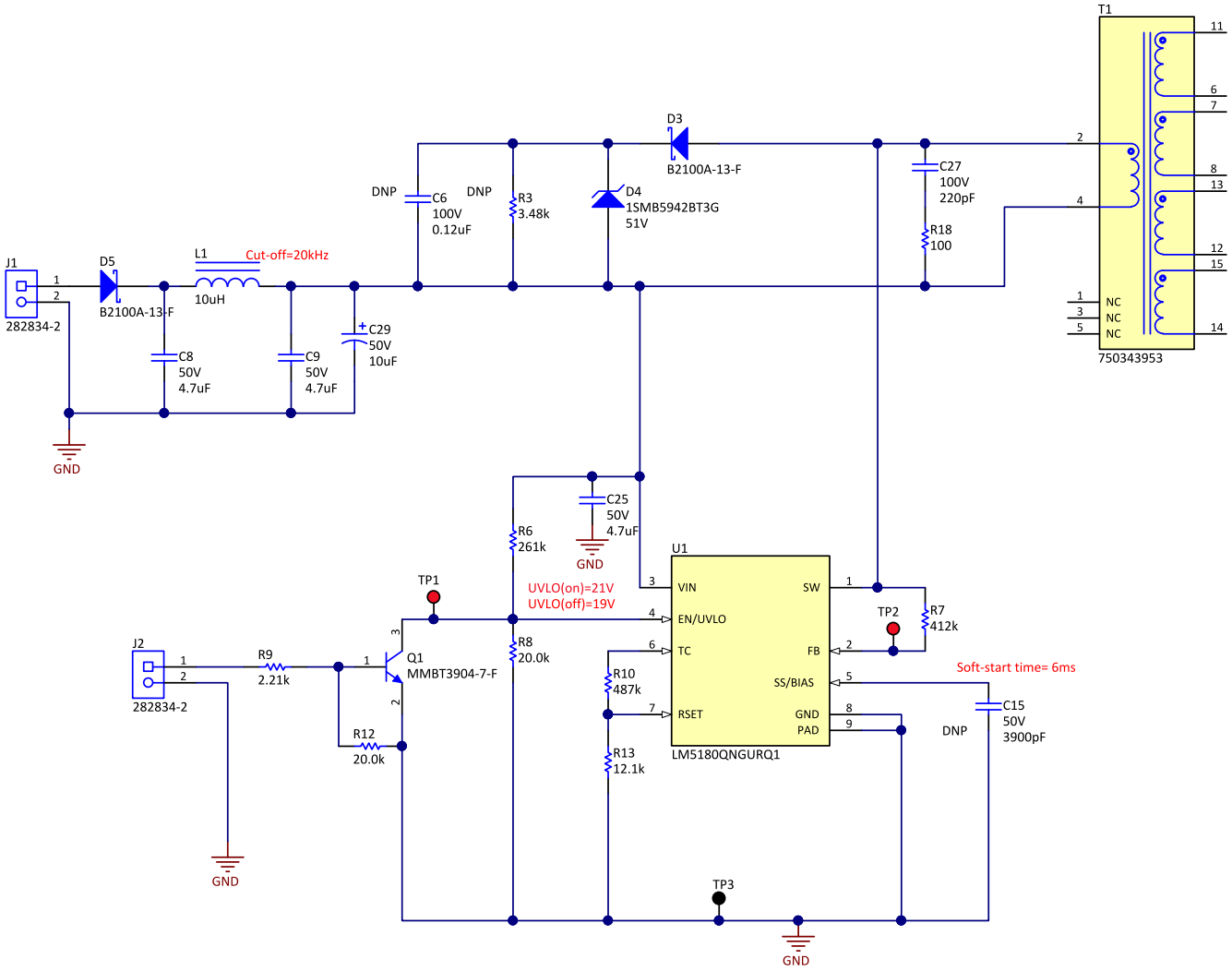
2.3.5.1 Start-up and Shut-Down Behavior

Figure 7 shows the LM5180 schematic. LM5180 provides an adjustable UVLO with hysteresis. This reference design has $V_{IN(UVLO-ON)}$ and $V_{IN(UVLO-OFF)}$ as 21 V and 19 V, respectively. The EN/UVLO input of the LM5180 device is enabled at 1.5 V (rising) with a hysteresis of 50 mV. Setting R6 (RUVL1) and R8 (RUV2) to 261 kΩ and 12.1 kΩ, respectively, yields 1.5 V when V_{IN} is 21 V and 1.45 when V_{IN} is 19 V, meeting the $V_{IN(UVLO-ON)}$ and $V_{IN(UVLO-OFF)}$ as Equation 11 and Equation 12 show:

$$RUV1 = \frac{V_{INON} \times \frac{V_{UVLO2}}{V_{UVLO1}} - V_{INOFF}}{I_{UVLO}} = \frac{21 \times \frac{1.45}{1.5} - 19}{5\ \mu A} = 260\ k\Omega \quad (11)$$

$$RUV2 = RUV1 \frac{V_{UVLO1}}{V_{INON} - V_{UVLO1}} = 260 \frac{1.5}{21 - 1.5} = 20\ k\Omega \quad (12)$$

Figure 7. LM5180 Schematic



Soft start prevents inrush current impacting the LM5180 device and the input supply when power is first applied, and is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. This design uses the 6-ms internally-fixed soft start by leaving the SS/BIAS pin open. However, in applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor (C15) from the SS/BIAS pin to GND.

2.3.5.2 Feedback and Thermal Compensation Resistor

For a given turns ratio of the transformer and secondary diode, the ratio between R7 (R_{FB}) and R13 (R_{RST}) determines the output voltage according to Equation 13. Taking R_{RST} as 12.1 kΩ, output voltage as 20-V, forward diode drop as 0.7 V, and the primary-to-secondary turns ratio as 1, R7 calculates as 207 kΩ.

$$R_{FB} = \frac{(V_{OUT} + V_{FWD}) \times N_{PS}}{0.1\text{mA}} = \frac{(20 + 0.7) \times 1}{0.1 \times 10^{-3}} = 207\,\text{k}\Omega \quad (13)$$

The LM5180 device employs a thermal-compensation circuit that adjusts the feedback set-point based on the forward voltage thermal coefficient of the flyback diode. The thermal compensation resistor value is determined to be 207 kΩ by Equation 14, where TC_{Diode} is the absolute value of the temperature coefficient of the flyback diode, equal to 1.33 mV/°C for this reference design.

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{3\frac{mV}{°C}}{TC_{Diode}\left(in\frac{mV}{°C}\right)} = \frac{207\,k\Omega}{1} \times \frac{3\frac{mV}{°C}}{1\frac{mV}{°C}} = 621\,k\Omega \quad (14)$$

2.3.6 Output Section

2.3.6.1 Flyback Diodes

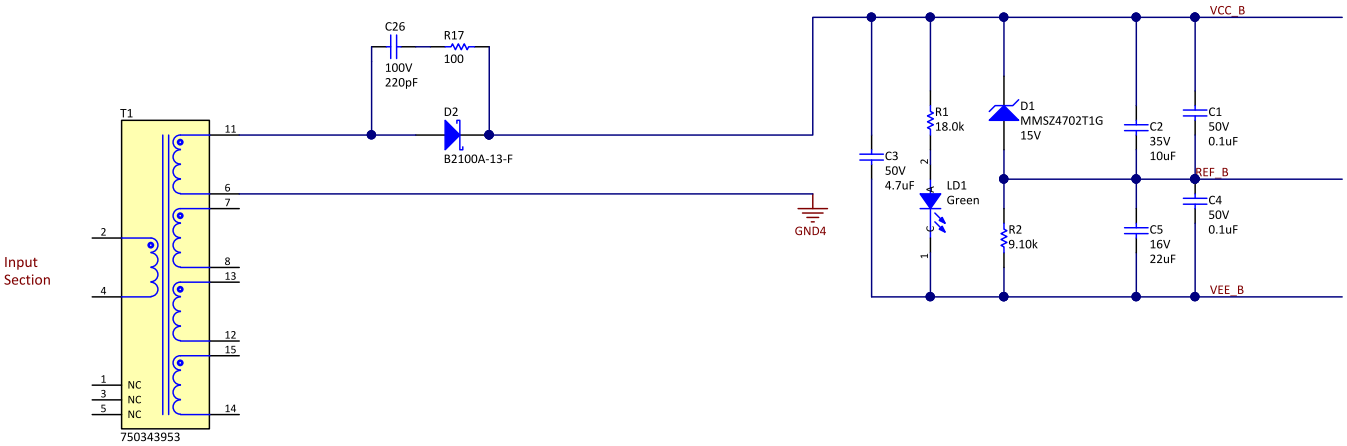
The secondary (flyback) diodes used in the design should withstand the maximum secondary current peak ($I_{PK,SEC}$) as well as the maximum reverse voltage across the diode. The diode should also have low-leakage current to avoid losses and hence a decrease in the efficiency; this can be achieved by using ultra-fast switching diodes.

The maximum primary peak current of the LM5180 device is 1.45 A which translates to a secondary peak current of 1.45 A with a turns ratio of 1:1. The maximum output average current to be provided by the design is 0.150 A. Thus, the flyback diode should have a surge current greater than 3 A at 350 kHz, and an average current rating greater than 0.3 A. The reverse voltage across the diode when the primary side MOSFET is turned on is given by Equation 15.

$$\left(\frac{V_{IN(MAX)}}{N_{PS}} + V_O + V_{RING}\right) = \left(\frac{28}{1} + 20 + 20\right) = 68\ V \quad (15)$$

Hence, the diode is rated to at least 70-V.

Figure 8. Output Section Schematic



The diodes used in the design and shown in Figure 8 are rated to 100-V, 2 A I_{AVG_MAX}. The surge current can be estimated to be greater than 3 A at 350 kHz from the data sheet. It has a leakage current of 1 mA at 80 V at a 25°C ambient temperature, which yields small losses.

2.3.6.2 Generation of Positive and Negative Bias for Gate Driver

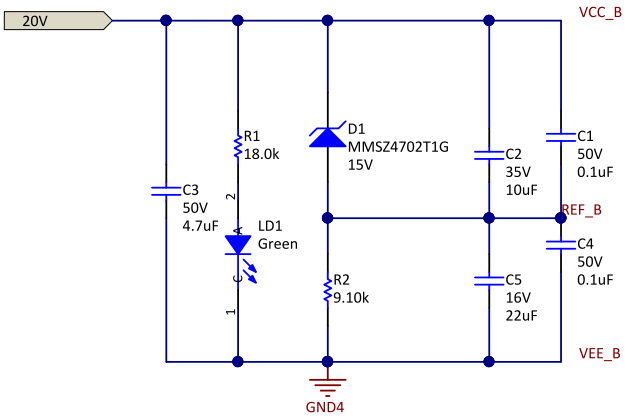
As specified in Section 1.1, this design generates 15 V and –5 V for the input to the gate drivers. Thus, the 20 V generated at the 4 output rails needs to be divided to 15 V and –5 V. This can be done in the following ways:

- Separate windings for 15 V and –5 V
- Voltage split circuit:
  - Two Zener diodes (15 V and 5 V) in series
  - Single Zener diode with a series resistor

The voltage split circuit is a compromise between the solution size and regulation. Using a separate winding for each output results in the best regulation and efficiency, but increases the size and pin count of the transformer. For this centralized-driver bias supply design, it is impractical to have eight windings for all eight outputs given the requirements of high-voltage insulation spacing. In addition, the voltage split scheme enables flexibility of setting the positive and negative voltage levels. Unlike the separate winding method, the voltage split scheme does not restrain to the transformer turns ratio.

With the Zener diode, the 15-V rail can have a stable output with a tight regulation tolerance, which is important for the turn-on speed of high power IGBTs. For –5 V, using the resistor provides a larger variation margin as compared to the 5-V Zener, but the negative bias is less critical in terms of the level of accuracy. The purpose of the negative bias is to prevent a high dV/dt induced false turn-on of the IGBT in motor drive and high-voltage inverter applications. As long as the negative bias has low enough potential, it can maintain the secure turn-off of an IGBT. Hence, a 15-V Zener diode along with series resistance is used for all four rails as Figure 9 shows.

Figure 9. Positive and Negative Bias for Gate-Driver Schematic



The selection of the Zener diode and the series resistance has to be decided with the target to minimize their power consumption while providing enough current required for the Zener to operate in the Zener region. Hence, use a Zener diode with far less knee current. This design uses a Zener diode with knee current rated at 50 µA. Thus, a very high resistance (9.10 kΩ) can be used in series with the diode thus minimizing the power losses.

2.3.6.3 Output Capacitors

Figure 9 shows a part of the schematic with the various output capacitors used on the secondary side of each rail. The minimum capacitance value can be calculated according to Equation 16.

$$C_{OUT} > \frac{I_{OUT} \times \left(I_{PK-PRI(MAX)} - \frac{I_{OUT}}{N_{PS}} \right)^2}{I^2_{PK-PRI(MAX)} \times f_{SW} \times \Delta V_{out}} \quad (16)$$

where

- $I_{PK-PRI(MAX)}$ is the maximum primary current that can be taken by MOSFET
- N_{PS} is the turns ratio
- ΔVout is the variation in output voltage

The design uses 4.7 µF, 50 V, and X7R rated capacitors across all the four 20-V rails.

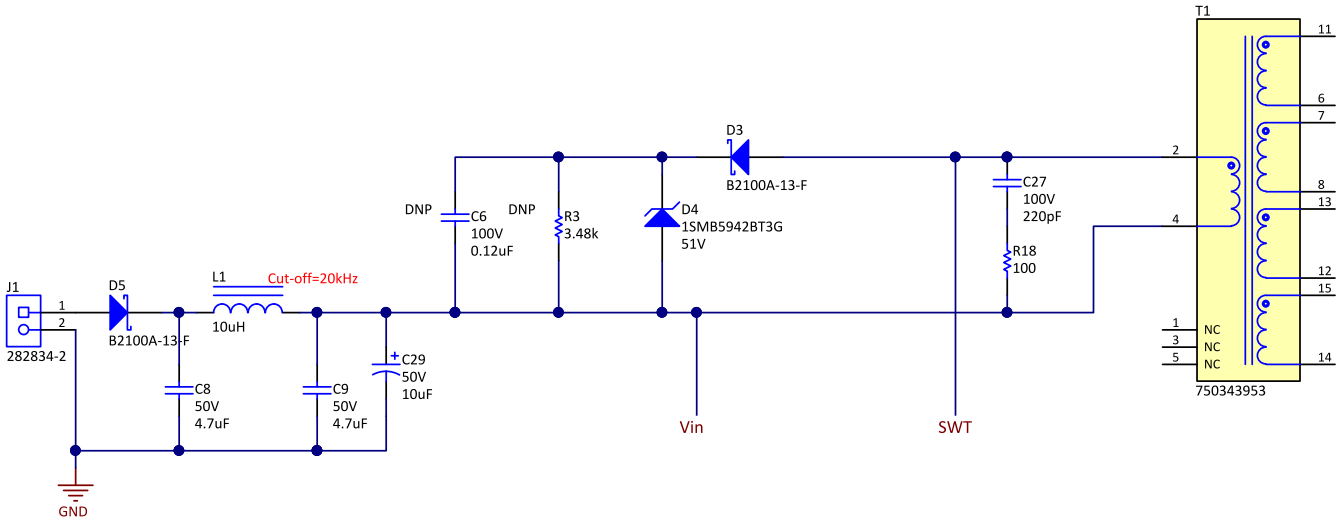
Since, this reference design is scalable to generate 24 V (15 V and –8 V), the voltage ratings of the capacitors used are 35 V and 16 V, respectively. In addition to C2 and C5 as Figure 9 shows, 0.1-µF capacitors are also added across the 15-V and –5-V rails to reduce the effect of ESL at frequencies beyond the self-resonant frequency of C2 and C5.

2.3.7 Leakage Energy Management

When the primary MOSFET is turned off, ideally the current should instantaneously become zero; however, some energy is trapped in the leakage inductance of the transformer windings. This inductance rings with the stray capacitances in the circuit, producing large amplitude, high-frequency oscillations. There are two problems with this: first, there is excessive voltage on the drain of the MOSFET which can lead to breakdown and eventually failure of the device. Second, the ringing energy is radiated and conducted throughout the power supply, load, and electronic system, creating noise issues. The ringing frequency also shows up as a peak of the EMI spectrum in both radiated and conducted EMI. Thus, there is a need to dissipate this leakage energy through an external snubber circuit. Three different snubber circuits can be explored on the basis of clamped voltage at the MOSFET drain, impact on overall efficiency, and suppression of ringing.

The RC-series snubber is used primarily in the case of excessive ringing, with transformers of high leakage inductance. However, the RC-series snubber continuously dissipates energy, reducing energy as compared to RCD, or Zener clamp snubber circuits. The transformer used in this design has relatively less leakage inductance (< 1%) hence, the RC-series snubber circuit is not required here. When comparing the Zener clamp and RCD snubber, the RCD snubber clamps the drain voltage of the MOSFET at a lesser value for light loads at the cost of efficiency. A Zener clamp is used in this reference design as Figure 10 shows, due to ease-of-design and higher light load efficiency than the RCD snubber.

Figure 10. Snubber Circuit Schematic



In the case of a Zener clamp snubber, the power dissipated in the snubber can be calculated using Equation 17 as follows:

$$P_{SNUBBER} = \frac{\frac{1}{2} \times L_{LK} \times I_{PK-PRI(MAX)}^2 \times f_{SW}}{1 - \frac{V_{REFLECTED}}{V_{ZENER}}} \quad (17)$$

where

- The leakage inductance (L_{LK}) of the transformer is measured to be 317 nH
- The primary peak current ($I_{PK,PRI}$) and switching frequency (f_{SW}) is calculated according to the mode of operation

A Zener diode of 51 V, 5 W (D4) is used along with a Schottky diode (D3) which only conducts when the drain voltage exceeds 75 V (V_{IN} + V_{ZENER}).

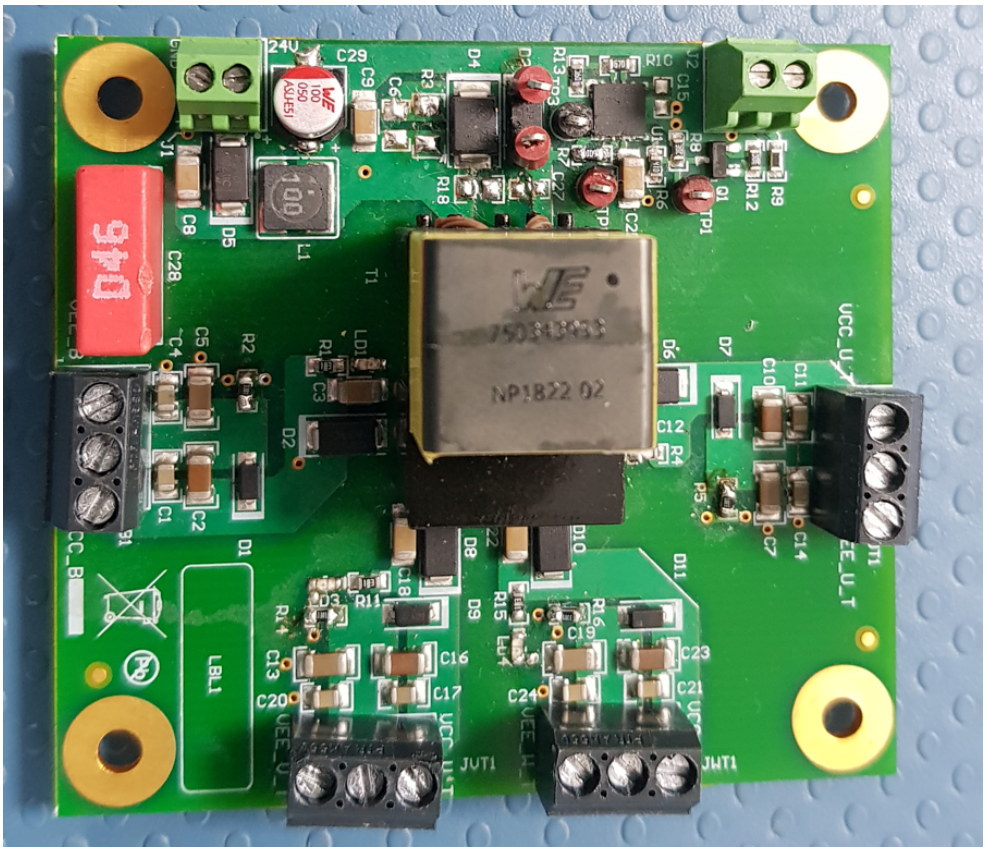
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Getting Started Hardware

3.1.1 PCB Overview

Figure 11 shows the top view of the TIDA-010006.

Figure 11. TIDA-010006 Top View



The TIDA-010006 board is very compact, with 57.20-mm × 60.00-mm dimensions. J1 is a 2-pin connector which supplies the 24-V input voltage. JUT1, JVT1, JWT1, and JB1 are 3-pin connectors giving the output voltage of 15 V and -8 V for the three top gate-driver power supplies and the bottom gate-driver supply, respectively.

3.2 Testing and Results

3.2.1 Startup and Shutdown Behavior

Figure 12 and Figure 13 highlight the VCC_B and VEE_B during V_{IN} UVLO at full load (150 mA) and no load, respectively, for the bottom gate-driver power supply. Figure 14 and Figure 15 highlights the VCC_U and VEE_U during V_{IN} UVLO at full load (50 mA) and no load respectively for one of the top gate-driver power supply This is in accordance with V_{INOFF}, which is set to be 19 V. Figure 16 and Figure 17 show the VCC_B and VEE_B V_{IN} UVLO during the power up of the supply at full load and no load respectively for the bottom gate-driver power supply.

Figure 18 and Figure 19 show the VCC_U and VEE_U V_{IN} UVLO during the power up of the supply at full load and no load respectively for one of the top gate-driver power supply. This is in accordance with V_{INON}, which is set to be 21 V .

Figure 12. VCC_B and VEE_B During V_{IN} UVLO at Full Load (150 mA)

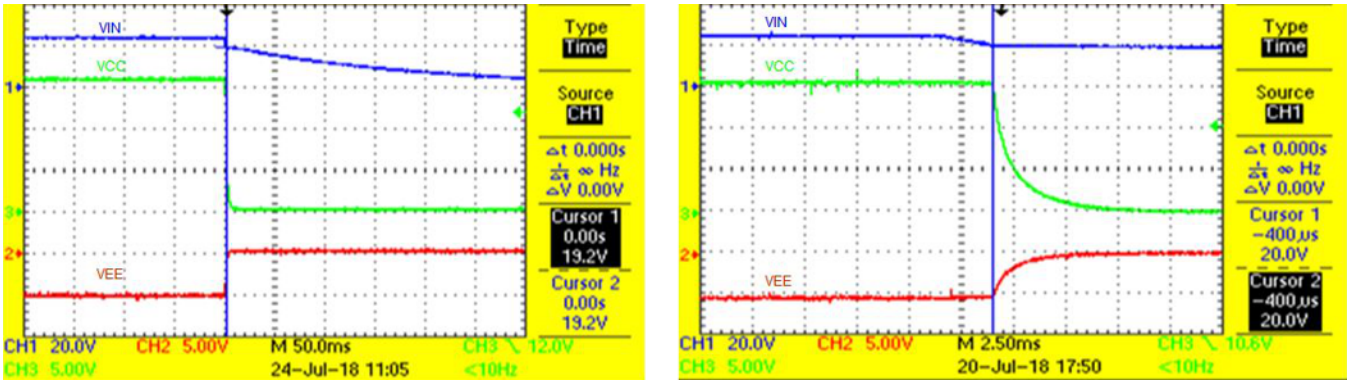


Figure 13. VCC_B and VEE_B During V_{IN} UVLO at No Load

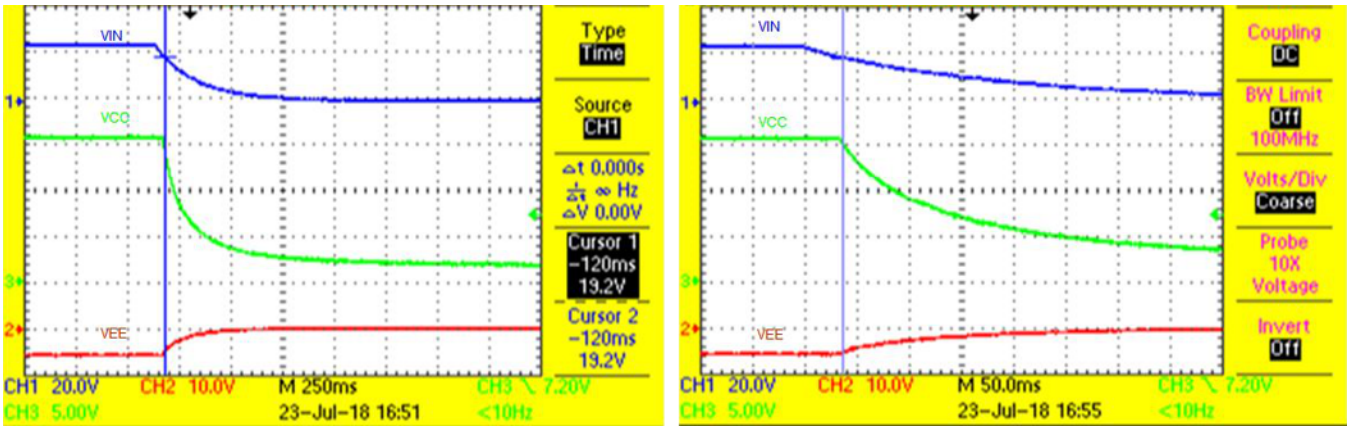


Figure 14. VCC_U and VEE_U During V_{IN} UVLO at Full Load (50 mA)

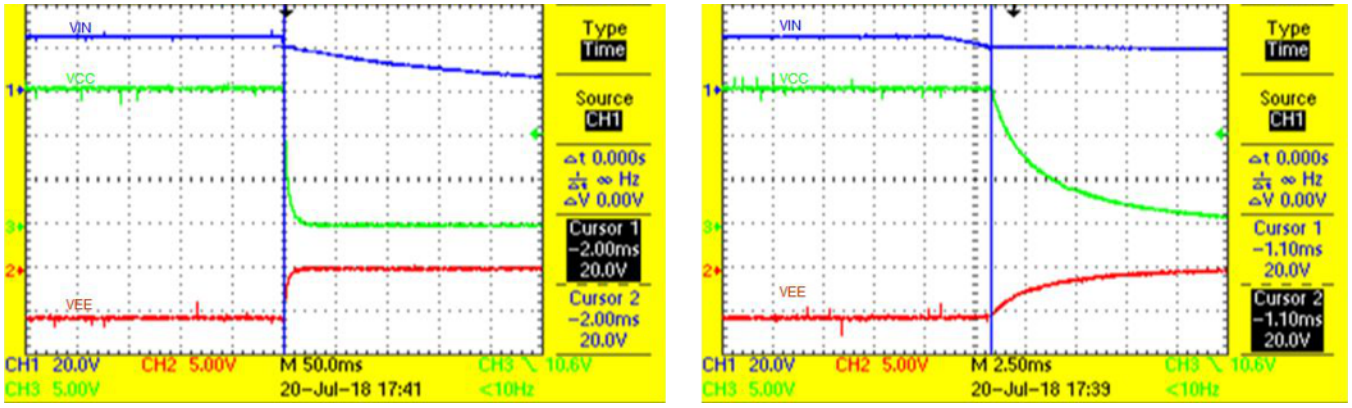


Figure 15. VCC_U and VEE_U During V_{IN} UVLO at No Load

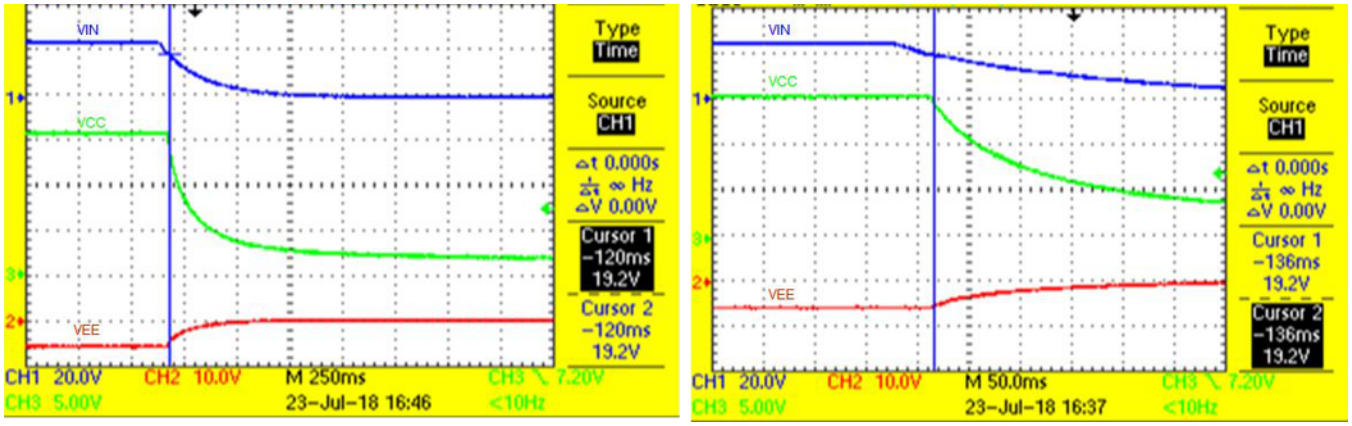


Figure 16. Power up - VCC_B and VEE_B at Full Load (150 mA)

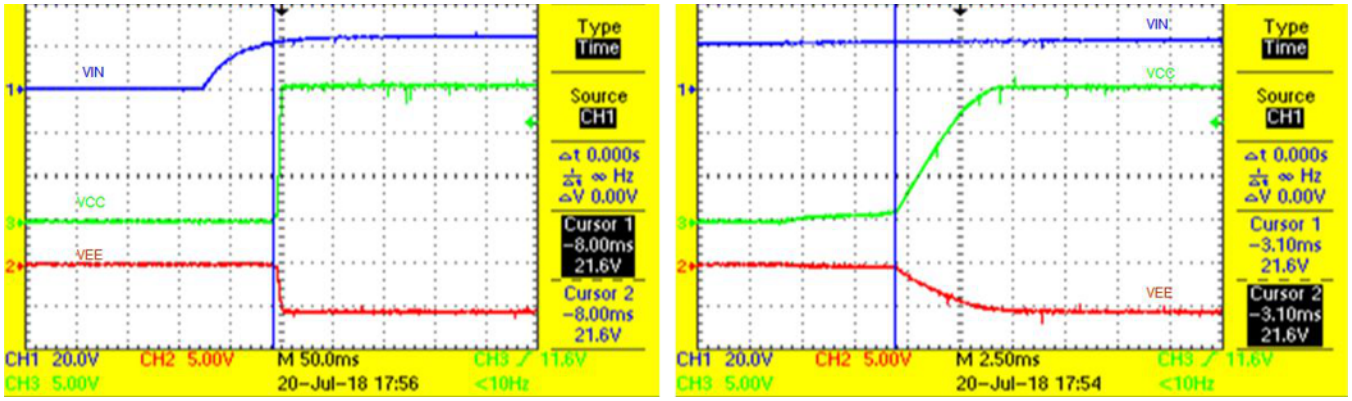


Figure 17. Power up - VCC_B and VEE_B at No Load

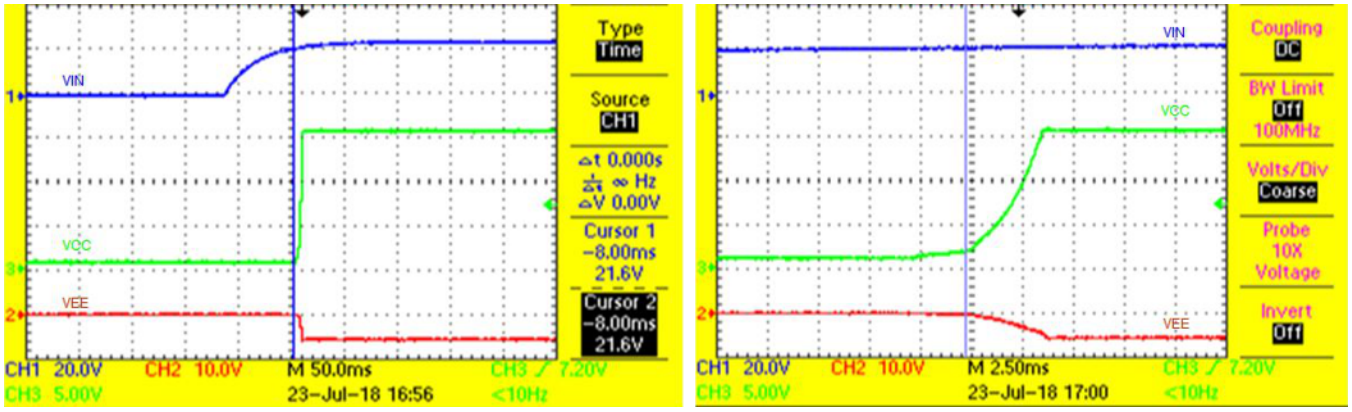


Figure 18. Power up - VCC_U and VEE_U at Full Load (50 mA)

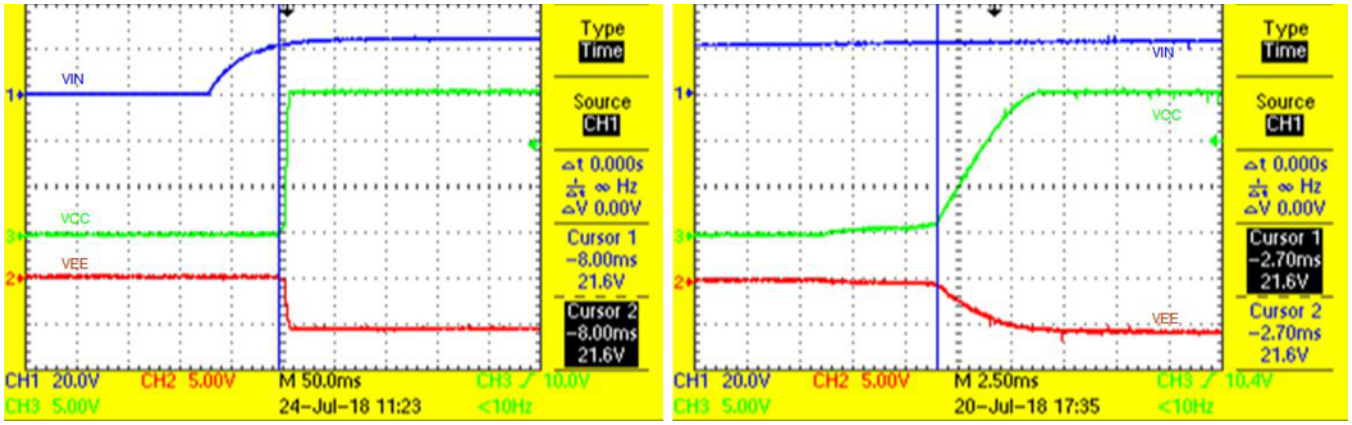


Figure 19. Power up - VCC_U and VEE_U at No Load

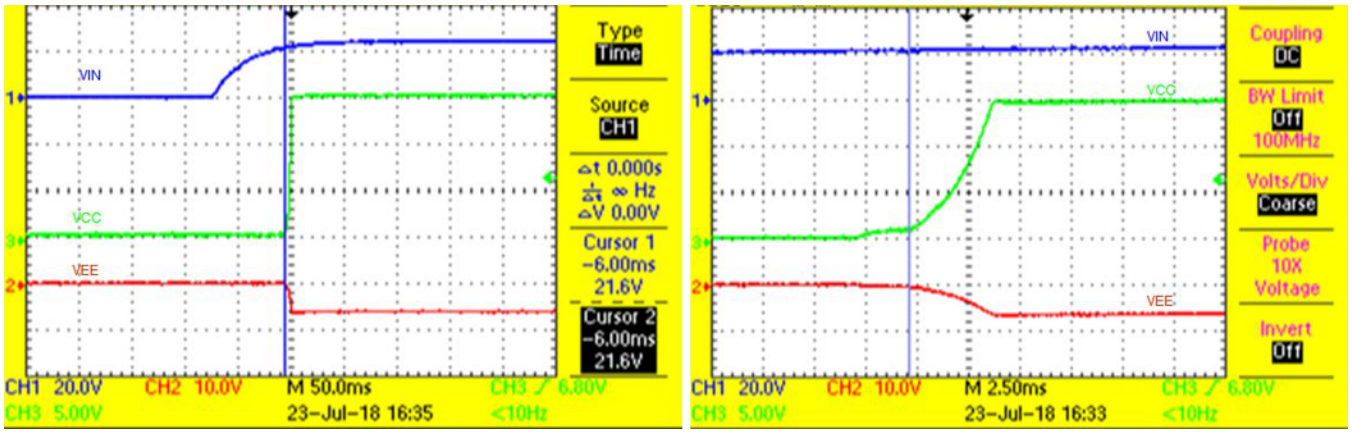
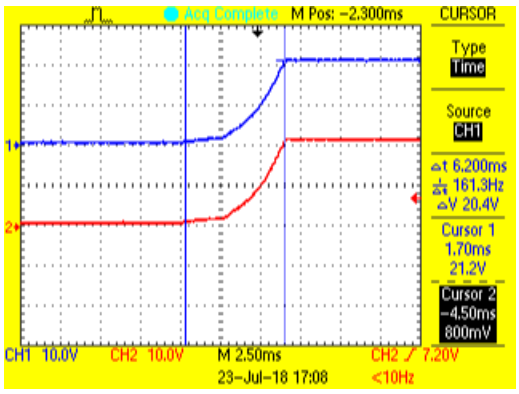


Figure 20 also shows the soft-start time of 6 ms which is set by default when the SS pin is left open.

Figure 20. Soft Start Time With SS Pin Open



3.2.2 Output Ripple

Figure 22 shows the output ripple across the maximum power output rail (intended to supply the top IGBTs) when the system is loaded at 100%. This rail provides the maximum load current (50 mA), 4.68 mV and 2 mV is the maximum output ripple across the 15-V (VCC_U) and –5-V (VEE_U) rails, respectively.

Figure 22 shows the output ripple across the maximum power output rail (intended to supply the bottom IGBTs) when the system is loaded at 100%. This rail provides the maximum load current (150 mA), 10.62 mV and 3.31 mV is the maximum output ripple across the 15-V (VCC_B) and –5-V (VEE_B) rails, respectively.

Figure 21. VCC_U and VEE_U Ripple Voltage at Full Load

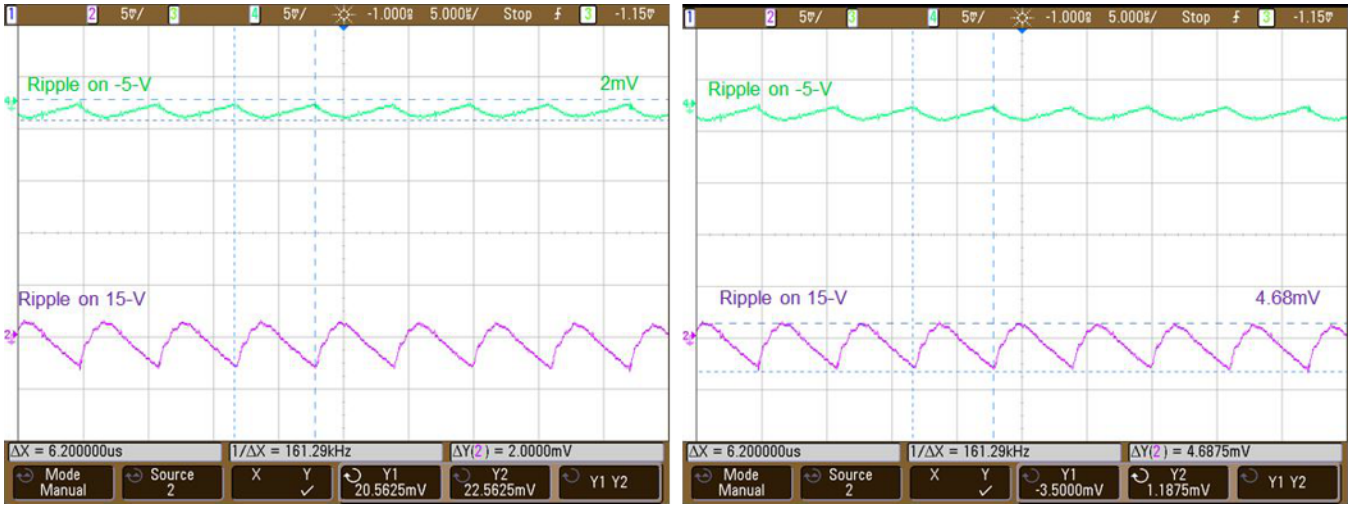
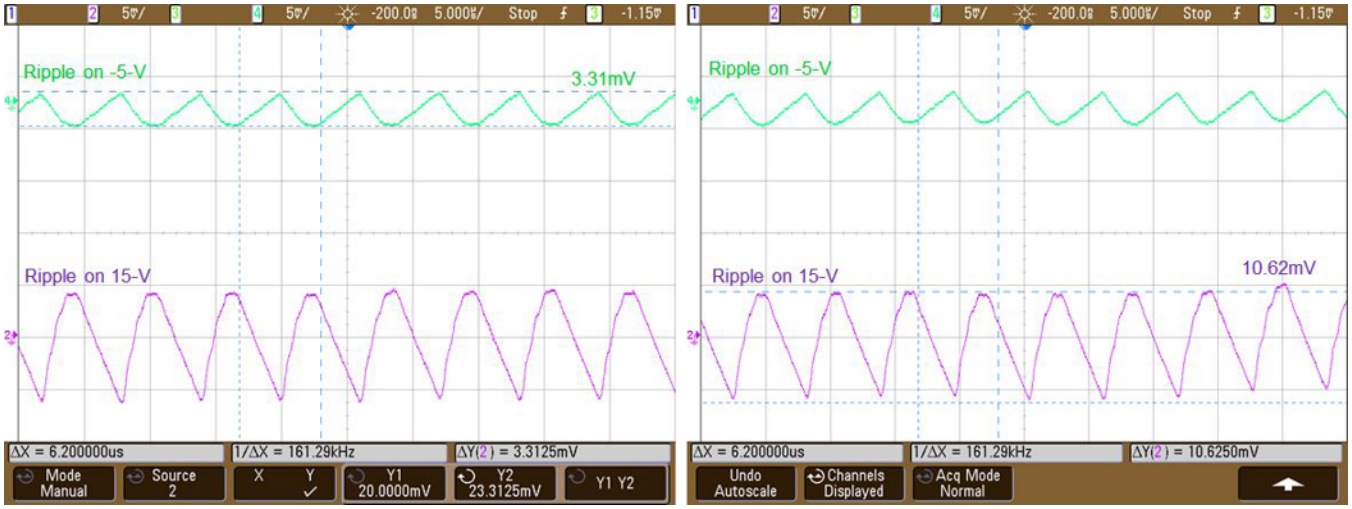


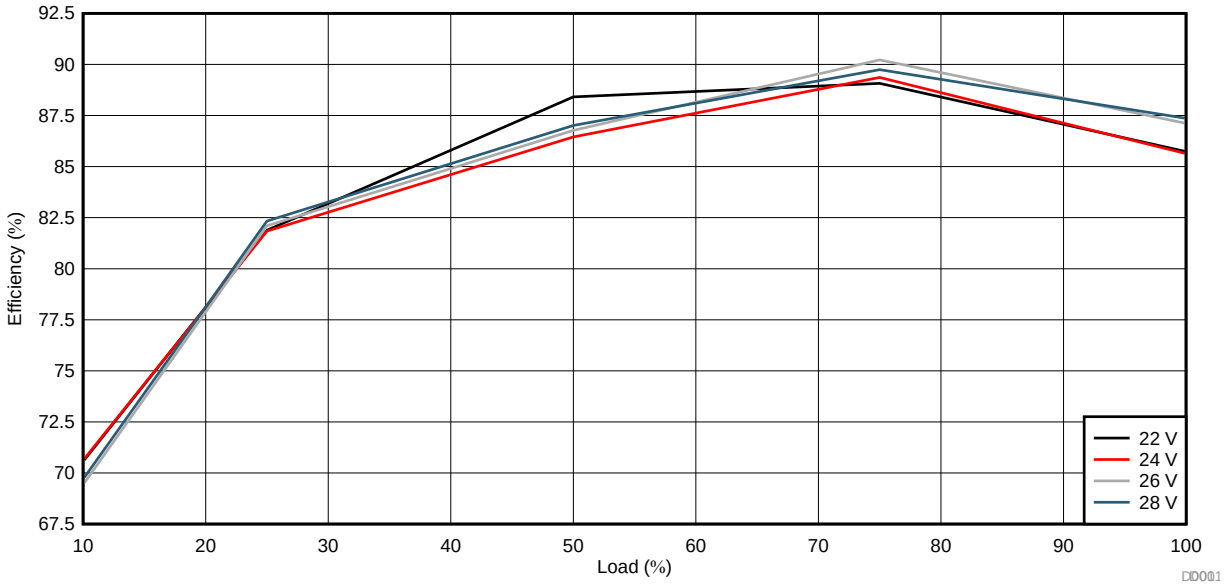
Figure 22. VCC_B and VEE_B Ripple Voltage at Full Load



3.2.3 Efficiency

The efficiency is measured at loads varying from 10% to 100%. When the system is loaded at 50% for example, each rail is loaded at 50% of its maximum load. Thus, the VCC and VEE for the bottom IGBTs are loaded with thrice the load of each VCC and VEE of the top IGBTs. Figure 23 shows that the efficiency ranges from 70% to 90% as the load is increased from 10% to 100%.

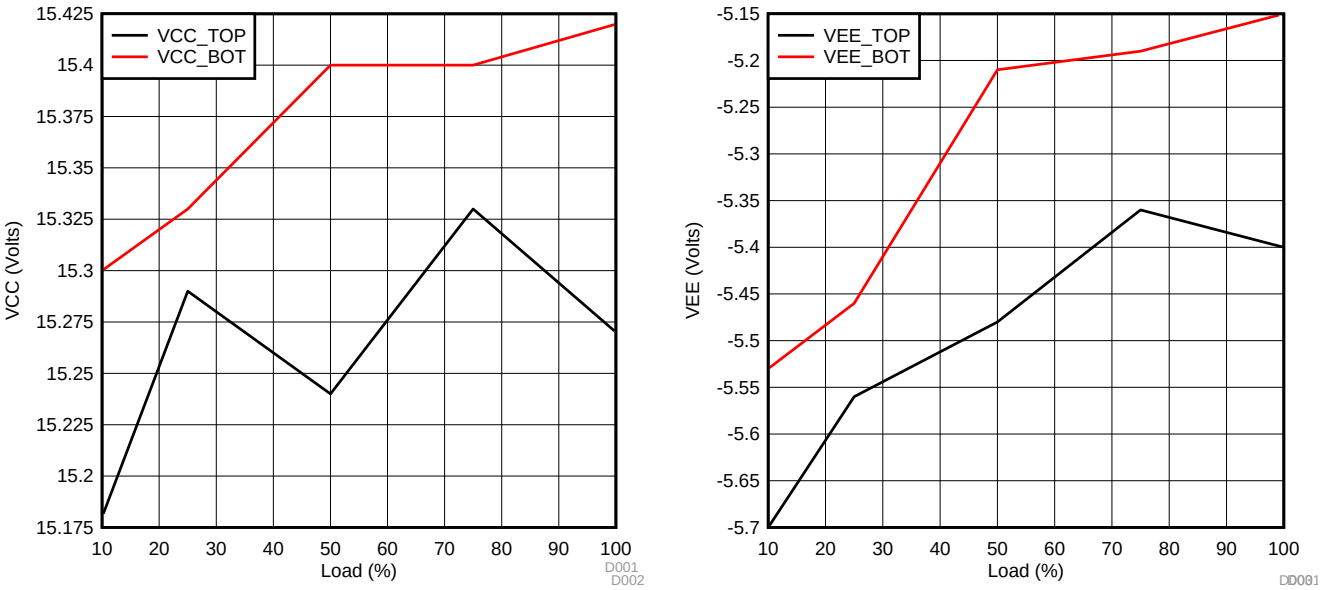
Figure 23. Efficiency Under Balanced Load at Different Input Voltages



3.2.4 Load, Line. and Cross Regulation

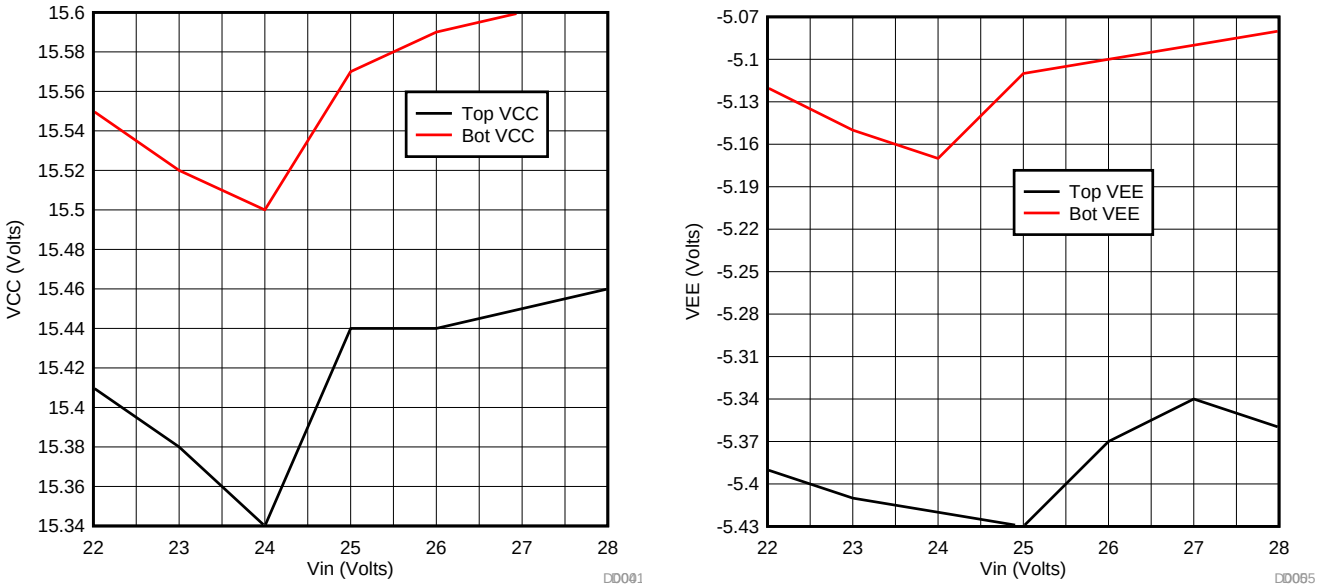
Figure 24 shows where the load regulation is measured for VCC_U and VCC_B, VEE_U and VEE_B at 24-V input voltage.

Figure 24. VCC and VEE Load Regulation at 24-V Input



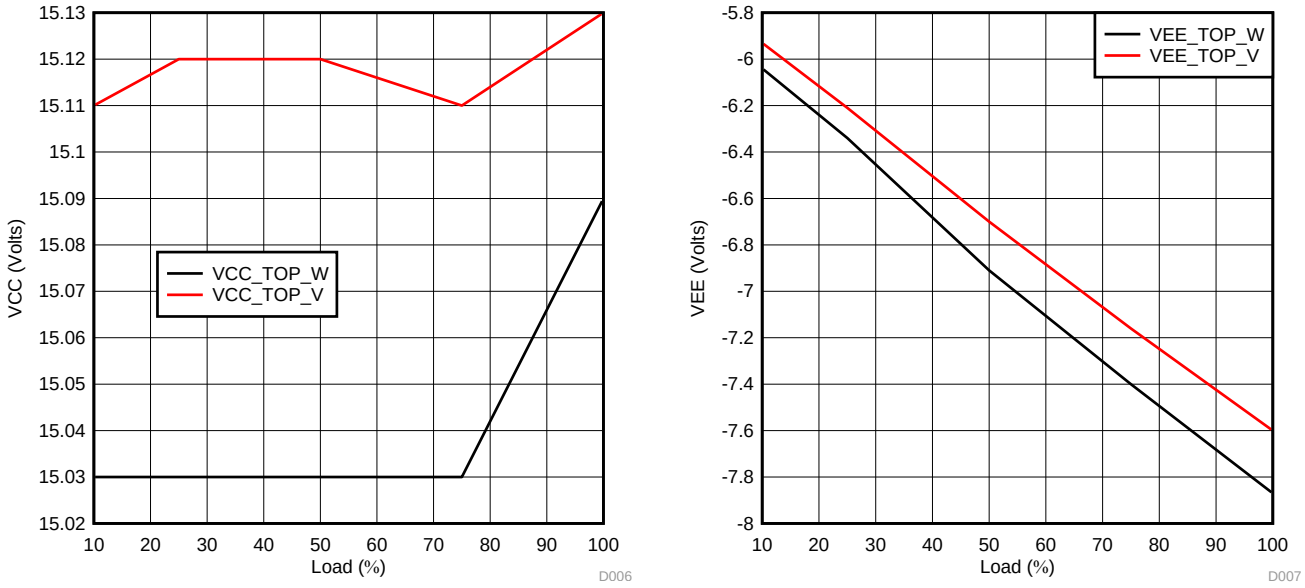
As Figure 25 shows, line regulation is measured at full load, by varying the input voltage from 22 V to 28 V.

Figure 25. Line Regulation at Full Load (6 W)



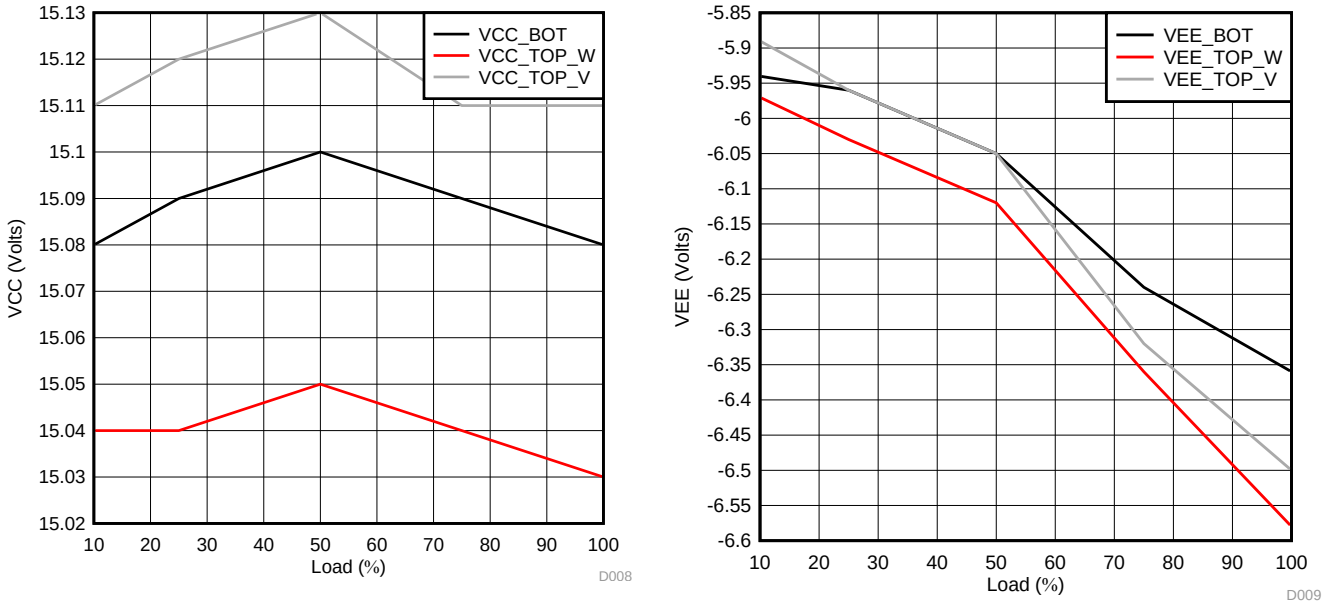
Cross regulation is measured by keeping the three output rails (VCC_U and VEE_U, VCC_V and VEE_V, VCC_W and VEE_W) for the top IGBTs at no load and varying the bottom IGBT output rail (VCC_B and VEE_B) from 10% to 100%. Figure 26 plots the output voltage for two of the top IGBT supply rails (VCC_V and VEE_V, VCC_W and VEE_W) as the load on the bottom IGBT rail is varied.

Figure 26. Cross Regulation With Top Rails Lightly Loaded and Load on the Bottom Rail is Varied From 10% to 100%



In Figure 27, cross regulation is measured by keeping the two output rails for the top IGBTs (VCC_V and VEE_V, VCC_W and VEE_W) and the output rail for the bottom IGBT (VCC_B and VEE_B) at no load and varying the top IGBT output rail (VCC_U and VEE_U) from 10% to 100%.

Figure 27. Cross Regulation With Two Top Rails and Bottom Rail Lightly Loaded and Load on the Third Top Rail is Varied From 10% to 100%



3.2.5 Snubber Circuit Performance at Full Load and Switch Node Voltage at No Load

Figure 28 shows the MOSFET drain at full-load and 24-V input voltage, when the leakage energy is maximum. Since a 51-V Zener diode is used, the drain voltage is clamped at roughly 68 V. Also, the switching frequency at full load is 170 kHz.

Figure 28. Switch Node Waveform at Full Load (6 W)

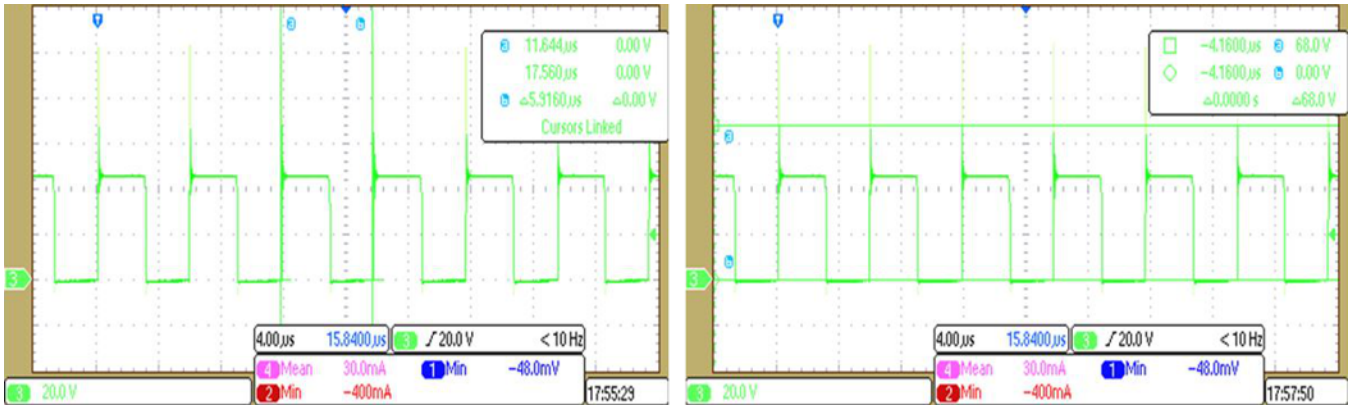
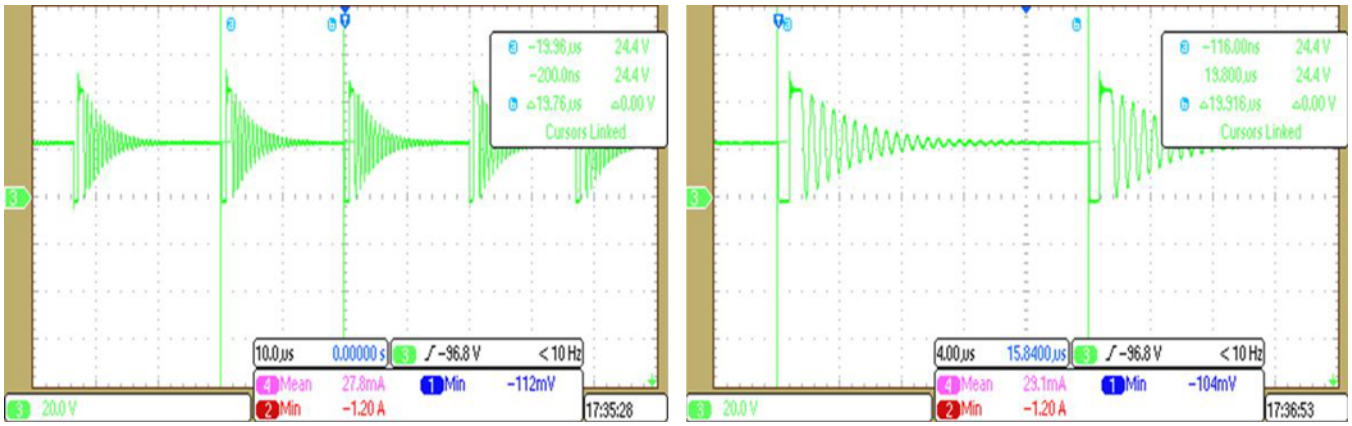


Figure 29 shows the MOSFET drain at no-load and 24-V input voltage. The switch node voltage reaches 50 V and the switching frequency goes down to 50 kHz to support the current requirement at light loads

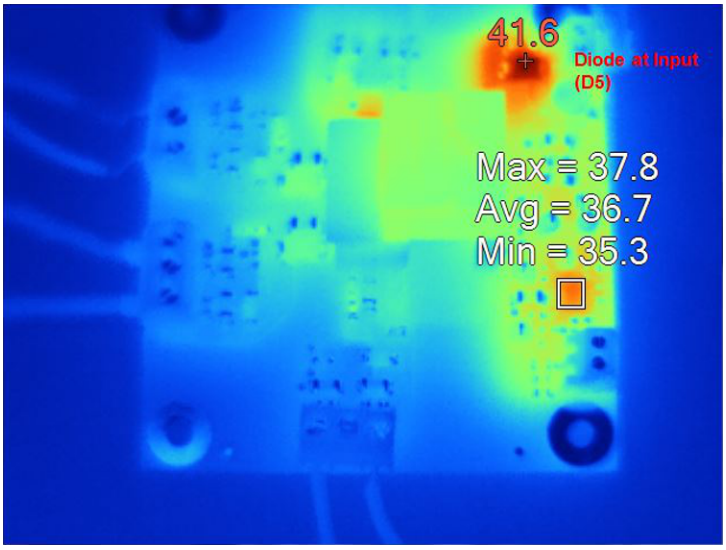
Figure 29. Switch Node Waveform at No Load



3.2.6 Temperature Measurement

Figure 30 shows the thermal image of the board when all the rails are loaded at 100% and ambient temperature is kept at 25°C. The board is kept in operation for 20-minutes to bring the package temperature rise to equilibrium.

Figure 30. TIDA-010006 Thermal Image After Running for 20 Minutes at Full Load



3.2.7 Testing with Gate-Drivers and IGBTs

To emulate the actual drive testing, this reference design is tested with TIDA-01420 (three-phase gate-driver power stage) along with 1200-V IGBTs. Six 16-kHz complementary PWM signals for IGBT gate driving are generated using the Piccolo™ LaunchPad™ from TI. These PWM signals are fed to six UCC5350s (each connected to one 1200-V IGBT). This reference design supplies the gate-drivers. VCC_B and VEE_B rails supply the bottom IGBT gate-drivers, and the other six rails supply the positive and negative bias of the gate-driver of the top three IGBTs. Figure 31 shows an image of the setup with all the boards.

Figure 31. Setup for Testing With Gate Drivers

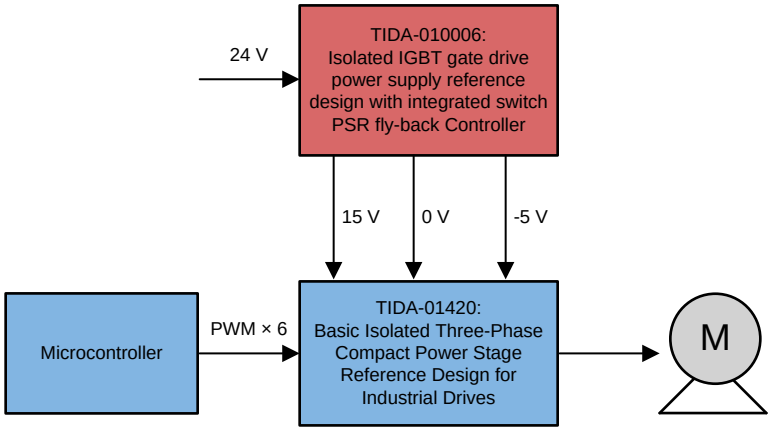


Figure 32 shows the ripple across the 15-V and –5-V rails supplying the bottom gate-drivers. Figure 33 shows the ripple across the 15-V and –5-V rails supplying the gate-driver one of the top IGBTs (phase-U).

Figure 32. Ripple Voltage Across Bottom Gate-Driver Rails

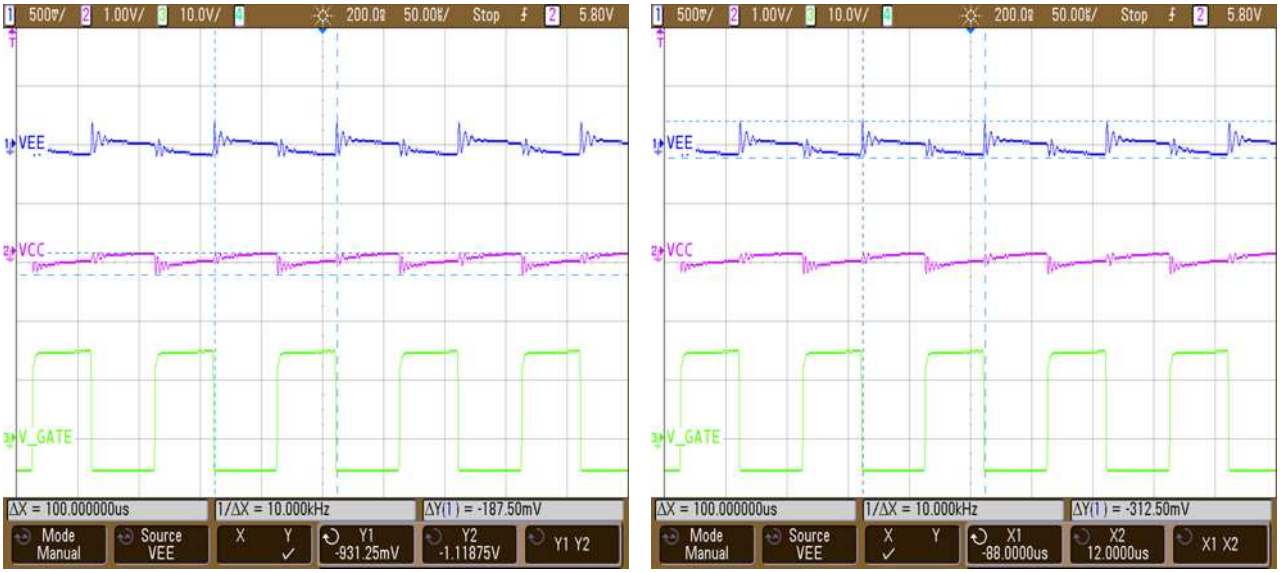
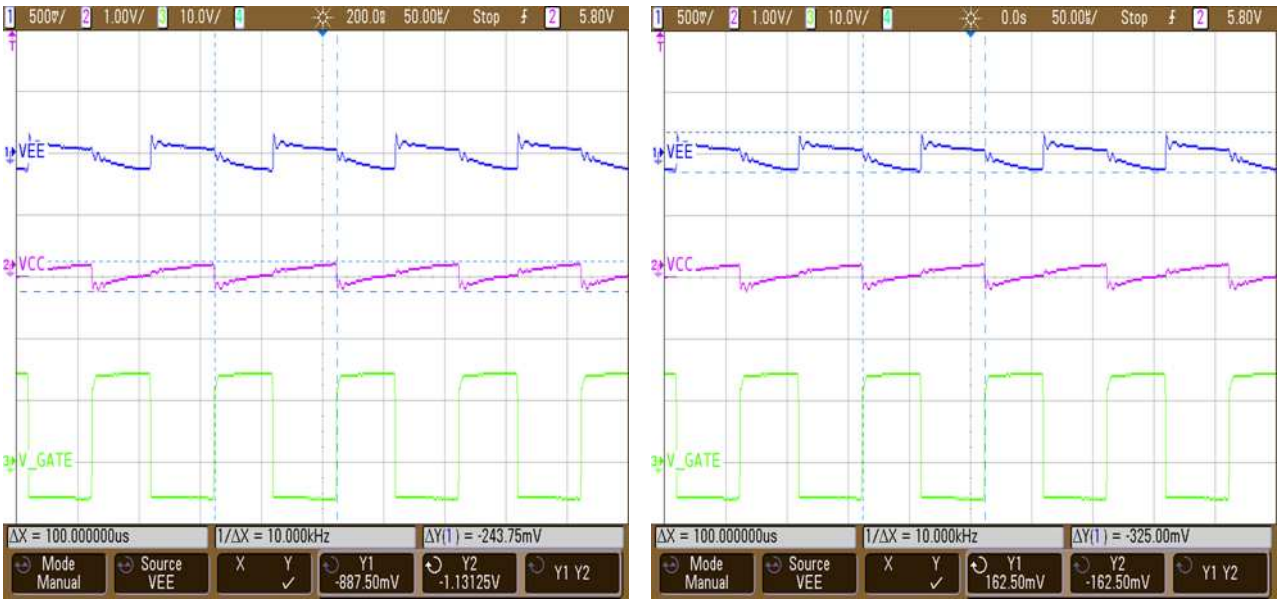


Figure 33. Ripple Voltage Across Top Gate-Driver Rail



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010006.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010006.

4.3 PCB Layout Recommendations

4.3.1 Localized Top-Layer Primary Ground Plane

The ground return paths of the primary-side components should consist of localized top-side planes that connect to the GND pin and exposed PAD. Having a ground plane only in the bottom layer necessitates the use of a via which not only creates an inductive loop but also increases the distance traveled by the signal and the risk of picking up noise along this path. Additionally, the top-layer ground plane is an important heat-dissipating area, connected to the PAD of the LM5180 device.

Figure 34. TIDA-010006 Top Layer Layout

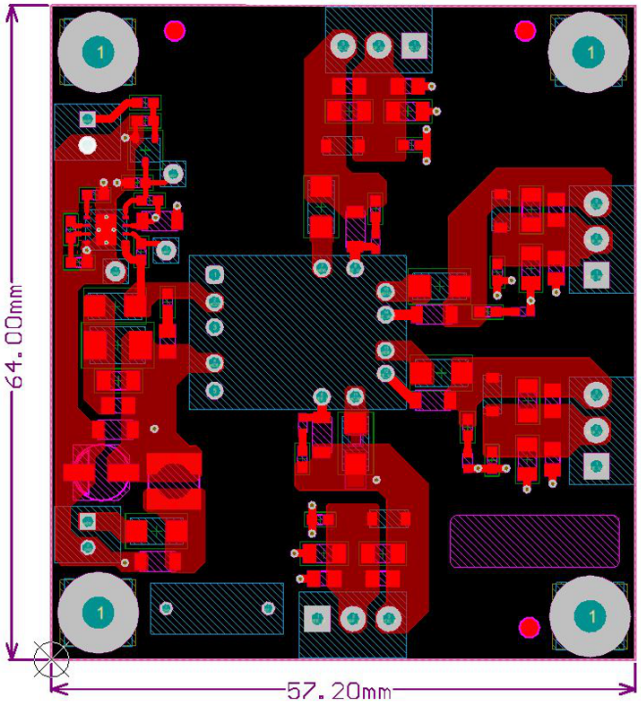


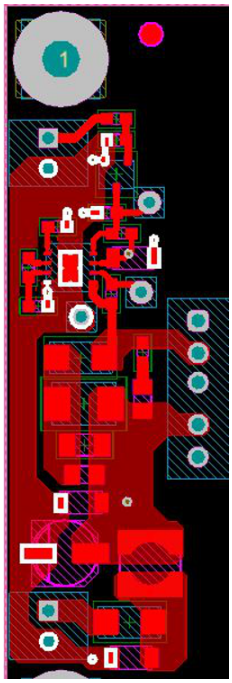
Image is not to scale.

There should be a single-point ground connection to the plane. The return connections for the reference resistor, soft-start, and enable components should be routed directly to the GND pin. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior. Figure 34 shows the top-layer of this reference design.

4.3.2 Placing Components Connected to LM5180 Pins Close to IC

Set components at RSET, TC, and SS as close as possible to the IC, and route with minimum length trace widths. Place CIN very close to the VIN pin, This eliminates as much trace inductance effects as possible and gives the internal IC rail a cleaner voltage supply. Figure 35 shows the layout of the connections made to the LM5180 device.

Figure 35. Layout of the Connections Made to LM5180 With Ground Pin Highlighted



4.3.3 Minimizing Area of Switching Loops

The LM5180 device has a maximum frequency of 350 kHz, and thus large switching loops can generate large changes in flux through the loop, resulting in higher EMI. Thus, the loop areas formed by the flyback rectifying diodes and capacitors should be minimized

4.3.4 Secondary Side Grounds Planes

Figure 36 shows the bottom layer of the layout of the TIDA-010006.

Figure 36. TIDA-010006 Bottom Layer Layout

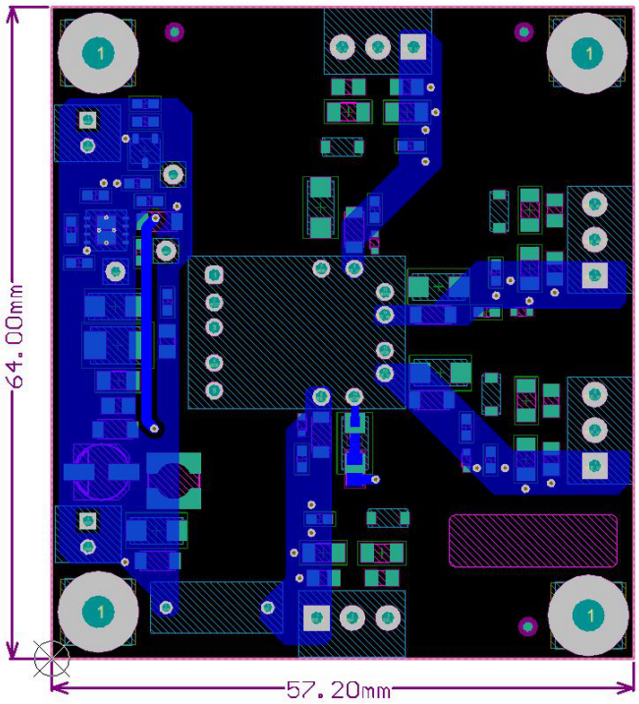


Image is not to scale.

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-010006.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010006.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010006.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010006.

5 Software Files

To download the software files, see the design files at TIDA-010006.

6 Related Documentation

1. Texas Instruments, *Power Supply Design Seminar*
2. Texas Instruments, *Reinforced Isolated IGBT Gate-Drive Flyback Power Supply With Eight Outputs Reference Guide*

6.1 Trademarks

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7 About the Author

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