Description
This reference design describes a 20.8 GSPS sampling system using RF sampling analog-to-digital converters (ADCs) in a time-interleaved configuration. The time interleaving method is a proven and traditional way of increasing sample rate; however, matching individual ADCs offset, gain, and sampling time mismatch is critical to achieve performance. The complexity of interleaving increases with a higher sampling clock. The phase matching between the ADCs is one of the critical specifications to achieve better spurious-free dynamic range (SFDR) and effective number of bits (ENOB). This reference design uses the noiseless aperture delay adjustment feature on the ADC12DJ5200RF device with a 19 fs precise phase control steps that eases 20.8 GSPS interleaving implementation. The reference design uses an onboard low-noise JESD204B clock generator based on the LMK04828 and LMX2594 devices that meets the 12-bit system performance requirement.

Features
- 20.8 GSPS time interleaved, 12-bit, RF-sampling ADCs
- 6-GHz analog front end
- Fine sample clock phase adjustment (19 fs resolution)
- Phase synchronization of multiple ADCs
- Companion power reference design with a > 85% efficiency at 12-V input
- JESD204B supporting 8, 16, or 32 JESD lanes, data rates up to 12.8 Gbps per lane
- Includes FMC+ connector compatible with TI’s TSW14J57EVM capture card

Applications
- Oscilloscope (DSO)
- Data acquisition (DAQ)
- Electronic warfare

Resources
- TIDA-010128 Design Folder
- ADC12DJ5200RF Product Folder
- LMK04828, LMX2594, LMK61E2 Product Folder
- LMH5401, LMH6401 Product Folder
- TPS259261 Product Folder
- TIDA-01027 Product Folder
- ADC12DJ5200RFEVM Tool Folder
- TSW14J57EVM Tool Folder
1 System Description

Figure 1 shows a typical high-speed digitizer front end block in which most components are common for high-speed applications like high-speed giga sample oscilloscope and high-speed digitizer. The key care about resolution, bandwidth, and sample rate are similar in specification. The digitizer can vary from the oscilloscope in terms of front-end attenuation, channel count with advanced triggering capability.

Figure 1. Typical High-Speed Digitizer Analog Font End

5G-enabled systems require test instruments with fast sampling and enough bandwidth to allow for the increased the channel capacity. These system must provide high signal-to-noise ratio, and wide dynamic range with low noise to enable accurate measurement.

The ADC is the main component limiting the performance of the system. Single ADC cores with higher sample rates and wider bandwidths require large investments. However, time-interleaving multiple ADCs help achieve a higher sample rate with lower cost. Precise multi-channel clock-phase alignment capability and ADC channel characteristic matching is required to reduce interleaving sampling distortion and achieve the required system ENOB.

This reference design helps to address onboard time interleaving ADC design challenges and demonstrates how to minimize timing errors to achieve system signal-to-noise ratio (SNR), SFDR, and ENOB performance.

1.1 Key System Specifications

Table 1 lists the key system level specifications for the TIDA-010128 board.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input channels</td>
<td>2 channels (on-chip interleaving)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 channel (onboard interleaving)</td>
<td></td>
</tr>
<tr>
<td>Input type</td>
<td>Single ended</td>
<td></td>
</tr>
<tr>
<td>Input impedance</td>
<td>50 Ω</td>
<td></td>
</tr>
<tr>
<td>Input analog bandwidth (~3 dB)</td>
<td>6 GHz, transformer input</td>
<td></td>
</tr>
<tr>
<td>Maximum sample rate</td>
<td>10.4 GSPS - 2 channels</td>
<td>Section 3.2.3</td>
</tr>
<tr>
<td></td>
<td>20.8 GSPS - 1 channel</td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bit</td>
<td></td>
</tr>
<tr>
<td>System performance (~1 dB full scale)</td>
<td>SNR</td>
<td></td>
</tr>
<tr>
<td>FS = 20.8 GHz</td>
<td>53.6 dB at 797 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>67.01 dB at 797 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8.5 bits at 797 MHz</td>
<td>Figure 31</td>
</tr>
<tr>
<td></td>
<td>53.5 dB at 997 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>66.4 dB at 997 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8.5 bits at 997 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>49.7 dB at 4000 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>56.5 dB at 4000 MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7.7 bits at 4000 MHz</td>
<td></td>
</tr>
<tr>
<td>Connectors</td>
<td>560-pin FMC+ interface connector supports TSW14J57 high-speed capture card</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>12 V DC, 4 A</td>
<td></td>
</tr>
<tr>
<td>Form factor (L × W)</td>
<td>295 mm x 176 mm</td>
<td></td>
</tr>
</tbody>
</table>
2 System Overview

2.1 Block Diagram

Figure 2 shows the system-level block diagram of the TIDA-010128 design which was developed using the hardware from the 12.8-GSPS analog front end reference design for high-speed oscilloscope and wide-band digitizer (TIDA-01028).

Figure 2. TIDA-010128 System Block Diagram
2.2 Design Considerations

In both high-speed oscilloscopes and digitizers, the total system performance is determined by the core ADC, jitter introduced by the clocking solution, and the analog front end signal chain, typically containing input attenuators, amplifiers, and filter blocks. To maximize system ENOB, the error sources from these companion devices must be minimized. Figure 3 shows the subsystem block with the associated error sources which limits system performance.

**Figure 3. Analog Front End With Error Sources**

![Analog Front End With Error Sources Diagram]

- Attenuator
- Pre-amp
- Filter
- Driver
- ADC
- Offset, Gain error
- Amplifier Noise
- Phase distortion
- Frequency flatness
- Clock
- Quantization noise
- Aperture Jitter
- Interleave error

2.2.1 Interleave Design Challenges

To achieve higher sample rates, multiple ADCs are time-interleaved into a single or composite ADC. Each ADC is sampled at the same time period with equally-spaced time intervals and then the captured data is formatted to achieve higher sample rates. To achieve accurate sampling, the individual ADCs offset, gain, and phase between ADCs should be exactly matched. However, in practical terms this is not possible and mismatch must be managed and minimized, otherwise system performance is degraded by the introduction of interleaving spurs.

**Figure 4. 2 × ADC Interleaved Non-Ideal ADC**

![2 × ADC Interleaved Non-Ideal ADC Diagram]

Figure 4 shows a two-ADC interleaved system with typical error sources like offset error, gain error, and time mismatch error between two ADCs which generate predictable spurs in the spectrum of the system.

These error sources and their impact are explained in the 12.8-GSPS Analog Front End Reference Design for High-Speed Oscilloscope and Wide-Band Digitizer Design Guide for the TIDA-01028 reference design.
2.2.2 Circuit Design

2.2.2.1 Analog Input Front End

Figure 5 shows the analog front end circuit of the TIDA-01022 reference design. A flexible analog input allows validation of the system performance with two different input paths; each input can accept the signal from either the transformer or the amplifier chain, based on the hardware jumper selection. All channels are well matched in terms of path delay, clock routing, and so forth.

Figure 5. TIDA-01022 Analog Front End

2.2.2.2 Interleave Clock Requirement

The TIDA-01022 hardware has a flexible clocking platform which helps designers validate system performance with various clocking source options. The default onboard clocking solution uses the LMX2594 clock synthesizer which has excellent phase noise at high frequency. A clock distribution chip, the LMK04828 device, is used to provide the reference signal to the LMX2594 device, FPGA DCLK, FPGA_CORECLK, and FPGA_SYSREF.
The ADC_SYSREF, FPGA_CORECLK, FPGA_REFCLK, and FPGA_SYSREF are to be calculated based on the ADC device clock (ADC_DEVCLK) requirement and SERDES lanes used for capture.

To achieve a 20.8-GSPS sample rate, the following clocks were generated by the onboard clocking solution provided in this design:

- ADC_DEVCLK = 5.2 GHz; to operate ADC in 10.4 GSPS single-channel mode
- ADC_SYSREF = 32 MHz
- FPGA_CORECLK = 260 MHz
- FPGA_SYSREF = 32.5 MHz SERDES lane rate = 16

Both the LMX2594-A and LMX2594-B devices are configured to generate 5.2 GHz at RFOutA for DEVCLK and 32.5 MHz at RFOutB for SYSREF from the 65-MHz reference at the OSCin input which is connected to the OSCout of the LMK04828 device via the LMK00304 clock buffer.
The LMK04828 device is used to provide the required FPGA clocks. Table 2, Table 3, and Table 4 show the signal definitions and clock output frequency.

### Table 2. LMK04828 Clock Definition for TIDA-010128

<table>
<thead>
<tr>
<th>SLNO</th>
<th>LMK04828 SIGNALS</th>
<th>FREQUENCY OUTPUT</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OSCout p/n</td>
<td>65 MHz</td>
<td>Connected to the LMX2594 reference input for generation of ADC, DEVCLK, and SYSREF</td>
</tr>
<tr>
<td>2</td>
<td>DCLKOUT0 p/n</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>3</td>
<td>SDCLKOUT1 p/n</td>
<td>-</td>
<td>Not used, LMX SYSREF or LMX SYSREFREQ</td>
</tr>
<tr>
<td>4</td>
<td>DCLKOUT2 p/n</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>5</td>
<td>SDCLKOUT3 p/n</td>
<td>-</td>
<td>Not used, LMX SYSREF or LMX SYSREFREQ</td>
</tr>
<tr>
<td>6</td>
<td>DCLKOUT4 p/n</td>
<td>260 MHz</td>
<td>FPGA_REF CLK, connected slave to capture FPGA (Optional)</td>
</tr>
<tr>
<td>7</td>
<td>SDCLKOUT5 p/n</td>
<td>-</td>
<td>SYNC signal to LMX2594-B</td>
</tr>
<tr>
<td>8</td>
<td>DCLKOUT6 p/n</td>
<td>260 MHz</td>
<td>FPGA_CORE CLK, connected slave to capture FPGA</td>
</tr>
<tr>
<td>9</td>
<td>SDCLKOUT7 p/n</td>
<td>32.5 MHz</td>
<td>FPGA_SYSREF, connected slave to capture FPGA</td>
</tr>
<tr>
<td>10</td>
<td>DCLKOUT8 p/n</td>
<td>260 MHz</td>
<td>FPGA_CORE CLK, connected master to capture FPGA</td>
</tr>
<tr>
<td>11</td>
<td>SDCLKOUT9 p/n</td>
<td>32.5 MHz</td>
<td>FPGA_SYSREF, connected master to capture FPGA</td>
</tr>
<tr>
<td>12</td>
<td>DCLKOUT10 p/n</td>
<td>260 MHz</td>
<td>FPGA_REF CLK, connected master to capture FPGA (Optional)</td>
</tr>
<tr>
<td>13</td>
<td>SDCLKOUT11 p/n</td>
<td>-</td>
<td>SYNC signal to LMX2594-A</td>
</tr>
<tr>
<td>14</td>
<td>DCLKOUT12 p/n</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>15</td>
<td>SDCLKOUT13 p/n</td>
<td>-</td>
<td>Not used</td>
</tr>
</tbody>
</table>

### Table 3. LMX2594-A Clock Definition for TIDA-010128

<table>
<thead>
<tr>
<th>SLNO</th>
<th>LMX2594-A</th>
<th>FREQUENCY OUTPUT</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OSCin p/n</td>
<td>65 MHz</td>
<td>Connected to the OSCout p/n of LMK04828</td>
</tr>
<tr>
<td>2</td>
<td>RFoutA p/n</td>
<td>5.2 GHz</td>
<td>Connected to ADC-1 device clock input</td>
</tr>
<tr>
<td>3</td>
<td>RFoutB p/n</td>
<td>32.5 MHz</td>
<td>Connected to ADC-1 SYSREF input</td>
</tr>
</tbody>
</table>

### Table 4. LMX2594-B Clock Definition for TIDA-010128

<table>
<thead>
<tr>
<th>SLNO</th>
<th>LMX2594-B</th>
<th>FREQUENCY OUTPUT</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OSCin p/n</td>
<td>65 MHz</td>
<td>Connected to OSCout p/n of LMK04828</td>
</tr>
<tr>
<td>2</td>
<td>RFoutA p/n</td>
<td>5.2 GHz</td>
<td>Connected to ADC-2 device clock input</td>
</tr>
<tr>
<td>3</td>
<td>RFoutB p/n</td>
<td>32.5 MHz</td>
<td>Connected to ADC-2 SYSREF input</td>
</tr>
</tbody>
</table>

Once all the clocks are generated, a 90° phase difference between the two ADC channels can be established with the following procedure:

The TICSPro GUI helps to create the configuration files for the LMK61E2, LMK04828, and LMX2594 devices. Download the latest High-Speed Data Converter (HSDC) TID GUI software from: [http://www.ti.com/tool/TICSPRO-SW](http://www.ti.com/tool/TICSPRO-SW).

### 2.2.2.3 Establishing 90-Degree Phase Alignment

The TIDA-01022 hardware has a flexible clocking solution with a number of clocking options to allow users to validate system performance with various clocking configurations. One clocking option in this reference design is selected which satisfies the interleaving design clocking requirements. This clocking solution provides flexibility to adjust the clock delay in three places in the clocking path. This delay can be done on the LMK04828 output, LMX2594 output, the ADC12DJ5200RF device, or a combination of these devices.

The LMK04828 device has both analog and digital delay elements in each clock output. The LMX2594 has a MASH SEED register that can tune the delay in 9-ps increments and the ADC12DJ3200 device has Noiseless Aperture Delay Adjustment ($t_{AD\,\text{adjust}}$) features on the device clock path that can be used to shift the sampling instant in 19-fs steps.
Figure 7 shows the internal clock subsystem of the ADC12DJ5200RF device and highlights t_{AD} components (TAD_INV, TAD_COARSE, and TAD_FINE). These registers allow maximum aperture delay adjustment up to t_{AD}(max) = 293 ps and ultra-low aperture jitter t_{AD}(max) = 70 fs to satisfy the low-phase noise requirements.

Figure 7. ADC12DJ5200RF Clocking Subsystem

This t_{AD} feature gives the flexibility to adjust any one or both registers of the ADC to make required phase shift between ADCs with 19-fs resolution.

Equation 1 helps to calculate the required phase delay between ADCs:

\[ t_{\text{PHASEDELAY}} = \frac{t_{\text{SAMPLECLK}} \times \text{Reg\_phase}}{360} \]

where

- \( t_{\text{SAMPLECLK}} \) = device clock time period . 1/Fs
- \( \text{Reg\_Phase} \) = required phase shift between two ADCs
- \( t_{\text{PHASEDELAY}} \) = phase delay between two ADCs

To interleave the two ADC12DJ5200RF devices onboard, a 90° phase shift between ADC clocks is required by using Equation 2 for a 5.2-GHz device clock:

\[ \frac{t_{\text{SAMPLECLK}}}{2^{16} \times \text{ADC device rate \_MHz}} = 192.3 \text{ ps} \]

\[ t_{\text{PHASEDELAY}} = 192.3 \times 10^{-12} \times 90 = 48.07 \text{ ps} \]

As previously discussed, a phase delay of 48.07 ps is attained either with the LMX2594 device using MASHSEED, or the ADC12DJ5200 device using t_{AD}, or a combination of both.

In this reference design, the required 90° (48.07 ps) phase shift was established with the LMX2594 device using the MASHSEED register.

2.2.2.4 Power Tree

This TI design uses a high-performance, optimized power solution from the TIDA-01027 reference design. This power module satisfies the power requirements of the TIDA-01022. The module contains both DC/DC and LDO regulators with an external frequency SYNC feature for synchronization of multiple switching regulators. Also, a method of clock phase shifting enables users to reduce both conducted and radiated EMI.
For more information, see the Low noise power-supply reference design maximizing performance in 12.8 GSPS data acquisition systems (TIDA-01027).

2.3 Highlighted Products

2.3.1 ADC12DJ5200RF - 12-Bit, Dual 5.2-GSPS or Single 10.4-GSPS, RF-Sampling ADC

The ADC12DJ5200RF device is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual-channel mode, it can sample up to 5.2-GSPS and in single channel mode up to 10.4-GSPS. It has full power input bandwidth (–3 dB) of 8.0 GHz, with usable frequencies exceeding the –3 dB point in both dual- and single-channel modes, and allows direct RF sampling of the L-band, S-band, C-band, and X-band for frequency agile systems.

2.3.1.1 Why Choose the ADC12DJ5200RF? Key Features

The ADC12DJ5200RF device has an integrated t\(_{AD}\) adjust feature which allows shifting of the clock instants in fine steps (19 fs) to achieve 90-degree phase between two ADCs for time interleave sampling. Figure 7 shows the ADC12DJxx00 family internal clocking subsystem.

- Automatic SYSREF calibration, uses the t\(_{AD}\) adjust feature to shift the device clock to maximize the SYSREF setup and hold times or align the sampling instance based on the SYSREF rising edge.
- SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins.

In addition to these features, this device family offers various sampling rates starting from 1600 MHz to 5200 MHz and 8 to 12 bits of resolution with the same pinout. It allows customers the flexibility to change the data converter speed and resolution based on their applications with the same printed circuit board (PCB). Also, there is no need for much hardware and software development.

In addition to the aperture adjustment, some of the key specifications taken into account include SNR, ENOB, and so forth – other similar devices considered are listed in Table 5.
### Table 5. ADC12DJ5200RF - Similar Devices

<table>
<thead>
<tr>
<th>ADC12DJ5200RF</th>
<th>ADC08DJ3200</th>
<th>ADC12DJ2700</th>
<th>ADC12DJ3200</th>
<th>ADC12J1600</th>
<th>ADC12J4000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order now</td>
<td>Order now</td>
<td>Order now</td>
<td>Order now</td>
<td>Order now</td>
<td>Order now</td>
</tr>
<tr>
<td>Online Data Sheet</td>
<td>Online Data Sheet</td>
<td>Online Data Sheet</td>
<td>Online Data Sheet</td>
<td>Online Data Sheet</td>
<td>Online Data Sheet</td>
</tr>
<tr>
<td>Sample rate (Max) (MSPS)</td>
<td>5200</td>
<td>3200</td>
<td>2700</td>
<td>3200</td>
<td>1600</td>
</tr>
<tr>
<td>Resolution (Bits)</td>
<td>12</td>
<td>8</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Number of input channels</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Interface</td>
<td>JESD204B</td>
<td>JESD204B</td>
<td>JESD204B</td>
<td>JESD204B</td>
<td>JESD204B</td>
</tr>
<tr>
<td>Analog input BW (MHz)</td>
<td>8000</td>
<td>8000</td>
<td>8000</td>
<td>8000</td>
<td>3300</td>
</tr>
<tr>
<td>Features</td>
<td>Ultra-high speed</td>
<td>Ultra-high speed</td>
<td>Ultra-high speed</td>
<td>Ultra-high speed</td>
<td>Ultra-high speed</td>
</tr>
<tr>
<td>Rating</td>
<td>Military</td>
<td>Catalog</td>
<td>Catalog</td>
<td>Catalog</td>
<td>Catalog</td>
</tr>
<tr>
<td>Input range (Vp-p)</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.725</td>
</tr>
<tr>
<td>Approx. price (US$)</td>
<td>896.50</td>
<td>100u</td>
<td>1619.50</td>
<td>100u</td>
<td>1919.50</td>
</tr>
<tr>
<td>Power consumption (Typ) (mW)</td>
<td>4010</td>
<td>2800</td>
<td>2700</td>
<td>3000</td>
<td>1600</td>
</tr>
<tr>
<td>Architecture</td>
<td>Folding interpolating</td>
<td>Folding interpolating</td>
<td>Folding interpolating</td>
<td>Folding interpolating</td>
<td>Folding interpolating</td>
</tr>
<tr>
<td>SNR (dB)</td>
<td>55.1</td>
<td>49.1</td>
<td>56.7</td>
<td>56.6</td>
<td>55</td>
</tr>
<tr>
<td>ENOB (Bits)</td>
<td>8.7</td>
<td>7.8</td>
<td>9</td>
<td>9</td>
<td>8.8</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>68</td>
<td>67</td>
<td>71</td>
<td>67</td>
<td>70</td>
</tr>
<tr>
<td>Operating temperature range (°C)</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
</tr>
</tbody>
</table>

#### 2.3.2 LMK04828- Ultra Low Noise JESD204B Compliant Clock Jitter Cleaner

The LMK0482x family is the highest performance clock conditioner with JESD204B support in the industry. The 14 outputs from PLL2 can drive up to seven JESD204B data convertors or other logic devices like FPGA. The device has both analog and digital delay in each clock output path and analog delay can be adjusted 25-ps fine steps.

Figure 9 shows by combining both LMK04828 and LMX2594 devices, high-performance, low-noise clocking subsystems are created that drive giga-sample speed data convertors with JESD204B support.
2.3.3 LMX2594- 15 GHz Wideband PLLatnum™ RF Synthesizer

The LMX2594 device is a high-performance, wideband PLL with integrated VCOs that can generate frequencies from 10 MHz to 15 GHz without using an internal doubler. The high-performance PLL with a figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very low in-band noise and integrated jitter.

The LMK2594 device is an ideal companion part for the ADC12DJxx00 family. The LMK2594 generates a very low noise clock for high-speed data convertor and generates repeating SYSREF which is compliant with the JESD204B standard.

2.3.4 LMK61E2- Ultra-Low Jitter, Fully-Programmable Oscillator

The LMK61E2 device is an ultra-low jitter PLLatinum programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly-used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL. The device offers ultra-low jitter, as low as 90-fs RMS and the maximum clock output can generate up to 1 GHz with 50 ppm frequency stability. In this reference design, the LMK61E2 device is used to provide a reference clock for the LMK04828 device.
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware components are needed to perform the test:
1. 1 × TIDA-01022 hardware
2. 2 × TSW14J57EVM
3. 1 × USB2ANY programmer
4. 1 × Splitter (supports up to 6 GHz)
5. 1 × Variable band-pass filter (100 MHz to 6 GHz)
6. 2 × Laptop or desktop PC (Microsoft® Windows® 10 OS installed)
7. 1 × 12 V, 4-A DC adapter or lab power supply

3.1.2 TIDA-01022 Hardware Functional Block

Figure 10 shows the TIDA-01022 board with the TIDA-01027 power board. For more information about hardware functional blocks and programming details, see the Flexible 3.2 GSPS multi-channel AFE reference design for DSOs, RADAR, and 5G wireless test systems (TIDA-01022).
Figure 11 shows the TIDA-01027 board image, in this reference design the TIDA-01027 board is configured as DC/DC free-running mode (default mode). The TIDA-01027 output connectors are made compatible with the TIDA-01022 power input headers J58, J59, J60, and J63.

Table 6 shows the input and output specification of the TIDA-01027 power-supply module.

Table 6. TIDA-01027 Key Specification

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5 V to 17 V</td>
</tr>
<tr>
<td>Number of outputs</td>
<td>5</td>
</tr>
<tr>
<td>Output voltage, maximum output current</td>
<td>1.9 V - 4 A, 1.1 V - 4 A, 3.3 V - 4 A, 2.5 V - 1 A, (-2.5 V - 800 mA)</td>
</tr>
<tr>
<td>Efficiency</td>
<td>85%</td>
</tr>
</tbody>
</table>
The board can be connected as Figure 10 shows.

Figure 11. TIDA-01027 Hardware Image

3.1.3 Software

The TIDA-01022 board requires three application software GUIs for validation: HSDC TID GUI, HSDC Pro GUI, and the LMK61xx oscillator programming tool.

1. Use the HSDC TID GUI to configure the data converter (ADC12DJ3200), clocking devices (LMK4828, LMX2594, and LMK61E2), and digital VGA (LMH6401). Use the low-level page to program the device with the respective configuration file. Download the latest HSDC TID GUI software from: http://www.ti.com/lit/zip/tidcfb3

2. Use the HSDC Pro GUI to capture the digitized data with the assistance of a TSW14J57 capture card and provide a spectrum and time domain plot. Download the latest HSDC Pro GUI software at: http://www.ti.com/tool/dataconverterpro-sw

3.1.3.1 Getting Started Application GUI

Figure 12, Figure 13, and Figure 14 show screenshots of starting the HSDC TID GUI configuration and the Programming tab for the low-level view, respectively.

Figure 12. HSDC TID GUI – Top-Level Navigation View

![Diagram showing top-level navigation view](image)

Figure 13. HSDC TID GUI – Low-Level Programming View

![Diagram showing low-level programming view](image)
Figure 14. HSDC TID GUI - NCO Programming, Alarm Monitor View

Figure 15 shows the ADC capture screen in HSDC Pro GUI

Figure 15. HSDC Pro ADC Capture GUI (Spectrum)
3.1.3.2 **Hardware Programming**

The TIDA-01022 hardware has an onboard FTDI-brand USB controller which is for programming the LMK61E2, LMK4828, and LMX2594 clocking devices and the LMH6401 amplifier using an SPI or I2C interface. The High-Speed Data Converter (HSDC TID) graphical user interface (GUI) supports low-level pages, which can be used to program these devices.

The board also features a USB2ANY programming interface which helps the user to evaluate hardware by using the respective evaluation module (EVM) GUI.

*Figure 16 shows the location of programming connector*

![Figure 16. Programming Connector Interface](image)

The programming procedure for the built-in programming interface is as follows:

1. Open the HSDC TID GUI and select the “TIDA1022_28_32A_32B” from device selection drop-down menu.

   *Figure 17. Select a Device in the HSDC TID GUI*

   ![Figure 17. Select a Device in the HSDC TID GUI](image)

2. Navigate to the *Low Level* tab, select the configuration files to be programmed, and click the *OK* button. Follow these steps as numbered and encircled in the screen shot in *Figure 18.*
3.1.4 Host Interface

The TIDA-010128 time interleaved system performance can be evaluated using TI’s TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card. Populated with an Intel® Arria® 10 FPGA device and using the Intel Altera® products JESD204B IP solution, the TSW14J57 device can be dynamically configured to support all lane speeds from 1.6 Gbps to 15 Gbps - from 1 to 16 lanes. Together with the accompanying High-Speed Data Converter Pro Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from the TIDA-01022 reference design. The TIDA-01022 can be directly interfaced with the TSW14J57 device using the FMC+ connector interface. Figure 19 shows the TIDA-01022 interface with the TSW14J57 capture module and trigger cable connection.
Figure 19. TIDA-01022 Interface With TSW14J57 Capture Card

For more information on the TSW14J57 EVM, see the TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide.
3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Hardware Setup

Figure 20 shows the test setup for onboard time interleaving using the TIDA-01022 reference design with transformer input.

Figure 20. Test Setup for 2 × ADC12DJ5200RF Devices

3.2.1.2 Master Slave Trigger Capture

The output data from the ADC is captured using the TSW14J57 capture card since TIDA-01028 has 2 × ADC12DJ5200RF devices, 2 × TSW14J57 devices are needed for capture. To enable synchronous capture, these two TSW14J57 devices can be configured as master and slave mode then enable the software trigger in HSDC Pro GUI software.

- Figure 21 shows the TSW14J57 master slave trigger connection.
- Connect master TSW14J57, J7 (TRIG OUT –A) to J13 (TRIG IN) using a high-speed SMA cable for master self-triggering
- Connect the master TSW14J57, J8 (TRIG OUT-B) to J13 (TRIG IN) of the slave TSW14J57 module using a high-speed SMA cable.
3.2.2 Onboard Interleaving Measurement

3.2.2.1 Configure Hardware Using HSDC TID and HSDC Pro GUI:

1. Use the J32 connector to program the LMK61E2 device at 65 MHz using the USB2ANY programmer associated with the LMK61E2 oscillator programming tool. Set the device address as 0x5A before programming.

2. Load the following configuration file in the LMK04828, LMX2594 and ADC12DJ5200RF using the HSDC TID GUI as Figure 22 shows. This generates 5.2-GHz DEVCLK and SYSREF 32.5 MHz for both ADC1 and ADC2. It also generates the FPGA reference at 260 MHz, the FPGA core clock at 260 MHz, and the FPGA SYSREF at 32.5 MHz for the FPGA capture card.

3. Configure both ADC12DJ5200RF devices to JMODE1 (single-channel mode) by loading the configuration file in the low level page of HSDC Pro GUI in the following order for both master and slave capture card.

   a. Master capture card:
      i. After powering up the TSW14J57 master capture card, establish the hardware connection.
      ii. Load “ADC12DJxx00_JMODE1_trig_sysref.ini” from the select ADC drop-down menu and then update ADC Output Data Rate as 10.4 GHz
      iii. Read capture and see the ADC1 spectrum
b. Slave capture card:
   i. Power on the TSW14J57 slave capture card then establish the connection with hardware similar to the master card.
   ii. Load “ADC12DJxx00_JMODE1_trig_sysref.ini” from the select ADC drop-down menu then update ADC Output Data Rate as 10.4 GHz
   iii. Read capture and see the ADC2 spectrum
   iv. Load “ADC12DJxx00_JMODE1_trig_sysref_skipreconfig.ini” from the select ADC drop-down menu
   v. Select Trigger Option from the Data Capture Options menu. In the Trigger Option selection menu item; select only Trigger mode enable:

   **Figure 23. Trigger Option Selection: Trigger mode enable**

   ![](image)

   vi. After enabling the trigger, the Capture button becomes Read DDR Memory (see Figure 24):

   **Figure 24. HSDC Pro Slave Capture Read: Read DDR Memory**

   ![](image)
c. Master capture card:
   i. Select **Trigger Option** from the **Data Capture Options** menu. In the selection menu item, enable both the **Trigger mode enable** and **Software Trigger enable** options:

   **Figure 25. Trigger Option Selection: ‘Trigger mode enable’ and ‘Software Trigger enable’**

   ![Trigger Option Selection](image)

   ii. After enabling the triggers, the **Capture** button becomes **Generate Trigger** (see **Figure 26**):

   **Figure 26. HSDC Pro Slave Capture Read: Generate Trigger**

   ![Generate Trigger](image)

3.2.2.2 *Interleave Capture*

1. Feed the input signal frequency 997 MHz, –1 dBFS to channel 1 (J12) and channel 3 (J29) from the signal source via splitter.

2. “Read DDR memory” from the slave capture card, make sure the slave is ready for trigger input for capture.

3. Apply “Generate Trigger” from the master capture card, this captures data from both ADCs.

4. Export both ADC1 and ADC2 data, then extract the phase information from the spectrum using the MATLAB® program and plot the data in the time domain for a channel-to-channel skew measurement.

5. Adjust MASHSEED of the LMZ2594 device or the $t_{ADJ}$ adjust register values to make channel-to-channel skew as 48.07 ps for 90° phase clock shift between CH1 and CH3.

6. After establishing a 90° phase shift, combine both ADC1 and ADC2 data to form interleaved data for a 20.8-GSPS sample rate.
3.2.3 Test Results

In this reference design, interleaving performance is measured with $F_s = 20.8$ GSPS, $F_{in} = 300$ MHz to 6 GHz input signal frequency. Figure 27 and Figure 28 show the measured spectrum of the TIDA-010128 design at a 997-MHz input, 10.4-GSPS sample rate of ADC1 and ADC2 with 90 degree time-interval sampling.

Figure 27. ADC1 Spectrum 10.4 GSPS
Figure 28. ADC2 Spectrum 10.4 GSPS
Figure 29 and Figure 30 show the resultant spectrum of 20.8 GSPS with and without I<sub>L</sub> spur. Figure 29 shows interleave spur at locations FS/2, FS/4, FS/2-FIN, FS/4-FIN, and FS/4+FIN associated with sampling clock Fs = 20.8 GHz for input signal Fin = 997 MHz.

Figure 29. Fin = 977 MHz, 20.8 GSPS Interleave Spectrum With IL Spur
The Interleave Design Challenges section of the 12.8-GSPS Analog Front End Reference Design for High-Speed Oscilloscope and Wide-Band Digitizer Design Guide discusses more on interleave spur and its effects. Even when the input signal chain path and clock sample timing are closely matched, there will always be some mismatch in the system. This will vary due to temperature and process variations which can be reduced with the help of an on-line calibration process.
Figure 31 shows the 20.8 GSPS interleaved plots for input signal frequencies from 100 MHz to 6 GHz without I\textsubscript{L} spurs. Interleaving spurs will reduce if the gain, offset, and time skew are matched.

**Figure 31. 20.8 GSPS Interleave Plot vs Input Frequency Without I\textsubscript{L} Spur**

In summary, the TIDA-010128 is a 20.8-GSPS interleaved reference design with an onboard high-performance clock and power solution that can be used for high-speed DSO and wideband digitizer applications where higher sampling rate and wider instantaneous bandwidth is required. This reference design demonstrates the ADC12DJ5200RF interleaving features to achieve a 20.8-GSPS sample rate with usable bandwidth greater than 6 GHz with ENOB better than 7.5 bits, excluding interleaving spurs.

This reference design demonstrates the \texttt{I\textsubscript{ADJ}} feature of the ADC12DJ5200RF device that eases interleaving at 20.8 GSPS. The reference design also demonstrates a low-noise multichannel JESD204B clock generator based on the LMK04828 and LMX2594 devices that help designers to achieve low phase noise, high-frequency clock up to 15 GHz for time interleaved sampling applications.
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-010128.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-010128.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-010128.

4.4 Altium Project
To download the Altium Designer® project files, see the design files at TIDA-010128.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-010128.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-010128.

5 Related Documentation

5.1 Related Reference Designs
1. Texas Instruments, 12.8-GSPS analog front end reference design for high-speed oscilloscope and wide-band digitizer (TIDA-01028)
2. Texas Instruments, Flexible 3.2 GSPS multi-channel AFE reference design for DSOs, RADAR, and 5G wireless test systems (TIDA-01022)
3. Texas Instruments, 50-Ohm 2-GHz oscilloscope front-end reference design (TIDA-00826)
4. Texas Instruments, Multi-channel JESD204B 15 GHz clocking reference design for DSO, Radar and 5G wireless testers (TIDA-01021)
5. Texas Instruments, High speed multi-channel ADC clock reference design for oscilloscopes, wireless testers and Radars (TIDA-01017)
Related Documentation

5.2 Summary of Related Reference Designs

Table 7 details of similar and associated reference designs.

Table 7. Summary of Related Reference Designs

<table>
<thead>
<tr>
<th>REFERENCE DESIGN NUMBER</th>
<th>MAXIMUM CLOCK FREQUENCY (GHz)</th>
<th>PHASE NOISE AT MAX FREQUENCY (dBc/Hz)</th>
<th>CLOCK SKEW (ps)</th>
<th># OF CHANNELS DEMONSTRATED [THEORETICAL MAXIMUM]</th>
<th>SAMPLING RATE (GSPS)</th>
<th>SNR @ 1 GHz (dB)</th>
<th>SFDR (dBc)</th>
<th>MAXIMUM BANDWIDTH (GHz)</th>
<th>DESCRIPTION, FOCUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIDA-010128</td>
<td>15.0</td>
<td>–105.9</td>
<td>-</td>
<td>2[4]</td>
<td>20.8</td>
<td>53.5</td>
<td>66.4</td>
<td>8.0</td>
<td>20.8 GSPS AFE with Interleaved ADCs (ADC12DJ5200RF)</td>
</tr>
<tr>
<td>TIDA-01028</td>
<td>15.0</td>
<td>–105.9</td>
<td>-</td>
<td>2[4]</td>
<td>12.8</td>
<td>55.0</td>
<td>63.5</td>
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<tr>
<td>TIDA-00626</td>
<td>10.0</td>
<td>–107.1</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>9.8 GHz RF CW Signal Generator</td>
</tr>
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<td>TIDA-01016</td>
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<td>-</td>
<td>1</td>
<td>3.0</td>
<td>60.0</td>
<td>-</td>
<td>3.2</td>
<td>Clocking Reference Design for ADC32RF45 (RF Sampling ADC)</td>
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<tr>
<td>TIDA-01021</td>
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<td>–105.9</td>
<td>9.2</td>
<td>2[6]</td>
<td>2.7</td>
<td>55.7</td>
<td>68.8</td>
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<td>Clocking and Synchronization of Multiple JESD204B ADCs</td>
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<td>TIDA-01023</td>
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<td>–105.9</td>
<td>8.0</td>
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<td>3.0</td>
<td>55.5</td>
<td>68.8</td>
<td>8.0</td>
<td>9.8 GHz RF CW Signal Generator</td>
</tr>
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<td>3.0</td>
<td>56.0</td>
<td>59.1</td>
<td>8.0</td>
<td>Clocking and Synchronization of JESD204B ADCs</td>
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<td>4</td>
<td>3.0</td>
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<td>Quad Channel 3.2 GSPS Digitizer System (Integrating ADC, Clocking and Power)</td>
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<td>–105.9</td>
<td>10.0</td>
<td>2[4]</td>
<td>1.4</td>
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<tr>
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<td>Power design for optimal ENOB in high-speed DAQ</td>
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<td></td>
</tr>
</tbody>
</table>
5.3 **Other Related Documents**

1. Texas Instruments, *Interleaving ADCs for Higher Sample Rates Technical White Paper*
2. Texas Instruments, *Maximizing SFDR Performance in the GSPS ADC: Spur Sources and Methods of Mitigation Application Report*
3. Texas Instruments, *Defining Skew, Propagation-Delay, Phase Offset (Phase Error) Application Report*

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6 **About the Author**

**ANBU MANI** is a systems engineer in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Anbu has experience in analog circuit design and digital circuit design for the Automatic Test Equipment in Modular platform. He is also engaged with the design and development of embedded products. Anbu earned his bachelor of engineering (BE) in electronic and communication from the Anna University, Chennai.

**SANKAR SADASIVAM** is a system architect in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for designing and developing reference design solutions for the industrial systems with a focus on Test and Measurement. Sankar brings to this role his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics. Sankar earned his master of science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

7 **Acknowledgment**

The authors would like to thank their colleagues Bryan Bloodworth, Taras Dudar, Victor Salomon, Jason Clark and Matthew Guibord for their unconditional support and critical feedback during the development of this design and design guide review.
Appendix A

Example MATLAB program for analyzing skew:

```matlab
%-------------------------------------------------------%
% Import Data %
%-------------------------------------------------------%
function varargout = SkewCheck_v5(varargin)
    close all;

    global N;
global samples_all;
global ax;
global num_bits;
global Fs;
global Fin;
global Decimation;
global popupA;
global popupB;

    % Declare variables for imported data
data1 = xlsread('read_csv1.csv');
data2 = xlsread('read_csv2.csv');

    Fs = 2700e6;
    Fin = 997e6;
    Fno = 0;
    Decimation = 1;
    N = length(data1);
    num_bits = 15;

    % Removing DC in all the channels
    samples_board_1 = data1;
samples_board_1 = samples_board_1 - repmat(mean(samples_board_1),size(samples_board_1,1),1);
samples_board_2 = data2;
samples_board_2 = samples_board_2 - repmat(mean(samples_board_2),size(samples_board_2,1),1);
samples_all = [samples_board_1 samples_board_2];

    fig=figure('Units', 'normalized', 'Position',[0.1,0.1,0.5,0.8]);
    set(0, 'CurrentFigure', fig);

    for i = 1:size(samples_board_1,2)
        waveDataSrc{i} = sprintf('File1_Ch%1d',i);
    end
    for k = 1:size(samples_board_2,2)
        waveDataSrc{size(samples_board_1,2)+k} = sprintf('File2_Ch%1d',k);
    end

    popupA = uicontrol('Style', 'popup', 'Units', 'normalized',
                      'String', waveDataSrc,...
                      'Position', [0.76,0.935, 0.2, 0.05],...
                      'Tag', 'PUA1', 'Callback', @setmap);

    popupB = uicontrol('Style', 'popup', 'Units', 'normalized',...
                      'String', waveDataSrc,...
                      'Position', [0.76,0.905, 0.2, 0.05],...
                      'Tag', 'PUB1', 'Callback', @setmap);

    ax(1) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
             'CameraViewAngleMode', 'auto',
             'Units', 'normalized', 'Position', [0.06+0,0.06+0.48*1,0.9,0.38]);
```

```
ax(2) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
'CameraViewAngleMode', 'auto', ...
'Units', 'normalized', 'Position', [0.06+0.06+0.48*0,0.9,0.38]);

PlotData(1, 1)

CalcSkewData

end

function PlotData(PUPA, PUPB)
global samples_all;
global ax;
global N;
global num_bits;
global Fs;
global Fin;
global Decimation;

Fsd = Fs/Decimation;

global popupA;
global popupB;

popupAStr = get(popupA, 'String');
popupBStr = get(popupB, 'String');

samples_board_1 = samples_all(:,PUPA);
samples_board_2 = samples_all(:,PUPB);

subplot(ax(1));
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

%magitude correction
samples_board_1 = samples_board_1 * (mag_x/mag_y);

plot((0:length(samples_board_1)-1)*(1/Fsd),samples_board_1,...
{(0:length(samples_board_2)-1)*(1/Fsd)}-0/(2*Fsd)),samples_board_2);
str_trace1 = sprintf('%s',popupAStr{PUPA});
str_trace2 = sprintf('%s',popupBStr{PUPB});
leg = legend(str_trace1, str_trace2);
set(leg, 'Interpreter', 'none');
title('Time Domain Plot');

% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

subplot(ax(2));
plot((0:N/2)*(Fsd/N), 20*log10(abs(X*2/N/A)), (0:N/2)*(Fsd/N), 20*log10(abs(Y*2/N/A)));
title('FFT Plot of ADC 1');
fprintf('\nIndex_x:%d; Index_y:%d\n',index_x, index_y);

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_x));

% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff = mod(phase_diff, 2*pi);
%phase_diff_deg = mod(phase_diff / pi * 180, 360);
boardstring = '';
if phase_diff > pi
    boardstring = 'Brd1 Lags Brd2';
    phase_diff = 2*pi-phase_diff;
else
    boardstring = 'Brd2 Lags Brd1';
    phase_diff = phase_diff;
end

phase_diff_deg = phase_diff / pi * 180;

skew_ps = phase_diff_deg / (360*Fin) / 1e-12;

abc_title1 = sprintf('%s by %3.3f deg or %3.3f ps', boardstring, phase_diff_deg, skew_ps);
subplot(ax(1));
title(abc_title1);

abc_title2 = sprintf('Fin = %3.3f MHz', Fin*1e-6);
subplot(ax(2));
title(abc_title2);
end

function skewdata=CalcSkewData()
global samples_all;
global N;
global num_bits;
global Fs;
global Fin;
global Decimation;
Fsd = Fs/Decimation;

for row = 1:size(samples_all,2)
    for col = 1:size(samples_all,2)
        samples_board_1 = samples_all(:,row);
        samples_board_2 = samples_all(:,col);

        % Get FFT of for each board.
        window = blackman(N);
        X=fftshift(fft(window.*samples_board_2));
        Y=fftshift(fft(window.*samples_board_1));
        X = X(N/2:end);
        Y = Y(N/2:end);
        A = 2^\(num_bits-1);
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

% magnitude correction
samples_board_1 = samples_board_1 * (mag_x/mag_y);

% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_x));

% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff_deg = phase_diff / pi * 180;
skew_ps = phase_diff_deg / (360*Fin) / 1e-12;
abc_title = sprintf('%3.3f°/%3.3fps', phase_diff_deg, skew_ps);
skewdata{row,col}=abc_title;
end

function setmap(source,callbackdata)
global popupA;
global popupB;
PlotData(get(popupA, 'Value'), get(popupB, 'Value'));
end
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