Design Guide: TIDA-010054

Bidirectional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations

Description

This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC/DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability are critical factors, making this design an excellent choice for EV charging stations and energy storage applications. Modularity and symmetrical structure in the DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

Resources

TIDA-010054	Design Folder
UCC21710, UCC14141-Q1, AMC1311	Product Folder
AMC1306M05, AMC1336, AMC1302	Product Folder
TPS2640, TLVM13620, TMCS1133	Product Folder
TPS7A20, TLV760	Product Folder
TMS320F280039	Product Folder

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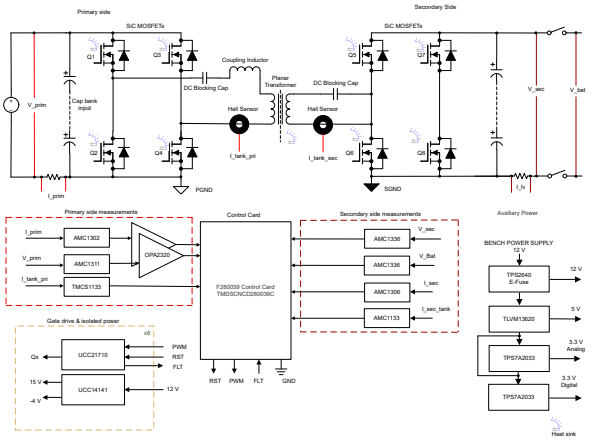
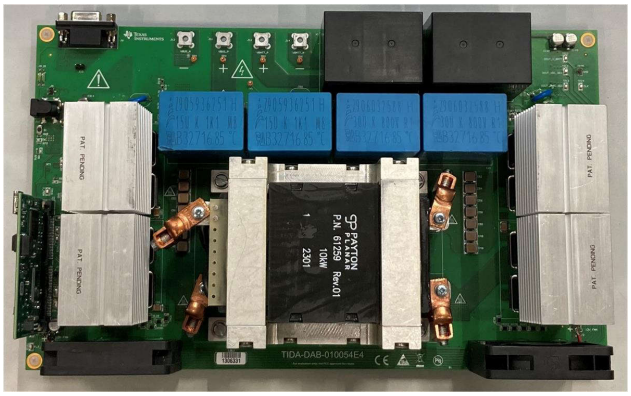
Features

- Bidirectional dual-active-bridge with Single- (SPS) and Extended-phase-shift (EPS) control
- Smart Gate driver UCC21710 providing integrated protection for SiC MOSFETs
- TMS320F280039 controller for implementation of digital control
- Isolated voltage and current sensing
- Maximum power output of 10 kW
- Achieves peak efficiency – 98.7%, full load efficiency – 98%
- Primary voltage of 700V–800V DC, secondary voltage of 350V – 500 V DC (SPS) 250V–500V (EPS)
- PWM switching frequency of 100 kHz and reduced transformer size enabled by planar magnetics
- Soft switching without auxiliary components

Applications

- DC fast charging station
- DC fast charging power module
- Power conversion system (PCS)
- Hybrid, electric and powertrain systems





1 System Description

The electric vehicle charging standards governed by the Combined Charging System and CHAdeMO® are constantly changing and are pushing for faster battery charging rates requiring typically less than 30 minutes spent at a charging station for one full charge of an electric vehicle. The DC charging station is typically a Level 3 charger which can cater to a very high power level between 120–240 kW. These DC charging stations are standalone units which house AC/DC and DC/DC power conversion stages. A number of power conversion modules are stacked together inside of a charging station to increase the power levels and enable fast charging. DC fast-charging stations provide a high power DC current to an electric vehicle's battery without passing through any onboard AC/DC converter, which means the current is connected directly to the battery. Most cars on the road today can handle only up to 50 kW. Newer cars have the ability to charge at greater rates of power. As EVs come with higher range and batteries get bigger, DC charging solutions are being developed to support long-range EV batteries through fast charging stations up to 250 kW or more.

The DC/DC converter in a charging station must be capable of interfacing with the rectified bus voltage (700–800 V) from a three-phase Vienna rectifier at the input and connect with the battery of an electric vehicle at the output, delivering rated power. The DC/DC converter finds important application in a number of end equipment. Figure 1-1 shows the use in charging stations, solar photovoltaic systems, energy storage systems, and electric vehicle traction applications.

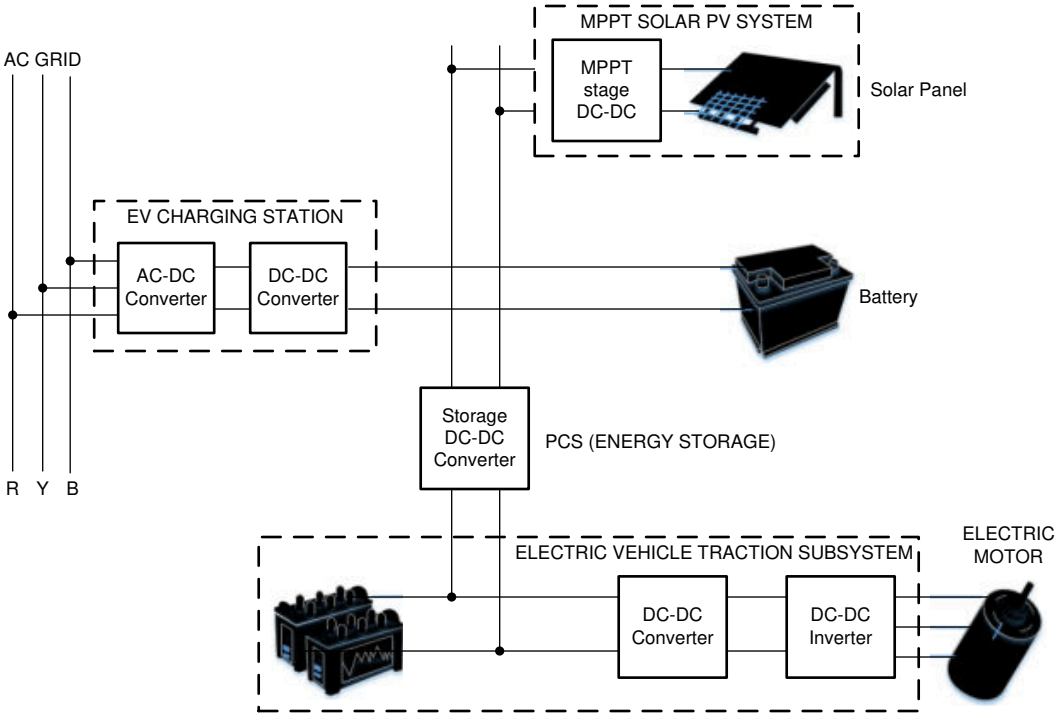


Figure 1-1. Role of DC/DC Converter

The DC/DC converter must be capable of handling high power levels. In addition to this, the converter must be modular, which enables single power stage converter units to be paralleled, whereby the output power throughput can be scaled to higher levels as required by DC charging station standards. Current trends in the charging station are moving toward converters that can handle bidirectional power flow. New practices, such as Vehicle-to-Grid (V2G), involve power transfer between the battery of an electric vehicle and the AC grid. Bidirectional DC/DC converters enable charging of the battery in the forward mode of operation and facilitate flow of power back to the grid from the battery during reverse mode of operation, which can be used to stabilize the grid during peak load periods.

Power density and system efficiency are two important requirements of a converter in a DC charging station. Operating at high switching frequencies enables reduced size of magnetics. By moving to higher bus voltage to facilitate fast charging, more power can be transferred at the same current level. This helps to reduce the amount of copper, thereby improving power density of the converter. The converter must also be highly efficient

as it results in significant cost savings and reduced thermal solution. This reduced thermal solution directly translates into reduced and compact heat sink size, which in turn increases the power density of the converter. The converter must also be capable of inherent soft switching like ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) without the addition any bulky passive components which might hamper power density.

The DC/DC converter must be capable of interfacing seamlessly with Lithium ion or a lead acid battery, which are predominantly used in EV charging stations. The DC/DC converter must also be capable of providing the required voltage conversion between the high-voltage and low-voltage side and provide galvanic isolation between them.

Traditional switching devices have a limit on how quickly the device can switch high voltages, or more appropriately, the dV/dt ability of the device. This slow ramping process increases switching loss because the device spends more time in switching transition. This increased switch time also increases the amount of dead time required in the control system to prevent shoot-through and shorts. The solution to this was developed in newer switching semiconductor technology such as SiC and GaN devices with high electron mobility. This reference design uses SiC MOSFETs alongside TI's SiC gate driver technology to demonstrate the potential benefits it translates when it comes to efficiency and power density.

The following four popular topologies were considered for analysis.

- LLC resonant converter
- Phase-shifted, full bridge
- Single-phase, dual-active bridge
- Dual-active bridge in CLLC mode

Based on this study, the dual-active bridge was chosen for implementation in this reference design, owing to the ease of bidirectional operation, modular structure, competitive efficiency, and power density numbers with respect to other competing topologies. This reference design focuses on addressing the challenges when designing a high-power, dual-active-bridge DC/DC converter for the EV charging station.

1.1 Key System Specifications

Table 1-1 lists some of the critical design specifications of the dual-active-bridge (DAB) DC/DC converter. The system has a full load efficiency of 97.6% at an output power of 10 kW.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	700–800-V DC	Section 3.1
Output voltage range	250–500-V DC	Section 3.1
Output power rating	10-kW maximum	Section 2.3.5
Output current	26-A maximum	Section 2.3.5
Efficiency	Peak 98.8% (at 4 kW) full load 98.0% (at 10 kW)	Section 4.5
PWM switching frequency	100 kHz	Section 2.3.4.6
Power density	> 2 kW/L	Section 4.5
Voltage ripple	< 5 %	Section 2.3.4.5

Table 1-1 shows that the input voltage range is between 700 V and 800 V. This range was considered because the DC/DC converter must interface with the front-end Vienna rectifier and the three-phase power factor correction (PFC), which has an output that is within this range. This converter can also be used in conjunction with single-phase PFC systems with an output that is in the range of 400 V, which must interface with 48- and 72-V batteries.

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board*. Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers it the responsibility of the user to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider the design as a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board***. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Overview

This section shows the block diagram of the dual-active-bridge DC/DC converter.

2.1 Block Diagram

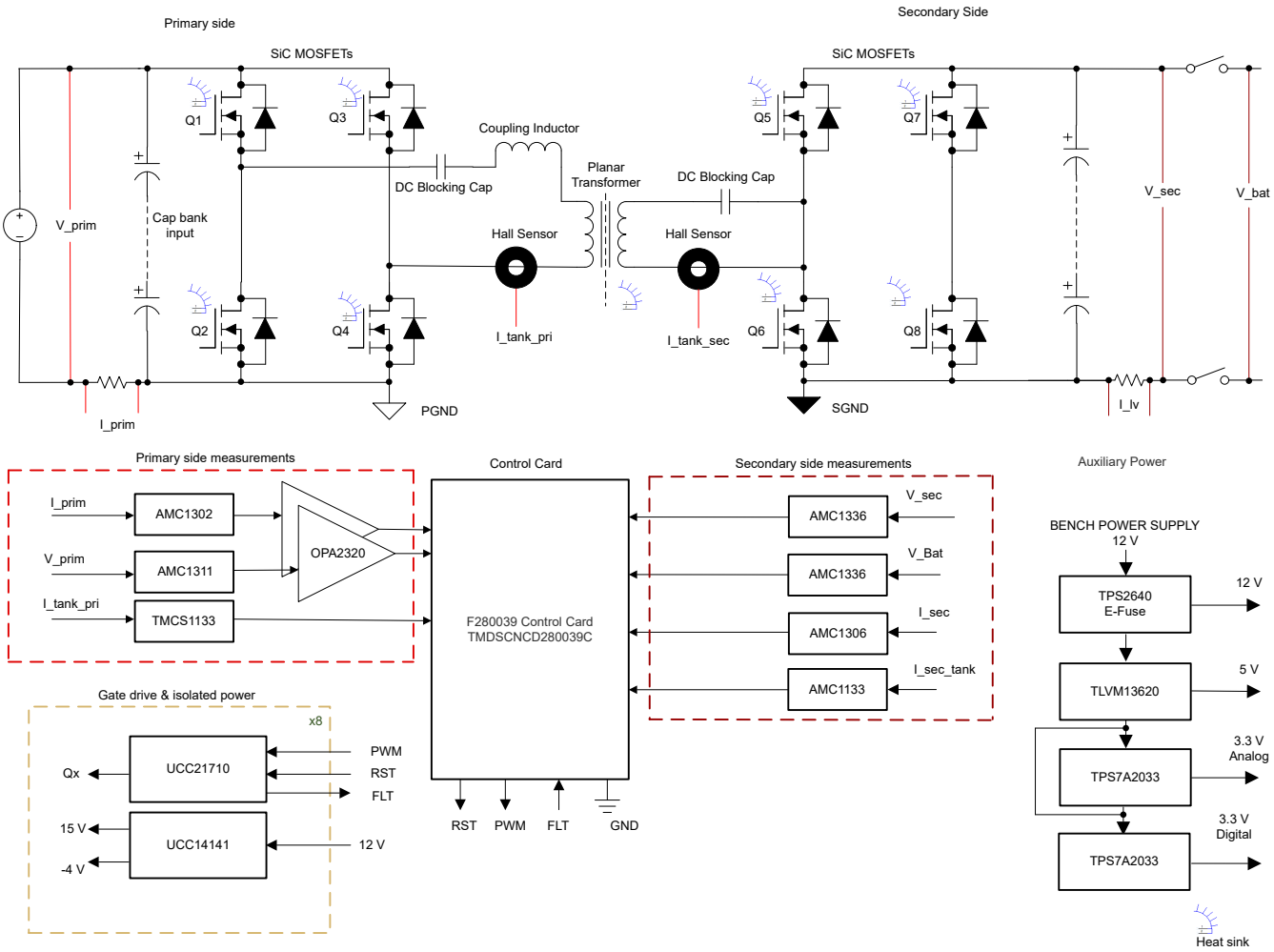


Figure 2-1. TIDA-010054 Block Diagram

This reference design consists of four main sections that intercommunicate:

- A power board comprising the power stage SiC MOSFETs, a high-frequency transformer, current sensing electronics, gate drivers, voltage and current sensing, and the system power tree
- A TMDSCNCD280039C control card to support digital control

2.2 Highlighted Products

This section highlights the critical components of the design which include the gate driver, F280049 controller, isolated amplifiers for current and voltage sensing, and generating voltage references.

2.2.1 UCC21710

The UCC21710 is a galvanically isolated single-channel gate driver designed to drive up to 1700-V SiC MOSFETs and IGBTs. The device features advanced integrated protection, best-in-class dynamic performance, and robustness. UCC21710 has up to ±10-A peak source and sink current. The input side is isolated from the output side with SiO2 capacitive isolation technology, supporting up to 1.5-kV_{RMS} working voltage with longer than 40 years isolation barrier life, 12.8-kV_{PK} surge immunity, as well as providing low part-to-part skew , and >150 V/ns common mode noise immunity (CMTI). The UCC21710 includes the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt current sensing support, fault reporting, active Miller clamp, and input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The isolated analog to PWM sensor can be utilized for easier temperature or voltage sensing, further increasing the versatility of the drivers and simplifying the system design effort, size and cost.

2.2.2 UCC14141-Q1

UCC14141-Q1 is an automotive qualified high-isolation voltage DC/DC power module designed to provide power to IGBT or SiC gate drivers. The UCC14141-Q1 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high density with very low emissions. The high-accuracy output voltages provide better channel enhancement for higher system efficiency without over-stressing the power device gate. The input voltage of UCC14141-Q1 supports both wide LiFePO4 battery voltage of electric vehicle (8 V–18 V) and regulated 12-V rail (10.8 V–13.2 V), with different output power. The fully-integrated module with on-chip device protection requires a minimum of external components, and provides extra features such as input undervoltage lockout, overvoltage lockout, output voltage power-good comparators, overtemperature shutdown, soft-start time-out, adjustable isolated positive and negative output voltage, an enable pin, and an open-drain output power-good pin.

2.2.3 AMC1311

The AMC1311 is used for DC voltage sensing at the input and output terminals. The device is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7-kV peak according to VDE V 0884-1 and UL1577. The high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems.

For more details on this device, see the AMC1311 product page.

2.2.4 AMC1302

The AMC1302 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577, and supports a working voltage of up to 1.5 kV_{RMS}. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC1302 is optimized for direct connection to a low-impedance shunt resistor or other low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current control in PFC stages, DC/DC converters, AC-motor and servo drives over the extended industrial temperature range from –40°C to +125°C. The integrated missing-shunt and missing high-side supply detection features simplify system-level design and diagnostics.

2.2.5 OPA320

The OPA320 (single) and OPA2320 (dual) are a new generation of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45 mA. The OPA320 series is an excellent choice for low-power, single-supply applications. Low-noise (7 nV/√Hz) and high-speed operation also make them well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification. The OPA320 features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of typically 114 dB over the full input range.

For more details on this device, see the OPA320 product page.

2.2.6 AMC1306M05

The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common mode voltage levels and protects lower-voltage parts from damage. The input of the AMC1306 is optimized for direct connection to shunt resistors or other low voltage level signal sources. The unique low input voltage range of the ±50-mV device allows significant reduction of the power dissipation through the shunt and supports excellent ac and dc performance. The output bitstream of the AMC1306 is Manchester coded (AMC1306Ex) or uncoded (AMC1306Mx), depending on the derivate. By using an integrated digital filter (such as those in the TMS320F2807x or TMS320F2837x microcontroller families) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS. The bitstream output of the Manchester coded AMC1306Ex versions support single-wire data and clock transfer without having to consider the setup and hold time requirements of the receiving device.

2.2.7 AMC1336

The AMC1336 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 8000 V_{PEAK} according to the DIN VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common mode voltage levels and protects lower-voltage parts from damage. The unique wide, bipolar. ±1-V input voltage range of the AMC1336 and the high input resistance support direct connection of the device to resistive dividers in high-voltage applications. When used with a digital filter to decimate the output bitstream, the device can achieve 16 bits of resolution with a dynamic range of 87 dB at a data rate of 82 kSPS. On the high side, the AMC1336 is supplied by a 3.3-V or 5-V power supply. The isolated digital interface operates from a 3.0-V, 3.3-V, or 5-V power supply. The AMC1336 performance is specified over the extended industrial temperature range of –40°C to +125°C.

2.2.8 TMCS1133

The TMCS1133 is a galvanically isolated Hall-effect current sensor with industry-leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 2.5% maximum total error over temperature and lifetime with no system level calibration, or less than 1.5% maximum total error with a one-time room temperature calibration (including both lifetime and temperature drift). AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated on-chip Hall-effect sensors. Coreless construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±96 A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding 5000 V_{RMS}, coupled with minimum 8.1-mm creepage and clearance provide up to 1100 V_{DC} reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the TMCS1133 to operate from a single 3-V to 5.5-V power supply, eliminates ratiometry errors, and improves supply noise rejection.

2.2.9 TMS320F280039C

The TMS320F28003x (F28003x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Motor drives
- Appliances
- Hybrid, electric and powertrain systems
- Solar and EV charging
- Digital power
- Body electronics and lighting
- Test and measurement

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Floating-Point Unit (FPU), Trigonometric Math Unit (TMU), and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has a dedicated memory resource and can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28003x supports up to 384KB (192KW) of flash memory divided into three 128KB (64KW) banks, which enable programming and execution in parallel. Up to 69KB (34.5KW) of on-chip SRAM is also available to supplement the flash memory.

The Live Firmware Update hardware enhancements on F28003x allow fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

High-performance analog blocks are integrated on the F28003x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide excellent real-time signal chain performance. Sixteen PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to power factor correction and advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, CAN and CAN FD) and offers multiple pin-MUXing options for the best signal placement. The Fast Serial Interface (FSI) enables up to 200Mbps of robust communications across an isolation boundary.

New to the C2000 platform is the Host Interface Controller (HIC), a high-throughput interface that allows an external host to access the resources of the TMS320F28003x directly.

Want to learn more about features that make C2000 Real-Time MCUs the right choice for your real-time control system? See *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* application note and visit the *C2000™ real-time MCUs* page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs)* getting started guide covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

To get started, see the TMDSCNCD280039C evaluation board and download C2000Ware.

2.2.10 TLVM13620

The TLVM13620 synchronous buck power module is a highly integrated 36-V, 2-A DC/DC design that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing. With an output voltage range from 1 V to 6 V, the TLVM13620 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total design requires as few as four external components and eliminates the magnetics and compensation part selection from the design process. Although designed for small size and simplicity in space-constrained applications, the TLVM13620 module offers many features for robust performance: precision enable with hysteresis for adjustable input voltage UVLO, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, negative output voltage capability for inverting applications, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

2.2.11 ISOW1044

The ISOW1044 device is a galvanically-isolated controller area network (CAN) transceiver with a built-in isolated DC-DC converter that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20-mA output current can be used to power other circuits on the board. An integrated 10Mbps GPIO channel is available and can help remove an additional digital isolator or optocoupler for diagnostics, LED indication, or supply monitoring.

2.2.12 TPS2640

The TPS26400 devices are compact, feature rich high-voltage eFuses with a full suite of protection features. The wide supply input range of 4.2 V to 42 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±42 V. Integrated back-to-back FETs provide a reverse current blocking feature making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source, and device protection are provided with many adjustable features including overcurrent, output slew rate and overvoltage, undervoltage thresholds. The internal robust protection control blocks along with the high-voltage rating of the TPS26400 helps to simplify the system designs for Surge protection. A shutdown pin provides external control for enabling and disabling the internal FETs as well as placing the device in a low-current shutdown mode. For system status monitoring and downstream load control, the device provides fault and precise current monitor output. The MODE pin allows flexibility to configure the device between the three current-limiting fault responses (circuit breaker, latch off, and Auto-retry modes).

2.3 System Design Theory

The following sections give an extensive overview of the operating principles of the dual-active bridge.

2.3.1 Dual Active Bridge Analogy With Power Systems

Power transfer between the two bridges in a dual active bridge is analogous to the power flow between two voltage buses in a power system. Consider two voltage sources connected by a line reactance as shown in Figure 2-2.

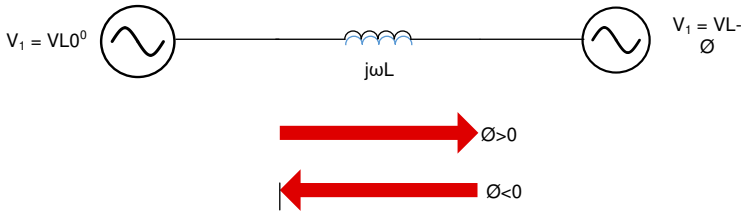


Figure 2-2. Power Transfer Between Voltage Bus

Figure 2-2 shows that the voltage source on the right is lagging with respect to the voltage source on the left. Hence, the power transfer takes place from the left towards the right as per Equation 1.

$$P = \frac{V_1 V_2 \sin(\varphi)}{\omega L} \quad (1)$$

Similarly, power transfer happens in a dual-active bridge where two high-frequency square waves are created in the primary and secondary side of the transformer by the switching action of MOSFETs. These high-frequency square waves are phase shifted with respect to each other. Power transfer takes place from the leading bridge to the lagging bridge, and this power flow direction can be easily changed by reversing the phase shift between the two bridges. Hence, it is possible to obtain bidirectional power transfer with ease in a dual-active bridge as shown in Figure 2-3.

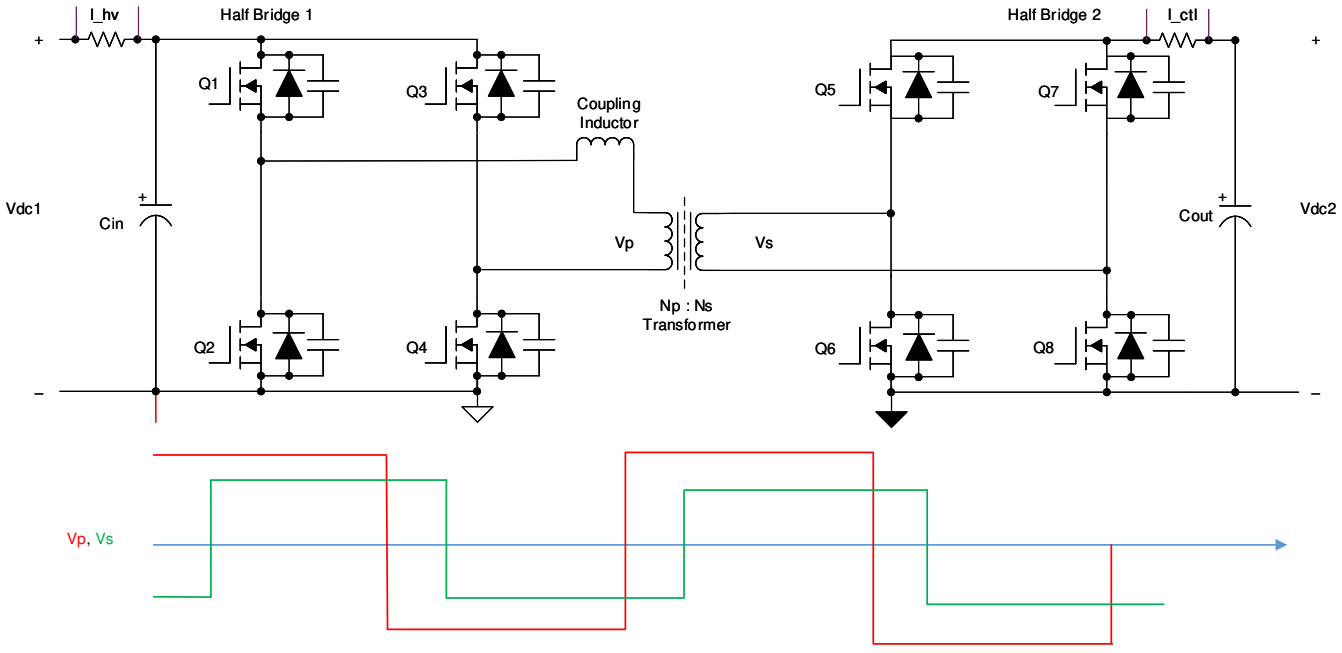


Figure 2-3. Dual-Active Bridge

2.3.2 Dual-Active Bridge – Switching Sequence

In a single-phase, dual-active bridge, primary and secondary bridges are controlled simultaneously. All switches operate at 50% duty ratio. The diagonal switches turn on and turn off together so that the output of each bridge is a square wave. The switching sequence of the converter is elaborated in detail in this section. For simplification the transformer is assumed with a windings ratio n = 1:1 and can be removed, for the description of the switching sequence.

The switching sequence is divided into four intervals based on the inductor current waveform and phase shift between the voltages at the primary and secondary of the transformer. The voltage and the current waveforms are depicted in Figure 2-10. During interval one, the inductor current waveform is both positive and negative, and hence, the current commutation follows the scheme shown in Figure 2-4 and Figure 2-5. During this interval, switches Q1 and Q4 in the primary and switches Q6 and Q7 in the secondary conduct current.

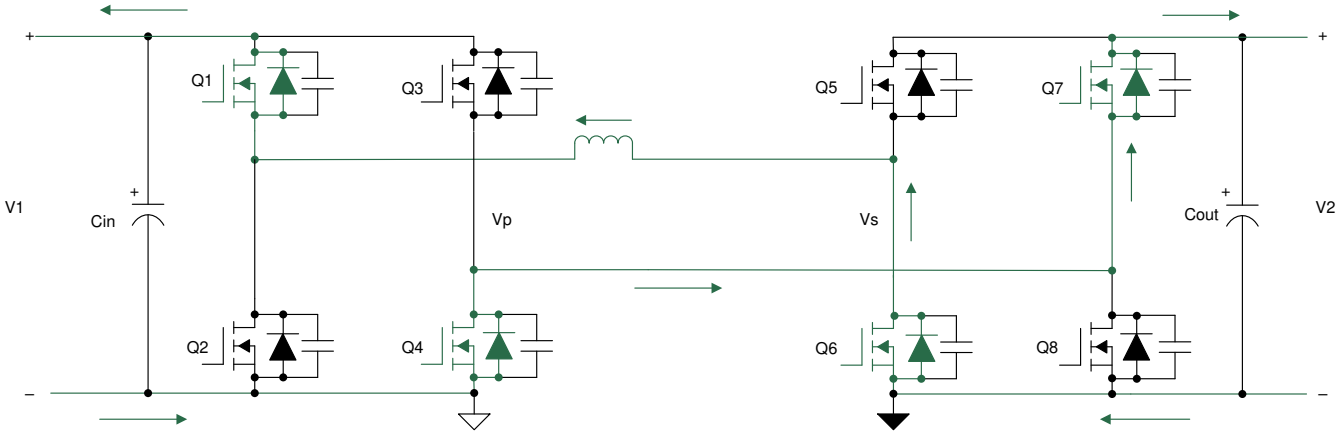


Figure 2-4. Interval 1: Negative Inductor Current

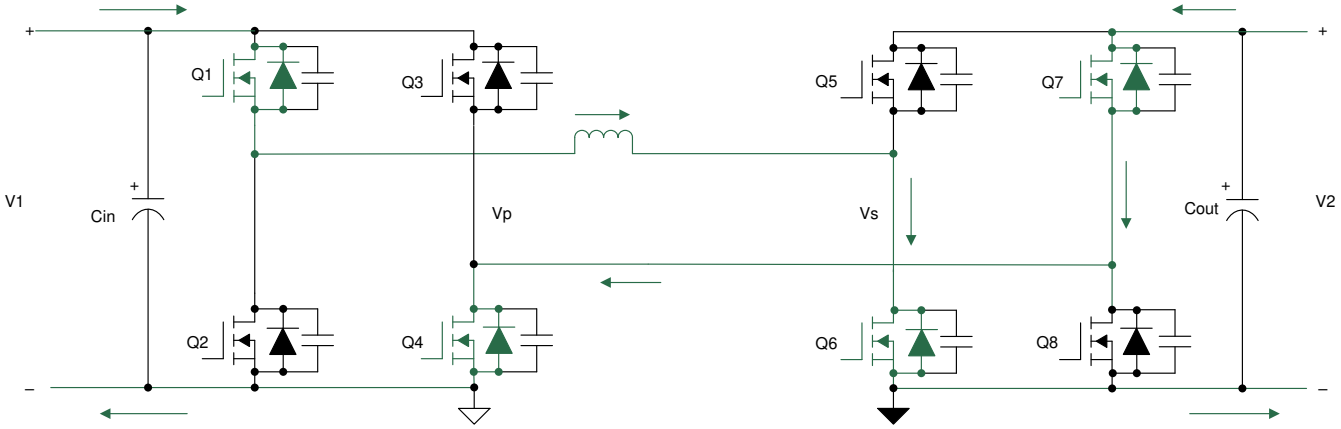


Figure 2-5. Interval 1: Positive Inductor Current

During this interval, the voltage across the primary, Vp, is equal to V1, and the voltage across the secondary, Vs, is equal to V2. The difference between these voltages appears across the leakage inductor, and the slope of the current during this interval can be approximated by Equation 2.

$$\frac{di}{dt} = \frac{V1 + V2}{L} \tag{2}$$

During interval two, the inductor current is positive. The voltage across the transformer primary is positive and is equal to V1, and the voltage across the secondary winding is positive and is equal to V2. Hence, the difference of these two voltages appears across the leakage inductor, and the slope of the rising current during this interval can be calculated by Equation 3.

$$\frac{di}{dt} = \frac{V1 - V2}{L} \quad (3)$$

During this interval, switches Q1 and Q4 remain turned on, but as the voltage across the secondary is now V2 with the inductor current positive, switches Q5 and Q8 turn on to conduct current. There is a small dead time period between the turn off of Q6 and Q7 and the turn on of Q5 and Q8. During this dead time, the phenomenon of zero voltage switching (ZVS) occurs, which is explained in detail in the following section. The commutation sequence for the second interval is shown in Figure 2-6.

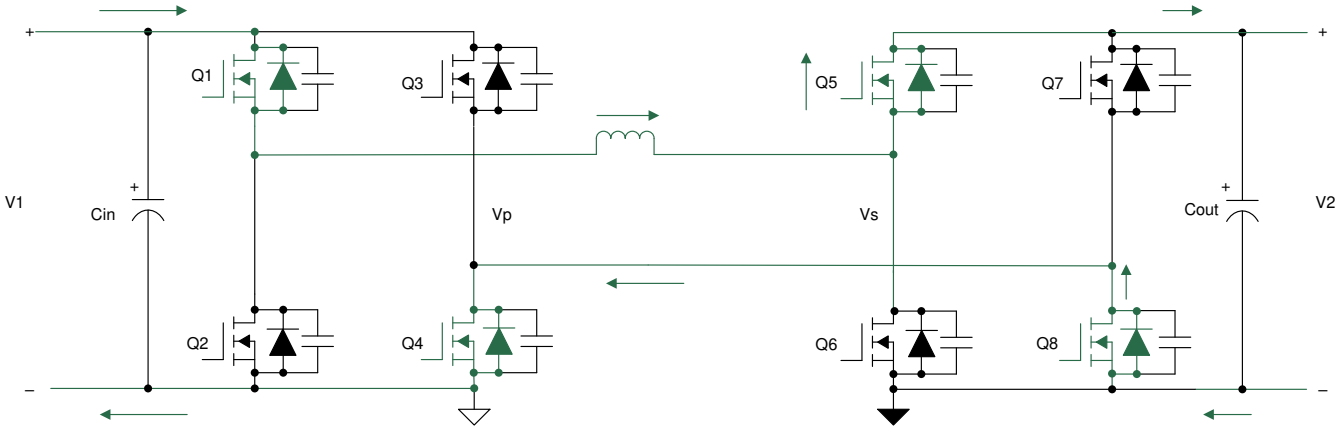


Figure 2-6. Interval 2

During interval three, the inductor current starts ramping down from the positive peak to a negative value as shown in Figure 2-10. In this interval, the voltage across the primary is –V1, and the voltage across the secondary is V2. The difference of these voltages, which is (-V1-V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 4.

$$\frac{di}{dt} = -\frac{V1 + V2}{L} \quad (4)$$

During this interval, switches Q5 and Q8 continue to remain turned on, but as the voltage across the primary is now –V1, switches Q2 and Q3 turn on to conduct current. The conduction for both directions of inductor current IL > 0 and IL < 0 is shown in Figure 2-7 and Figure 2-8, respectively.

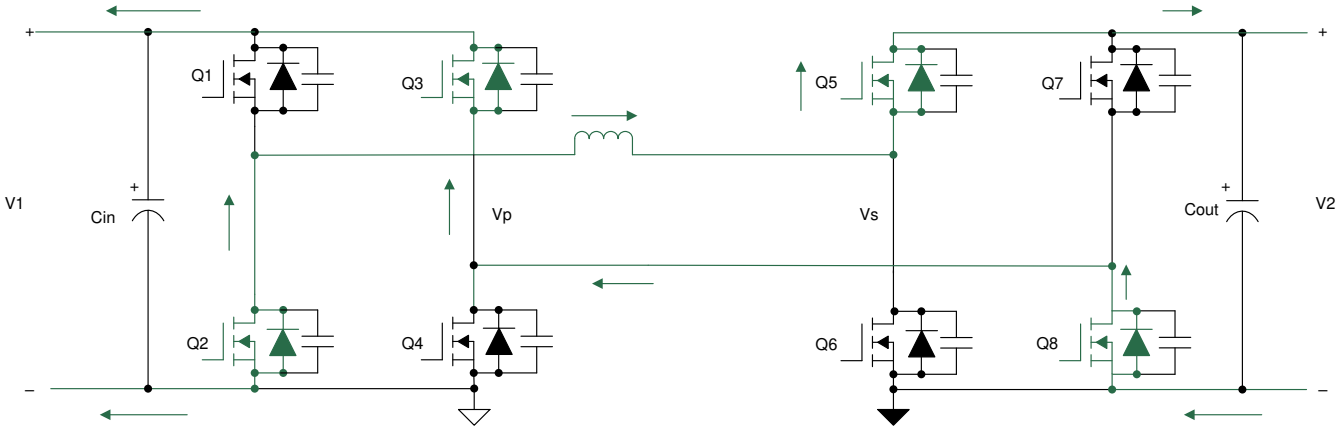


Figure 2-7. Interval 3: Positive Inductor Current

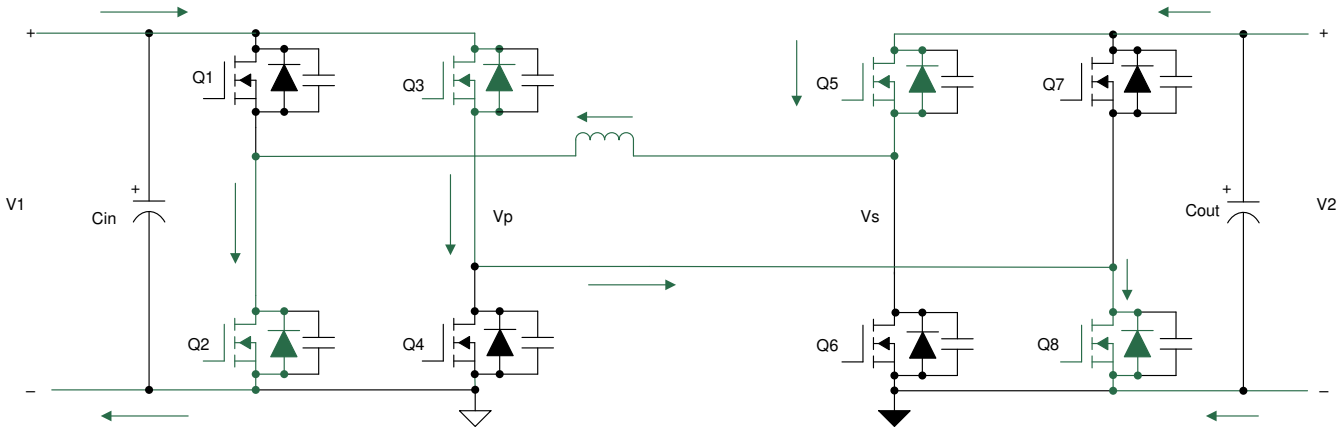


Figure 2-8. Interval 3: Negative Inductor Current

During interval four, the inductor current continues to be negative. During this interval, the voltage across the primary is –V1 and, and the voltage across the secondary is -V2. The difference in these voltages, which is (-V1+V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 5.

$$\frac{di}{dt} = -\frac{V1 - V2}{L} \tag{5}$$

During this interval, switches Q2 and Q3 continue to remain turned on, but as the voltage across the secondary are now –V2, switches Q6 and Q7 turn on to conduct current as shown in Figure 2-9.

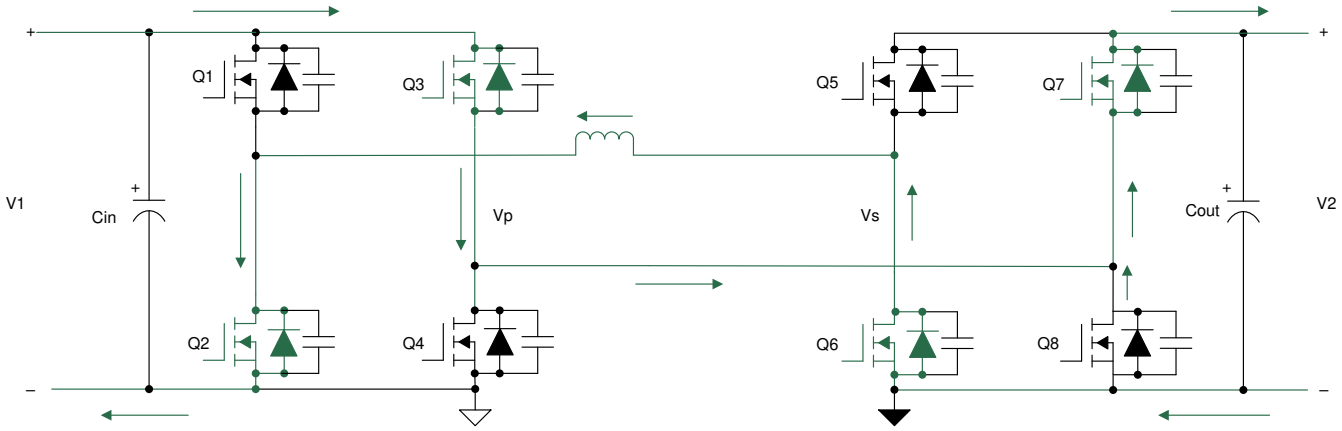


Figure 2-9. Interval 4

Figure 2-10 shows the gating pulses of the switches on the primary and secondary side. The variable Ø represents the phase shift between the PWM pulses of the primary and secondary side. Vp and Vs represent the voltage on the primary and secondary winding of the transformer. IL represents the transformer current.

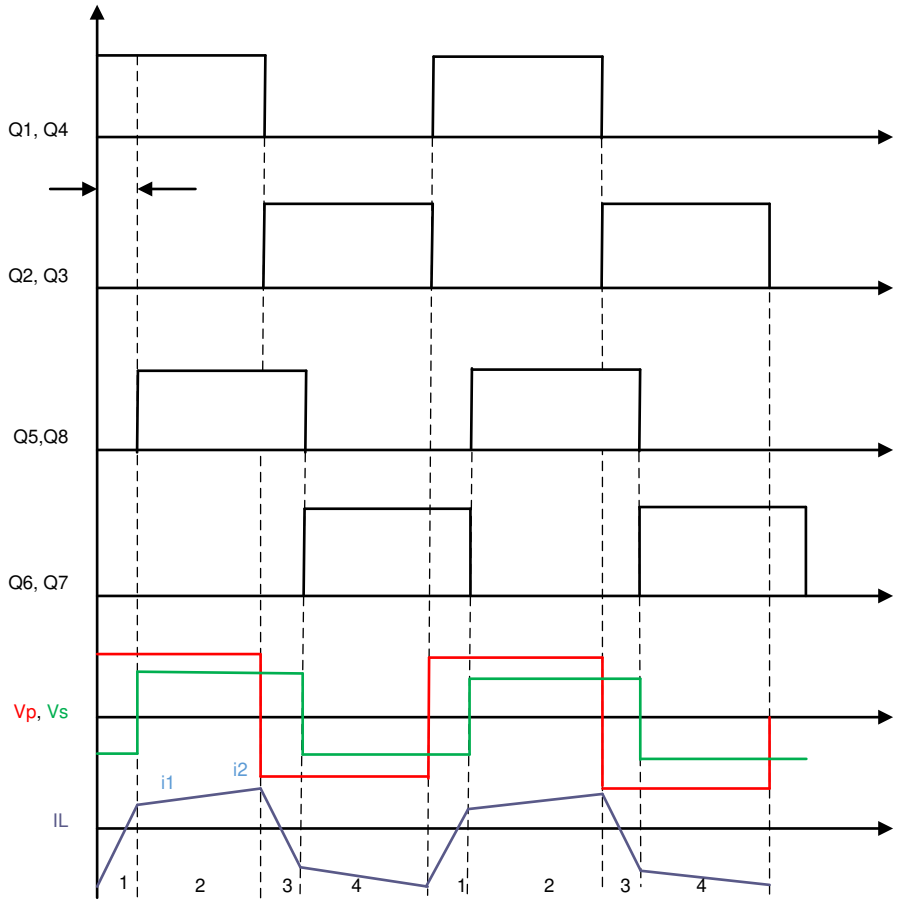


Figure 2-10. Gate Signals, Transformer Primary and Secondary Voltages, and Inductor Current

2.3.3 Dual-Active Bridge – Zero Voltage Switching (ZVS)

Between turn-off of one MOSFET and turn-on of the other MOSFET of a branch there is dead time. During this dead time the energy stored in the inductor discharges the output capacitances of the MOSFETs and holds them close to zero voltage before they are turned on. This phenomenon, where the voltage across the MOSFET is close to zero at turn on, is referred to as zero voltage switching (ZVS). This is a major advantage with this topology, where due to the natural lagging current in one of the bridges, the inductive stored energy causes ZVS of all of the lagging bridge switches and some of the switches of the leading bridge. This depends on the stored inductive energy ($E_L = 0.5LI^2$) available to charge and discharge the output capacitances of MOSFETs ($E_C = 0.5CV^2$), which again depends on the load of the converter and the input to output voltage ratio. A more detailed look on the boundaries of ZVS is documented in Section 2.3.4.2. Here the principal of ZVS is explained with the transition from interval one to interval two. Similar analysis can be done for all turn-on events.

When transition happens from interval one to two, the primary side switches Q_1 and Q_5 continue conduction, whereas in the secondary, Q_6 and Q_7 turn off and Q_5 and Q_8 turn on. Initially the voltage across Q_6 and Q_7 is zero when conducting, and Q_5 and Q_8 block the entire secondary voltage. During dead time, when all of the switches in the secondary are off, the inductor-stored energy circulates current which discharges the capacitor across MOSFETs Q_5 and Q_8 to zero and charges the capacitor across MOSFETs Q_6 and Q_7 to the full secondary voltage. The current commutation is shown in Figure 2-11.

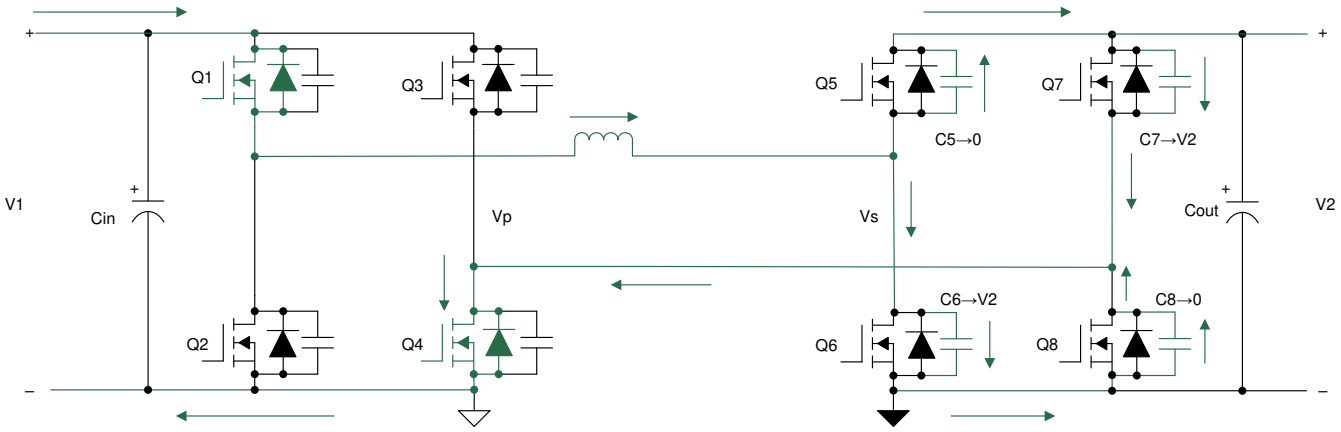


Figure 2-11. ZVS Transition in Secondary Side - Capacitor

Once the capacitors have been charged and discharged, the current must continue to flow. The current flows through the diodes D_5 and D_8, thereby clamping the voltage across MOSFETs Q_5 and Q_8 to zero as shown in Figure 2-12. During the next interval, MOSFETs Q_5 and Q_8 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.

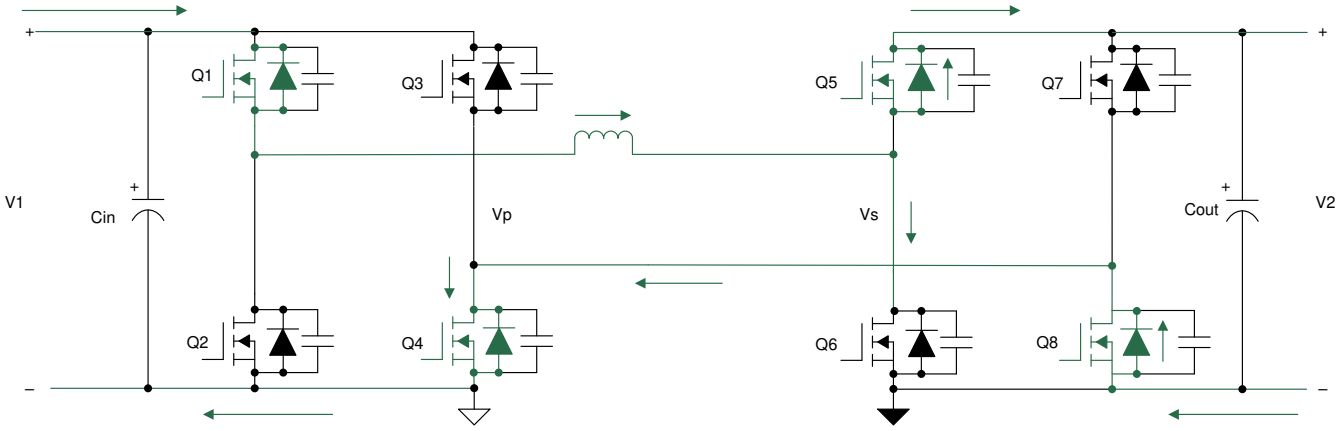


Figure 2-12. ZVS Transition in Secondary Side - Diode

Similarly, zero voltage switching across the switches of the primary during the transition from interval 2 to 3 is explained in the following section. When transition happens from interval two to three, the secondary side switches Q_5 and Q_8 continue conduction, whereas in the primary, Q_1 and Q_4 turn off and Q_2 and Q_3 turn on. Initially, the voltage across Q_1 and Q_4 is zero when conducting, and Q_2 and Q_3 block the entire secondary voltage. During dead time when all of the switches in the primary are off, the inductor stored energy circulates current, which discharges the capacitor across MOSFETs Q_2 and Q_3 to zero and charges the capacitor across MOSFETs Q_1 and Q_4 to the full primary voltage. The current commutation is shown in Figure 2-13.

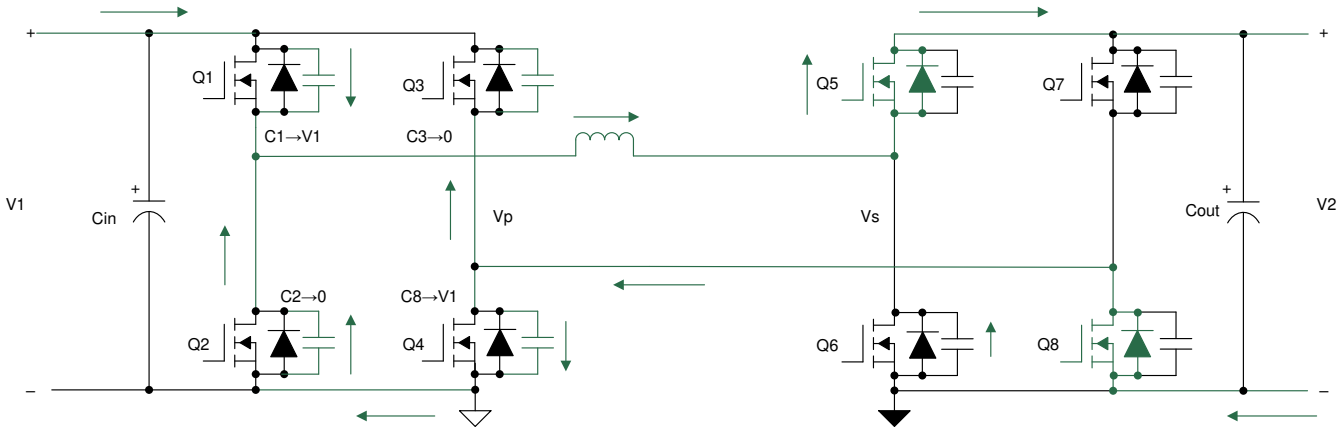


Figure 2-13. ZVS Transition in Primary Side - Capacitor

Once the capacitors have been charged and discharged, the current must continue to flow. The current flows through diodes D_2 and D_3, thereby clamping the voltage across MOSFETs Q_2 and Q_3 to zero as shown in Figure 2-14. During the next interval, MOSFETs Q_2 and Q_3 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.

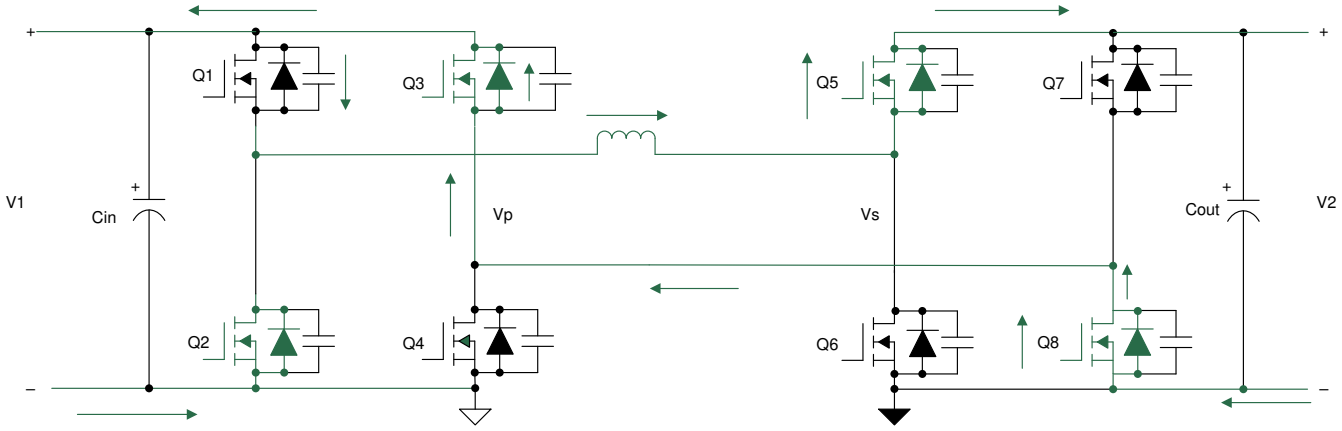


Figure 2-14. ZVS Transition in Primary Side - Diode

2.3.4 Dual-Active Bridge - Design Considerations

A number of factors are critical in the design of the power stage of a dual-active bridge. The most important factors are the selection of leakage inductor, desired phase shift of operation, output capacitor rating, switching frequency of operation, selection of SiC MOSFETs, transformer, and intended ZVS range of operation. Many of these design parameters are interrelated, and selection of any one of them has a direct impact on the others. For example, the selection of leakage inductor has a direct effect on the maximum power transferred, which in turn affects the phase shift of operation of the converter at the intended power level. Each of these factors are discussed in detail in the following sections.

2.3.4.1 Leakage Inductor

The primary specifications for designing a power converter system are input voltage V_1, output voltage V_2, and the maximum required power transfer. The power transfer relation of the dual-active bridge is given by Equation 6. The best value for N is $V_{1,nom}/V_{2,nom}$, which is 1.6 for this designs specifications.

$$P = \frac{NV_1V_2\varphi(\pi - |\varphi|)}{2\pi^2 F_s L} \tag{6}$$

where

- V_1 is the primary-side voltage

- V_2 is the secondary-side voltage
- N is the primary to secondary turns ratio
- φ is the phase shift in radians
- F_s is the switching frequency
- L is the leakage or coupling inductance

Equation 6 shows that the power transfer can be controlled with the phase shift φ, where the maximum power transfer occurs for φ = π / 2.

With V_1 and V_2 fixed, there are two variables left to design for the required output power. These are the switching frequency F_s and the leakage inductance L. With $F_S$set to 100 kHz, L is selected as 35 µH. This allows a theoretical maximum power transfer of 22.85 kW. This leaves some headroom above the target power of 10 kW, which is required for lower output voltages.

The selection of the inductor defines the maximum current stress in the switch node of the converter.

Figure 2-15 shows the inductor current waveform. The currents at points i_1 and i_2 can be derived from this waveform.

$$i_1 = 0.5 \times (2 \times \varphi - (1 - d) \times \pi) \times I_{base} \quad (7)$$

$$i_2 = 0.5 \times (2 \times d \times \varphi + (1 - d) \times \pi) \times I_{base} \quad (8)$$

where

- d is the voltage transfer ratio of the converter given in Equation 9
- I_{base} is the nominal base current of the converter given in Equation 10

$$d = N \times \frac{V_2}{V1} \quad (9)$$

$$I_{base} = \frac{V_1}{\omega L} \quad (10)$$

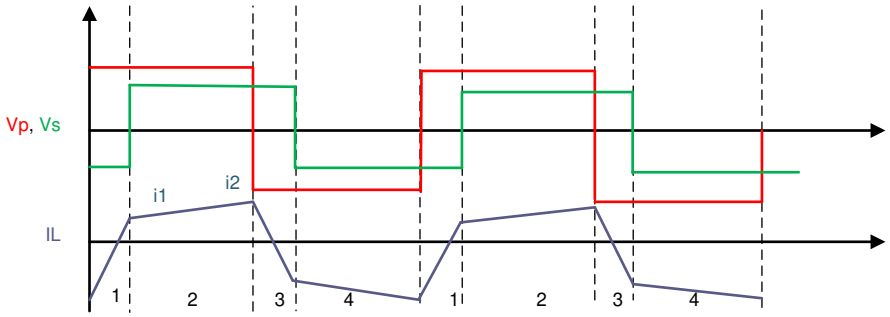


Figure 2-15. Inductor Current Waveform

2.3.4.2 Soft Switching Range

As explained in Section 2.3.2 the zero voltage switching is dependent on the inductor current I_L. To enable a ZVS transition between interval one and interval two, I_L needs to be positive when Q_5 and Q_8 is turned on. The current at this point is defined as i_1 (see Equation 9). For ZVS transition between interval two and three, I_L needs to be positive as well. This current point is defined as i_2 (see Equation 10). For ZVS transition between interval three and interval four and interval four and interval one, I_L needs to be negative. Since the current waveform is symmetric, the currents at these points are equal to $-i_1$ and $-i_2$.

Neglecting output capacitance of the MOSFETs, the ZVS range can derived by setting equations Equation 9 and Equation 10 to zero and solving for φ. This gives the minimum required phase shift for ZVS depending on input and output voltage ratio d. This leads to Equation 11 and Equation 12.

$$\varphi_{ZVS,\,pri} > \frac{\left(1 - \frac{1}{d}\right) \times \pi}{2} \quad (11)$$

$$\varphi_{ZVS,\,sec} > \frac{(1-d)\times\pi}{2} \quad (12)$$

Since the phase shift is proportional to the output power, the ZVS range can be plotted on a output power over voltage ratio graph as shown in Figure 2-16. The power is normed to P_{base}.

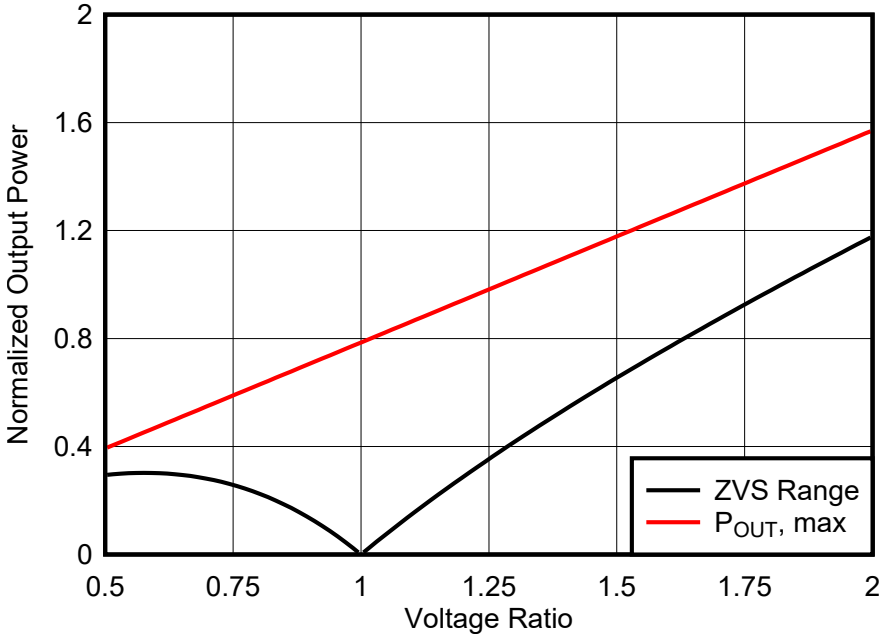


Figure 2-16. ZVS Range and Maximum Output Power Over Voltage Ratio

$$P_{base} = \frac{V_1^2}{\omega L} \quad (13)$$

The red line in Figure 2-16 shows the maximum possible output power $P_{out,max}$ for a certain voltage ratio. For light loads (output power below ZVS boundary plotted in black) and a voltage ratio d < 1, the secondary side experiences hard switching, while for d > 1 and low load the primary side experiences hard switching. For voltage ratios d close to one ZVS can be achieved down to very low loads. The ZVS range can be increased by applying different control schemes like extended-, dual- or triple-phase shift control.

Extended-phase shift control is implemented and available in software. For detailed information see Section 6.

2.3.4.3 Effect of Inductance on Current

The selection of leakage inductance also determines the currents in the converter. Equation 14 and Equation 15 show the RMS currents across the primary winding and secondary winding of the transformer. It is important not only to calculate currents in the nominal operating point where d = 1, since for other voltage ratios RMS currents can increase for the same power transferred as shown in Figure 2-17. The RMS current is normalized to I_{base} (see Equation 10).

$$I_{P\_RMS} = \sqrt{\frac{1}{3}\times\left(i_1^2 + i_2^2 + \left(1-\frac{2\varphi}{\pi}\right)\times i_2 \times i_1\right)} \quad (14)$$

$$I_{S\_RMS} = N \times I_{P\_RMS} \quad (15)$$

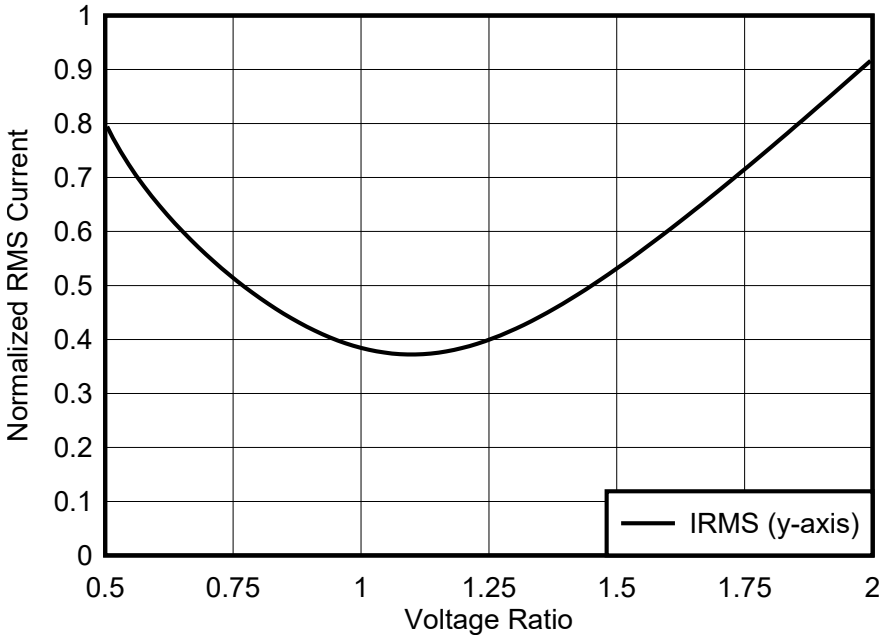


Figure 2-17. RMS Currents in Leakage Inductor for Equal Output Power Over Different Voltage Ratio

2.3.4.4 Phase Shift

The phase shift of the converter is dependent on the value leakage inductor. The phase shift for required power transfer is given by Equation 16.

$$\varphi = \frac{\pi}{2} \times \left(1 - \sqrt{1 - \frac{8 \times F_S \times L \times P_{out}}{N \times V_1 \times V_2}}\right) \quad (16)$$

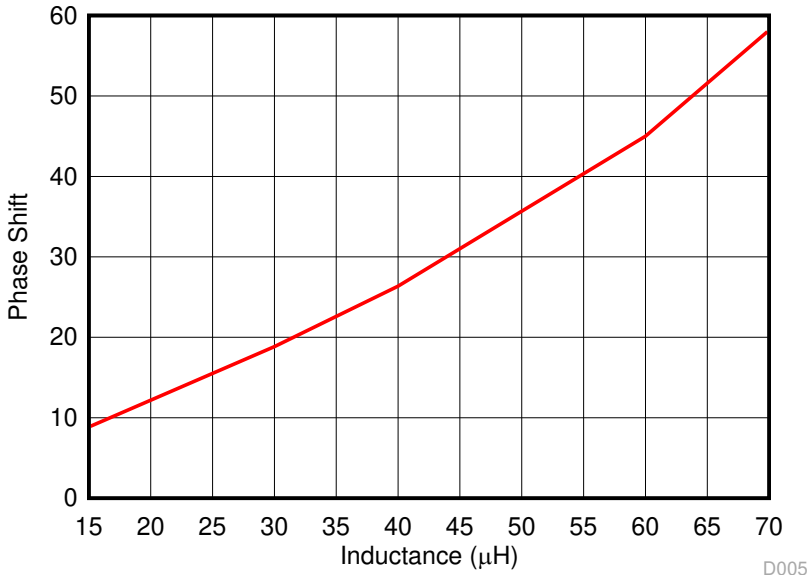


Figure 2-18. Variation of Phase Shift With Leakage Inductance

Figure 2-18 shows the required phase shift in degrees over leakage inductance for V_1 = 800 V, V_2 = 500 V, N = 1.6, F_S= 100 kHz, and P_{out}= 10 kW. The graph illustrates that for a small value of inductance, a maximum power transfer at a small value of phase shift is obtained. To have fine control over power transferred, fine high-resolution steps in which the phase can be varied must be obtained. Alternatively, a larger inductor can obtain maximum power transfer at a high value of phase shift for better control. For the selected L = 35 µH, a phase shift of 23 degrees or 0.4 radians is required.

2.3.4.5 Capacitor Selection

The output capacitor in the dual-active bridge must be designed to handle the ripple. Figure 2-19 illustrates that the capacitor current is the difference between the current I_{HB2} and the output current I_{Load}, also called I_{out} as shown in Equation 17. The waveforms are also shown in Figure 2-20. I_{HB2} is the rectified and scaled inductor current. The best output current I_{out} is obtained by P_{out} / V_2. From the difference between I_{out} and I_{HB2} the charge ΔQ (marked in blue) can be obtained. Afterwards, the required capacitance can be calculated using Equation 18 for a maximum allowed ripple voltage.

$$I_{cap} = I_{HB2} - I_{out} \tag{17}$$

$$C_{out} = \frac{\Delta Q}{V_{ripple}} \tag{18}$$

Since the current waveforms depend on input-to-output voltage ratio and phase shift, this analysis needs to be done for all corner cases.

A MATLAB® script is used to obtain ΔQ for different input-to-output voltage ratios. The script first interpolates the ideal capacitor current waveform shown in Figure 2-20 and subtracts I_{out}. The resulting waveform is the capacitor current $I_{C,out}$. Next, the integral of $I_{C,out}$ is calculated. Subtracting min($\int I_{C,out}$) of max($\int I_{C,out}$) provides ΔQ. This results in ΔQ of 12 µC for 10-kW output power and nominal input and output voltages. For lower output voltages, ΔQ increases to 50 µC. Using Equation 18 and a voltage ripple of 5 V leads to a required output capacitance of 10 µF. These are the best values assuming no parasitics in the capacitors. In the current design Aluminum Electrolytic Capacitors with relatively high ESR are used. Therefore 470 µF of output capacitance is necessary to reduce the ripple to 5%. In the next design revision, the design is changed to film-capacitors, with much lower ESR which allows a significant reduction in output capacitance.

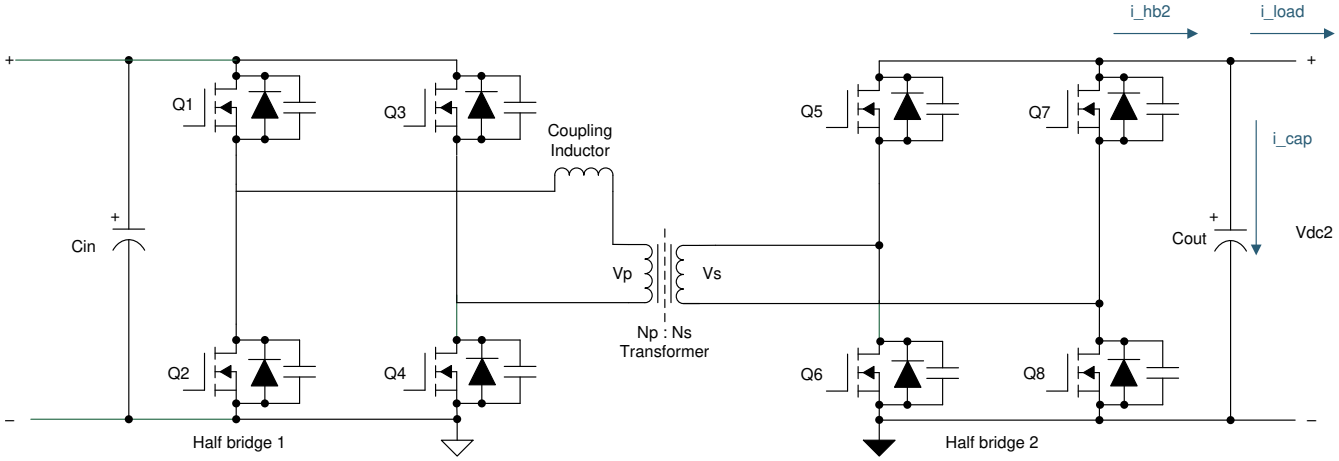


Figure 2-19. Output Current in Dual-Active Bridge

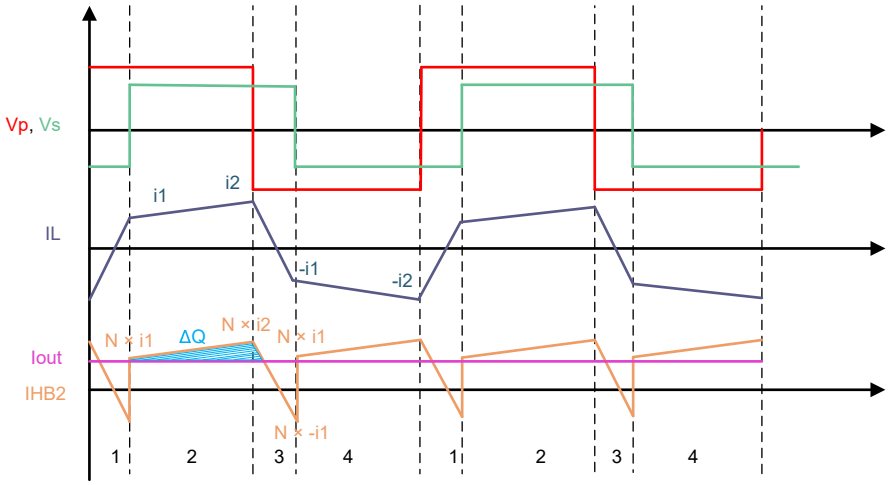


Figure 2-20. Output Capacitor Current

The capacitor also needs to be able to handle the RMS current, which is calculated with Equation 19.

$$I_{C,\,RMS} = \sqrt{\frac{\varphi}{2 \times \pi} \times \frac{1}{3} \times \left(i_{C2}^2 + i_{C2} \times i_{C3} + i_{C3}^2\right) + \left(1 - \frac{\varphi}{2 \times \pi}\right) \times \frac{1}{3} \times \left(i_{C1}^2 + i_{C1} \times i_{C2} + i_{C2}^2\right)} \quad (19)$$

where

$$i_{C1} = (i_1 \times N) - I_{out}$$

$$i_{C2} = (i_2 \times N) - I_{out}$$

$$i_{C3} = (-i_1 \times N) - I_{out}$$

2.3.4.5.1 DC-Blocking Capacitors

DC Blocking capacitors are introduced in the power stage to avoid saturation of the transformer in case of unbalanced currents, which can be caused by mismatched PWM signals, mismatched propagation delays in gate drivers or other asymmetries in the system. Especially during start-up and load transients unbalanced currents can occur. The DC blocking capacitors must be designed to handle the RMS currents on the transformer, be able to withstand the full-voltage and provide enough capacitance to not influence the switch-node voltage waveforms in a significant manner.

$$C_{DCBlock,\,min} = \frac{100}{4 \times \pi^2 \times F_S^2 \times L} = 7.2\ \mu F \quad (20)$$

2.3.4.6 Switching Frequency

Switching frequency is an important design parameter which affects the efficiency and power density of the power converter. The input and output voltage levels primarily determine the type of switches used in the power stage. Usage of SiC MOSFETs in the power stage enables high switching frequencies. Operating at higher switching frequencies enables a reduced size of magnetics which improves thermal conditions, thereby improving the power density of the converter. Therefore, selection of switching frequency is primarily a tradeoff between the allowable heat sink design and the transformer size for a given efficiency target. Secondly, if the output capacitance (Ecoss) of MOSFET is very high, selection of high switching frequency leads to high switching losses at light load and hampers efficiency. Selection of switching frequency also affects the control-loop bandwidth implementation. Considering all of these parameters, 100 kHz was used as the switching frequency for this application.

2.3.4.7 Transformer Selection

In a power supply design, transformers and inductors are major contributors to size. Increasing the operating frequency reduces the size, but increasing the switching frequency beyond a particular value affects the

efficiency of the power module. This is because the skin effect becomes very high at that frequency where the current flows through the surface of the conductor. Similar to the skin effect, there is a proximity effect, which causes current to only flow on surfaces closest to each other. Furthermore, from a proximity standpoint in high-frequency designs, conductor size and the number of layers must be optimized. With a planar transformer, more interleaving to reduce the proximity effect can be achieved. This interleaving can be tailored to produce a specific amount of leakage so as to aid in power transfer and to contribute to ZVS.

Planar transformers offer the following advantages over conventional transformers and hence were used in this reference design:

- Planar magnetics have very high power density. They are more compact and consume less space when compared to a conventional transformer of the same power rating.
- They have the ability to do more interleaving to reduce AC conductor losses.
- They have consistent spacing between turns and layers which translate into consistent parasitics. Both leakage inductance and intra-winding capacitances can be maintained to very predictable and tight values.
- Tight control over the leakage inductance is possible with planar magnetics.
- The compact size of the transformer can support integration of the additional shim inductor with the transformer itself without the need for a separate component on board.

The leakage inductor alone cannot provide soft switching up to light loads. As seen previously, increasing the soft switching range by increasing inductor value increases the RMS currents. In practice, a leakage inductor is chosen to provide soft switching only up to ½ or ⅓ of rated load. To increase the soft switching range, multiphase-shift controls can be applied. In some applications increased switching losses because of hard switching are acceptable for low loads since conduction losses decrease for low loads.

2.3.4.8 SiC MOSFET Selection

As shown in Figure 2-1, the main power stage switching devices of the primary and secondary must block the full input and output DC voltages. SiC switches were chosen for the following reasons:

- The switching speed of the SiC MOSFET is faster than a traditional Si device, thereby reducing switching losses.
- The reverse recovery charge is significantly smaller in the SiC MOSFET for the DAB application, resulting in reduced voltage and current overshoot.
- Lower state resistance significantly reduces conduction losses during on time of the device.
- The switches have the ability to block higher voltages without breaking down.

For this design, 1200-V Cree® devices with on-state resistance of 75 mΩ were used on the primary side, and a 900 V, voltage-blocking Cree device with on-state resistance of 30 mΩ was used in the secondary. Both are four-pin devices with a Kelvin connection for better switching performance. The actual conduction and switching loss calculations are shown in the following sections.

2.3.5 Loss Analysis

This section reviews the theoretical efficiency numbers obtained in the dual-active bridge. To arrive at the losses in different elements, the average and the RMS currents across the primary and secondary side are calculated. Details on the actual derivation of equations are out of scope for this design. The maximum power transfer in a dual-active bridge occurs at a phase shift of 90°. However, a high phase shift requires a high leakage inductance for power transfer. Using a high inductor leads to increased RMS currents in the primary and secondary side, which affects the efficiency of the converter.

Figure 2-18 shows the relationship between phase shift and the required inductance obtained from MATLAB simulations. The system specifications are tabulated in Table 2-1.

Table 2-1. DC/DC Converter Electrical Parameters

PARAMETER	SPECIFICATIONS
Phase shift	–0.44 < φ < 0.44 (rad)
Total Leakage Inductance	35 µH
Turns Ratio	1: 0.625
Load resistance	25 Ω

Table 2-1. DC/DC Converter Electrical Parameters (continued)

PARAMETER	SPECIFICATIONS
Input Voltage	800 V
Output voltage	500 V
Input current	12.5 A
Output current	20 A
Output Power	10 kW

2.3.5.1 SiC MOSFET and Diode Losses

As SiC is used in the power stage, the body diodes conduct only during the dead time, causing ZVS. In all other instances, the channel of SiC is turned on to conduct current. The peak current in the primary is calculated using Equation 7 and Equation 8. For the nominal operating conditions:

- V_1 = 800 V
- V_2 = 500 V
- F_s= 100 kHz
- T_s=10 µs
- N = 1.6
- φ = 0.4 rad
- P = 10 kW
- L = 35 µH

Calculating i_1 and i_2 for these inputs leads to $i_1 = i_2$ = 14.3 A. $i_1 = i_2$ is only true for the nominal output voltage $V_2 = V_1 / N$.

Figure 2-21 shows the current waveform of the switches on the primary side. The RMS value can be calculated from equation Equation 21. Inserting the values mentioned above leads to 9.67 A of RMS current for primary side switches.

$$I_{switch,\,prim,\,rms} = \sqrt{\frac{1}{6} \times \left(i_1^2 + i_2^2 + \left(1 - \frac{2\varphi}{\pi}\right) \times i_2 \times i_1\right)} = 9.67\ A \tag{21}$$

The diode conducts for only a small fraction of time during the switching period, as in the dead time causing ZVS. The dead time chosen for this application is 200 ns.

$$I_{diode,\,prim} = i_2 \times \frac{t_{dead}}{T_s} = 0.286\ A \tag{22}$$

The value of drain-source resistance corresponding to the applied gate voltage waveform is obtained from the SiC MOSFETs data sheet. This value is 75 mΩ. The forward voltage drop across the body diode is 5.5 V. The conduction losses across the four primary side FETs is calculated using Equation 23:

$$P_{cond,\,prim} = 4 \times \left(I_{switch,\,prim,\,rms}^2 \times R_{ds,\,on} + I_{diode,\,prim} \times V_{fd,\,prim}\right) = 34.34\ W \tag{23}$$

Similarly, the conduction losses are calculated across the secondary side FETs by scaling the primary side RMS currents with transformer turns ratio using Equation 24 and Equation 25. The on state resistance of the secondary side MOSFET is 30 mΩ. The forward voltage drop across the body diode is 5.5 V

$$I_{switch,\,sec,\,rms} = N \times I_{switch,\,prim,\,rms} = 15.47\ A \tag{24}$$

$$I_{diode,\,sec} = N \times I_{diode,\,prim} = 0.458\ A \tag{25}$$

$$P_{cond,\,sec} = 4 \times \left(I_{switch,\,sec,\,rms}^2 \times R_{ds,\,on} + I_{diode,sec} \times V_{fd,\,sec}\right) = 37.88\ W \tag{26}$$

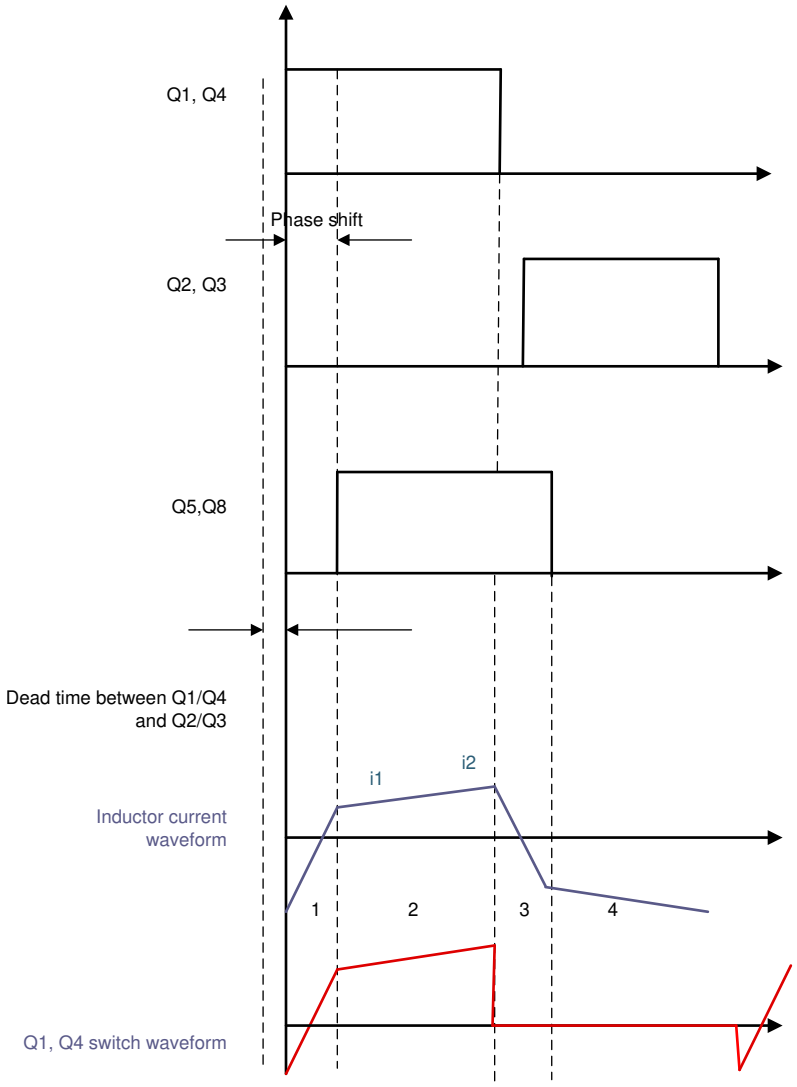


Figure 2-21. Switch Current Waveforms for Calculating RMS Value of Current

The switching loss curves from the manufacturer are used to calculate switching losses.

Because the FETs turn on at zero voltage, only the turn-off loss coefficients are used for calculating the switching losses. Using the C3M0030090K data sheet information, a turn-off energy of 60 µJ is estimated for this operating condition. The values of switching loss per device is obtained using the information in Equation 27. This leads to 24 W of switching losses for the secondary side.

$$P_{sw,\,tunroff,\,sec} = F_s \times E_{off} = 6\ W \tag{27}$$

For the primary side switch C3M0075120K the turn-off energy is estimated at 75 µJ. Which leads to 30 W of switching losses on the primary side.

$$P_{sw,\,tunroff,\,prim} = F_s \times E_{off} = 7.5\ W \tag{28}$$

Total turn off switching losses in the primary and secondary side across all eight switches comes to 54 W.

These calculations are done for the nominal operating conditions. For different operating points these calculations need to be adjusted. For non-nominal output voltages, the zero-voltage-switching can be lost and the turn-on losses must be taken into account.

2.3.5.2 Transformer Losses

For this reference design a planar transformer was selected and was designed with the specifications shown in Table 2-2. The estimated power losses under normal operating conditions are 50 W.

Table 2-2. Transformer Specifications

FUNCTIONAL SPECIFICATIONS	RATINGS
Total output power	10 kW (500 V/20 Adc)
Operating frequency	100–200 kHz
Input voltage of transformer	800 V (V_{OUT} = 500 V), Bipolar Square waveform
Volt-second product	8000 V µs – for V_{OUT} = 500 V, 100 kHz
Primary-to-secondary ratio	24:15
Primary current maximum	13.5 Arms (20 A peak) – for V_{OUT} = 500 V
Secondary current maximum	20 Arms (30 A peak) – for V_{OUT} = 500 V
Estimated power losses	50 W – for V_{OUT} = 500 V, 100 kHz;
Primary winding DC resistance	43 mΩ
Secondary winding DC resistance	16 mΩ
Leakage inductance	34 µH
Magnetizing inductance	720 µH

More details of this transformer are available from Payton.

2.3.5.3 Inductor Losses

The inductor used for this design is a custom inductor, which is integrated in the Payton planar transformer. The total leakage inductance is 34 µH and the total estimated power loss provided by the manufacturer is 15 W (for V_{OUT} = 500 V, F_s=100 kHz).

2.3.5.4 Gate Driver Losses

The power loss in the gate driver circuit includes the losses in the UCC21530 and losses in the peripheral circuitry like the gate resistors. The power losses consist of the static power loss, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. Values of the quiescent current flowing into the V_{cc} pin (I_{VCCQ}) and V_{DD} pin (I_{VDDQ}) are extracted from the data sheet.

$$P_Q = \left(V_{CC} \times I_{VCCQ}\right) + \left(V_{DD} \times I_{VDDQ}\right) = \left(3.3\ V \times 3\ mA\right) + \left(15\ V \times 4\ mA\right) = 70\ mW \quad (29)$$

By substituting the values from the data sheet in Equation 29, the result is P_Q losses of the gate driver around 70 mW. The other component of gate driver loss is the switching operation loss. Which result in a total of 560 mW for eight gate drivers.

$$P_{sw} = 2 \times \left(V_{DD} - V_{EE}\right) \times Q_G \times F_s = 0.2\ W \quad (30)$$

By substituting the value of V_{DD} = 15 V, V_{EE} = –4 V, F_{SW} = 100 kHz, Q_G = 53 nC in Equation 30, the switching loss comes to 0.2 W per FET on primary.. The gate charge for C3M0075120K (primary side MOSFET) is extracted from the data sheet. Similarly, for the secondary side, the switching losses are calculated to be approximately 0.33 W. Gate charge, Q_G, for the C3M0030090K MOSFET is 87 nC and is obtained from the data sheet. Also during turn on and turn off of the MOSFETs, losses occur in the gate resistors. The turn on and turn off gate resistors are 2 Ω . These resistors are chosen to dampen out the oscillations at the gate. The gate driver IC can sink and source 10-A peak current during the switching process. Taking an average value of this current pulse over a switching cycle, the turn on and turn off losses occurring in the gate resistors is given by Equation 31.

$$P_{cond} = \frac{Q_G \times \left(V_{DD} - V_{EE}\right) \times F_s}{2} \times \left(\frac{R_{on}}{R_{Gin}} + \frac{R_{off}}{R_{Gin}}\right) = 18\ mW \quad (31)$$

This value comes to 18 mW for each switch on primary side and 30 mW per switch on secondary side, summing up to 192 mW in total. Thus, the total losses occurring in all gate drivers is approximately 3 W.

2.3.5.5 Efficiency

Table 2-3 summarizes the loss numbers from the previous sections and computes the theoretical efficiency at 10 kW.

Table 2-3. Loss Analysis

TYPE OF LOSS	LOSS (WATTS)
SiC conduction loss in primary and secondary side	72
SiC turn off switching loss	54
Transformer loss	50
Gate driver loss + shunt resistor losses	3
Inductor loss	15
Efficiency	98%

2.3.5.6 Thermal Considerations

Heat sinks are used to cool CR201-50VE. Two FETs are mounted per heat sink: therefore, insulation must be used between the exposed drain of the FETs and the heat sink. CD-02-05-247 insulation sheets are used. Additionally two 12-V (CFM-6015V-154-362) fans are mounted to provide sufficient airflow. The heat sink data sheet provides a thermal resistance of 0.5 C / W ($R_{th,HS}$). The insulation sheet adds another 0.1 C / W ($R_{th,iso}$) of thermal resistance. The primary side FET C3M0075120K has a thermal resistance $R_{th,JC}$ of 1.1 C / W and a maximum operating temperature of 150°C, while the secondary sided FET (C3M0030090K) has a thermal resistance $R_{th,JC}$ of 0.48 C / W and also a maximum junction temperature of 150°C. With this information, the maximum allowable power dissipation per FET can be calculated with Equation 32. This assumes 2 FETs are connected to one heat sink like in the reference design.

$$P_{max} = \frac{T_{J,max} - T_A}{2 \times R_{th,HS} + R_{th,iso} + R_{th,JC}} \quad (32)$$

This leads to a maximum of 50 W of losses per FET on primary side and 69 W per FET on secondary side assuming an ambient temperature T_A of 40°C.

3 Circuit Description

3.1 Power Stage

Figure 3-1 shows the power stage of a single-phase, dual-active bridge. The primary side consists of 1200-V, 75-mΩ silicon carbide FETs C3M0075120K to block a DC voltage of 800 V, and the secondary side consists of 900-V, 30-mΩ silicon carbide FETs C3M0030090K to block DC voltage of 500 V. The full bridges are connected with a high-frequency switching transformer (T1). Four CR201-50VE heat sinks in combination with two fans are used to cool the FETs. CD-02-05-247 insulation sheets are used between the FETs and the heat sinks to provide necessary insulation and a good thermal interface.

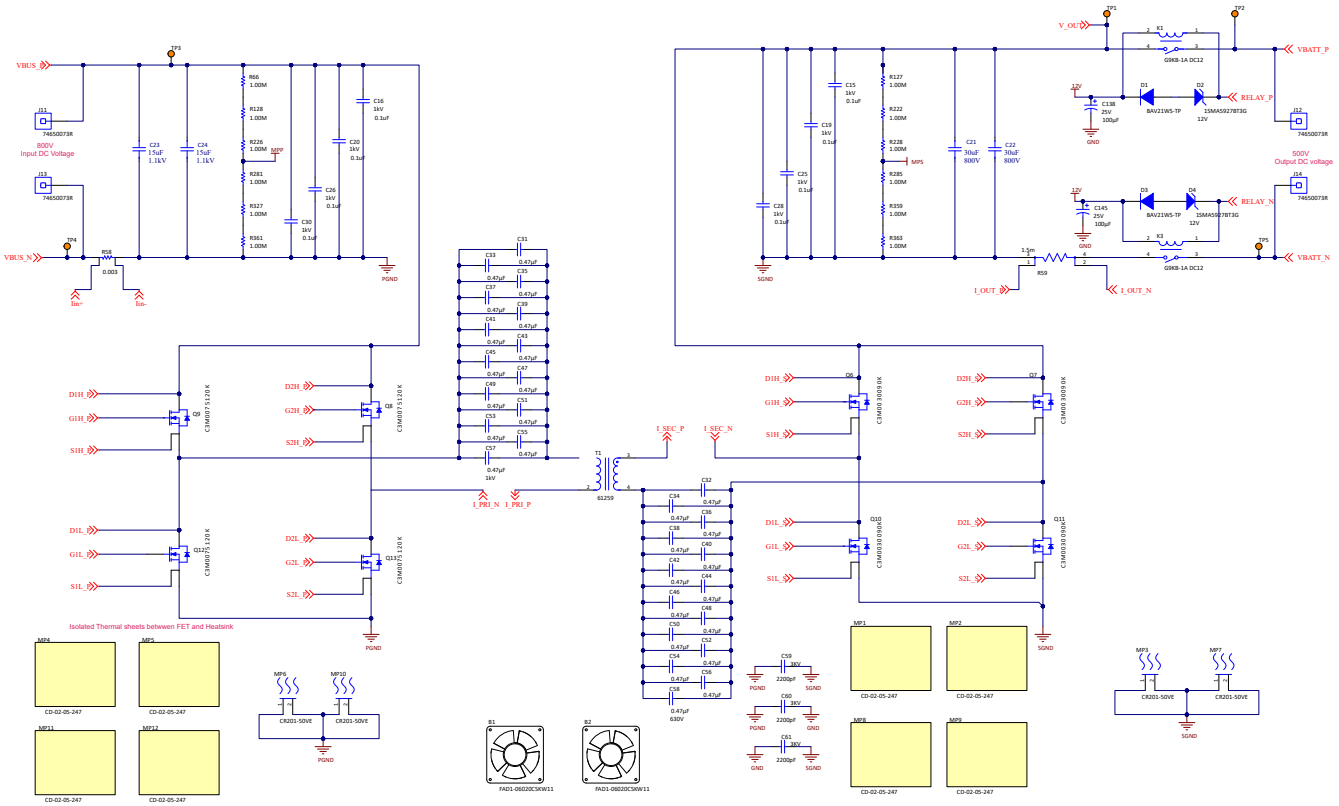


Figure 3-1. Power Stage

3.2 DC Voltage Sensing

3.2.1 Primary DC Voltage Sensing

Figure 3-2 shows the primary voltage sensing circuit. The maximum primary input voltage to be sensed is 800 V and is scaled down by a resistor divider network to 1.57 V, which is compatible to the 2-V input of the AMC1311. Figure 3-2 shows eight 634-kΩ resistors and one 10-kΩ resistor used to drop the primary voltage signal. The signal is then processed by one channel of the OPA2320, which converts it in the range of 0 V to 3.3 V as required by the ADC.

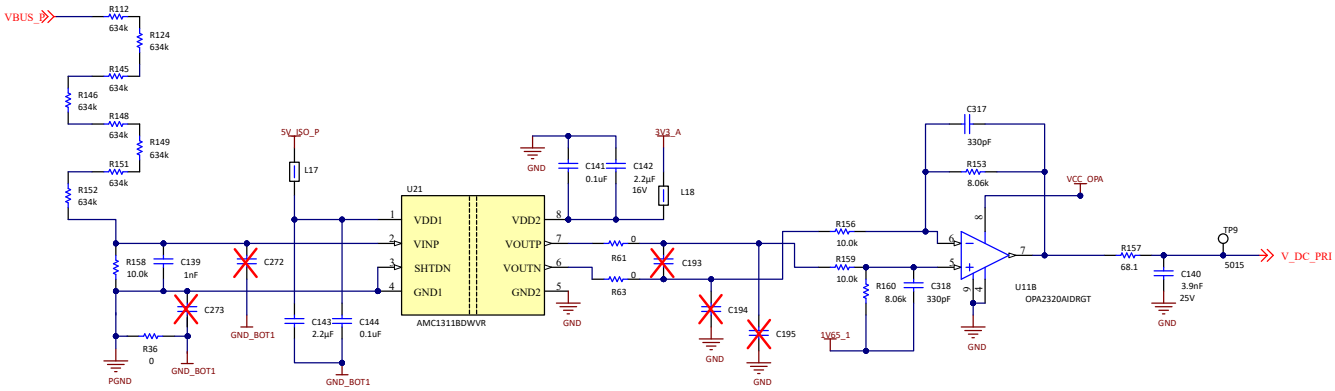


Figure 3-2. Primary Side DC Voltage Sensing

Figure 3-2 shows the isolated power supply circuit for powering the AMC1311. An isolated 3.3-V supply is needed to power the primary side of the AMC1311. The isolated power supply is shared with a low-side gate driver bias supply, generated by a UCC1414-Q1. The 15-V output voltage of the UCC14141-Q1 is used but a TLV760 is necessary to generate the 5 V for the AMC1311. This isolated supply is also used for the isolated current sensing on the primary side.

3.2.2 Secondary DC Voltage Sensing

On the secondary side an isolated modulator is used for voltage sensing. A digital interface is preferred here, since the secondary side sensing is much further away from the controller. A digital interface is not as vulnerable to noise and therefore a better fit for long traces inside a power conversion system. The necessary clock is generated by a spare PWM module of the microcontroller. The output bit stream is fed into the SDFM Module of the C2000. Using the configurable decimation filters within the SDFM module allows for accurate measurements and fast protection. The 500 V is scaled down to 0.76 V which fits the ±1-V input of the AMC1336.

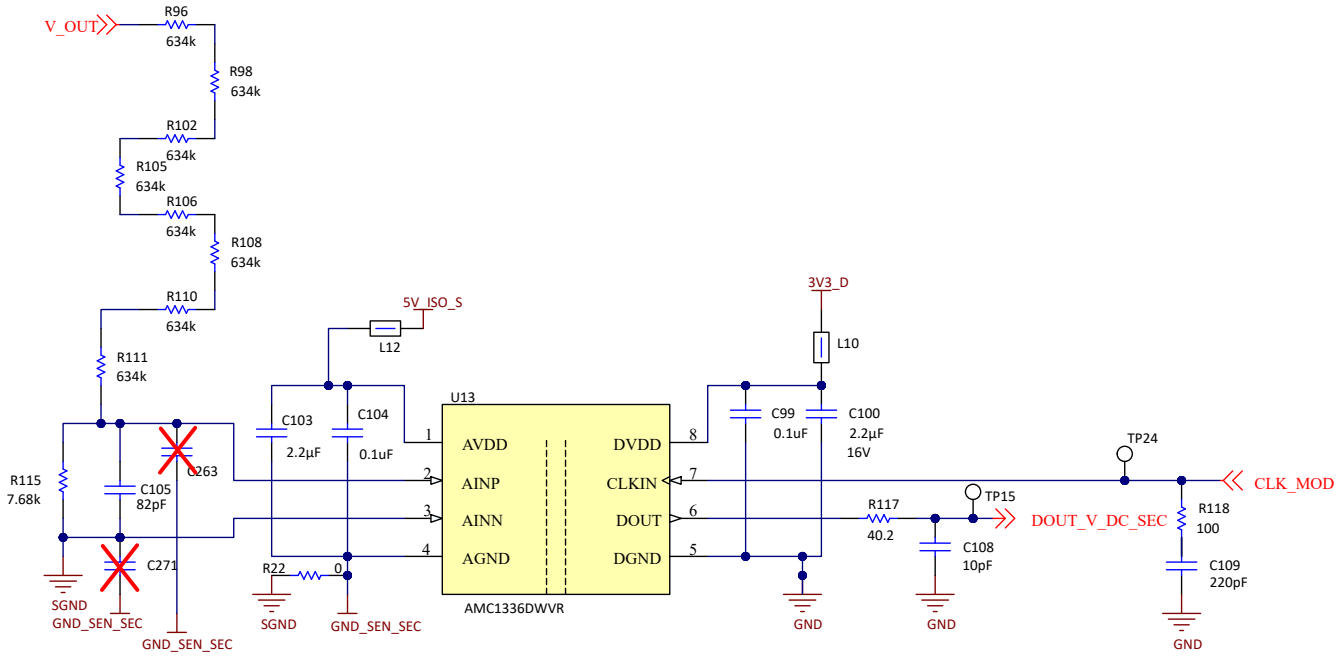


Figure 3-3. Secondary Side Output Voltage Sensing

3.2.2.1 Secondary Side Battery Voltage Sensing

In addition to the DC voltage sensing, a battery voltage sensing is implemented inside the relays, which allows for active pre-charging from the primary side. This modulator uses the same clock as the DC voltage sensing inside the relays. The output is connected to another SDFM channel. For the resistor divider there are two scenarios. If the relay is open GND_SEN_SEC is floating with regards to VBATT_N. In the case the full resistor divider is active, scaling down the 500 V to 0.33 V. IN case the relay is closed VBATT_N is shorted with GND_SEN_SEC; therefore, only the upper part of the resistor divider is active. In this configuration 500 V is scaled down to 0.65 V.

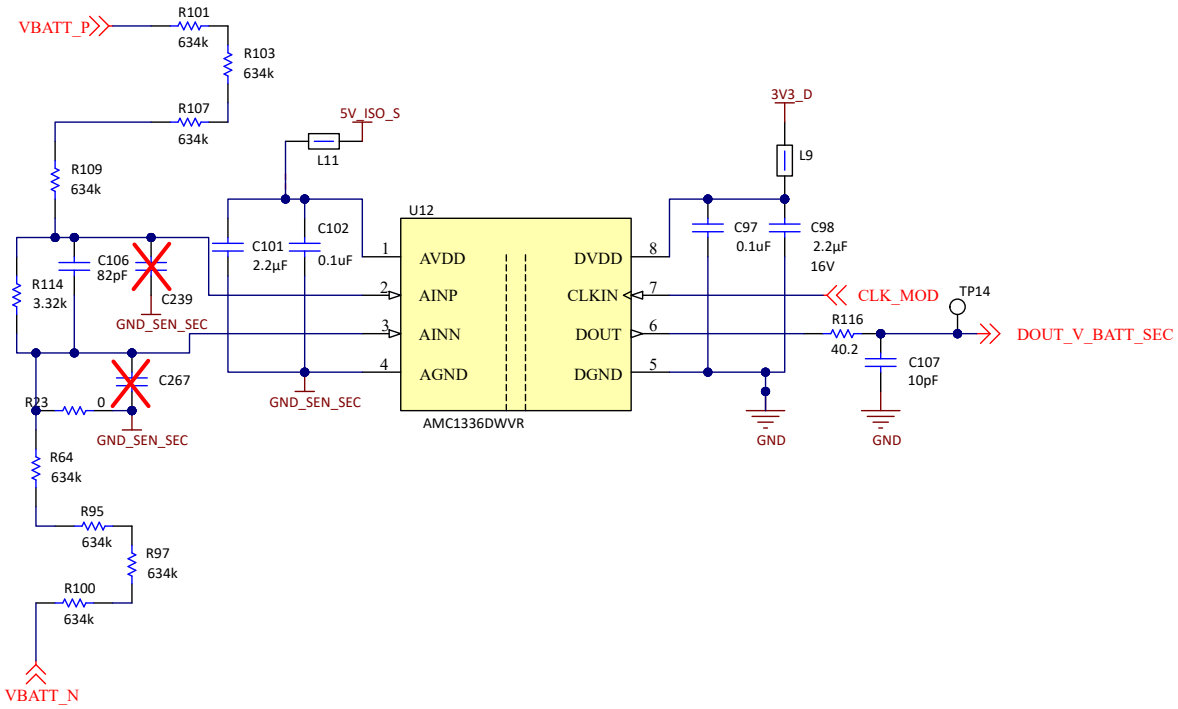


Figure 3-4. Secondary Side Battery Voltage Sensing

3.3 Current Sensing

Current sensing is important for sensing overcurrent and getting a closed loop system to work accurately. In this design, current sensing is done at multiple locations with different sensing methods. The first is on the input and output side DC terminals using current sense resistors. The isolated amplifier AMC1302 is used on the primary side and has a input voltage of 50 mV. Therefore, a 3-mΩ shunt resistor is used, converting the maximum input current of 12.5 A to 37.5 mV.

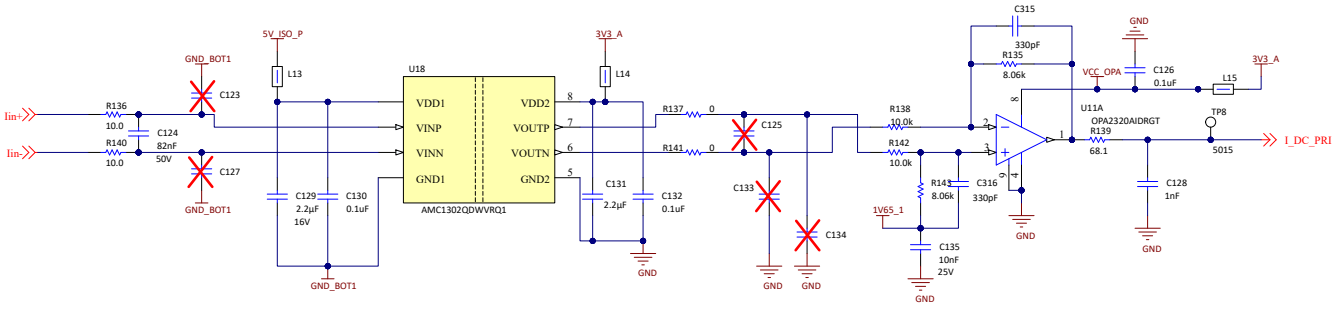


Figure 3-5. Primary Side Input Current Sensing

The isolated modulator AMC1306M05 is used on the secondary side. Here a 1.5-mΩ shunt converts the maximum output current of 20 A to 30 mV, which fits the 50-mV input of the AMC1306M05. Now for lower output voltages, higher output currents can be achieved, which can need a smaller shunt to measure the full current range.

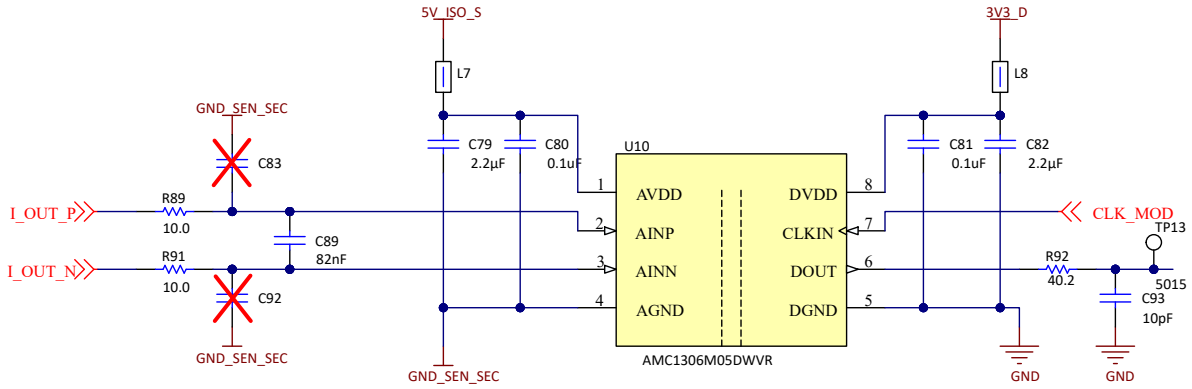


Figure 3-6. Secondary Side Output Current Sensing

The Hall sensor TMCS1133 is used to measure the transformer current on the primary and secondary side. Here a Hall sensor is preferred because of the lower propagation delay which is needed to implement an overcurrent protection at the switch nodes. TMCS1133 offers 1 MHz of bandwidth, which is necessary to measure an accurate current waveform at 100 kHz switching frequency. TMCS1133 also offers a built-in overcurrent protection which is set to 45 A on the primary side and to 70 A on secondary side by the resistor divider on the VOC pin. The fault output indicates this overcurrent scenario. This pin is connected to a GPIO of the C2000 MCU, which is configured to trip the PWM signal in case of overcurrent.

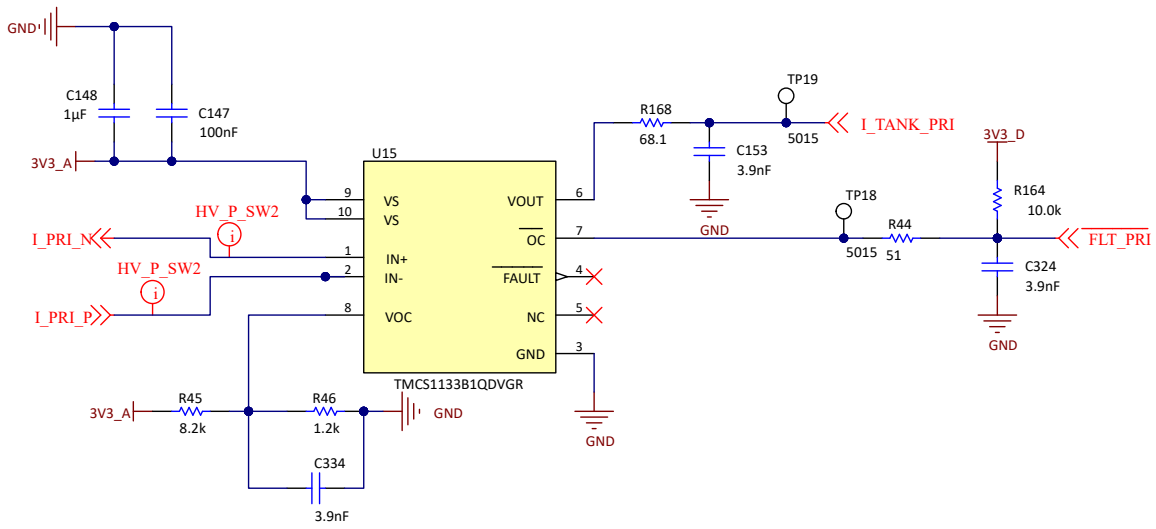


Figure 3-7. Transformer Current Sensing

3.4 Power Architecture

The power tree of this reference design consists of multiple ICs providing the necessary system voltages:

- An external 12-V power supply is necessary to operate the board. This 12-V rail directly powers the fans, relays, and UCC14141 isolated bias supplies
- 5 V to the Control Card and 3.3-V LDOs
- Two LDOs are used to generate 3.3-V digital and 3.3-V analog supplies for the Cs
- Isolated bias supply provides +15 V and 4 V for gate drivers
- An LDO is used on the high side to generate isolated 5 V to power the high sides of the isolated sensing circuits

3.4.1 Auxiliary Power Supply

The external power is directly used to power fans, relays and isolated bias supplies. Therefore, the eFuse TPS2640 is used to protect the system. Overvoltage protection is set to 15 V, undervoltage lockout is set to 9 V and a current limit is set to 2.2 A. A detailed design procedure is found in the device data sheet. Two LEDs are used to indicate the status. The green LED D8 indicates normal status, while the red LED D6 indicates a fault state. Use the S1 push-button to reset the device.

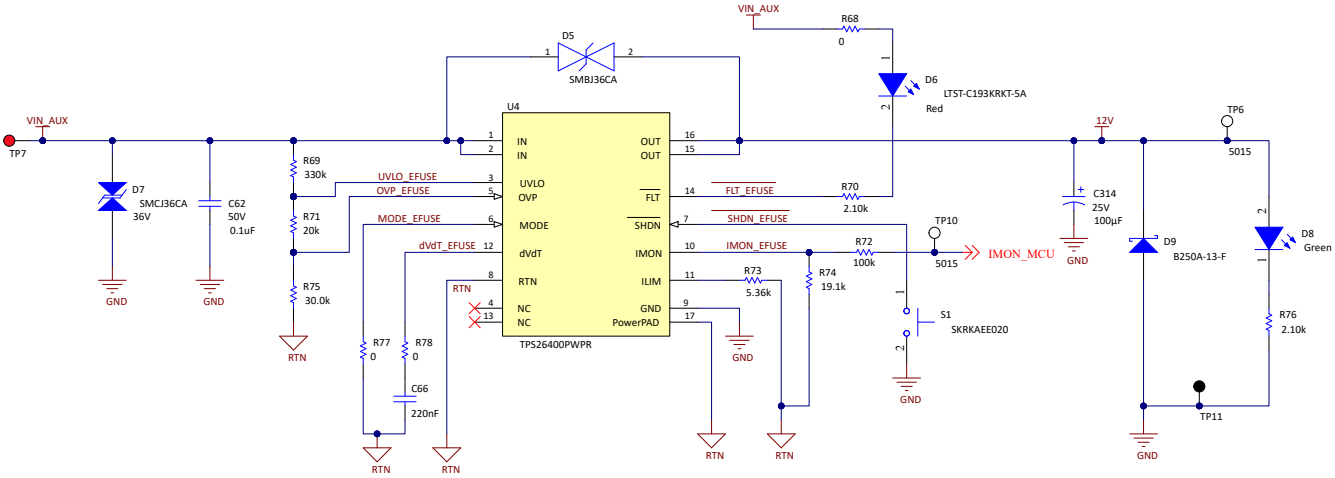


Figure 3-8. eFuse Circuitry

The power module TLVM13620 is used to generate a 5-V rail from the input. LED D10 indicates the 5-V output. A module with integrated inductor is used for the design simplicity and small footprint.

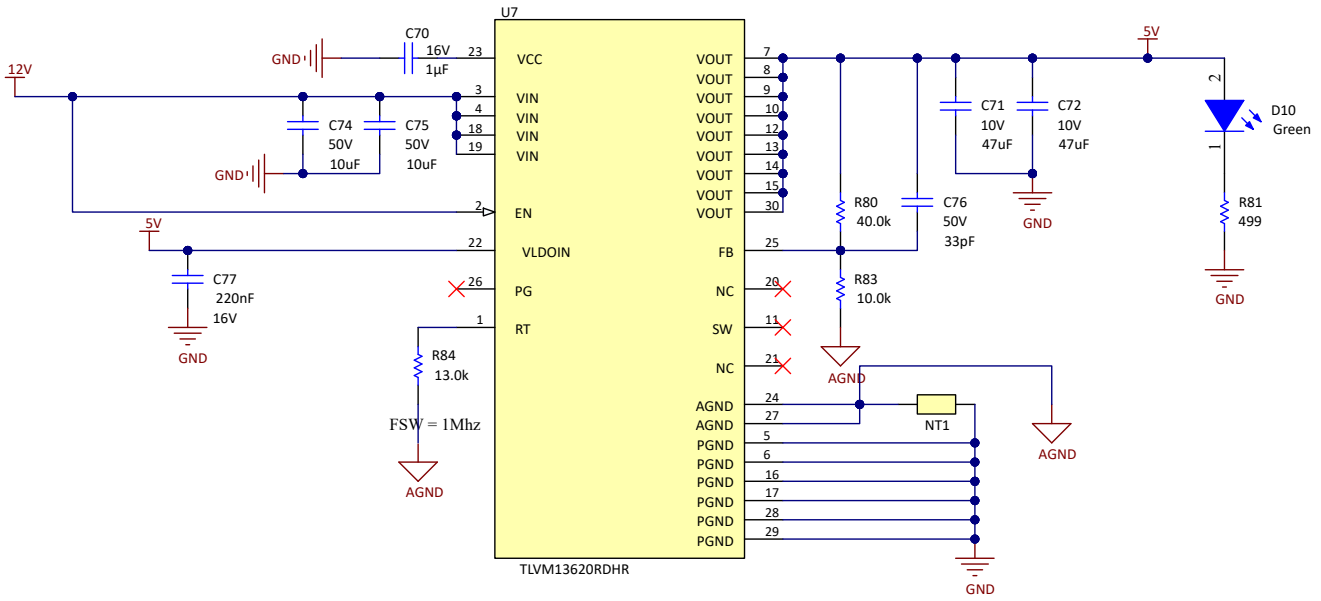


Figure 3-9. 5-V Power Module

Two LDOs are used to generate a 3.3-V analog and a 3.3-V digital rail.

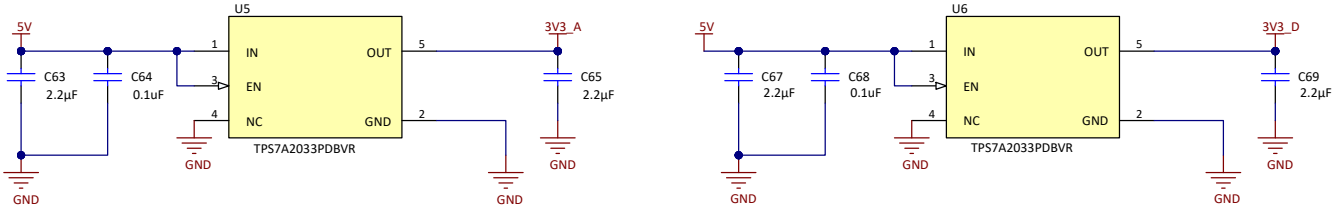


Figure 3-10. LDOs for Analog and Digital 3.3-V Rails

3.4.2 Gate Driver Bias Power Supply

The UCC14141 device is selected as an isolated bias supply. This is a isolated bias module with an integrated transformer, offering the smallest footprint and height. The output is configured in a dual rail configuration to +15 V and –4 V. The maximum power drawn per device is calculated using the UCC14141-Q1 calculator tool available on the product folder. With this the value of the current-limiting resistor (RLim) (RLIM in Figure 3-11). Here 1 kΩ is selected for the devices only supplying one gate driver and 600 Ω is selected for the devices supplying one gate driver and the high side of the isolated sensing. Each output is connected to an LED indicating that isolated power is present. There are precautions on the board to share the isolated bias supply between the two low-side FETs on each side. For this jumper the resistors need to be placed and RLim needs to be adjusted. This is not tested yet. Additionally there is the option to populate a bootstrap supply for the high-side FETS, which is also not yet tested.

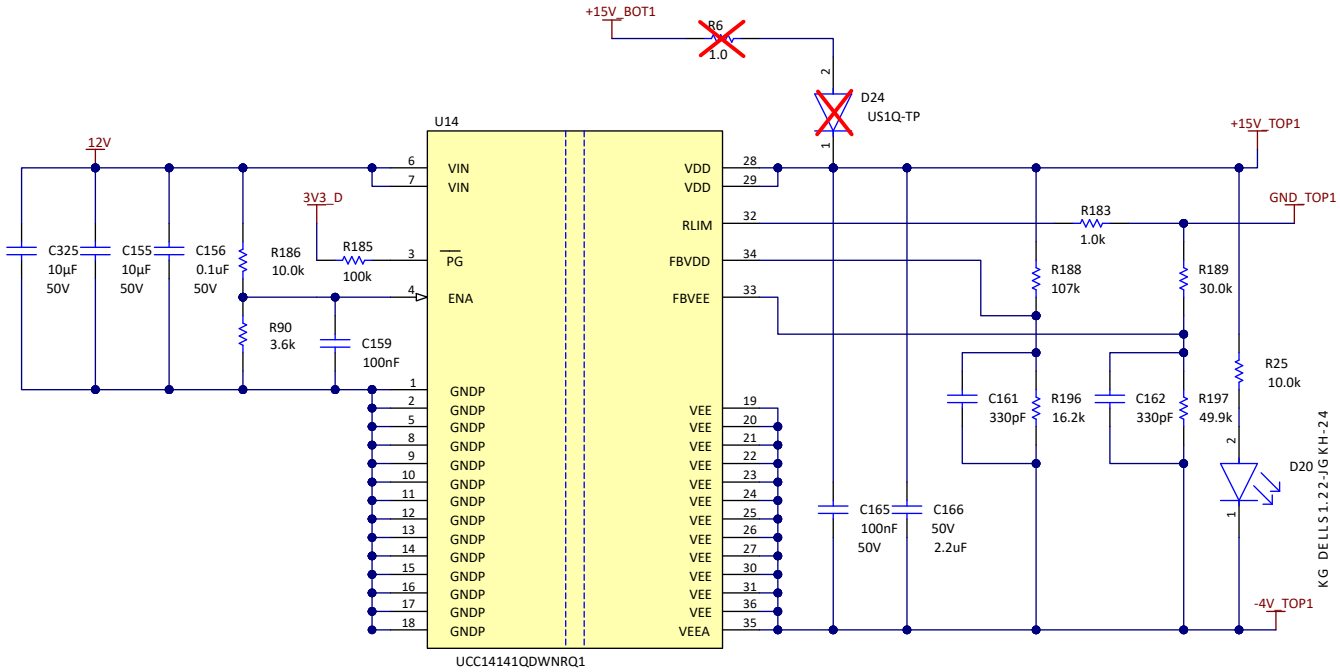


Figure 3-11. Gate Driver Bias Supply Circuit

3.4.3 Isolated Power Supply for Sense Circuits

To generate the isolated supply for the isolated amplifiers and modulators the low-side gate driver bias supply is reused. The 15-V isolated rail is converted down to a 5-V rail using a TLV760 with fixed 5-V output. A series resistor is used at the input to reduce the power dissipated in the LDO.

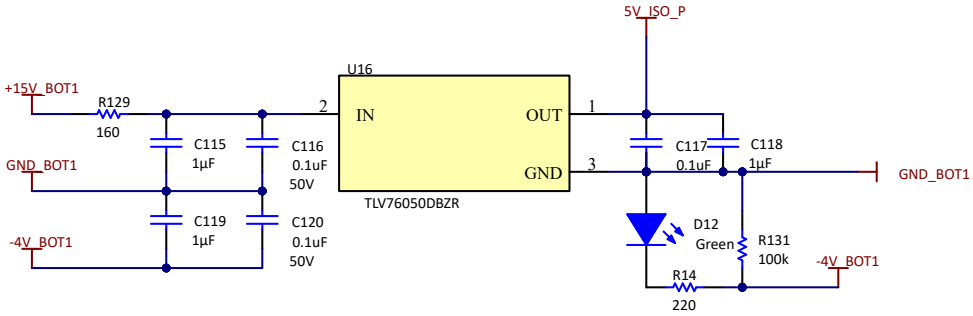


Figure 3-12. Supply for Voltage and Current Sense Derived From Gate Driver Bias Supplies

3.5 Gate Driver Circuit

The UCC21710 is used as a gate driver. This device was selected for the integrated features for SiC, like DESAT protection, internal active Miller clamp and soft turn-off. The PWM interlock makes sure that at no time both complimentary PWMs of on H-Bridge are turned on. The analog-to-PWM channel, can be used for isolated temperature sensing on the high side. The DESAT voltage was configured to 6.4 V with a blanking time of 1 µs using the UCC217xx XL Calculator Tool available in the device product folder. The undervoltage lockout function of UCC21710 is used to check if both the isolated power (VCC) and the non isolated power (VCC) are in a valid range which is indicated on the RDY pin.

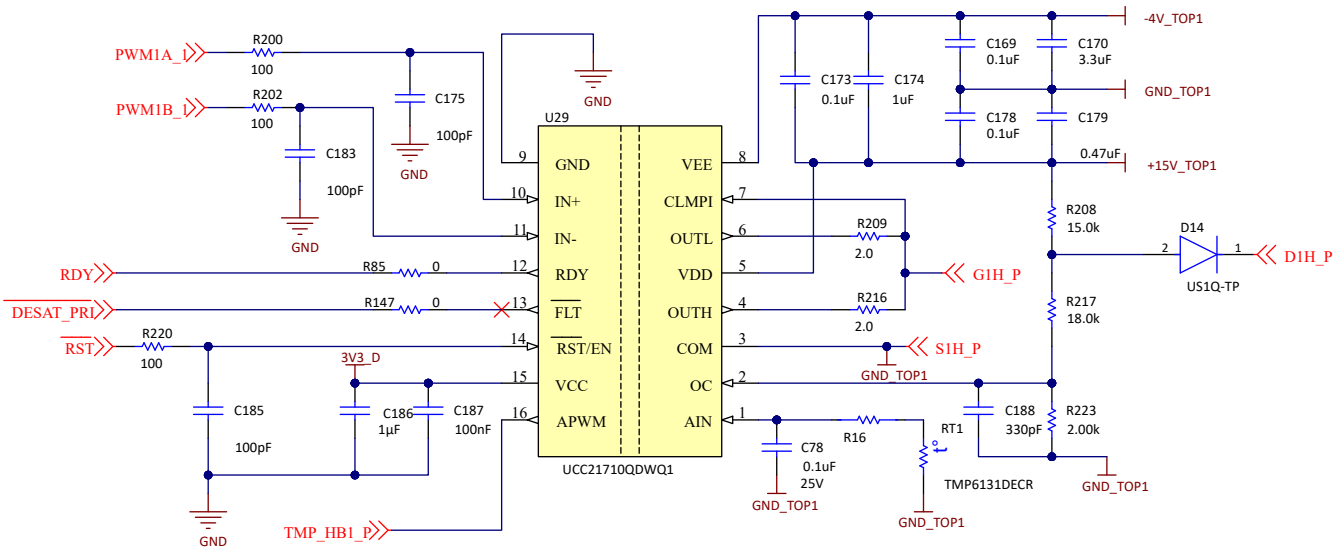


Figure 3-13. UCC21710 Gate Drive Circuit

3.6 Additional Circuitry

The isolated CAN transceiver ISOW1044 is used to enable CAN communication. The device is connected to the MCU through the D-Sub 9 pin connector. CAN Communication is not implemented in the current state of this design.

The TMUX1204 is used to interface the outputs of UCC21710 APWM channels to the control card connector. SN74LVC126A buffers are used to redrive the PWM signals.

3.7 Simulation

To support evaluation of this reference design, a PLECS simulation deck is provided in the product folder. This simulation can be used to evaluate both single-phase shift and extended- phase shift modulation, in regards to efficiency and thermal behavior. The simulation is available for PLECS standalone and PLECS Blockset in combination with MATLAB and Simulink.

Note

PLECS is a third party tool. The tool is available as PLECS Blockset (MATLAB Simulink extension) or standalone. For more information, see plexim.com.

3.7.1 Setup

Figure 3-14 shows the folder structure of the downloadable file.

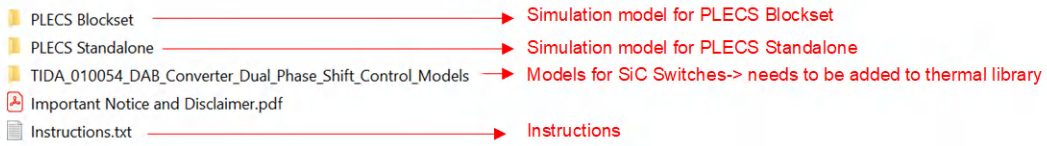


Figure 3-14. PLECS Simulation - Folder Overview

Figure 3-15 shows the PLECS simulation deck.

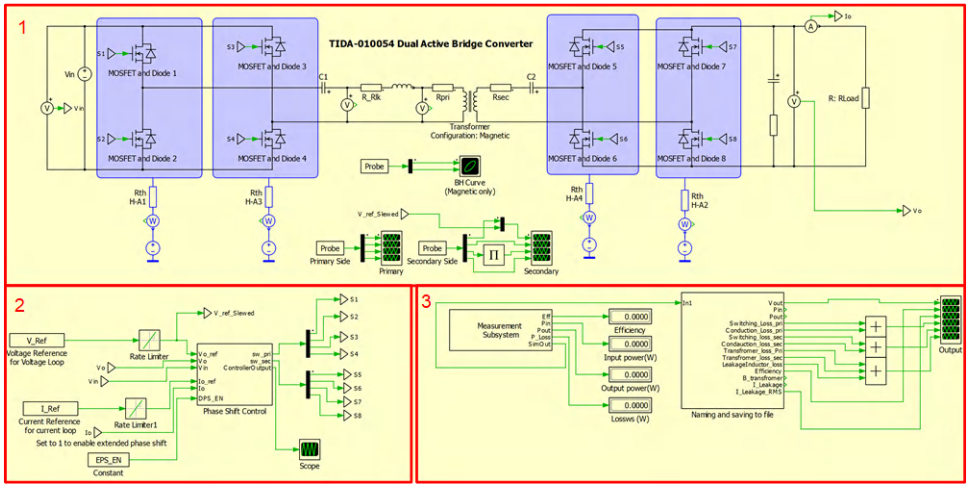


Figure 3-15. PLECS Simulation Deck

The PLECS simulation deck consists of three major parts:

1. Power converter:
   a. Contains power converter, with manufacturer silicon carbide field-effect transistor (SiC-FET) models
   b. Heat sinks, the setup is similar to TIDA-010054 for thermal analysis
   c. Primary scope for analyzing switch node waveforms
   d. Secondary scope to analyze output voltage, current, and power
   e. BH Curve to analyze magnetic behavior of the transformer
2. Phase shift control:
   a. Contains controller for voltage and current loop. Allows to switch between voltage and current loop by opening Phase Shift Control block and changing the configuration of the controller.
   b. Extended phase shift modulation can be enabled by setting EPS_EN = 1 in the initialization script.
3. Measurement subsystem:
   a. Measures and adds up losses in the system, to calculate efficiency
   b. Displays to see input power. Output power efficiency and losses while simulation is running
   c. Naming and saving to a file block, to name signals from the measurement subsystem and enabling to save to Microsoft® Excel® file (only for the standalone version)

3.7.2 Running Simulations

This section contains instructions for PLECS using the Blockset and standalone setup.

Instructions PLECS Blockset:

1. Open both TIDA_010054_DAB_Converter_Parameters.m and TIDA_010054_DAB_Converter_Simulation.slx files in MATLAB
2. Open the PLECS circuit in TIDA_010054_DAB_Converter_Simulation.slx
3. Add the TIDA_010054_DAB_Converter_Models folder to the thermal library (File → PLECS Preferences → Thermal → (Press the plus sign))

4. Run TIDA_010054_DAB_Converter_Parameters.m to populate parameters in the MATLAB workspace. These can be modified to simulate different operation points or to enable and disable extended-phase-shift control (EPS_EN = 1 or EPS_EN = 0)
5. Run simulation either by pressing Run in TIDA_010054_DAB_Converter_Simulation.slx or by pressing Simulation → Run in the PLECS Simulation Deck
6. Simulation can be observed in scopes and displays within the PLECS circuit

Instructions PLECS Standalone:

1. Open the TIDA_010054_DAB_standalone.plecs file in PLECS
2. Add the TIDA_010054_DAB_Converter_Models folder to the thermal library (File → PLECS Preferences → Thermal → (Press the plus sign))
3. Initialization is found under Simulation → Simulation parameters → Initialization. These can be modified to simulate different operation points or to enable and disable extended-phase-shift control (EPS_EN = 1 or EPS_EN = 0)
4. Run the simulation by pressing Simulation → Run in the PLECS Simulation Deck
5. Simulation can be observed in scopes and displays within the PLECS circuit

Figure 3-16 shows the primary scope. Use this scope to evaluate the switching waveforms.

Figure 3-17 shows the secondary scope. Use this window to observe output voltage, current, and power, as well as the output voltage ripple and capacitor current.

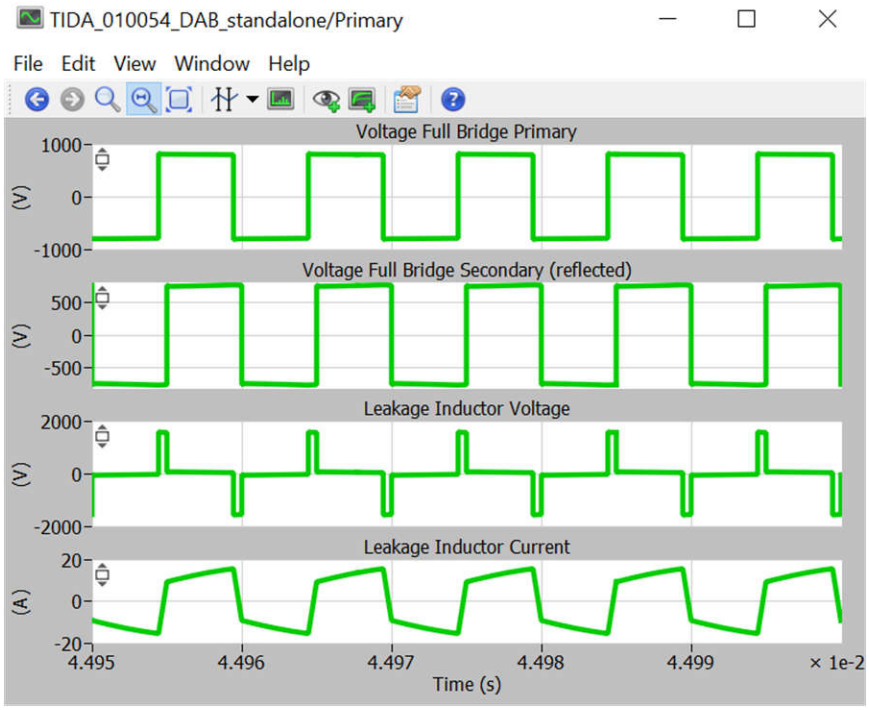


Figure 3-16. PLECS - Primary Scope

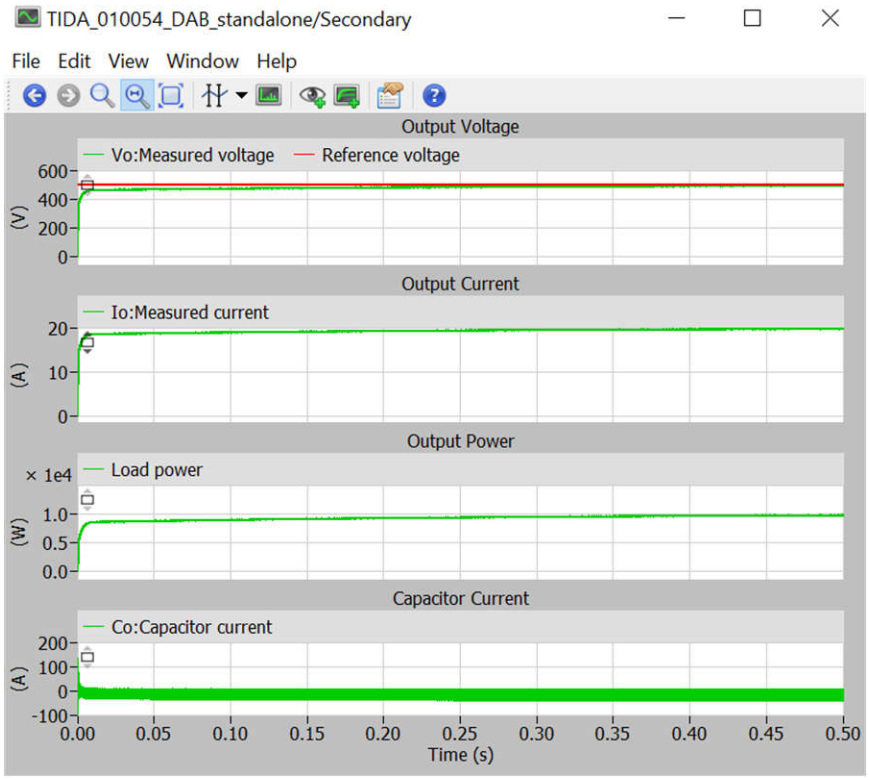


Figure 3-17. PLECS - Secondary Scope

Note

This simulation deck is for system level evaluation. Not all parasitic effects can be simulated accurately. Simulation results can vary from measurement results.
For example, SiC-FET manufacturer models do not include output capacitances. Therefore, soft-switching is achieved down to very light loads in simulation. Efficiencies under light load vary from actual measurements.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware and Software

4.1.1 Hardware

The following hardware is required for this reference design:

- One TIDA-010054 power board
- One TMDSCNCD280039C control card
- USB Type-C® cable
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- 10-kW DC source capable of delivering voltage between 700 V–800 V at required current
- 10-kW resistive load bank
- Power analyzer
- Auxiliary power supply with jack connector 12-V, 2.5-A rated
- Oscilloscope
- Isolated voltage probes and current probes

4.1.2 Software

Code Composer Studio™ with C2000 powerSUITE and C2000WARE-DIGITALPOWER-SDK used in this design.

The general structure of the project follows C2000Ware-DigitalPower-SDK Structure. For this design, <solution> is "DAB". The solution name is also used as the module name for all the variables and defines used in the solution. Hence, all variables and function calls are prepended by the DAB name (for example, `DAB_vSecSensed_pu`). This naming convention lets the user combine different solutions while avoiding naming conflicts.

1. The "<solution>.c/h" are solution-specific and device-independent files that consist of the core algorithmic code.
2. The “<solution>_board.c/h" are board-specific and device-dependent. This file consists of device-specific drivers to run the solution. If the user wants to use a different modulation scheme or a different device, the user is required only to make changes to these files, besides changing the device support files in the project.
3. The "<solution>-main.c" file consists of the main framework of the project. This file consists of calls to the board and solution file that help in creating the system framework, along with the interrupt service routines (ISRs) and slow background tasks.
4. The "<solution>-settings.h” file is where all project-level settings are made like defining frequency, mapping PWM and ADC channels to signals on the control card. This is a device specific file and needs to change from device to device.

4.1.2.1 Getting Started With Software

1. Install *Code Composer Studio (CSS)*
2. Download software (TIDA-010054-FW) via mySecure Software
   - Software to be released fully in SDK in 2Q2024
3. Download and install C2000WARE-DIGITALPOWER-SDK
4. Replace exiting TIDA-010054 folders:
   a. Replace
      `C:\ti\c2000\C2000Ware_DigitalPower_SDK_5_01_00_00\solutions\tida_010054`
      with
      `TIDA-010054_Firmware\solutiontida_010054` folder from mySecure Software
   b. Replace
      `C:\ti\c2000\C2000Ware_DigitalPower_SDK_5_01_00_00\powerSUITE\source\devkits\.meta\TIDA_010054`
      with
      `TIDA-010054_Firmware\powersuite\TIDA-010054`

5. Open CCS, go to project → Import project and browse to the folder `C:\ti\c2000\C2000Ware_DigitalPower_SDK_5_01_00_00\solutions\tida_010054\f28003x\ccs`. The DAB project is listed. Complete the steps to import the project.
6. The code is designed for the F28004x control card.Figure 4-1 shows the loaded project explorer view. Open main.syscfg in the Project Explorer window, choose lab and then compile, then program the device.
7. Once loaded, enable real-time mode and run the code.
8. To add the variables in the watch or expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open and then browse to the "setupdebugenv_lab1.js" script file located inside the project folder. This populates the watch window with appropriate variables needed to debug the system.
9. Select the *Continuous Refresh* button on the watch window to enable continuous updates of values from the controller. Figure 4-13 illustrates the watch window.

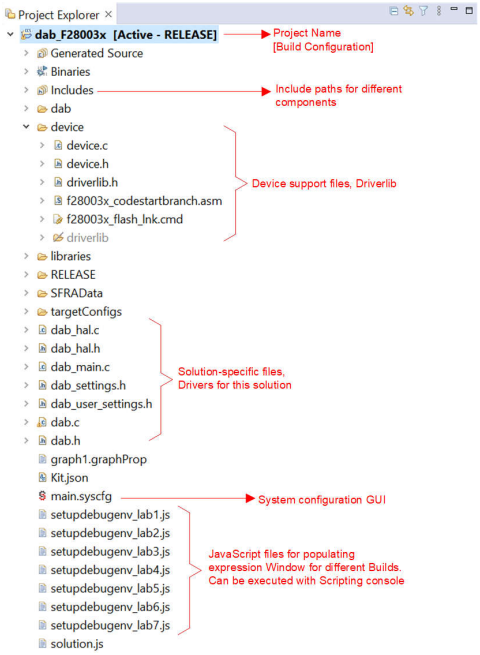


Figure 4-1. Project Explorer View

4.1.2.2 Pin Configuration

Table 4-1 shows the key signal connections between the TMS320F280039C control card and TIDA-010054 base board.

Table 4-1. Key Peripherals for Control of the Power Stage on the Board

SIGNAL NAME	DESCRIPTION	CONNECTION TO ControlCARD (HSEC PIN)
PWM-1A	Primary side leg-1 high side drive	GPIO-00 (49)
PWM-1B	Primary side leg-1 low side drive	GPIO-01 (51)
PWM-2A	Primary side leg-2 high side drive	GPIO-02 (53)
PWM-2B	Primary side leg-2 high side drive	GPIO-03 (55)
PWM-3A	Secondary side leg-1 high side drive	GPIO-04 (50)
PWM-3B	Secondary side leg-1 low side drive	GPIO-05 (52)
PWM-4A	Secondary side leg-2 high side drive	GPIO-06 (54)
PWM-4B	Secondary side leg-2 high side drive	GPIO-07 (56)
I_DC_PRI	Primary side DC current sense	ADC-C6 (14)
V_DC_PRI	Primary side voltage sense	ADC-B11 (24)
I_TANK_PRI	Primary tank current sense	ADC-B1 (25)
I_TANK_SEC	Secondary tank current sense	ADC-A6 (23)
IMON_MCU	Current monitor of eFuse	ADC-C9 (15)

Table 4-1. Key Peripherals for Control of the Power Stage on the Board (continued)

SIGNAL NAME	DESCRIPTION	CONNECTION TO ControlCARD (HSEC PIN)
ID_A	Hardware identification pin	ADC-A0 (9)
CLK_MOD	Clock output for delta sigma modulators	GPIO8 (57)
CLK_MOD_DELAYED	Delayed clock output for SDFM input to compensate propagation delay	GPIO9 (59) (output) GPIO49 (101) (input) GPIO51 (105) (input) GPIO55 (102) (input)
PWM_EN	Enable for PWM buffers	GPIO12 (58)
FAN_CTL	Enable pin for Fans	GPIO13 (60)
Prof_GPIO1	Profiling pin 1	GPIO14 (62)
Prof_GPIO2	Profiling pin 2	GPIO15 (64)
TEMP_SENSE	ECap input for temperature sensing (not implemented)	GPIO20 (68)
MUX_A0	Control signal 1 of TMUX1204 for selection of temperature signal (not implemented)	GPIO21 (70)
MUX_A1	Control signal 2 of TMUX1204 for selection of temperature signal (not implemented)	GPIO22(72)
$\overline{\text{DESAT\_PRI}}$	DESAT signal from primary side gate drivers	GPIO10 (61)
$\overline{\text{DESAT\_SEC}}$	DESAT signal from secondary side gate drivers	GPIO16 (67)
$\overline{\text{RST\_MCU}}$	Reset signal from MCU (not used)	GPIO11 (63)
RDY	Power good indicator form gate drivers	GPIO17 (69)
$\overline{\text{FLT\_PRI}}$	Fault signal for primary side current sensor	GPIO26 (79)
$\overline{\text{FLT\_SEC}}$	Fault signal for secondary side current sensor	GPIO27 (81)
DOUT_V_BATT_SEC	SDFM input D1	GPIO48 (99)
DOUT_V_DC_SEC	SDFM input D2	GPIO50 (101)
DOUT_I_DC_SEC	SDFM input D4	GPIO54 (100)

4.1.2.3 PWM Configuration

Up-down count mode is used to generate the PWMs for the primary and secondary legs of the dual active bridge. To use the high-resolution PWMs, the PRIM_LEG1_H PWM pulse is centered on the period event and the time base is configured to be up-down count. A complementary pulse with high-resolution dead time is then generated for the complementary switch. Between LEG1 and LEG2, there is a 180-degree phase shift for a full-bridge operation. This is achieved by using the feature on the PWM module to swap the xA and xB output. The PWM frequency for this application is 100 kHz. The TBPRD register is set to a value 500 in up-down count mode.

The duty cycle value is loaded in CMPA register of the EPWM base and is configured to generate 50% duty cycle. The action qualifier module outputs the required action for controlling the PWM output on a compare A event. The global link mechanism on the Type-4 PWM is used to reduce the number of cycles needed to update the registers and enables high-frequency operation. For example, the following code in the `DAB_HAL_setupPWM()` function links the TBPRD registers for all the PWM Legs.

Using this linkage, a single write to the PRIM_LEG1 TBPRD register writes the value to PRIM_LEG2, SEC_LEG1, and SEC_LEG2.

```
EPWM_setupEPWMLinks(DAB_PRIM_LEG2_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);

EPWM_setupEPWMLinks(DAB_SEC_LEG1_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);

EPWM_setupEPWMLinks(DAB_SEC_LEG2_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);
```

Figure 4-2. PWM Write

4.1.2.4 High-Resolution Phase Shift Configuration

High-resolution features used:

- High-Resolution Phase Shift
- High-Resolution Dead Band
- High-Resolution Duty → Not available, CTMODEB is set to 1
- High-Resolution Period → Not available, CTMODEB is set to 1

The PWM pulses of the secondary side are phase-shifted with respect to the PWM pulses of the primary. Controlling the phase shift enables transfer of power between the primary and secondary and vice versa. The maximum power transferred is very sensitive to the value of phase shift in a Dual Active Bridge. A small series inductor can lead to maximum power transfer at a small value of phase shift. Since the range over which the phase shift is going to be varied is small, and accurate control requires fine increment and decrement steps of phase. The phase control is implemented using Hi-Res (high resolution) feature of F28004x. The function `DAB_calculatePWMDutyPeriodPhaseShiftTicks()` inside ISR1 calculates the required the required high resolution phase control for both voltage and current mode control. This helps in handling sudden load changes smoothly without producing huge overshoots/transients in the current waveforms.

```
static inline void DAB_calculatePWMDutyPeriodPhaseShiftTicks(void)
{
...
   //
    // first the phase shift in pu is converter to ns
    // this is done for better debug and user friendliness
    //
    DAB_pwmPhaseShiftPrimSec_ns = DAB_pwmPhaseShiftPrimSec_pu *
            ((float32_t)1.0 / DAB_pwmFrequency_Hz) *
            (1 / ONE_NANO_SEC);

    //
    // next this ns is simply converted to ticks
    //
    DAB_pwmPhaseShiftPrimSec_ticks =
            (int32_t)((float32_t)DAB_pwmPhaseShiftPrimSec_ns *
                      DAB_PWMSYSCLOCK_FREQ_HZ * ONE_NANO_SEC *
                      TWO_RAISED_TO_THE_POWER_SIXTEEN) -
             ((int32_t)2 << 16);

    //
    // due to the delay line implementation depending on whether it is
    // a phase delay or an advance we need to adjust the
    // HR phase shift ticks calculations
    //
    if(DAB_pwmPhaseShiftPrimSec_ticks >= 0)
    {
        DAB_phaseSyncPrimToSecCountDirection = EPWM_COUNT_MODE_DOWN_AFTER_SYNC;

        //
        // DAB_pwmPhaseShiftPrimSec_ticks has the correct value already
        //
    }
    else
    {
        DAB_phaseSyncPrimToSecCountDirection =  EPWM_COUNT_MODE_UP_AFTER_SYNC;
        DAB_pwmPhaseShiftPrimSec_ticks = DAB_pwmPhaseShiftPrimSec_ticks * -1;

        DAB_pwmPhaseShiftPrimSec_HiResticks =  ((uint16_t) 0xFF - ((uint16_t)
                  (DAB_pwmPhaseShiftPrimSec_ticks & 0x0000FFFF)>>8));

        DAB_pwmPhaseShiftPrimSec_ticks = ((DAB_pwmPhaseShiftPrimSec_ticks & 0xFFFF0000) + 0x10000) +
                (DAB_pwmPhaseShiftPrimSec_HiResticks << 8);
    }
}
```

Figure 4-3. PWM Function 1

```
static inline void DAB_HAL_updatePWMDutyPeriodPhaseShift(uint32_t period_ticks,
                                uint32_t dutyAPrim_ticks,
                                uint32_t dutyASec_ticks,
                                uint32_t phaseShiftPrimSec_ticks,
                                uint16_t phaseShiftPrimSec_direction)
{
...
    EALLOW;
    HWREG(DAB_SEC_LEG1_PWM_BASE + HRPWM_O_TBPHS) = phaseShiftPrimSec_ticks;
    HWREG(DAB_SEC_LEG2_PWM_BASE + HRPWM_O_TBPHS) = phaseShiftPrimSec_ticks;
    EDIS;
}
```

Figure 4-4. PWM Function 2

The variable `DAB_phaseSyncPrimToSecCountDirection` is updated to control the forward mode or reverse mode of power flow.

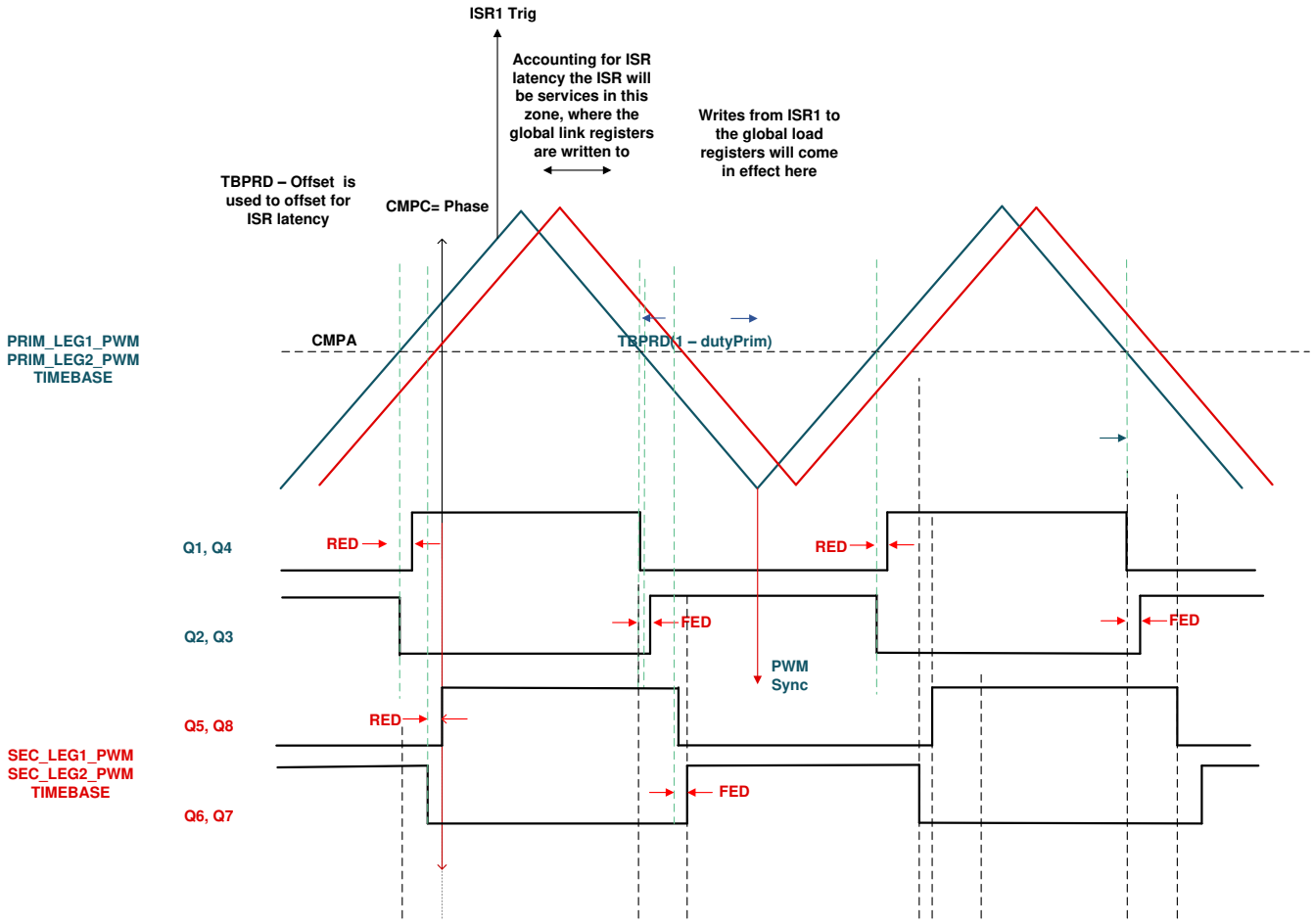


Figure 4-5. PWM Configuration

4.1.2.5 ADC Configuration

The configuration for ADC is done in the dab_main.c using the function `DAB_HAL_setupADC()`. The reference voltage, prescaling the clock and setting up SOC (start of conversions) for the voltage and current signals are done here. The trigger for ADC is generated from a start of conversion (SOC) signal from EPWM1. This configuration is done inside the function `DAB_HAL_setupTrigForADC()` in the `dab_main.c` file. All other settings mapping the HSEC card pin connector signals to the control card are done in the dab_settings.h file.

4.1.2.6 ISR Structure

The DAB project consists of two ISRs (ISR1 and ISR2) with ISR1 being the fastest and non-nestable ISR. ISR1 is reserved for the control loop and the PWM update. ISR1 is triggered by the PRIM_LEG1_PWM_BASE → EPWM_INT_TBCTR_U_CMPC event.

The following are the defines related to this ISR:

```
#define DAB_ISR1_PERIPHERAL_TRIG_BASE DAB_PRIM_LEG1_PWM_BASE
#define DAB_ISR1_TRIG INT_EPWM1
#define DAB_ISR1_PIE_GROUP INTERRUPT_ACK_GROUP3
#define DAB_ISR1_TRIG_CLA CLA_TRIGGER_EPWM1INT
```

ISR2 is triggered by CPU Timer INT which is initiated by an overflow on CPU timer. ISR2 runs the slew rate function for commanded references.

```
#define DAB_ISR2_TIMEBASE CLLLC_TASKC_CPUTIMER_BASE
#define DAB_ISR2_TRIG INT_TINT2
```

Additionally, CPU timers are used to trigger slow background tasks (these are not interrupt-driven but polled). "A" tasks are triggered at TASKA_FREQ, which is 100 Hz. The SFRA GUI must be called at this rate. One task, A1, is executed at this rate. "B" tasks are triggered at TASKB_FREQ, which is 10 Hz. These are used for some basic LED toggles and state machine items that are not timing-critical. Three tasks—B1, B2, and B3—are serviced by this.

Figure 4-6 illustrates the ISR software diagram.

Note

The EMAVG_RUN function is not used in the current software.

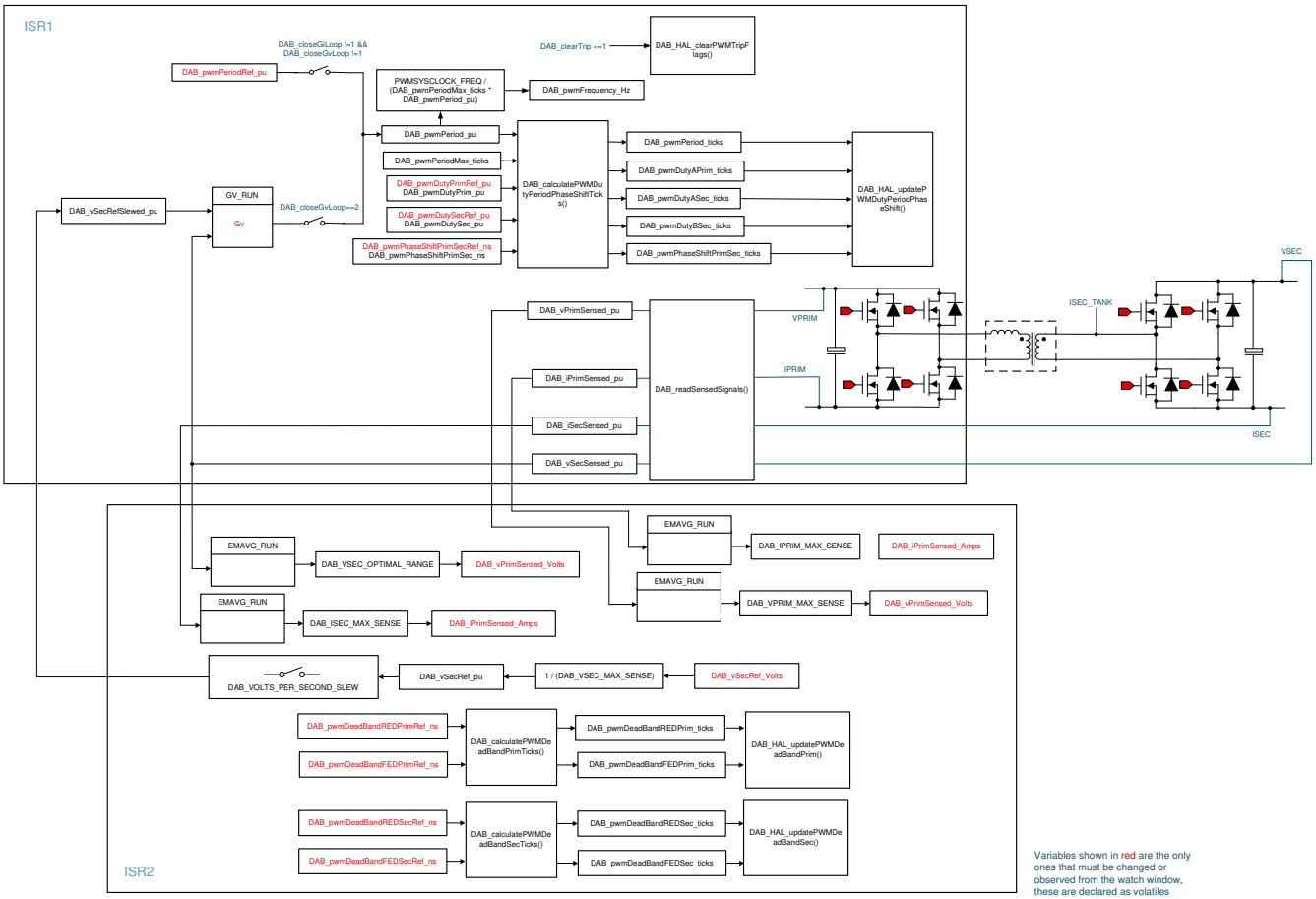


Figure 4-6. Software Diagram

Note

For extended phase shift control the variables `DAB_pwmEPSAlphaPRef_pu`, `DAB_pwmEPSAlphaP_pu`, `DAB_pwmEPSAlphaSRef_pu`, `DAB_pwmEPSAlphaS_pu`, `DAB_pwmEPSPhaseShift_P1_P2_ticks`, `DAB_pwmEPSPhaseShift_P1_S1_ticks` and `DAB_pwmEPSPhaseShift_P1_S2_ticks` are introduced. The functions `DAB_calculatePWMPhaseShift` ticks and `DAB_HAL_ipdatePWMDutyPeriodPhaseShift()` are modified accordingly.

4.2 Test Setup

To test the efficiency of this reference design, use the setup shown in Figure 4-7.

- 10-kW DC power supply: 800 V, 12.5 A
- 10-kW resistive load: 500 V, 20 A
- Auxiliary power supply to provide 12 V, 2 .5 A
- TMDSCNCD280039C control card
- Power Analyzer
- Oscilloscope with isolated probes for voltage and current
- 12-V fans to provide sufficient airflow to the heat sinks

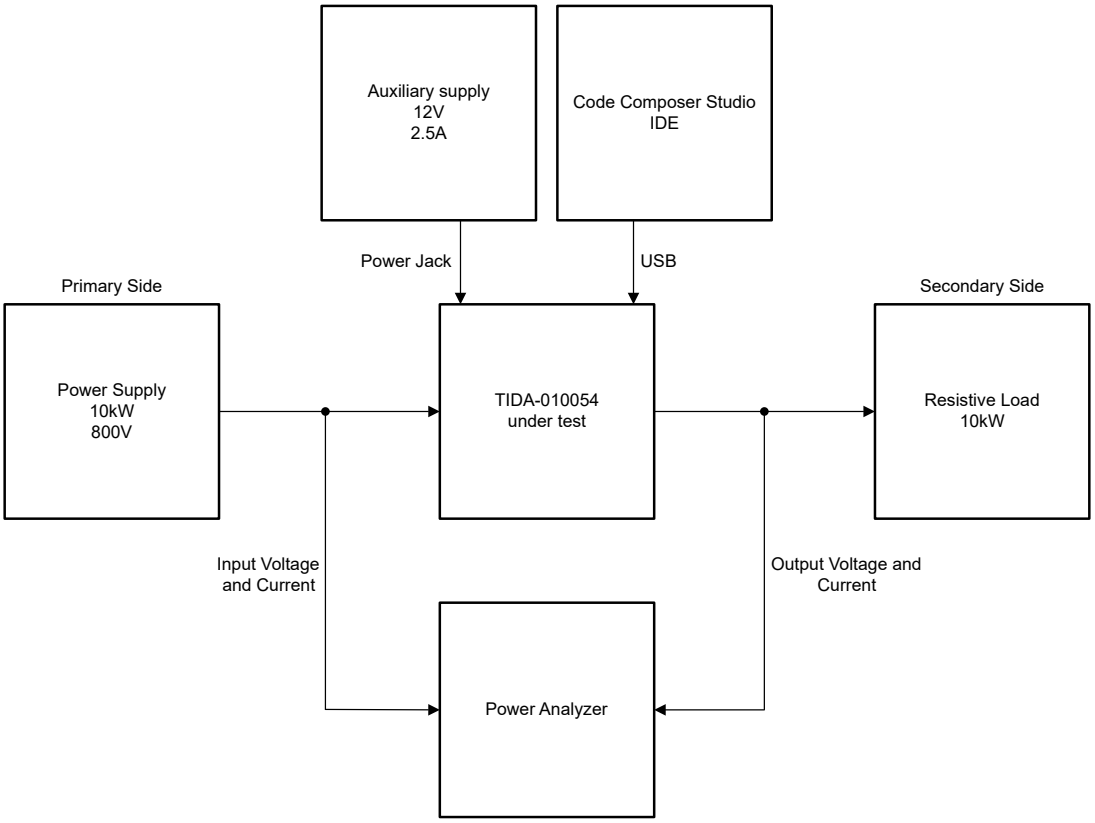


Figure 4-7. Test Setup

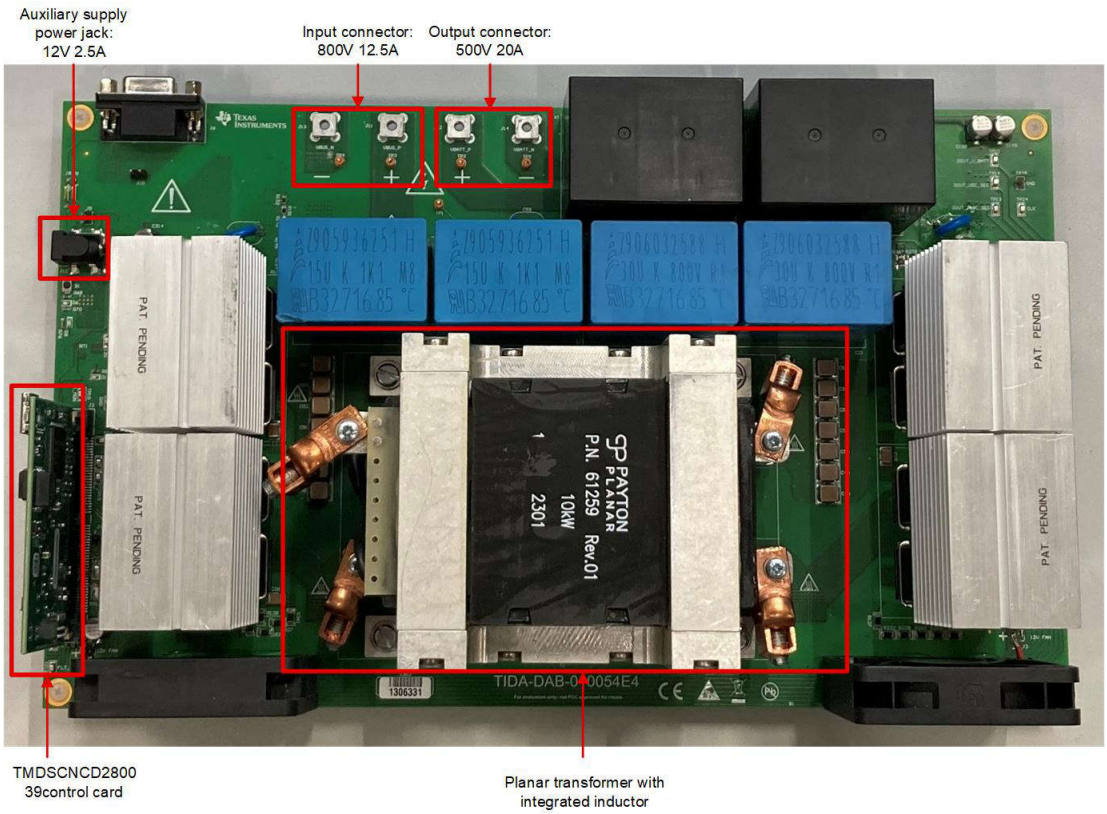


Figure 4-8. Board Image

Before powering the board to perform open-loop testing, use the following steps to set up the board:

1. Connect the terminals J11 and J13 to the input power supply and terminals J12 and J14 to the output load bank. Use a 4-mm^2 wire to make these connections so that the wire can handle high currents without getting heated quickly.
2. Connect the auxiliary power supply to terminal J15 using a PJ-002 female connector to power the controller, gate driver, and sense circuits

There is a cut-out area provided at the center of the board to mount the transformer. The transformer is directly connected to the board using M3 screws. Take care while mounting the transformer so that the primary and secondary sides are not interchanged.

The control card is programmed using a USB connection from the laptop to generate PWM pulses at 100 kHz. Once programmed, the auxiliary power supply is set to 12 V. Do not apply voltage across terminals J2 and J4. In this state the current consumption on the 12-V rail is supposed to be approximately 700 mA. This consumption increases after relays are closed and fans are enabled.

Connect two 12-V fans to the fan connectors J1 and J3. The polarity is marked on the PCB and in the schematics.

Follow Lab 1 to Lab 7 to get familiar with the design and provide proper operation.

CONNECTOR TERMINALS	FUNCTION	COMMENTS
J11–J13	Input high-voltage power supply	800-V DC power supply capable of sourcing 10-kW power
J12–J14	Output load terminals	10-kW resistive load bank is connected here
J15	Auxiliary power supply for gate driver, control card, and sense circuits	15-V DC power supply current limited to 700 mA
J2	TMDSCNCD280049C Control card	Insert the control card here
J6	CAN Connector	Not supported in current revision
J1, J3	Fan connector	12-V fan connectors for cooling

4.3 PowerSUITE GUI

PowerSUITE GUI was designed in this project for quick configuration of testing specifications. Figure 4-9 provides a detailed description of the PowerSUITE GUI. Open main.syscfg to configure the parameters for running various lab exercises.

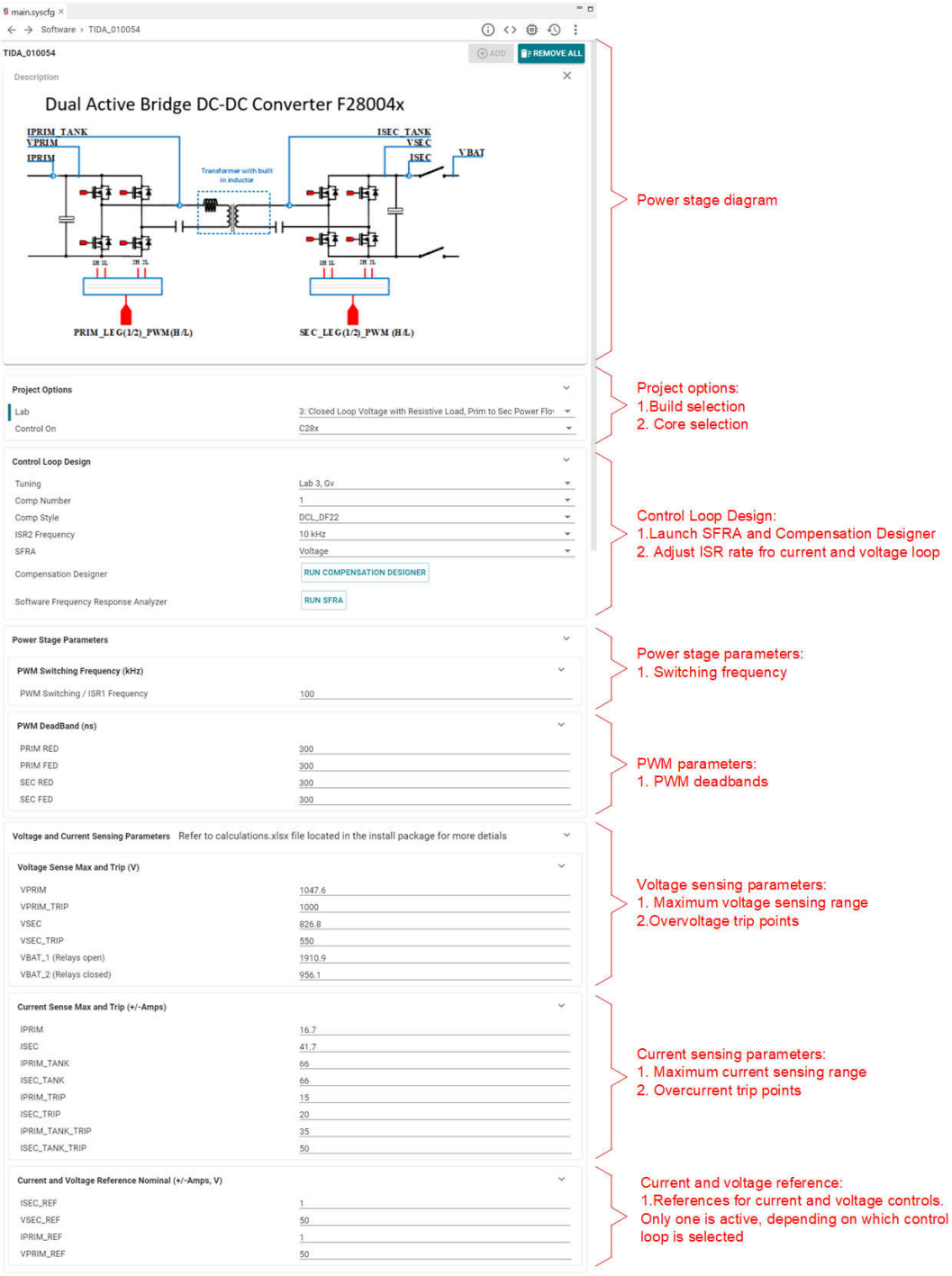


Figure 4-9. PowerSUITE GUI Description

4.4 LABs

The software of this reference design is organized in five labs. These tests simplify the system bringup and design.

Table 4-2. Summary of Labs

LAB		WHAT DOES THE LAB CHECK?	COMMENTS
1	PWM Check, Power Flow Prim→ Sec	Verify power transfer from primary to secondary. Check PWM frequencies and also check if Phase shift is working	
2	PWM Check, ADC check, Protection Check	Measure open loop plant for voltage and current. Check the feedback from Voltage and Current sensors. Make sure PWM signals are disabled while protection is enabled and trip flags are set.	Check the variable `DAB_clearTrip`
3	Closed Voltage Loop - Vsec	Run the voltage mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	DF22 compensator implemented. The feedback variable is `DAB_vSecSensed_pu`
4	Closed current loop → Isec	Run the current mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	PI compensator implemented. The feedback variable is `DAB_iSecSensed_pu`
5	Reverse power flow Sec→ Prim	Verify power transfer from secondary to primary. Check PWM frequencies and also if Phase shift is working	
6	Reverse power flow Sec→ Prim closed voltage loop	Run the voltage mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	DF22 compensator implemented. The feedback variable is `DAB_vPriSensed_pu`
7	Reverse power flow Sec→ Prim closed current loop	Run the current mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	PI compensator implemented. The feedback variable is `DAB_iPriSensed_pu`

4.4.1 Lab 1

Compile the project by selecting *Lab 1: Open Loop PWM* in the drop-down menu of *Project Options* from PowerSUITE GUI. This lab is intended to validate the PWM outputs and can be checked directly using the TIDA-010054 hardware (HW) or using the F2804X control card with a docking station.

Run the project by clicking the green run button in CCS.

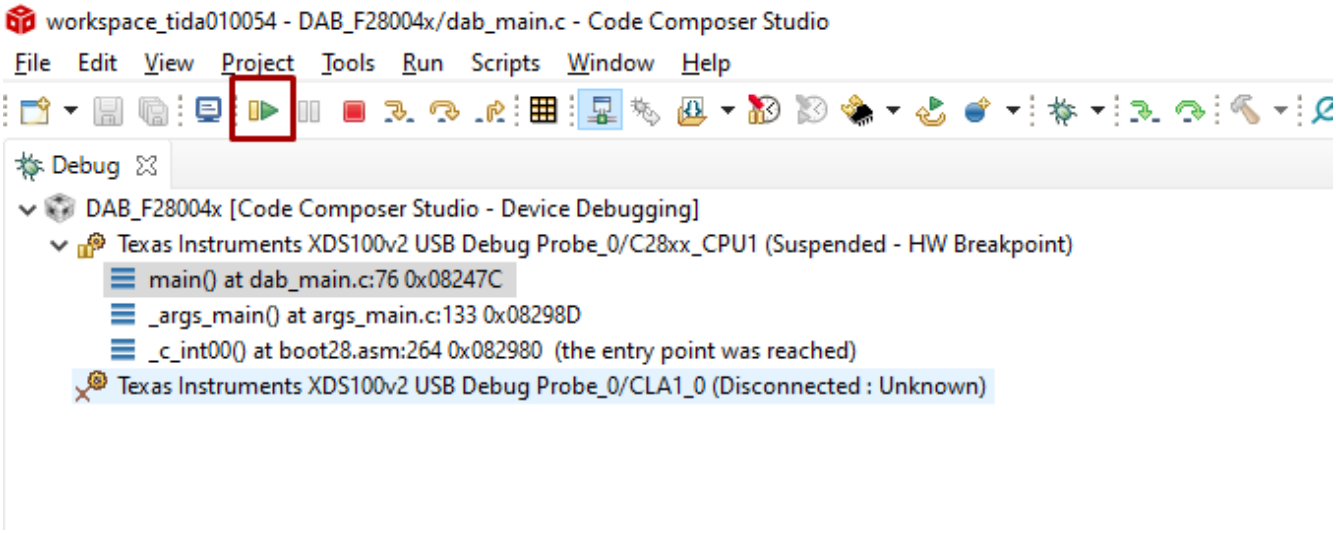


Figure 4-10. Run CCS

Populate the required variables in the watch window by loading JavaScript® `setupdebugenv_lab1.js` in the scripting console.

Figure 4-11. Loading Labs

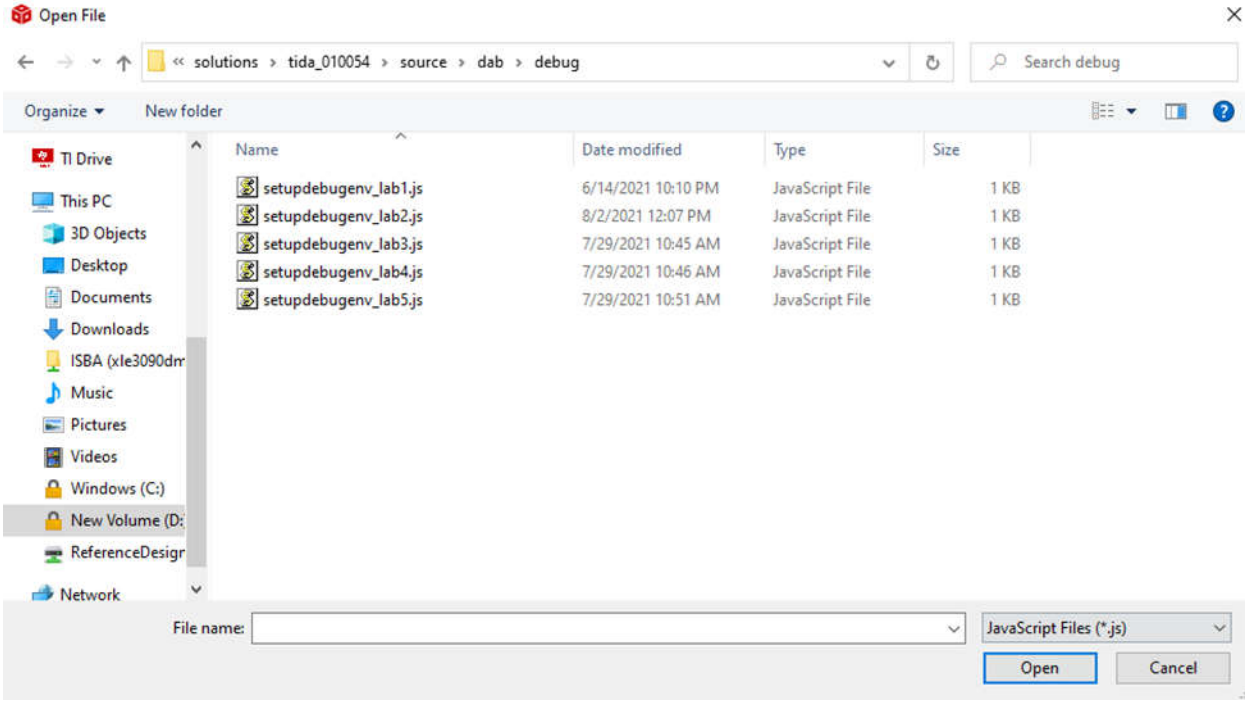


Figure 4-12. Select a Lab

1. After running the script, the watch window is populated with the variables in Figure 4-13.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusFAIL	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryCharging	0x0000800E@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	0	0x00008110@Data
DAB_enableRelay	long	0	0x0000810E@Data
DAB_pwmPhaseShiftPrimSecRef_pu	float	0.0199999996	0x00008120@Data
DAB_pwmPhaseShiftPrimSec_ns	float	199.999985	0x0000805E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
EPwm1Regs.TBPRD	Register	0x0258	
EPwm3Regs.TBPHS	Register	0x0015FF00	
EPwm1Regs.TZFLG	Register	0x0004	
isr1Ticker	long	6971065	0x0000F328@Data
isr2Ticker	long	697060	0x0000F32A@Data

Figure 4-13. Watch Window

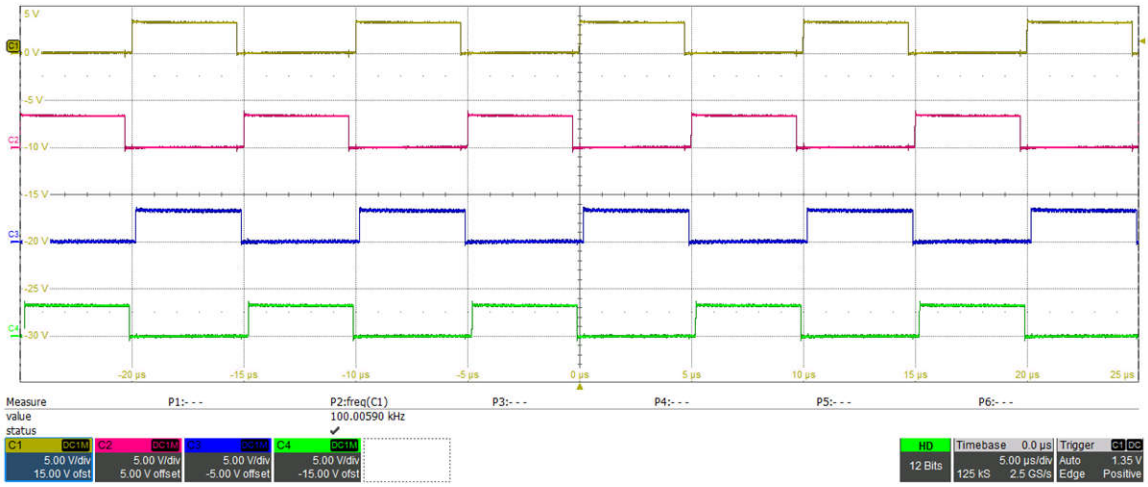
2. Enable *Continuous refresh* on the top right of the expression window.
3. Enable PWM by writing “1” to the `DAB_clearTrip` variable. (This variable resets to zero post writing and the normal.)

- **Pass criteria for Lab1**
  Connect probes on PWM1A (Q1), PWM1B (Q2), PWM3A(Q5), and PWM3B (Q6).

  1A and 1B are a complimentary pair, 3A is in sync with 1A with the specified phase shift, and the phase shift is controlled by the variable, DAB_pwmPhaseShiftPrimSecRef_pu.

  Check the following:

  1. Frequency is 100 kHz



PWM1A (yellow), PWM1B (red), PWM3A (blue), PWM3B (green)

Figure 4-14. 100 kHz PWM

  2. Now change the phase shift to 0.05 → 500 ns, to see more observable phase shift.

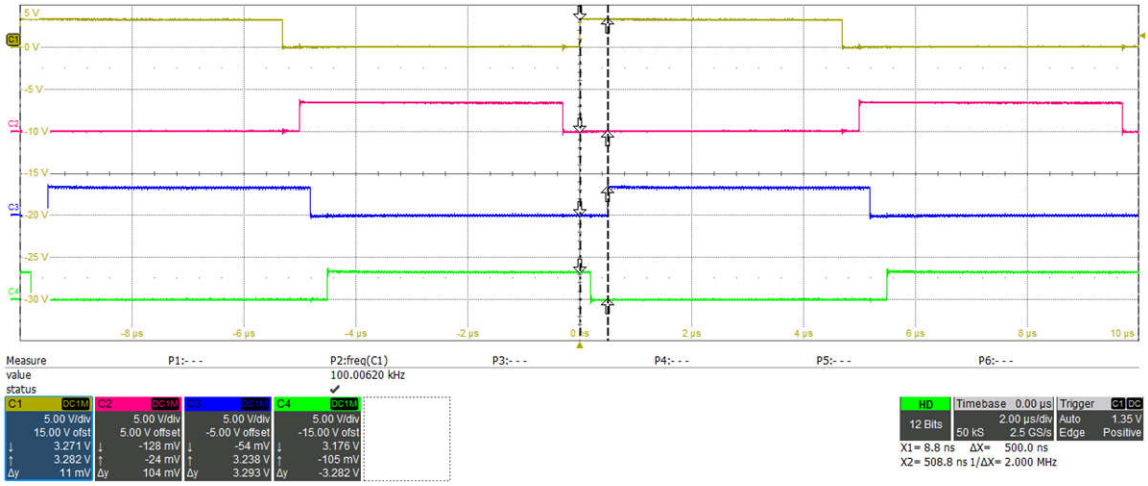
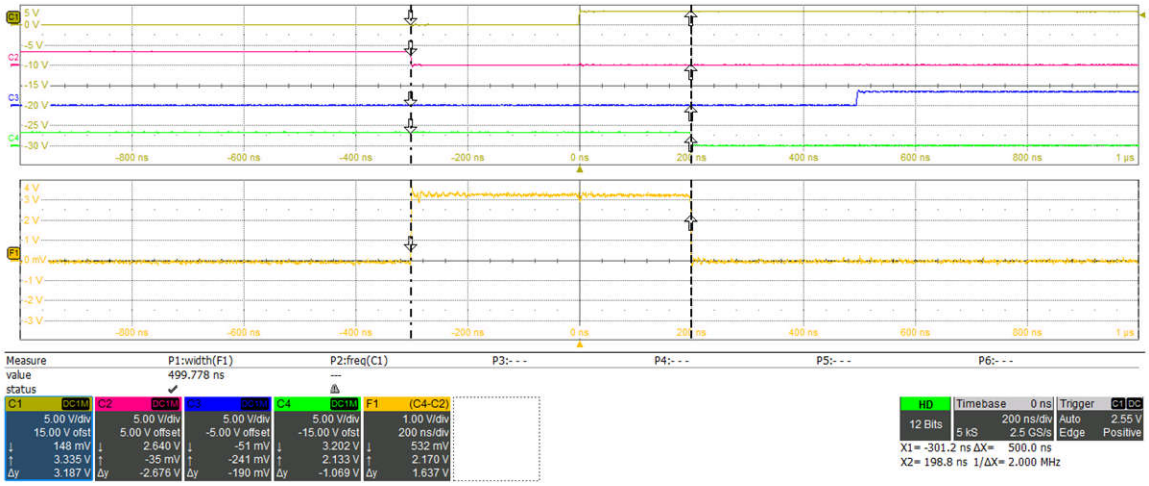


Figure 4-15. Phase Shift 500 ns

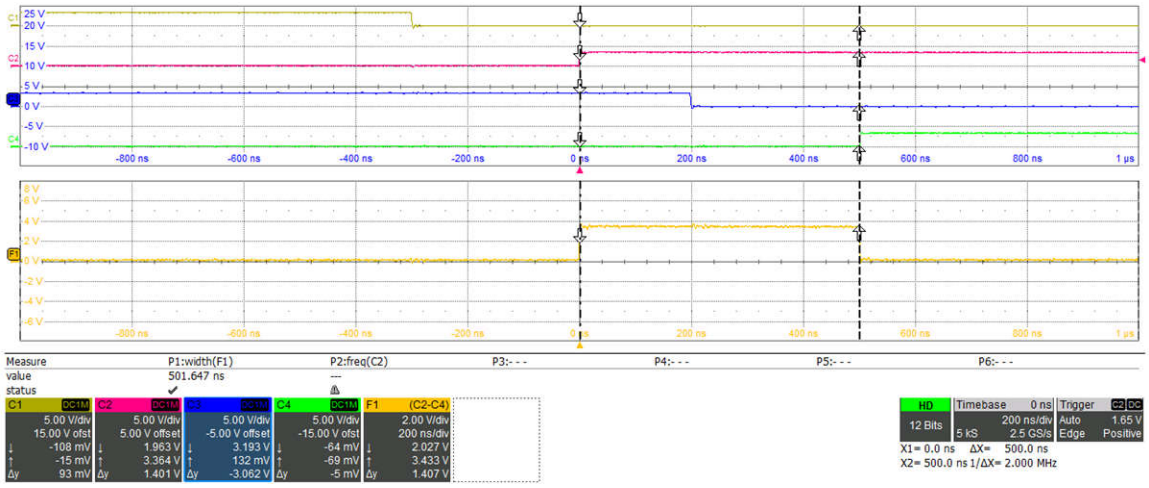
3. Verify on the oscilloscope, that the phase shift matches the specified value. To verify high-resolution operation select values which do not align with the system-clock, which means are not divisible by 10 ns. In Figure 4-16 and Figure 4-17, the phase shift is measured using the oscilloscope to be approximately 500 ns for 500-ns setpoint and approximately 502 ns for a 502-ns setpoint, a small jitter of approximately 1–2 ns can be the measurement error.

CAUTION
Phase shift is not recommended to be operated beyond 0.45 pu.



Phase shift is measured by using the math channel of the oscilloscope. The orange waveform is PWM3B – PWM1B. The width is equal to phase shift. The measured phase shift = 499.8 ns.

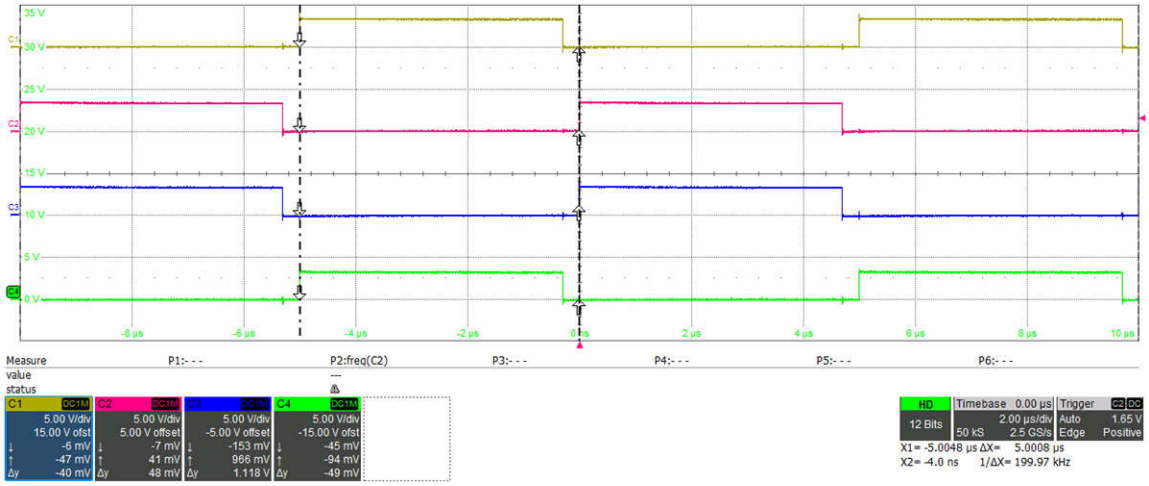
Figure 4-16. High-Resolution Phase Shift 500 ns



Phase shift is measured by using the math channel of the oscilloscope. The orange waveform is PWM3B – PWM1B. The width is equal to phase shift. The measured phase shift = 501.6 ns.

Figure 4-17. High Resolution Phase Shift 502 ns

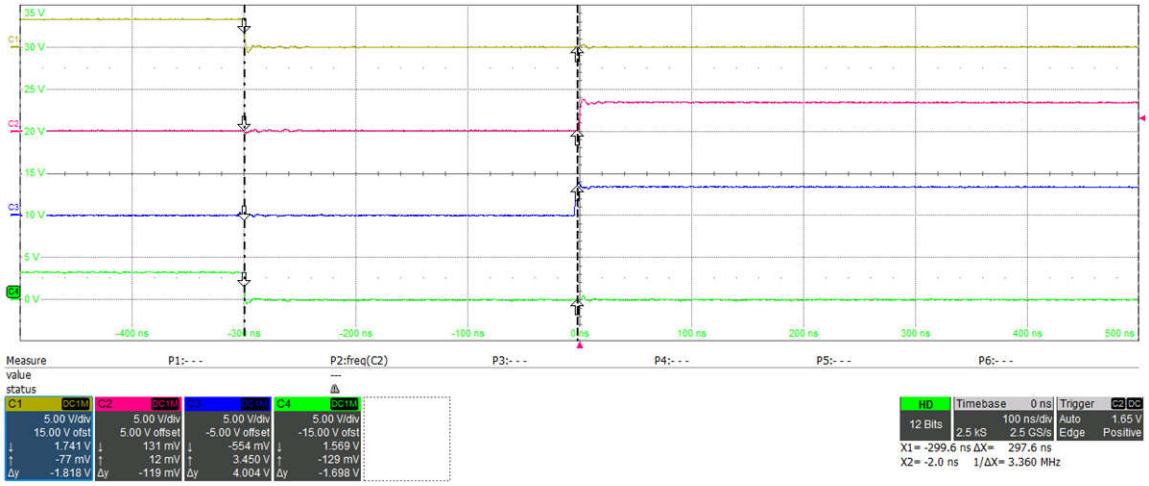
4. Change the PWM probes to PWM1A, PWM1B, PWM2A, and PWM2B.
   - Verify PWM1A and 2B are in sync and in phase
   - Verify PWM1B and 2A are in sync and in phase



PWM1A (yellow), PWM1B (red), PWM2A (green), PWM2B (blue)

Figure 4-18. PWM in Sync

5. Verify that they remain in sync and in phase as the phase shift for the secondary side PWM is changed.



PWM1A (yellow), PWM1B (red), PWM2A (green), PWM2B (blue)

Figure 4-19. PWM in Sync With Phase Shift

4.4.2 Lab 2

In the lab 2 build, the board is excited in open-loop fashion with a specified frequency (100 kHz) and phase shift. The phase shift can be changed through the watch window. The phase shift is controlled with the `DAB_pwmPhaseShiftPrimSec_pu` variable. This build verifies the sensing of feedback values from the power stage, operation of the PWM gate driver, HW protection, and makes sure there are no hardware issues. Additionally, calibrate the input and output voltage sensing in this build. For the HW test setup see Section 4.2.

- **Software Setup for Lab 2**

  The following defines are set in the `settings.h` file for this build. The settings can be defined by selecting *Lab 2: Open Loop PWM with Protection* in the drop-down menu of *Project Options* from PowerSUITE GUI.

```
#if DAB_LAB == 2
#define DAB_CONTROL_RUNNING_ON C28x_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
#define DAB_INCR_BUILD DAB_OPEN_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_SFRA_TYPE  DAB_SFRA_VOLTAGE
#if DAB_SFRA_TYPE == DAB_SFRA_CURRENT
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL3
#else
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
#endif
```

Figure 4-20. Lab 2 Software Setup

1. Run the project by clicking the green run button in CCS.
2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab2.js` in the scripting console.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unname...	openLoopCheck	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unname...	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unname...	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unname...	powerFlow_BatteryCharging	0x0000800E@Data
DAB_tripFlag.tripFlag	enum <unname...	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_pwmPhaseShiftPrimSecRef_pu	float	0.0199999996	0x00008120@Data
DAB_pwmPhaseShiftPrimSec_pu	float	0.0199999996	0x00008122@Data
DAB_vPrimSensed_Volts	float	400.011322	0x0000803C@Data
DAB_iPrimSensed_Amps	float	1.10083008	0x00008028@Data
DAB_vSecSensed_Volts	float	249.405045	0x00008078@Data
DAB_vBatSensed_Volts	float	249.215363	0x00008086@Data
DAB_iSecSensed_Amps	float	1.61314011	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.3340832	0x00008052@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_vSecSensed_pu	float	0.301643372	0x0000807A@Data
DAB_iSecSensed_pu	float	0.0388183594	0x0000806C@Data
isr1Ticker	long	8283494	0x0000F732@Data
isr2Ticker	long	828289	0x0000F734@Data

Figure 4-21. Lab 2 Watch View Configuration

3. In the watch view, check if the DAB_vPrimSensed_Volts, DAB_iPrimSensed_Amps, DAB_vSecSensed_Volts, and DAB_iSecSensed_Amps variables are updating periodically.

Note

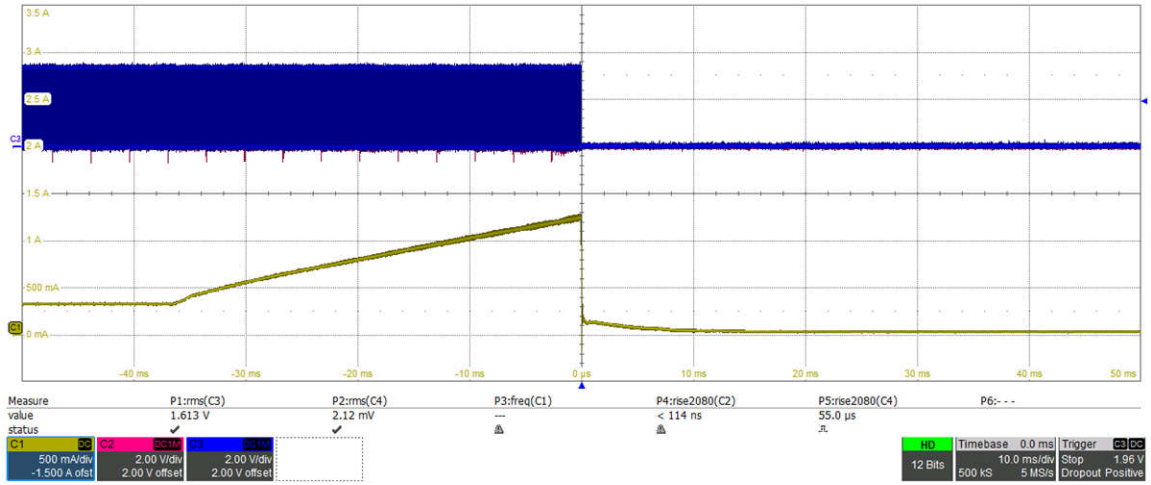
Because no power is applied at this point, these variables are close to zero.

- **Relay and fan validation**
  - In idle state the auxiliary 12-V power supply needs to consume approximately 700 mA.
  - Write a "1" to DAB_enableRelay. The typical clicking is usually audible and the current consumption needs to increase to approximately 1.14 A.
  - Write a "1" to DAB_enableFan. The fans start spinning and the current consumption increases to 1.43 A (here two CFM6015V-154-362 fans are used).
- **Power transfer validation**
  - Apply a low-input voltage (for example, 50 V)
  - Clear PWM trip by writing "1" into DAB_clear trip
  - Verify that voltage and current appear on the output
  - Phase shift can be varied by modifying DAB_pwmPhaseShuftPrimSecRef_pu

  By default, the DAB_pwmPhaseShiftPrimSec_pu variable is set to 0.02. Vary this phase shift slowly in steps of 0.002 pu and observe the change in voltage at the output of the converter. Make sure to not increase the phase shift very high as the phase shift can boost the output voltage greater than the input voltage and can lead to breakdown of MOSFETs at the maximum applied voltage.
- **Protection validation**

  Before actual high-voltage and high-power testing, validate the protection features. Validation can also be done at low voltages (for example, 50-V input). The limits for overcurrent and overvoltage protection can be modified from PowerSUITE GUI, see Figure 4-9.

1. **Primary overcurrent protection:**
   a. Set IPRIM_TRIP to 1 A
   b. Connect 50-V input voltage
   c. Enable relays and clear PWM
   d. Increase phase shift step by step to increase primary current
   e. Observe trip after 1 A is crossed

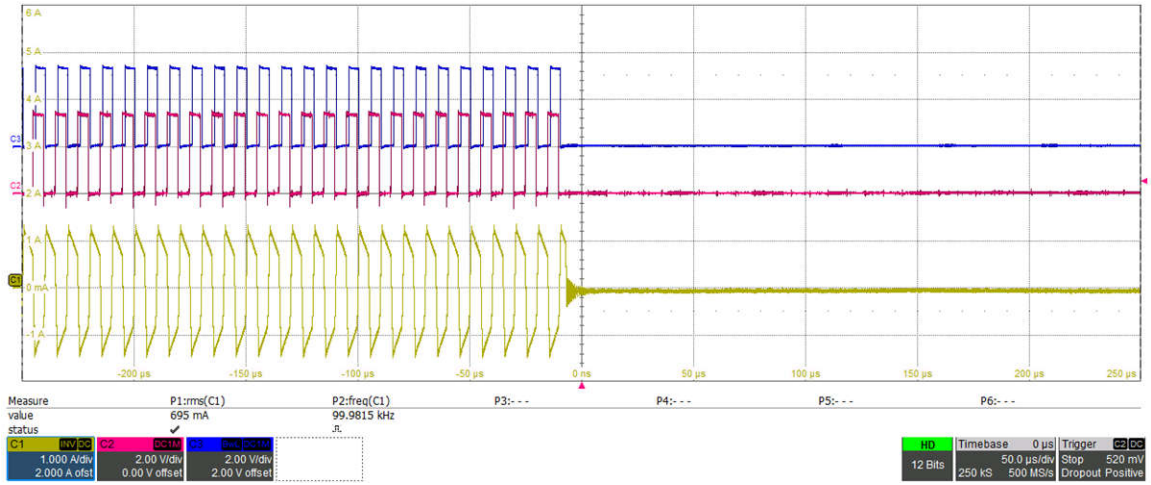


Primary - overcurrent protection, limit set = 1 A

Figure 4-22. Lab 2 - Primary Overcurrent Protection

2. **Primary tank overcurrent protection**
   a. Set IPRIM_TANK_TRIP to 1.5 A
   b. Connect 50-V input voltage
   c. Enable relays and clear PWM
   d. Increase phase shift step by step to increase primary tank current

e. Observe trip after 1.5 A is crossed



Primary - tank overcurrent protection, limit set = 1.5 A

Figure 4-23. Lab 2 - Primary Tank Overcurrent Protection

3. **Secondary overcurrent protection**
   a. Set ISEC_TRIP to 1.5 A
   b. Connect 50-V input voltage
   c. Enable relays and clear PWM
   d. Increase phase shift step by step to increase secondary current
   e. Observe trip after 1.5 A is crossed

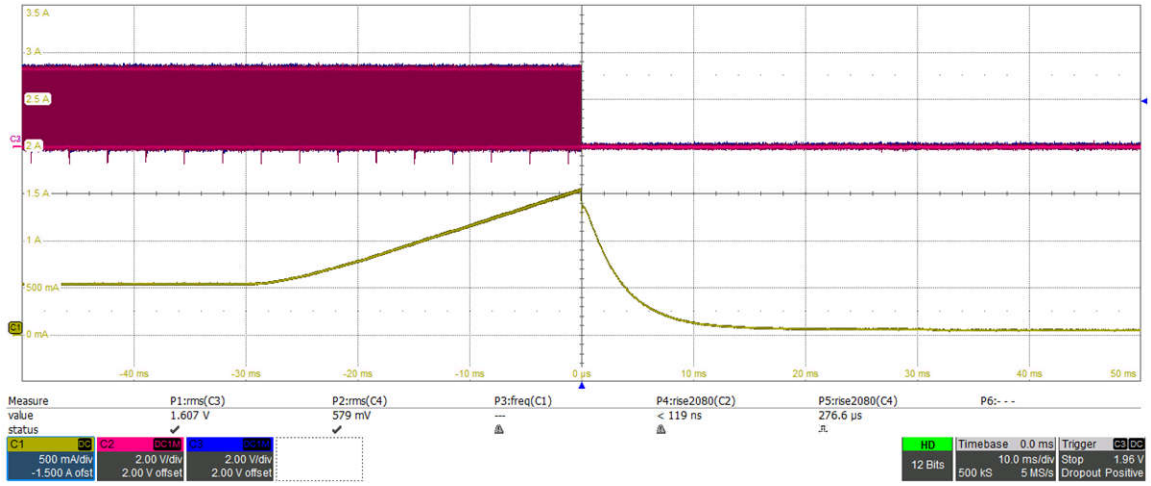


Figure 4-24. LAB 2 - Secondary Overcurrent Protection

4. **Secondary overvoltage protection**
   a. Set VSEC_TRIP to 40 V
   b. Connect 50-V input voltage
   c. Enable relays and clear PWM
   d. Increase phase shift step by step to increase secondary voltage
   e. Observe trip after 40 V is crossed

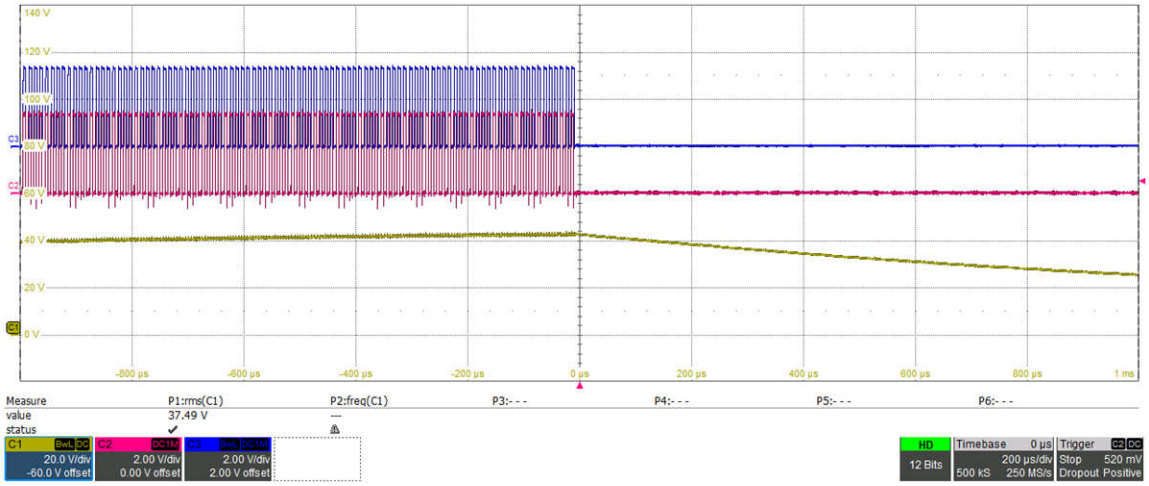


Figure 4-25. LAB 2 - Overvoltage Protection

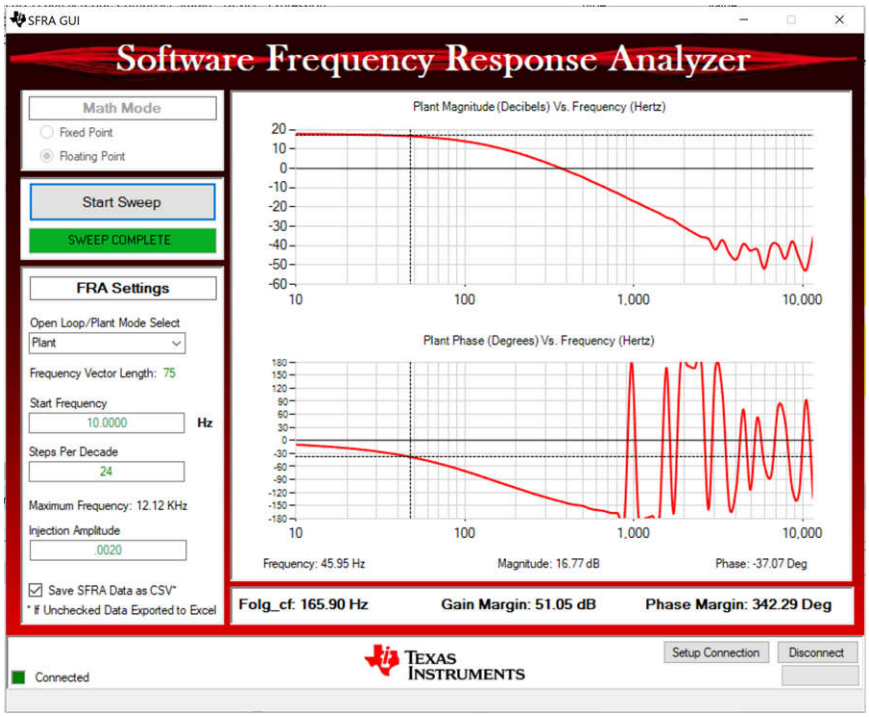
The previous waveforms show PWM is shut off by the comparator subsystem during fault events. The type of fault is displayed in the watch window through variable `DAB_tripFlag`, see Figure 4-26. The trip can be reset by selecting *noTrip* under the drop-down menu and re-enabling the PWM by writing "1" to the `DAB_clearTrip` variable. Make sure the fault condition is removed before re-enabling the PWM.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryCharging	0x0000800E@Data
DAB_tripFlag.tripFlag	enum <unnamed>	primOverCurrentTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_pwmPhaseShiftPrimSecRef_pu	float	0.129999995	0x00008120@Data
DAB_pwmPhaseShiftPrimSec_pu	float	0.129999995	0x00008122@Data
DAB_vPrimSensed_Volts	float	49.1062469	0x0000803C@Data
DAB_iPrimSensed_Amps	float	0.0244873054	0x00008028@Data
DAB_vSecSensed_Volts	float	-0.0567718484	0x00008078@Data
DAB_vBatSensed_Volts	float	0.131121814	0x00008086@Data
DAB_iSecSensed_Amps	float	0.00413589505	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.27593374	0x00008052@Data

Figure 4-26. Trip Indication in Expression Window

- **Measure SFRA Plant for Voltage Loop**
  1. The SFRA is integrated in the **C2000Ware-DigitalPower-SDK** kit to measure the plant response which can then be used to design a compensator. Run the SFRA by clicking on the SFRA icon. The SFRA GUI opens.
  2. Select the options for the device on the SFRA GUI; for example, for F280039, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click the *Connect* button.
  3. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking the *Start Sweep* button. The complete SFRA sweep takes a few minutes to complete. Monitor the activity in the progress bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.



Test Condition: V_{IN} = 800 V, V_{OUT} = 500 V, I_{OUT} = 10 A, phase shift = 0.047 pu.
Noise in the phase plot is expected for higher frequencies due to noise in the output voltage measurement and small plant gain.

Figure 4-27. Lab 2 SFRA Plant Plot for the Open Voltage Loop Test

4. The Frequency Response Data `SFRA.csv` is saved in the project folder, under an SFRA Data Folder, and is time-stamped with the time of the SFRA run. SFRA can be run at different frequency setpoints to cover the range of operation of the system. A compensator is designed using these measured plots through compensator designer. Compensation designer can be opened from the main.syscfg GUI.

   Inside ISR1, the SFRA injects small signal perturbations in phase and observes the sensed output voltage variations. The following lines of code inside the dab.h file perform the SFRA signal injection and collection.

```
            #else
                DAB_pwmPeriod_pu = DAB_pwmPeriodRef_pu;
                DAB_pwmPhaseShiftPrimSec_pu =
                        DAB_SFRA_INJECT(DAB_pwmPhaseShiftPrimSecRef_pu);
            #endif

#else
    DAB_SFRA_COLLECT((float32_t*)&DAB_pwmPhaseShiftPrimSec_pu ,
                (float32_t*)&DAB_vSecSensed_pu);
#endif
```

Figure 4-28. Lab 2 Code for SFRA Signal Injection

- **Measure SFRA Plant for Current Loop**
  1. Follow the same steps as in voltage loop to get started with SFRA measurement for current loop.
  2. In the PowerSUITE GUI under SFRA tab, choose *current* prior to running the SFRA current loop.

```
#define DAB_SFRA_TYPE   DAB_SFRA_CURRENT
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL3
```

Figure 4-29. Lab 2 Code Defines SFRA Current Loop

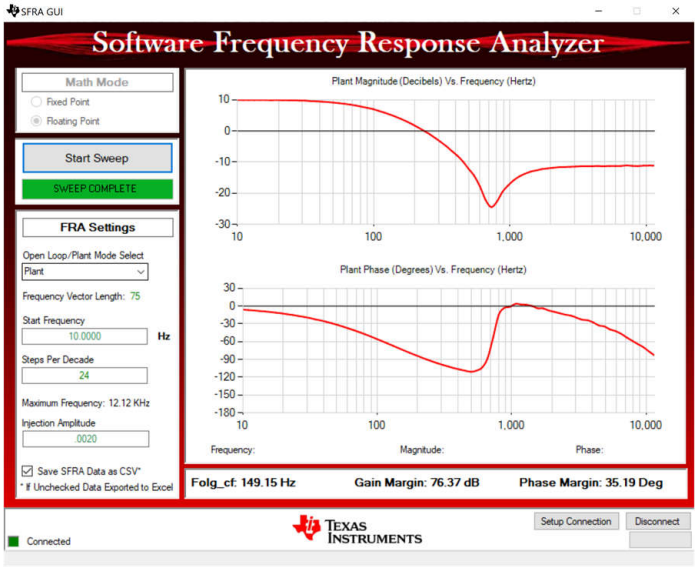
3. Inside ISR1, the SFRA injects small signal perturbations in phase and observes the sensed output current variations. The following lines of code inside the dab.h file perform the SFRA signal injection and collection.

```
        #else
            DAB_pwmPeriod_pu = DAB_pwmPeriodRef_pu;
            DAB_pwmPhaseShiftPrimSec_pu =
                    DAB_SFRA_INJECT(DAB_pwmPhaseShiftPrimSecRef_pu);
        #endif

#if DAB_SFRA_TYPE != DAB_SFRA_DISABLED
    #if DAB_SFRA_TYPE == DAB_SFRA_CURRENT
        DAB_SFRA_COLLECT((float32_t *)&DAB_pwmPhaseShiftPrimSec_pu,
                         (float32_t *)&DAB_iSecSensed_pu);
```

Figure 4-30. Lab 2 Code for SFRA Signal Injection

4. Measure the plant response from SFRA GUI. The open loop and plant response are stored in the file named `SFRA.csv`. Use this file to tune the compensator for the current loop.



Test Condition: V_{IN} = 800 V, V_{OUT} = 500 V, I_{OUT} = 10 A, phase shift = 0.047 pu

Figure 4-31. Lab 2 SFRA Plant Plot for the Open Current Loop Test

4.4.3 Lab 3

In Lab 3, the converter is run in secondary voltage close-loop configuration (`DAB_vSecSensed_Volts`).

This lab runs the voltage mode compensator, obtains the open-loop transfer function of plant from SFRA, and runs the design compensator for the plant in the compensator design tool.

Launch the compensation designer which prompts the selection of a valid SFRA data file. Import the SFRA data from the run in Lab 2 into the compensation designer to design a 2P2Zcompensator. Keep more margins during this iteration of the design to make sure that when the loop is closed, the system is stable. The following coefficient values are hard-coded in the software. The compensation designer GUI gives information about the stability of the loop, gain margin, phase margin, and bandwidth of the loop. The coefficients can be modified in the compensation designer GUI.

```
#define DAB_GV_2P2Z_A1 ((float32_t) -1.8756666)
#define DAB_GV_2P2Z_A2 ((float32_t) 0.8756666)
#define DAB_GV_2P2Z_B0 (float32_t) 1.4329852)
#define DAB_GV_2P2Z_B1 ((float32_t) -2.7994568)
#define DAB_GV_2P2Z_B2 (float32_t) 1.3664965)
```

- **Test Setup for Lab 3 (Closed Voltage Loop - Sec)**

  Compile the project by selecting *Lab 3: Closed Loop Voltage with Resistive Load* in the drop-down menu of *Project Options* from PowerSUITE GUI. Make sure current and voltage limits are set per operating conditions.

  ```
  #if DAB_LAB == 3
  #define DAB_CONTROL_RUNNING_ON C28X_CORE
  #define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
  #define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
  #define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
  #define DAB_PROTECTION DAB_PROTECTION_ENABLED
  #define DAB_CONTROL_MODE DAB_VOLTAGE_MODE
  #define DAB_SFRA_TYPE 2
  #define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
  #endif
  ```

  Use the following steps to run voltage close loop:

  1. Run the project by clicking the green run button in CCS.
  2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab3.js` in the scripting console.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unname...	closedLoopCheck_Voltage	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unname...	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unname...	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unname...	powerFlow_BatteryCharging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	0.0199999996	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unname...	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGvLoop	long	0	0x0000810A@Data
DAB_vSecRef_Volts	float	50.0	0x00008080@Data
DAB_vPrimSensed_Volts	float	50.1292953	0x0000803C@Data
DAB_iPrimSensed_Amps	float	0.032617189	0x00008028@Data
DAB_vSecSensed_Volts	float	0.0252319332	0x00008078@Data
DAB_vBatSensed_Volts	float	-0.0146112442	0x00008086@Data
DAB_iSecSensed_Amps	float	-0.00286331191	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.22160268	0x00008052@Data
isr1Ticker	long	2892989	0x0000F732@Data
isr2Ticker	long	289284	0x0000F734@Data

Figure 4-32. Lab 3 - Watch View Configuration

3. Enable fans and relays by writing "1" into `DAB_enableFan` and `DAB_enableRelay`.
4. Enable PWM by writing “1” to the `DAB_clearTrip` variable.
5. In the watch view, check if the `DAB_vPrimSensed_Volts`, `DAB_iPrimSensed_Amps`, `DAB_vSecSensed_Volts`, and `DAB_iSecSensed_Amps` variables are updating periodically.
6. Set the output voltage by writing to `DAB_vSecRef_Volts` (in this example 50Vdc).
7. Enable closed loop operation by writing “1” to the `DAB_closeGvLoop` variable. The controller automatically adjusts the phase shift , depending upon the operating conditions to generate secondary output voltage to match with that of `DAB_vSecRef_Volts`.

Note

In the software the maximum phase shift is limited to 0.13 as a safety precaution. Adjust the primary voltage to stay within the phase shift limits and still generate the required secondary voltage.

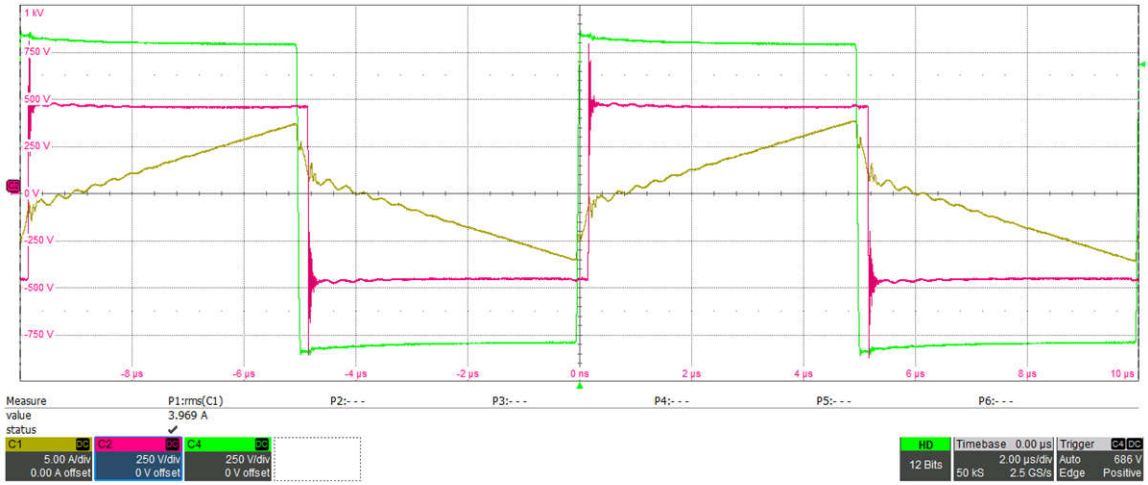
8. Slowly increase the input VPRIM DC voltage and adjust `DAB_vSecRef_Volts` accordingly, to reach to the required operating point.
9. Test the closed-loop operation by varying `DAB_vSecRef_Volts` from 400 V to 500 V. Observe that the `DAB_vSecSensed_Volts` tracks this command reference.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unname...	closedLoopCheck_Voltage	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unname...	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unname...	pwmSwState_singlePhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unname...	powerFlow_BatteryCharging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	-0.00698885322	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unname...	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGvLoop	long	1	0x0000810A@Data
DAB_vSecRef_Volts	float	450.0	0x00008080@Data
DAB_vPrimSensed_Volts	float	802.068726	0x0000803C@Data
DAB_iPrimSensed_Amps	float	2.7235353	0x00008028@Data
DAB_vSecSensed_Volts	float	449.89798	0x00008078@Data
DAB_vBatSensed_Volts	float	449.754761	0x00008086@Data
DAB_iSecSensed_Amps	float	4.64485645	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.31840086	0x00008052@Data
isr1Ticker	long	49549774	0x0000F732@Data
isr2Ticker	long	4954574	0x0000F734@Data

Figure 4-33. Lab 3 - Closed Voltage Loop Expression Window

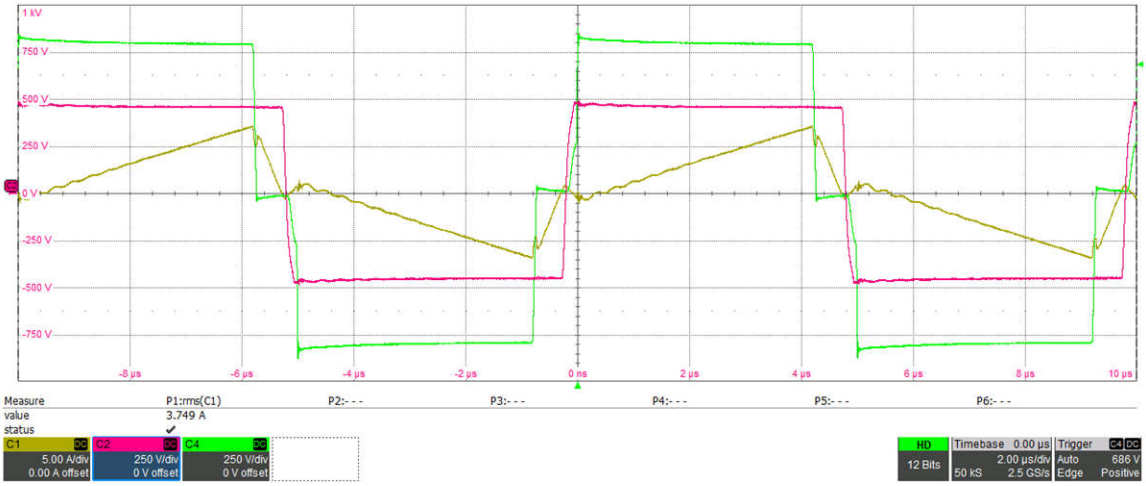
10. The control scheme can be changed between single phase shift SPS and extended phase shift EPS, by selecting the according variable in the *DAB_pwmSwState.pwmSwState* drop down.



Primary side switch node voltage (green), secondary side switch node voltage (red), inductor current (yellow)
Test condition: V_{IN} = 800 V, V_{OUT} = 450 V, I_{OUT} = 6.5 A

Figure 4-34. Lab 3 - Waveforms in Single Phase Shift Control (SPS)

Figure 4-34 shows that secondary side is hard-switching in this condition with SPS control.



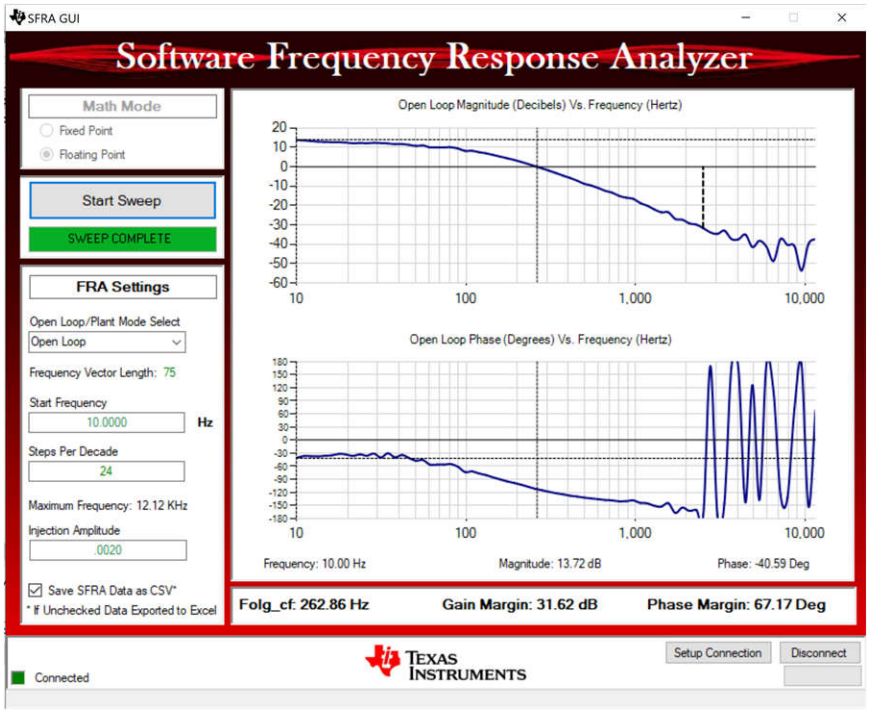
Primary side switch node voltage (green), secondary side switch node voltage (red), inductor current (yellow)
Test condition: V_{IN} = 800 V, V_{OUT} = 450 V, I_{OUT} = 6.5 A

Figure 4-35. Lab 3 - Waveforms in Extended Phase Shift Control (EPS)

The additional phase shift on the primary side introduced with EPS control is seen in Figure 4-35. Here both the primary side and the secondary side are soft-switching.

- **Frequency response of closed loop voltage**
  1. Run the SFRA by clicking on the SFRA icon. The SFRA GUI opens.
  2. Select the options for the device on the SFRA GUI; for example, for F280039, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click the *Connect* button.
  3. The SFRA GUI connects to the device. An SFRA sweep can now be started by clicking the *Start Sweep* button. The complete SFRA sweep takes a few minutes to finish. Monitor the activity in the progress bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.

     The bode plot in Figure 4-36 is captured using a DF22 compensator.



Test condition: V_{IN}= 800 V, V_{OUT} = 500 V, I_{OUT} = 10 A, SFRA amplitude = 0.002

Figure 4-36. Lab 3 - SFRA Open Loop Plot for the Closed Voltage Loop

4.4.4 Lab 4

- **Test Setup for Lab 4 (Closed Current Loop - Isec)**

  Compile the project by selecting *Lab 4: Closed Loop Current with Resistive Load* in the drop-down menu of *Project Options* from PowerSUITE GUI. Make sure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 4
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
#define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE DAB_CURRENT_MODE
#define DAB_SFRA_TYPE 1
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL1
#endif
```

1. Run the project by clicking the green run button in CCS.
2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab4.js` in the scripting console.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryCharging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	0.0199999996	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGiLoop	long	0	0x00008108@Data
DAB_iSecRef_Amps	float	1.0	0x00008134@Data
DAB_vPrimSensed_Volts	float	49.1062469	0x0000803C@Data
DAB_iPrimSensed_Amps	float	0.032617189	0x00008028@Data
DAB_vSecSensed_Volts	float	-0.100927733	0x00008078@Data
DAB_vBatSensed_Volts	float	0.0729446411	0x00008086@Data
DAB_iSecSensed_Amps	float	0.00509033212	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.29514766	0x00008052@Data
isr1Ticker	long	6646069	0x0000F638@Data
isr2Ticker	long	664562	0x0000F63A@Data

Figure 4-37. Lab 4 Watch View Configuration

3. Enable fans and relays by writing "1" into `DAB_enableFan` and `DAB_enableRelay`.
4. Enable PWM by writing “1” to the `DAB_clearTrip` variable.
5. In the watch view, check if the `DAB_vPrimSensed_Volts`, `DAB_iPrimSensed_Amps`, `DAB_vSecSensed_Volts`, and `DAB_iSecSensed_Amps` variables are updating periodically.
6. Set the output current by writing to `DAB_iSecRef_Amps` (in this example 1Adc).
7. Enable closed loop operation by writing “1” to the `DAB_closeGiLoop` variable. The controller automatically adjusts the phase shift depending upon the operating conditions to generate secondary output current to match with that of `DAB_iSecRef_Amps`.

Note

In the software, the maximum phase shift is limited to 0.13 as a safety precaution. Please adjust the primary voltage to stay within the phase shift limits and still generate the required secondary current.

8. Now, slowly increase the input VPRIM DC voltage and adjust `DAB_iSecRef_Amps` accordingly to reach to the required operating point.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryCharging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	0.0318166986	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGiLoop	long	1	0x00008108@Data
DAB_iSecRef_Amps	float	5.0	0x00008134@Data
DAB_vPrimSensed_Volts	float	800.022644	0x0000803C@Data
DAB_iPrimSensed_Amps	float	3.45742202	0x00008028@Data
DAB_vSecSensed_Volts	float	514.548523	0x00008078@Data
DAB_vBatSensed_Volts	float	514.055481	0x00008086@Data
DAB_iSecSensed_Amps	float	4.9913888	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.32975698	0x00008052@Data
isr1Ticker	long	19356168	0x0000F638@Data
isr2Ticker	long	1935466	0x0000F63A@Data

Figure 4-38. Lab 4 - Expression Window Closed Current Loop

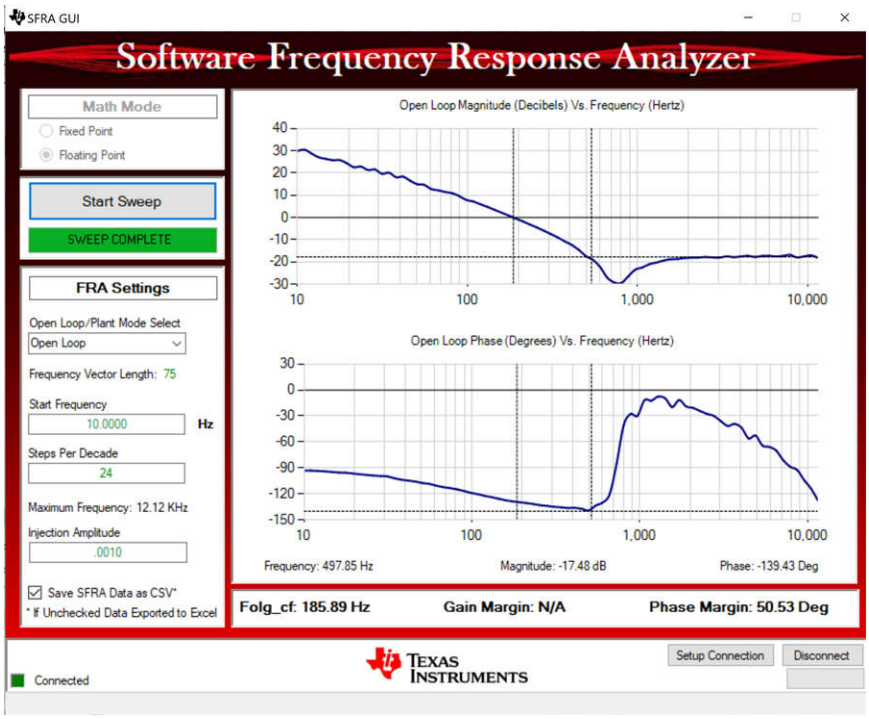
CAUTION

Make sure the secondary current is limited to a safe value depending upon the output load. High-impedance load can lead to dangerous secondary voltage which can destroy the board. Make sure secondary overvoltage protection is enabled and the threshold is set to a safe value.

```
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_VSEC_TRIP_LIMIT ((float32_t)500)
#define DAB_BOARD_PROTECTION_VSEC_OVERVOLTAGE 1
```

- **Frequency response of closed loop current**
  1. Run the SFRA by clicking on the SFRA icon. The SFRA GUI opens.
  2. Select the options for the device on the SFRA GUI; for example, for F280039, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click *Connect*.
  3. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking *Start Sweep*. The complete SFRA sweep takes a few minutes to finish. Monitor the activity in the progress bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.

     The plot in Figure 4-39 is captured with the PI compensator (gain of 0.5).



Test condition: V_{IN}= 800 V, V_{OUT} = 500 V, I_{OUT} = 10 A, SFRA amplitude = 0.002

Figure 4-39. Lab 4 SFRA Open Loop Plot for the Closed Current Loop

```
#define DAB_GI_KP (float32_t) 0.5
#define DAB_GI_KI (float32_t) 0.0063030
#define DAB_GI_UMAX (float32_t) 0.13
#define DAB_GI_UMIN (float32_t) -0.13
#define DAB_GI_IMAX (float32_t) 2.0
#define DAB_GI_IMIN (float32_t) -2.0
```

4.4.5 Lab 5

Figure 4-40 shows test setup for lab 5 (Open Loop voltage - Reverse power flow).

In this setup, the DC source is connected to the secondary side and the resistive load is connected to the primary side.

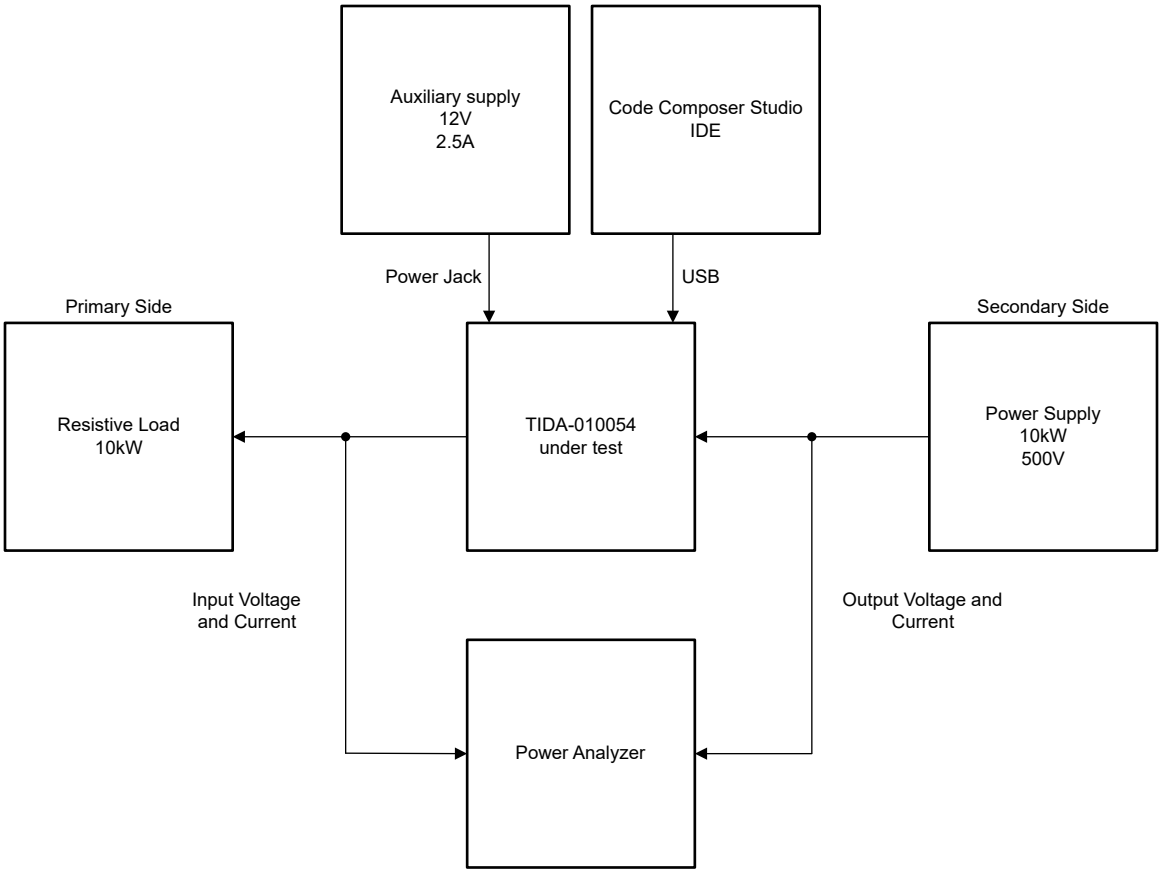


Figure 4-40. Lab 5 Test Setup

Compile the project by selecting *Lab 5: Open Loop PWM, Sec to Prim Power Flow* in the drop-down menu of *Project Options* from PowerSUITE GUI. Make sure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 5
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_SEC_PRI
#define DAB_INCR_BUILD DAB_OPEN_LOOP_BUILD
#define DAB_CONTROL_MODE  DAB_VOLTAGE_MODE
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_SFRA_TYPE  2
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
```

1. Run the project by clicking the green run button in CCS.
2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab5.js` in the scripting console.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryDischarging	0x0000800E@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSecRef_pu	float	-0.0199999996	0x00008120@Data
DAB_vPrimSensed_Volts	float	-2.0460937	0x0000803C@Data
DAB_iPrimSensed_Amps	float	0.0244628917	0x00008028@Data
DAB_vSecSensed_Volts	float	49.8353882	0x00008078@Data
DAB_vBatSensed_Volts	float	49.9160156	0x00008086@Data
DAB_iSecSensed_Amps	float	0.00222702022	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.28746212	0x00008052@Data
DAB_pwmPhaseShiftPrimSec_pu	float	-0.0199999996	0x00008122@Data

Figure 4-41. Lab 5 - Watch View

3. Enable fans and relays by writing "1" into `DAB_enableFan` and `DAB_enableRelay`.
4. Enable PWM by writing “1” to the `DAB_clearTrip` variable.
5. Vary phase shift slowly in steps of 0.002 pu by writing to `DAB_pwmPhaseShiftPrimSec_pu` and observe the change in voltage at the output of converter.

Note

The negative sign in the phase shift value is required for the reverse power flow.

6. Before increasing voltages validate primary side overvoltage protection.
7. Set VPRIM_TRIP to 50 V.
8. Slowly increase (negative) phase shift and observe trip when voltage hits 50 V.

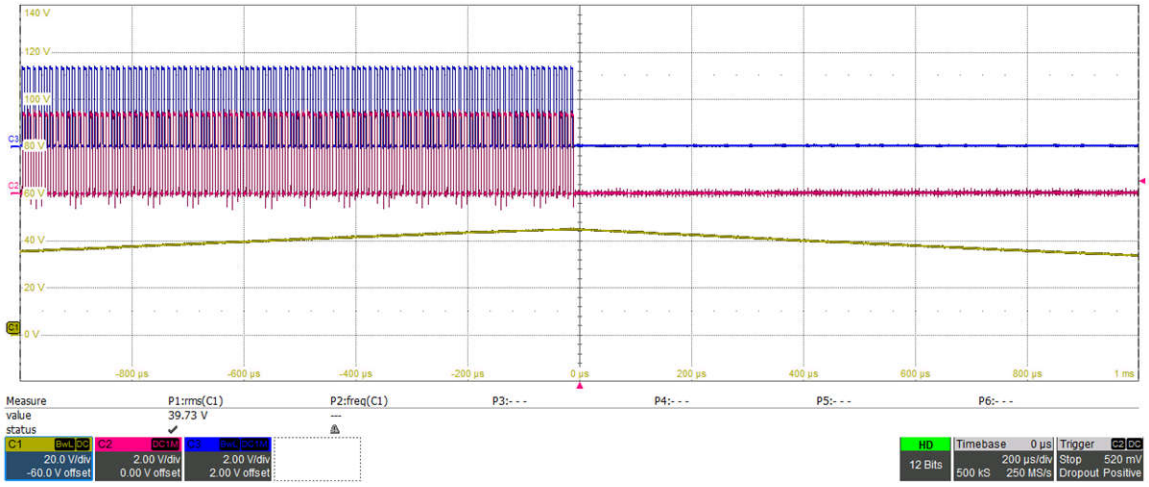


Figure 4-42. Lab 5 - Primary Side Overvoltage Protection

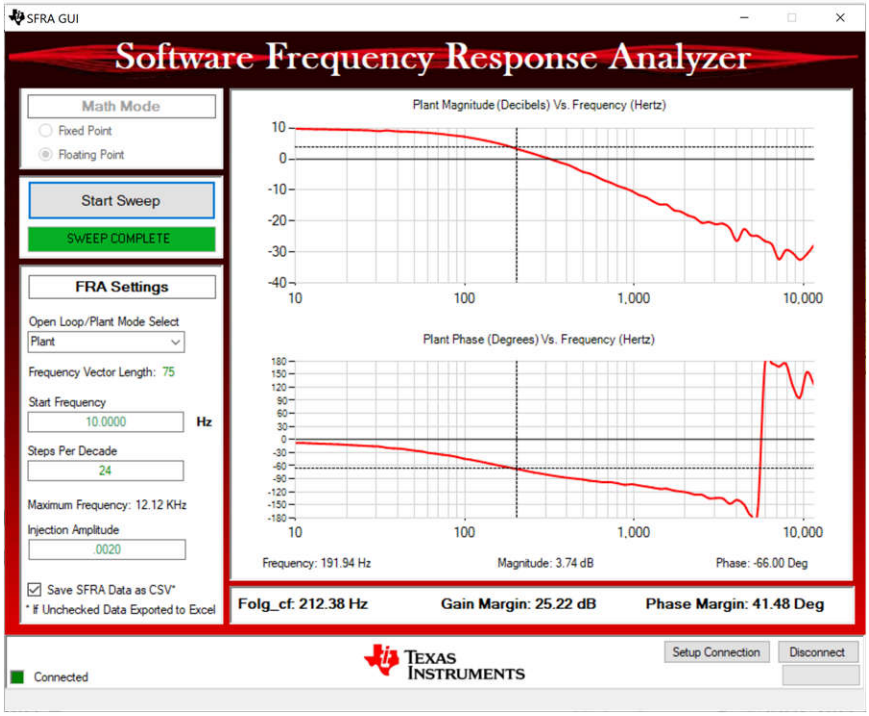
9. After verifying that overvoltage protection is working, set VPRIM_TRIP back to 1000 V.
10. Now voltage on the secondary side can be slowly increased and phase shift can be modified to observe the primary side voltage and current.

Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_singlePhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryDischarging	0x0000800E@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSecRef_pu	float	-0.0160000008	0x00008120@Data
DAB_vPrimSensed_Volts	float	800.022644	0x0000803C@Data
DAB_iPrimSensed_Amps	float	-3.16386724	0x00008028@Data
DAB_vSecSensed_Volts	float	499.062408	0x00008078@Data
DAB_vBatSensed_Volts	float	498.85379	0x00008086@Data
DAB_iSecSensed_Amps	float	-5.0664711	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.40330195	0x00008052@Data
DAB_pwmPhaseShiftPrimSec_pu	float	-0.0160000008	0x00008122@Data

Figure 4-43. Lab 5 Expression Window High Voltage

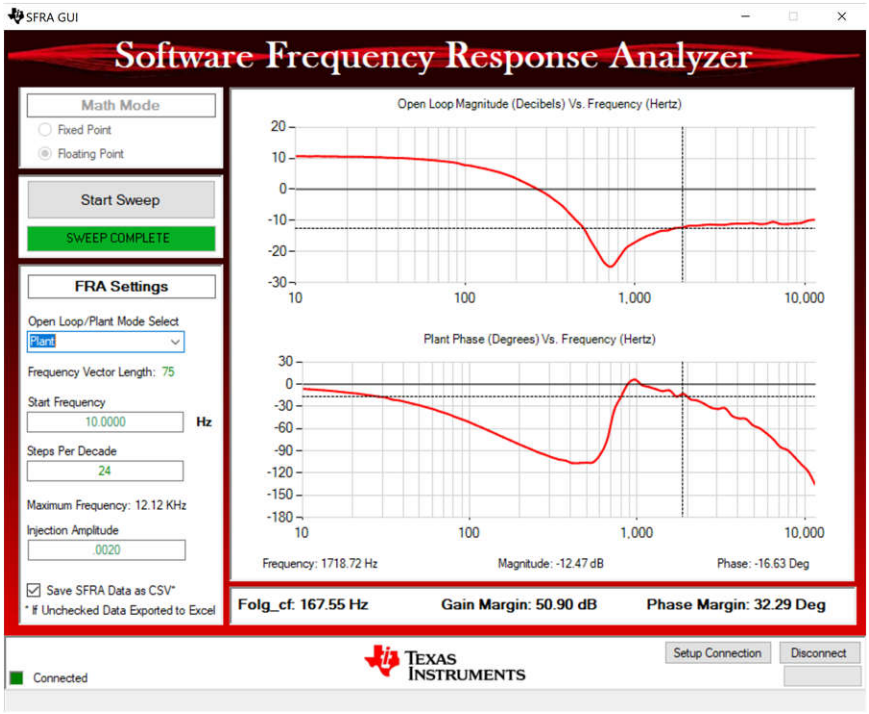
- **Measure SFRA Plant for Voltage Loop**
  1. Follow the same instructions as in Lab 2.



Test Condition: V_{IN} = 350 V, V_{OUT} = 550 V, I_{OUT} = 9 A.
V_{IN} refers to secondary side voltage, V_{OUT} and I_{OUT} refer to primary side voltage and current in reverse direction (DAB_IprimSensed_Amps = –9 A).

Figure 4-44. Lab 5 - SFRA Plant Plot for the Open Voltage Loop Test

- **Measure SFRA Plant for Current Loop**
  1. Follow the same steps as in Lab 2.



Test Condition: V_{IN} = 350 V, V_{OUT} = 550 V, I_{OUT} = 9 A.
V_{IN} refers to secondary side voltage, V_{OUT} and I_{OUT} refer to primary side voltage and current in reverse direction (DAB_IprimSensed_Amps = –9 A).

Figure 4-45. Lab 5 - SFRA Plant Plot for the Open Current Loop Test

4.4.6 Lab 6

In this setup, the DC source is connected to the secondary side and the resistive load is connected to the primary side. The design is operated with closed-voltage loop in the reverse direction.

Compile the project by selecting *6: Closed Loop Voltage with Resistive Load, Sec to Prim Power Flow* in the drop-down menu of *Project Options* from PowerSUITE GUI. Make sure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 6
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_SEC_PRI
#define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE  DAB_VOLTAGE_MODE
#define DAB_SFRA_TYPE  2
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
```

- **Test Setup for Lab 6 (Closed Voltage Loop - Vprim - Reverse power flow)**
  1. Run the project by clicking the green run button in CCS.
  2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab6.js` in the scripting console.

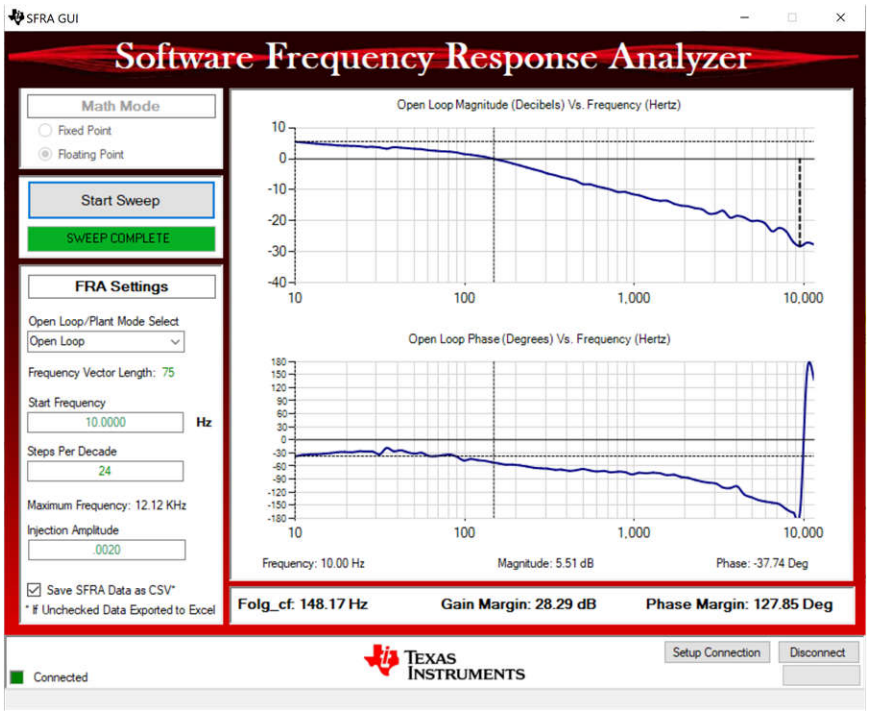
Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	closedLoopCheck_Voltage	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryDischarging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	-0.0199999996	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGvLoop	long	0	0x0000810A@Data
DAB_vPrimRef_Volts	float	50.0	0x00008044@Data
DAB_vPrimSensed_Volts	float	0.0	0x0000803C@Data
DAB_iPrimSensed_Amps	float	0.0244628917	0x00008028@Data
DAB_vSecSensed_Volts	float	3.97402954	0x00008078@Data
DAB_vBatSensed_Volts	float	4.03383875	0x00008086@Data
DAB_iSecSensed_Amps	float	0.00318145752	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.18699336	0x00008052@Data
isr1Ticker	long	931593	0x0000F638@Data
isr2Ticker	long	93174	0x0000F63A@Data
DAB_vPrimRefSlewed_pu	float	0.0444407165	0x00008048@Data
DAB_vPrimRef_pu	float	0.0477281436	0x00008046@Data

Figure 4-46. Lab 6 - Watch View

3. Enable fans and relays by writing "1" into `DAB_enableFan` and `DAB_enableRelay`.
4. Enable PWM by writing “1” to the `DAB_clearTrip` variable in the watch view.
5. Check if the `DAB_IprimSensed_Amps`, `DAB_iPrimSensed_Amps`, `DAB_vSecSensed_Volts`, and `DAB_iSecSensed_Amps` variables are updating periodically.
6. Set the output voltage by writing to `DAB_vPrimRef_Volts` (in this example 50 Vdc).
7. Enable closed loop operation by writing “1” to the `DAB_closeGvLoop` variable. The controller automatically adjusts the phase shift , depending upon the operating conditions to generate primary output voltage to match with that of `DAB_vPrimRef_Volts`.
8. Now secondary side voltage and `DAB_vPrimRef_Volts` can be increased in steps and the control behavior can be observed.

- **Frequency response of closed loop voltage**
  1. Follow the same steps as in Lab 3.



Test Condition: V_{IN} = 350 V, V_{OUT} = 550 V, I_{OUT} = 9 A

V_{IN} refers to secondary side voltage, V_{OUT} and I_{OUT} refer to primary side voltage and current in reverse direction.
(DAB_IprimSensed_Amps = –9 A)

Figure 4-47. Lab 6 - SFRA Open Loop Plot for the Closed Voltage Loop With Reverse Power Flow

The same controller and gains as in Lab 3 are used.

4.4.7 Lab 7

In this setup, the DC source is connected to secondary side and the resistive load is connected to primary side. The design is operated with closed-current loop in the reverse direction.

Compile the project by selecting *7: Closed Loop Current with Resistive Load, Sec to Prim Power Flow* in the drop-down menu of *Project Options* from PowerSUITE GUI. Make sure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 7
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_SEC_PRI
#define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE  DAB_CURRENT_MODE
#define DAB_SFRA_TYPE  1
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL1
#endif
```

- **Test Setup for Lab 7 (Closed Current Loop - Iprim - Reverse power flow)**
  1. Run the project by clicking the green run button in CCS.
  2. Populate the required variables in the watch window by loading JavaScript `setupdebugenv_lab7.js` in the scripting console.

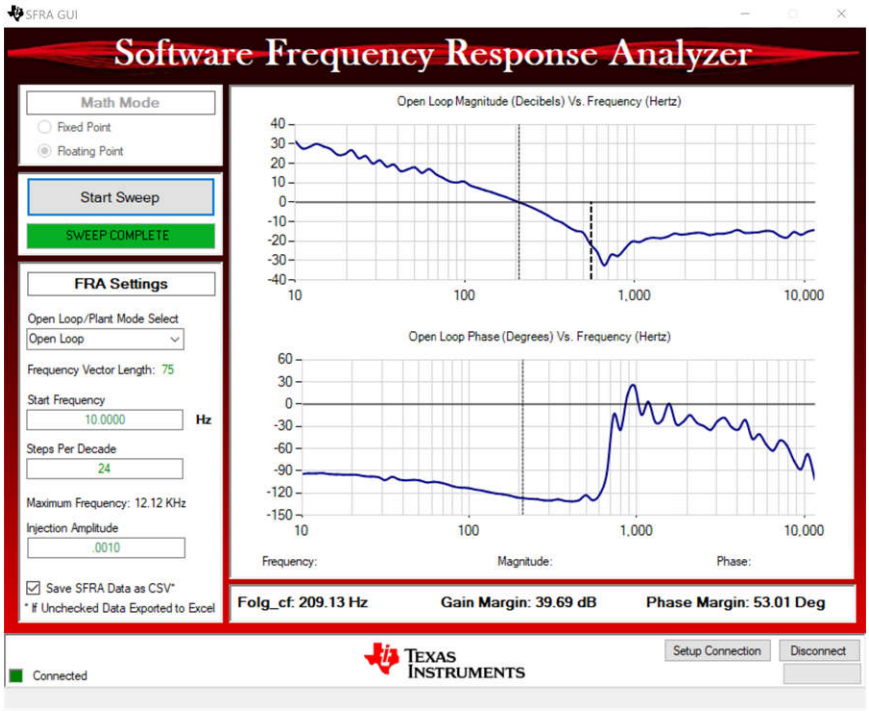
Variables | Expressions | Registers

Expression	Type	Value	Address
DAB_buildLevel.buildLevel	enum <unnamed>	closedLoopCheck_Current	0x00008004@Data
DAB_revisionStatus.revisionStatus	enum <unnamed>	revisionStatusOK	0x00008010@Data
DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_extendedPhaseShiftControl	0x0000800A@Data
DAB_powerFlowState.powerFlowState	enum <unnamed>	powerFlow_BatteryDischarging	0x0000800E@Data
DAB_pwmFrequency_Hz	float	100000.0	0x00008114@Data
DAB_pwmPhaseShiftPrimSec_pu	float	-0.0170364846	0x00008122@Data
DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008006@Data
DAB_clearTrip	long	0	0x0000810C@Data
DAB_enableFan	long	1	0x00008110@Data
DAB_enableRelay	long	1	0x0000810E@Data
DAB_closeGiLoop	long	1	0x00008108@Data
DAB_iPrimRef_Amps	float	-3.1500001	0x0000804A@Data
DAB_vPrimSensed_Volts	float	802.068726	0x0000803C@Data
DAB_iPrimSensed_Amps	float	-3.16386724	0x00008028@Data
DAB_vSecSensed_Volts	float	498.967773	0x00008078@Data
DAB_vBatSensed_Volts	float	498.817322	0x00008086@Data
DAB_iSecSensed_Amps	float	-5.12801695	0x0000806A@Data
DAB_iEfuseSensed_Amps	float	1.38383412	0x00008052@Data
isr1Ticker	long	42600984	0x0000F638@Data
isr2Ticker	long	4259754	0x0000F63A@Data
DAB_iPrimRefSlewed_pu	float	-0.188622758	0x0000804E@Data
DAB_iPrimRef_pu	float	-0.188622758	0x0000804C@Data

Figure 4-48. Lab 7 - Watch View

  3. Enable fans and relays by writing "1" into `DAB_enableFan` and `DAB_enableRelay`.
  4. Enable PWM by writing “1” to the `DAB_clearTrip` variable in the watch view.
  5. Check if the `DAB_vPrimSensed_Volts`, `DAB_iPrimSensed_Amps`, `DAB_vSecSensed_Volts`, and `DAB_iSecSensed_Amps` variables are updating periodically.
  6. Set the output voltage by writing to `DAB_iPrimRef_Volts` (in this example –3 A).
  7. Enable closed loop operation by writing “1” to the `DAB_closeGvLoop` variable. The controller automatically adjusts the phase shift , depending upon the operating conditions to generate primary output current to match with that of `DAB_iPrimRef_Volts`.
  8. Now the secondary side voltage and `DAB_iPrimRef_Volts` can be increased in steps and the control behavior can be observed.

- **Frequency response of closed loop current**
  1. Follow the same steps as in Lab 4.



Test Condition: V_{IN} = 350 V, V_{OUT} = 550 V, I_{OUT} = 9 A.
V_{IN} refers to secondary side voltage, V_{OUT} and I_{OUT} refer to primary side voltage and current in reverse direction (DAB_IprimSensed_Amps = –9 A).

Figure 4-49. Lab 7 - SFRA Open Loop Plot for the Closed Current Loop With Reverse Power Flow

The same controller and gains as in Lab 4 are used.

4.5 Test Results

The following efficiency measurements are done in the closed-voltage-loop configuration, with forward power flow.

4.5.1 Closed-Loop Performance

The closed-loop performance was done with output voltage control using Lab 3. Figure 4-50 shows the results. The drop in efficiency for lower output voltages is apparent. There are two main contributors to the drop in efficiency. First the lower efficiency for high loads is due two increasing circulating currents in the system, which increases the RMS currents and therefore conduction losses. The second contribution impacting light-load efficiency is loss of ZVS for light loads.

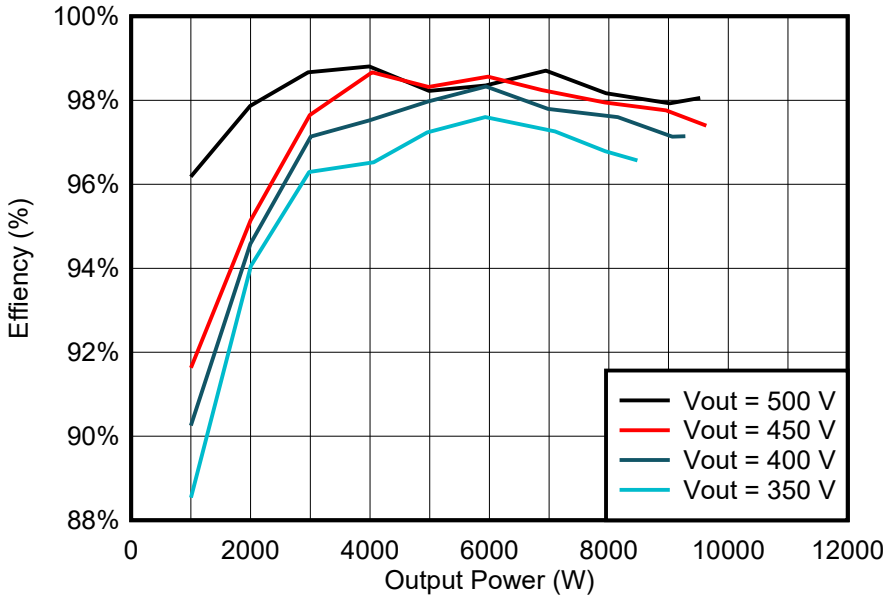


Figure 4-50. Closed-Loop Efficiency for Single-Phase-Shift (SPS) Control

With extended-phase-shift (EPS) control circulating currents are reduced and the ZVS range is increased. This improves both light-load and full-load efficiency. EPS control enables this reference design to work at lower output voltages, which is not possible with single-phase-shift (SPS) due to the higher losses. A value of 10 kW can be achieved down to 350-V output and 5 kW can be reached at 250-V output voltage.

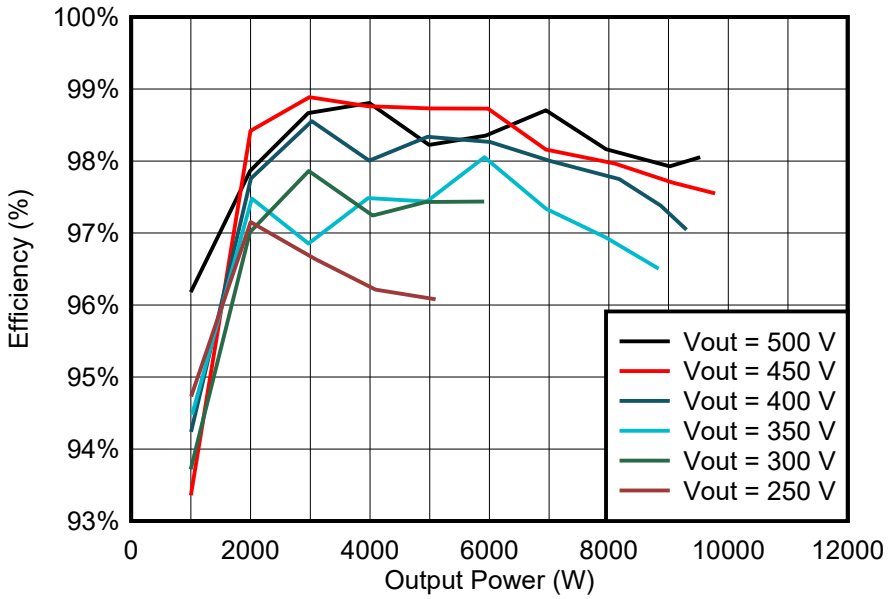


Figure 4-51. Closed-Loop Efficiency for Extended-Phase-Shift (EPS) Control

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-010054.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010054.

5.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010054.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010054.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010054.

6 Related Documentation

1. *Pwm control of dual active bridge: Comprehensive analysis and experimental verification*
2. *Comparison of Control Strategies for Dual Active Bridge Converter*

6.1 Trademarks

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7 Terminology

SiC	Silicon Carbide
DAB	Dual-Active Bridge
ZVS	Zero Voltage Switching
EV	Electric Vehicle
CCS	Code Composer Studio
V2G	Vehicle-to-Grid
SPS	Single phase shift
EPS	Extended phase shift

8 About the Author

ANDREAS LECHNER is working as systems engineer focusing on Grid Infrastructure and Renewable Energies at Texas Instruments and currently responsible for this reference design. Before joining TI he received his master's degree in electrical engineering at the University for Applied Sciences, Landshut.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2022) to Revision D (February 2024) **Page**

- Updated document to reflect new hardware revision of TIDA-010054. This includes new gate drivers, bias supplies, current sensors, and the C2000 MCU. The thermal design is improved and relays are added to the secondary side output. Software is updated to support new hardware features and extended-phase-shift control for improved light load efficiency is added. Two additional Labs for closed-loop voltage and current control are included for reverse power flow operation....1
- Updated, corrected and aligned equations and figures in Section 2.3.4 17
- Updated, corrected, and aligned equations and figures in Section 2.3.5....23
- Updated equations in Section 2.3.5.4....27
- Added closed loop test results in Section 4.5.1....77

Changes from Revision B (October 2021) to Revision C (July 2022) **Page**

- Updated Equation 7 and Equation 8 in Section 2.3.4.1....17
- Updated equations in Section 2.3.5.1....24
- Updated equation in Section 2.3.5.2....26

Changes from Revision A (September 2021) to Revision B (October 2021) **Page**

- Updated Figure 2-3....11
- Changed value in step 2 from 0.01 ns to 0.05 ns....51

Changes from Revision * (June 2019) to Revision A (September 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated the front page block diagram and board photo....1
- Updated Figure 2-1 and added a note to Section 2.1....6
- Updated devices in Section 2.2....7
- Updated the schematics in the *Circuit Description* section....28
- Updated the Power Architecture drawing in Section 3.4....32
- Updated the *Software* section....39
- Added PowerSUITE GUI section....49
- Added five sections detailing lab results. 50

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