Design Guide: TIDA-010062
1-kW, 80 Plus Titanium, GaN CCM Totem Pole Bridgeless PFC and Half-Bridge LLC Reference Design

Description
This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features TI's LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80 Plus Titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V dc output at 1-kW. Two control cards use C2000™ Piccolo™ microcontrollers to control both power stages.

Features
- 80 Plus Titanium efficiency, $\eta = >95\%$ at 20%-100% load
- CCM GaN based totem pole bridgeless PFC stage with >99% peak efficiency, enabled by LMG341x GaN FET with integrated driver
- Half-bridge Si MOSFET LLC stage with >98% peak efficiency
- Fast load transient, $V_o$ change within 300 mV at 2.5-A/us slew rate
- Low THD, <10% at 10% load, <5% at 20% load, <2% at >50% load
- Power density 41-W/in³, 38-mm by 66-mm by 160-mm

Applications
- Merchant network & server PSU
- Merchant telecom rectifiers
- Industrial AC-DC

Resources
TIDA-010062 Design Folder
TMS320F280049, LMG3410, TMCS1100 Product Folder
UCC21540, UCC27524, ISO7742, INA180 Product Folder
OPA2376, TPS560430, UCC28911 Product Folder

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1 System Description

In network, server, and datacenter systems, high efficiency across a full load range of power supply units (PSU) is a key requirement. Because server computers are continuously working with high power consumption for calculation and communication, high-efficiency PSUs reduce the operating investment. 80 PLUS® is a voluntary certification program intended to promote efficient energy use in computer PSUs. The program certifies products that have greater than 80% energy efficiency at 20%, 50%, and 100% of rated load. The highest level has reached Titanium level.

This reference design is a 1000-W AC/DC power supply for merchant server PSU applications, demonstrating high efficiency operation in a small form factor (160 mm × 66 mm × 38 mm). This reference design consists of a continuous conduction mode (CCM) totem pole power factor correction (PFC) as the front stage, an isolated half bridge LLC as the output stage, and a primary side regulation (PSR) flyback generates bias power for the control stage. The PFC stage operates from an input voltage range of 100-V - 265-V AC RMS and generates a 380-V DC bus. The second stage is made up of an isolated half bridge LLC stage, which generates a 12-V, 84-A nominal output.

1.1 Key System Specifications

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<th>PARAMETER</th>
<th>TEST CONDITION</th>
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<th>NOMINAL</th>
<th>MAXIMUM</th>
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<td>W/in³</td>
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</table>
2 System Overview

2.1 Block Diagram

Figure 1 shows the high-level block diagram of the design. In this design, two TMS320F280049 C2000™ Piccolo™ control cards are used respectively for the controller of the PFC stage and LLC stage, and an LMG3410 GaN daughter card is used for totem pole half-bridge switching. A silicon MOSFET-based synchronous rectifier, driven by the UCC27714 half-bridge driver, reduces power loss in the low-frequency half bridge at the input. Another silicon MOSFET-based synchronous rectifier used is driven by the UCC21540 isolated half-bridge driver for LLC half-bridge switching. The input current is sensed by a Hall-effect sensor TMCS1100, and the DC link voltage is processed by a variable-gain amplifier stage built using the OPA237 amplifier for better accuracy at low current levels. The output current is sensed by the INA180 current-sense amplifier. For communication between the primary and secondary control card, Fast Serial Interface (FSI) is sensed by the four-channel digital isolator ISO7742. An onboard auxiliary power supply is implemented using the UCC28911 and provides a 12-V bias for the primary side and a 6-V bias for the secondary side. The TPS560430 is used in both the primary and secondary side for regulated $V_{cc}$ in control cards and control circuits.

2.2 Design Considerations

In the totem pole PFC stage, which benefits from gallium nitride (GaN), the switching loss and reverse recovery loss are reduced significantly. CCM control can be implemented with high efficiency. In the LLC stage, which benefits from a high-resolution PWM control of C2000 and powerful calculation ability, both the primary side and secondary side can achieve soft switching with accurate deadtime and SR control.
For higher efficiency, the LLC stage of this design uses an interleaved structure in the transformer to reduce the proximity effect and uses a PCB winding with a copper strip in parallel to reduce the winding loss on the secondary side. In the LLC transformer, there are four secondary PCB windings with an SR MOSFET and a dual-channel driver, connected in parallel, and three primary windings connected in serial. These windings are not connection joints, but all three use the same wire twisting. For the detailed design, refer to the documents from ASIAINFO®, the transformer vendor for this design.

2.3 **Highlighted Products**

The following highlighted products are used in this reference design. Key features for selecting the devices for this reference design are explained in the following sections. Complete details of the highlighted devices is referred to in the respective product data sheets.

2.3.1 **F28004x — C2000™ Piccolo™ controlCARD**

C2000 MCUs are part of an optimized MCU family for real-time control application. Fast and high-quality analog-to-digital controller enables accurate measurement of the current and voltage signals, and an integrated comparator subsystem (CMPSS) provides protection for overcurrent and overvoltage without use of any external devices. The optimized CPU core enables fast execution of control loop. Trigonometric operations are accelerated using the on-chip trigonometric math unit (TMU). The solution also provides an option to use the control law accelerator (CLA) on the F28004x and F2837x. The CLA is a co-processor that can be used to alleviate CPU burden and enable faster-running loops or more functions on the C2000 MCU.

2.3.2 **LMG3410 — 600-V GaN With Integrated Driver and Protection**

The LMG3410 single-channel GaN power stage contains a 70mR (/50mR/150mR), 600-V GaN power transistor and specialized driver in an 8-mm x 8-mm QFN package. Direct drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off through its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally-generated negative voltage supply. The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and undervoltage lockout (UVLO) protections help create a fail-safe system. The device’s status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

2.3.3 **TMCS1100 — Precision Isolated Current Sense Monitor**

The TMCS1100 is an isolated bidirectional Hall-effect current sensor, with high accuracy, excellent linearity, and stability across temperature.

A low-drift, temperature-compensated signal chain provides <1% full-scale error across the entire device temperature range. The output voltage is proportional to input current with four sensitivity options: 50 mV/A, 100 mV/A, 200 mV/A, and 400 mV/A.

The TMCS1100 operates from a single 3-V to 5.5-V power supply, drawing a maximum supply current of 5 mA. All versions are specified over an extended operating temperature range of 40°C to +125°C and are offered in an 8-pin SOIC package.

2.3.4 **UCC27524 — Dual, 5-A, High-Speed Low-Side Power MOSFET Driver**

The UCC2752x family of devices are dual-channel, high-speed, low-side gate-driver devices capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC2752x can deliver high peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay (typically 13 ns). In addition, the drivers feature matched internal propagation delays between the two channels. These
delays are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal. The input pin thresholds are based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

2.3.5 UCC27714 — 620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver

The UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability that is targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to -8 VDC on HS pin (at VDD = 12 V).

2.3.6 UCC21540 — Reinforced Isolation Dual-Channel Gate Driver With 3.3-mm Channel-to-Channel Spacing Option

The UCC2154x is an isolated dual channel gate driver family designed with up to 4-A/6-A peak source/sink current to drive power MOSFET, IGBT, and GaN transistors, and UCC21540 in DWK package also offers 3.3-mm minimum channel-to-channel spacing which facilitates higher bus voltage. The UCC2154x family can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 5.7-kVRMS isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, integrated de-glitch filter that rejects input transients shorter than 5 ns, and negative voltage handling for up to –2-V spikes for 200-ns on input and output pins. All supplies have UVLO protection.

2.3.7 ISO7740 and ISO7720 — High-Speed, Low-Power, Robust EMC Digital Isolators

The ISO774x devices are high-performance, quad channel digital isolators with 5000 VRMS (DW package) and 3000 VRMS (DBQ package) isolation ratings per UL1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LV CMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon diodes (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward and one reverse-direction channels, and the ISO7742 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is high for devices without suffix F and low for devices with suffix F.

2.3.8 OPA237 — Single-Supply Operational Amplifier

The OPA237 operational amplifier (op amp) family is one of TI's micro amplifiers in a series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. They are ideal for single-supply applications. When operated from a single supply, the input common-mode range extends below ground, and the output can swing to within 10 mV of ground.

2.3.9 INA180 — Low- and High-Side Voltage Output, Current-Sense Amplifiers

The INA180, INA2180, and INA4180 (INAx180) current sense amplifiers are designed for cost optimized applications. These devices are part of a family of current-sense amplifiers (also called current shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to +26 V, independent of the supply voltage. The INA1x80 integrate a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

All of these devices operate from a single 2.7-V to 5.5-V power supply. The single-channel INA180 draws a maximum supply current of 260 μA; whereas, the dual-channel INA2180 draws a maximum supply current of 500 μA, and the quad channel INA4180 draws a maximum supply current of 900 μA.
The INA180 is available in a 5-pin, SOT-23 package with two different pin configurations. The INA2180 is available in an 8-pin, VSSOP package. The INA4180 is available in a 14-pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to +125°C.

2.3.10 **TPS560430 — SIMPLE SWITCHER® 4-V to 36-V, 600-mA Synchronous Step-Down Converter**

The TPS560430 is an easy-to-use synchronous step-down DC-DC converter capable of driving up to 600-mA load current. With a wide input range of 4 V to 36 V, the device is suitable for a wide range of applications from industrial to automotive for power conditioning from an unregulated source. The TPS560430 has 1.1-MHz and 2.1-MHz operating frequency versions for either high efficiency or small solution size. The TPS560430 also has a FPWM (forced PWM) version to achieve constant frequency and small output voltage ripple over the full load range. Soft-start and compensation circuits are implemented internally which allows the device to be used with minimum external components. The device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The TPS560430 is available in SOT-23-6 package.

2.3.11 **TLV713 — 150-mA Low-Dropout (LDO) Regulator With Foldback Current Limit for Portable Devices**

The TLV713 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.

The TLV713 series of devices is designed to be stable without an output capacitor. The removal of the output capacitor allows for a very small solution size. However, the TLV713 series is also stable with any output capacitor if an output capacitor is used.

The TLV713 also provides inrush current control during device power up and enabling. The TLV713 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV713 series is available in standard DQN and DBV packages. The TLV713P provides an active pulldown circuit to quickly discharge output loads.

2.3.12 **TMP61 — Small Silicon-Based Linear Thermistor for Temperature Sensing**

The TMP61 series of small silicon linear thermistors are designed for temperature measurement, protection, compensation, and control systems. Compared to traditional NTC thermistors, the TMP61 device offers enhanced linearity and consistent sensitivity across the full temperature range. The TMP61 offers robust performance due to device immunity to environmental variation and built-in fail-safe behaviors at high temperatures. This device is currently available in a 2-pin, surface-mount, 0402 footprint-compatible X1SON package.

2.3.13 **CSD18510Q5B — 40-V, N-Channel NexFET™ MOSFET, Single SON5x6, 0.96 mΩ**

This 40-V, 0.79-mΩ, SON 5-mm × 6-mm NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

2.3.14 **UCC28911 — 700-V Flyback Switcher With Constant-Voltage, Constant-Current, and Primary-Side Regulation**

The UCC28910 and UCC28911 are high-voltage flyback switches that provide output voltage and current regulation without the use of an optical coupler. Both devices incorporate a 700-V power FET and a controller that process operating information from the flyback auxiliary winding and power FET to provide a precise output voltage and current control. The integrated high-voltage current source for startup that is switched off during device operation, and the controller current consumption is dynamically adjusted with load. Both enable the very low stand-by power consumption.
Control algorithms in the UCC28910 and UCC28911, combining switching frequency and peak primary current modulation, allow operating efficiencies to meet or exceed applicable standards. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. Built-in protection features help to keep secondary and primary component stress levels in check across the operating range. The frequency jitter helps to reduce EMI filter cost.

2.3.15 **SN74LVC1G3157DRYR — Single-Pole Double-Throw Analog Switch**

This single channel single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC1G3157 device can handle both analog and digital signals. The SN74LVC1G3157 device permits signals with amplitudes of up to VCC (peak) to be transmitted in either direction. Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

2.4 **System Design Theory**

This reference design provides a universal AC mains-powered, 1000-W nominal output at 12 V and 84 A. This design comprises a front-end totem pole PFC power stage followed by an isolated DC/DC LLC power stage.

2.4.1 **Totem Pole PFC Stage Design**

The totem pole bridgeless PFC is an old structure that has been presented for many years, but it has not been applied in products because of the poor reverse recovery performance of the MOSFET's body diode. However, in recent years, benefitting from GaN HEMT's no reverse recovery feature, the totem pole PFC is now being applied and has become a simple structure. Generally, the totem pole PFC has one fast-switching leg and one slow-switching leg. The slow-switching leg can use both a rectifier diode or MOSFET. When using a MOSFET as a slow-switching leg, the totem pole PFC can achieve higher efficiency and bidirectional power conversion between the AC side and the DC side.

2.4.1.1 **Design Parameters of the PFC stage**

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<th>SYMBOL</th>
<th>PARAMETER</th>
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2.4.1.2 **Current Calculations**

The input fuse, bridge rectifier, and input capacitor are selected based on the input current calculations. First, determine the maximum average output current, I<sub>OUT(max)</sub>, as per Equation 1:

\[
I_{\text{OUT(max)}} = \frac{P_{\text{OUT(max)}}}{V_{\text{dcinking}}} = \frac{1050 \text{ W}}{385 \text{ V}} = 2.73 \text{ A}
\]

The maximum input RMS line current, I<sub>IN_RMS(max)</sub>, is calculated using the parameters from Table 2, and the efficiency and power factor initial assumptions are calculated as follows:

\[
I_{\text{IN RMS(max)}} = \frac{P_{\text{OUT(max)}}}{\eta_{\text{PFC}} \times V_{\text{IN(min)}} \times PF} = \frac{1050 \text{ W}}{98\% \times 100 \text{ V} \times 0.99} = 10.8 \text{ A}
\]
2.4.1.3 PFC Boost Inductor

To determine the boost inductor, the maximum-allowed ripple current is calculated first. The maximum ripple current is observed at the lowest input voltage and maximum load. Assuming a maximum 40% ripple in the inductor current, the ripple current would be calculated as follows:

\[ I_{\text{Lripple(max)}} = \Delta \text{ripple} \times I_{\text{INrms(max)}} = 0.2 \times \sqrt{2} \times 10.7 \text{A} = 6.06 \text{A} \]  
\[ \text{(3)} \]

The duty cycle, \( DUTY_{(\text{max})} \), at the peak of the minimum input voltage can be calculated as:

\[ DUTY_{(\text{max})} = \frac{V_{\text{OUT(max)}} - V_{\text{INmin}} \times \sqrt{2}}{V_{\text{dc, link}}} = \frac{385 \text{V} - 100 \text{V} \times \sqrt{2}}{385 \text{V}} = 0.63 \]  
\[ \text{(4)} \]

The minimum value of the boost inductor is calculated based on the acceptable ripple current, at a worst-case duty cycle of 0.63:

\[ L_{\text{Boost}} \geq V_{\text{OUT(max)}} \times DUTY_{(\text{max})} \times \frac{1 - DUTY_{(\text{max})}}{F_{\text{SW}} \times I_{\text{Lripple(max)}}} = 295 \mu \text{H} \]  
\[ \text{(5)} \]

The actual value of the inductor chosen is 300 \( \mu \text{H} \). The required saturation current for the boost inductor is calculated using Equation 6 for the minimum input voltage and short time maximum overload conditions.

\[ I_{\text{L(max)}} = \sqrt{2} \times \frac{P_{\text{OUT(max)}}}{V_{\text{INrms(min)}}} \times (1 + \frac{\Delta \text{ripple0}}{2}) = 16.67 \text{A} \]  
\[ \text{(6)} \]

2.4.1.4 Output Capacitor

The output capacitor, \( C_{\text{bus}} \), is sized to meet the DC link ripple and holdup requirements of the converter. The ripple of DC link voltage can be calculated by Equation 7:

\[ V_{\text{ripple}} = \frac{P_{\text{OUT}}}{C_{\text{bus}} \times V_{\text{Bus}}} \times 0.0032 \]  
\[ \text{(7)} \]

The holdup time required by this design, \( T_{\text{Holdup}} \), is 10 ms. The average bus voltage is set at 385 V, which is correlated with the LLC transformer ratio. Considering the DC link voltage has +/-10-V ripple at full load, the DC BUS voltage will be \( V_{\text{BUS(norm)}} = 365 \text{V} \) in the valley point.

Considering the gain of LLC can not be too wide, the minimum input of LLC is set at \( V_{\text{BUS(min)}} = 320 \text{V} \). For energy, the minimum value of BUS capacitance can be calculated using Equation 8, and for the calculation of Equation 9, the available capacitance value of 680 \( \mu \text{F} \) was chosen.

\[ C_{\text{OUT}} \geq 2 \times P_{\text{OUT(nominal)}} \times \frac{T_{\text{Holdup}}}{V_{\text{OUT(norm)}}^2 - V_{\text{OUT(min)}}^2} \]  
\[ \text{(8)} \]

\[ C_{\text{OUT}} \geq 2 \times 1000 \text{W} \times \frac{10 \text{ms}}{365 \text{V}^2 - 320 \text{V}^2} = 648 \mu \text{F} \]  
\[ \text{(9)} \]

2.4.1.5 Fast and Slow Switches

Given the calculation of \( I_{\text{IN Rms(max)}} \), all current ratings of the switches should be greater than 10.8 A. In a CCM totem pole PFC, a GaN switch is required for the fast bridge. The 70-m\( \Omega \) GaN LMG3410R070 was selected, which is recommended for 12-A \( I_{\text{DS}} \) on 125\( ^\circ \text{C} \) \( T_{\text{j}} \).

The slow bridge is only line frequency switching, so the minimum \( R_{\text{dsOn}} \) is preferred for better efficiency. To save space, the Toshiba\( ^\circ \) 50-m\( \Omega \) MOSFET TK39A60W was chosen. This device has a low \( R_{\text{dsOn}} \) with a TO220 package that is available on the market.

2.4.1.6 AC Current Sensing Circuits

In this design, AC current is sensed for current loop control. Only average current is required in the CCM boost PFC control loop. The TMCS1100, a 120-kHz Hall sensor, is a good option for this design. The TMCS1100 has high accuracy across a full temperature range and a very low offset current drift, helping achieve accuracy in input power metering.
The TMCS1100 has four options: 50 mV/A, 100 mV/A, 200 mV/A, and 400 mV/A. The supply voltage could be 3 V to 5.5 V. The offset voltage is set externally. 1.65 V was chosen for this design, which is half of the $V_{cc}$ of the controller. The maximum input current will reach 14 A at the peak value. In considering the worst case and leaving some margin, the TMCS1100A1 was chosen. The sensing circuits used the OPA376 with one analog switch, SN74LVC1G3157, to scale the voltage to match the ADC range at both the low line and high line. The circuits are shown in Figure 2.

**Figure 2. Current Sensing and Signal Scaling Circuits**

![Figure 2. Current Sensing and Signal Scaling Circuits](image)

$$I_{\text{sense}}(S) = \frac{R_s}{R_e} \frac{V_{\text{ref}}}{2} \times \frac{1}{1 + RC_s}$$

2.4.1.7 **Temperature Sensing**

TI’s silicon-based linear thermistor TPM61 is used for temperature sensing. The implementation circuits are shown in Figure 3.

**Figure 3. Temperature Sensing Circuits**

![Figure 3. Temperature Sensing Circuits](image)

$$V_{\text{Temp}} = \frac{V_{\text{Bias}}}{R_{\text{Bias}}} \times \frac{R_{\text{TMP61}}}{R_{\text{Bias}} + R_{\text{TMP61}}}$$

2.4.2 **Design Parameters of the LLC Stage**

The LLC stage is the end stage for output regulation. Its input is the output of the PFC stage, so the LLC stage should be able to keep the output voltage stable at 12 V between the $V_{\text{BUS(max)}}$, the peak value with full load, and the $V_{\text{BUS(min)}}$, the minimum $V_{\text{Bus}}$ voltage for holdup time when AC drop occurs.

**Table 3. Design Parameters for the LLC Stage**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>NOMINAL</th>
<th>MAXIMUM</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN}}$</td>
<td>DC input voltage</td>
<td>320</td>
<td>385</td>
<td>395</td>
<td>V DC</td>
</tr>
<tr>
<td>$V_{\text{out}}$</td>
<td>Output voltage</td>
<td>11.4</td>
<td>12</td>
<td>12.8</td>
<td>V DC</td>
</tr>
<tr>
<td>$P_{\text{out}}$</td>
<td>Maximum output power</td>
<td>1000</td>
<td>1000</td>
<td>1000</td>
<td>Watt</td>
</tr>
<tr>
<td>$f_{\text{sw}}$</td>
<td>Switch frequency</td>
<td>80</td>
<td>140</td>
<td>250</td>
<td>kHz</td>
</tr>
<tr>
<td>$\eta$</td>
<td>Targeted efficiency</td>
<td>98</td>
<td>98</td>
<td>98</td>
<td>%</td>
</tr>
</tbody>
</table>
2.4.2.1 Determining LLC Transformer Turns Ratio N

The LLC tank is designed to have a nominal gain, \( M_g \), of 1 at the resonant frequency. Use Equation 10 to estimate the required turns ratio.

\[
n = \frac{V_{\text{BUS(nom)}}}{2 \times V_{\text{out(nom)}}} = \frac{385 \text{ V}}{2 \times 12.0 \text{ V}} = 16
\]

(10)

The transformer turns ratio is set to 16.

2.4.2.2 Determining \( M_{g_{\text{min}}} \) and \( M_{g_{\text{max}}} \)

Determine \( M_{g_{\text{min}}} \) and \( M_{g_{\text{max}}} \) using Equation 11 and Equation 12, respectively.

\[
M_{g_{\text{min}}} = n \times \frac{V_O + V_F}{V_{\text{bus(max)}} / 2} = 16 \times \frac{12 \text{ V} + 0.01 \text{ V}}{395 \text{ V} / 2} = 0.972
\]

(11)

\[
M_{g_{\text{max}}} = n \times \frac{V_O + V_F}{V_{\text{bus(min)}} / 2} = 16 \times \frac{12 \text{ V} + 0.01 \text{ V}}{320 \text{ V} / 2} = 1.2
\]

(12)

The dimensioned \( M_{g_{\text{max}}} \) is increased to one. One times the required value to have some margin is \( M_{g_{\text{max}}} = 1.1 \times 1.2 \approx 1.3 \).

2.4.2.3 Determining Equivalent Load Resistance (\( R_e \)) of Resonant Network

Equation 13 calculates the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage.

\[
R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_O}{I_O} = \frac{8 \times 16^2}{\pi^2} \times \frac{12}{84} = 29.64 \Omega
\]

(13)

2.4.2.4 Selecting \( L_m \) and \( L_r \) Ratio (\( L_n \)) and \( Q_e \)

Set the resonance point for the LLC converter close to 140 kHz to minimize the dimension of the LLC transformer set. The operating point of the LLC power stage is close to this frequency during a full load condition. Choose a value of \( L_r = 19 \mu \text{H} \) and \( C_r = 66 \text{ nF} \) to calculate the value of the resonant frequency as follows:

\[
f_r = \frac{1}{2\pi\sqrt{L_rC_r}} = 140 \text{ kHz}
\]

(14)

A PQ 32/30 core has been used to realize the LLC transformer. The resonant inductance is provided through an additional shim inductor built on a 20/16 PQ core.

2.4.2.5 Determining Primary-Side Currents

Use Equation 15 to calculate the primary-side RMS load current (\( I_{\text{pri}} \)) at a full load condition:

\[
I_{\text{pri}} = \frac{\pi}{2\sqrt{2}} \times \frac{I_{\text{b(nom)}}}{n} = 1.11 \times \frac{84}{16} = 5.83 \text{ A}
\]

(15)

As calculated in Equation 16, the RMS magnetizing current (\( I_m \)) at \( f_{\text{SW,min}} = 140 \text{ kHz} \) is:

\[
I_m = \frac{2\sqrt{2}}{\pi} \left( \frac{n \times V_{O(nom)} + V_F}{2\pi \times f_{\text{sw(min)}} \times L_m} \right) = 0.66 \text{ A}
\]

(16)

Equation 17 calculates the resonant circuit current (\( I_r \)):

\[
I_r = \sqrt{I_{\text{pri}}^2 + I_m^2} = 5.86 \text{ A}
\]

(17)

This value is also equal to the transformer primary winding current at \( f_{\text{SW,min}} \).
2.4.2.6 Determining Secondary-Side Currents

The secondary-side RMS currents can be calculated from the average load current. Assuming that the LLC power stage is operating close to its second resonant frequency, the RMS current through each rectifier in the secondary-side push-pull output is calculated in Equation 18:

\[ I_{\text{sec,RMS}} = I_{\text{sec}} \times \frac{\pi}{2\sqrt{2}} = 92.56 \text{ A} \]  

(18)

2.4.2.7 Primary-Side MOSFETs and Driver

For the LLC power stage working in ZVS, the turn-on losses can be neglected. The choice of the MOSFET should be based on \( R_{\text{DS(on)}} \) and Coss. Optimizing the Coss helps in minimizing the dead time required for achieving ZVS, thereby minimizing duty cycle loss. In this design, the TK39A60W MOSFET is used.

To drive the primary-side MOSFET on the secondary side, one isolated half-bridge driver, UCC21540, is used to achieve accurate and safe driving ability.

2.4.2.8 Secondary-Side Synchronous MOSFETs

The output diode rectifier/SR MOSFET voltage rating is determined using Equation 19:

\[ V_{\text{ds(max)}} = 1.2 \times 2 \times V_{\text{o(nom)}} = 28.8 \text{ V} \]  

(19)

The RMS currents through the output SR MOSFET is given with Equation 20:

\[ I_{\text{SRMOS,RMS}} = I_{\text{sec,RMS}} \times \frac{1}{2} = \frac{92.56 \text{ A}}{2} = 46.28 \text{ A} \]  

(20)

To reduce the losses in the synchronous rectifier, the 4-pcs CSD1851005B with very low \( R_{\text{DS(on)}} \) and \( Q_g \) is used in parallel. Each MOSFET used one dual-channel, non-isolated driver, the UCC27524, to reduce the conduction losses in the LLC output stage.

2.4.2.9 Output Current Sensing

In this design, output current is sensed to optimize the system efficiency, adjust the deadtime and SR pulse, and is used for current sharing control between different PSUs. Also, this signal can be used in the control loop of the LLC stage to reduce the overshoot and undershoot during load transient.

A benefit of the high common-mode range of the INAx180 is the ability to put the sensing resistor either on high-side \( VO+ \) or low-side \( VO- \). The INAx180 integrates a matched resistor gain network in four fixed-gain device options: 20, 50, 100, and 200. This matched gain resistor network minimizes gain error and reduces the temperature drift. To reduce the power loss on the current-sensing resistor, the 200-V/V A4 devices should be chosen, and by adjusting the resistor to scale, the voltage to match the ADC range of the MCU. The sensing resistor can be calculated using Equation 21:

\[ R_{\text{CS}} = \frac{V_{\text{ADC}}}{1.5 \times I_{\text{bmax}} \times 200} \times \frac{3.3 \text{ V}}{1.5 \times 84 \text{ A} \times 200} = 0.131 \text{ m\Omega} \]  

(21)

When the resistor is smaller than 1 m\( \Omega \), the accuracy will drop and the cost will increase. Therefore, a 4-pcs, 0.5-m\( \Omega \) resistor with 1% accuracy is used while getting 0.125 m\( \Omega \) in parallel.

2.4.3 Communication Between the Primary Side and the Secondary Side

In this design, both the primary and secondary side use the F280049. The C2000 MCU’s Fast Serial Interface (FSI) communication is a good option for this design.

FSI originated as a solution for higher-bandwidth digital communication across the air gap, or hot-side to cold-side and vice versa, in high-voltage systems such as those used in industrial drives and digital power applications. FSI achieves the top clock rate of 50 MHz for \( L_{\text{VC莫斯}} \) IO and can take as few as two pins, CLK and Data, in each direction. FSI also has a dual-data rate. It latches the data on both the rising and falling clock edges, making the raw transmit bandwidth 100 Mbps and the raw receive bandwidth 100 Mbps as well.
The configuration of two signals in each direction that also requires reinforced isolation is addressed perfectly by another TI component, the ISO7742. A single SOIC16 packaged ISO7742 is all that is needed to isolate the 100 Mbps FSI signals up to 8000 Vpk and carries reinforced isolation certifications according to VDE, CSA, CQC, and TUV. This single chip, when using FSI, can replace the cost of multiple isolation devices while saving significant board space and also reducing the PCB routing and voltage plane definition challenges associated with mixed-plane, high-voltage PCB designs.
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This section details the necessary equipment, test setup, and procedure instructions for the TIDA-010062 board testing and validation.

3.1.1.1 Test Conditions

For input, the power supply source (VIN) must range from 100-V to 265-V AC. Set the input current limit of the input AC source to 15 A. For output, use an electronic variable load or a variable resistive load, which must be rated for ≥15 V and must vary the load current from 0 A to 90 A.

3.1.1.2 Test Equipment Required for Board Validation

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- High voltage probe (>600 V)
- Current probe
- Multimeters
- Electronic or resistive load
- 12V1A cooling FAN

3.1.1.3 Test Procedure

1. Connect the GaN daughter cards and C2000 Piccolo controlCard to the mother board as follows. The details of the connections to each pin of the connectors can be found in the schematic of the 1-kW, 80+ Titanium AC/DC Power Supply Reference Design.
   - One GaN daughter card ‘LMG3410-HB-EVM’ at connectors Brd1 position
   - C2000 Piccolo controlCard ‘TMDSCNCD280049C’ at the connector J1 and J3
2. Connect the 3 Pins AC terminal of reference board to the AC power source.
3. Connect output terminals with wires to the electronic load, and maintain correct polarity.
4. Put a cooling FAN at the AC side to keep the board in wind;
5. Set and maintain a small load of approximately 10 A.
6. Current and voltage probes can be connected to observe the input current, input voltage, and output voltages.
3.2 Testing and Results

The test results are divided into multiple sections that cover the steady state performance, functional performance waveforms and test data, and transient performance waveforms.

3.2.1 Performance, Data, and Curve

3.2.1.1 Efficiency, iTHD, and PF of the PFC stage

Table 4 shows the efficiency data of the PFC stage at a 230-V AC input.

Table 4. Efficiency, iTHD, and PF of the PFC Stage at 230-V AC Input (Without CTRL and DRV Loss)

<table>
<thead>
<tr>
<th>(V_{\text{in}}) (V)</th>
<th>(I_{\text{in}}) (A)</th>
<th>(P_{\text{in}}) (W)</th>
<th>(V_{\text{out}}) (V)</th>
<th>(I_{\text{out}}) (A)</th>
<th>(P_{\text{out}}) (W)</th>
<th>Efficiency Without CTRL and DRV</th>
<th>Efficiency With CTRL and DRV</th>
<th>iTHD (%)</th>
<th>PF</th>
</tr>
</thead>
<tbody>
<tr>
<td>230.18</td>
<td>0.412</td>
<td>91.3</td>
<td>387.3</td>
<td>0.232</td>
<td>89.8536</td>
<td>98.42%</td>
<td>96.99%</td>
<td>8.96%</td>
<td>0.962</td>
</tr>
<tr>
<td>230.08</td>
<td>0.828</td>
<td>188.9</td>
<td>387.3</td>
<td>0.4818</td>
<td>186.6011</td>
<td>98.78%</td>
<td>98.09%</td>
<td>6.43%</td>
<td>0.991</td>
</tr>
<tr>
<td>230.05</td>
<td>1.2503</td>
<td>286.6</td>
<td>387.4</td>
<td>0.7319</td>
<td>283.5381</td>
<td>98.93%</td>
<td>98.47%</td>
<td>3.86%</td>
<td>0.997</td>
</tr>
<tr>
<td>229.88</td>
<td>1.674</td>
<td>384.1</td>
<td>387.4</td>
<td>0.9818</td>
<td>380.3493</td>
<td>99.02%</td>
<td>98.68%</td>
<td>2.07%</td>
<td>0.998</td>
</tr>
<tr>
<td>229.81</td>
<td>2.0963</td>
<td>481.2</td>
<td>387.4</td>
<td>1.2307</td>
<td>476.7732</td>
<td>99.08%</td>
<td>98.80%</td>
<td>1.62%</td>
<td>0.998</td>
</tr>
<tr>
<td>229.74</td>
<td>2.52</td>
<td>578</td>
<td>387.4</td>
<td>1.4806</td>
<td>573.5844</td>
<td>99.24%</td>
<td>99.01%</td>
<td>1.75%</td>
<td>0.999</td>
</tr>
<tr>
<td>229.66</td>
<td>2.946</td>
<td>675.5</td>
<td>387.4</td>
<td>1.7307</td>
<td>670.3001</td>
<td>99.26%</td>
<td>99.03%</td>
<td>1.71%</td>
<td>0.999</td>
</tr>
<tr>
<td>229.67</td>
<td>3.366</td>
<td>772</td>
<td>387</td>
<td>1.9807</td>
<td>766.5309</td>
<td>99.29%</td>
<td>99.12%</td>
<td>1.63%</td>
<td>0.999</td>
</tr>
<tr>
<td>229.51</td>
<td>3.802</td>
<td>871</td>
<td>387.4</td>
<td>2.2311</td>
<td>864.3281</td>
<td>99.23%</td>
<td>99.08%</td>
<td>1.53%</td>
<td>0.999</td>
</tr>
<tr>
<td>229.53</td>
<td>4.224</td>
<td>969</td>
<td>387.4</td>
<td>2.4811</td>
<td>961.1781</td>
<td>99.19%</td>
<td>99.06%</td>
<td>1.45%</td>
<td>0.999</td>
</tr>
<tr>
<td>229.55</td>
<td>4.574</td>
<td>1049</td>
<td>387.4</td>
<td>2.6813</td>
<td>1038.736</td>
<td>99.02%</td>
<td>98.90%</td>
<td>1.39%</td>
<td>0.999</td>
</tr>
</tbody>
</table>
Figure 4. Efficiency of the PFC Stage at 230-V AC

Figure 5. THD at 230-V AC

Figure 6. PF at 230-V AC
3.2.1.2 Efficiency of the LLC stage

Table 5 shows the efficiency of the LLC stage with an open-loop test.

```
<table>
<thead>
<tr>
<th>V_in (V)</th>
<th>I_in (A)</th>
<th>V_o (V)</th>
<th>I_o (A)</th>
<th>P_o</th>
<th>Efficiency Without CTRL and DRV</th>
<th>Efficiency With CTRL and DRV</th>
</tr>
</thead>
<tbody>
<tr>
<td>386.1</td>
<td>0.324</td>
<td>12.182</td>
<td>10</td>
<td>122</td>
<td>97.38%</td>
<td>96.32%</td>
</tr>
<tr>
<td>386</td>
<td>0.641</td>
<td>12.149</td>
<td>20</td>
<td>243</td>
<td>98.20%</td>
<td>97.66%</td>
</tr>
<tr>
<td>386</td>
<td>0.959</td>
<td>12.127</td>
<td>30</td>
<td>364</td>
<td>98.28%</td>
<td>97.92%</td>
</tr>
<tr>
<td>386</td>
<td>1.276</td>
<td>12.103</td>
<td>40</td>
<td>484</td>
<td>98.29%</td>
<td>98.02%</td>
</tr>
<tr>
<td>385.9</td>
<td>1.594</td>
<td>12.07</td>
<td>50</td>
<td>604</td>
<td>98.11%</td>
<td>97.89%</td>
</tr>
<tr>
<td>385.9</td>
<td>1.911</td>
<td>12.038</td>
<td>60</td>
<td>722</td>
<td>97.94%</td>
<td>97.76%</td>
</tr>
<tr>
<td>385.8</td>
<td>2.227</td>
<td>12</td>
<td>70</td>
<td>840</td>
<td>97.77%</td>
<td>97.61%</td>
</tr>
<tr>
<td>385.8</td>
<td>2.5481</td>
<td>11.99</td>
<td>80</td>
<td>959</td>
<td>97.57%</td>
<td>97.44%</td>
</tr>
<tr>
<td>385.7</td>
<td>2.6751</td>
<td>11.96</td>
<td>84</td>
<td>1005</td>
<td>97.37%</td>
<td>97.24%</td>
</tr>
</tbody>
</table>
```

3.2.1.3 Efficiency of the Whole System

Table 6 shows the system efficiency of two stages without control loss.

```
<table>
<thead>
<tr>
<th>V_in (V)</th>
<th>I_in (A)</th>
<th>Pin (W)</th>
<th>THD (%)</th>
<th>PF</th>
<th>V_o (V)</th>
<th>I_o (A)</th>
<th>V_bus (V)</th>
<th>Efficiency Without DRV and CTRL (%)</th>
<th>P_drv (W)</th>
<th>Efficiency With only P_drv (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>229.96</td>
<td>0.558</td>
<td>126.8</td>
<td>7.45%</td>
<td>0.988</td>
<td>12.15</td>
<td>10</td>
<td>385.8</td>
<td>95.82%</td>
<td>1.56</td>
<td>94.66%</td>
</tr>
<tr>
<td>229.96</td>
<td>1.0933</td>
<td>250.4</td>
<td>4.25%</td>
<td>0.997</td>
<td>12.15</td>
<td>20</td>
<td>385.8</td>
<td>97.04%</td>
<td>1.56</td>
<td>96.44%</td>
</tr>
<tr>
<td>229.37</td>
<td>1.6352</td>
<td>374.7</td>
<td>2.11%</td>
<td>0.999</td>
<td>12.15</td>
<td>30</td>
<td>385.8</td>
<td>97.28%</td>
<td>1.56</td>
<td>96.87%</td>
</tr>
<tr>
<td>229.84</td>
<td>2.184</td>
<td>500</td>
<td>1.60%</td>
<td>0.999</td>
<td>12.16</td>
<td>40</td>
<td>386.0</td>
<td>97.28%</td>
<td>1.56</td>
<td>96.98%</td>
</tr>
<tr>
<td>228.65</td>
<td>2.738</td>
<td>626</td>
<td>1.54%</td>
<td>0.998</td>
<td>12.16</td>
<td>50</td>
<td>385.7</td>
<td>97.12%</td>
<td>1.56</td>
<td>96.88%</td>
</tr>
<tr>
<td>228.34</td>
<td>3.301</td>
<td>753</td>
<td>1.40%</td>
<td>0.999</td>
<td>12.16</td>
<td>60</td>
<td>386.0</td>
<td>96.89%</td>
<td>1.44</td>
<td>96.71%</td>
</tr>
<tr>
<td>228.01</td>
<td>3.867</td>
<td>881</td>
<td>1.36%</td>
<td>0.999</td>
<td>12.16</td>
<td>70</td>
<td>386.0</td>
<td>96.62%</td>
<td>1.44</td>
<td>96.46%</td>
</tr>
<tr>
<td>227.73</td>
<td>4.451</td>
<td>1013</td>
<td>1.31%</td>
<td>1.000</td>
<td>12.16</td>
<td>80</td>
<td>386.0</td>
<td>96.03%</td>
<td>1.5</td>
<td>95.89%</td>
</tr>
<tr>
<td>227.62</td>
<td>4.683</td>
<td>1066</td>
<td>1.14%</td>
<td>1.000</td>
<td>12.16</td>
<td>84</td>
<td>385.7</td>
<td>95.82%</td>
<td>1.56</td>
<td>95.68%</td>
</tr>
</tbody>
</table>
```
3.2.2 Functional Waveforms

3.2.2.1 Start-up

Figure 9 shows the no-load, start-up waveform. Figure 10 shows the half-load, start-up waveform.
3.2.2.2 Hall sensor

Figure 11 shows TMCS1100 Hall sensor's output correspond with AC input current.

Figure 12 shows the ADC sample value correspond with the actual current flow through primary of Hall sensor, which proves the hall sensor linearity is perfect.
Figure 11. TMCS1100 Hall sensing waveform

Figure 12. ADC value corresponding with actual current
3.2.2.3 **PFC Working Waveforms**

This section shows the PFC input and switching waveforms. Figure 13 and Figure 14 show the input voltage and current at 230-V AC input with no load and 20% load, and Figure 15 shows the switching waveform of the PFC stage with a GaN card.

**Figure 13. 230-V AC, No Load Input Voltage and Current**

**Figure 14. 230-V AC, 20% Load Input Voltage and Current**
3.2.2.4 **LLC Working Waveforms**

**Figure 15. PFC Switching Waveform**

**Figure 16. Current Ripple 50% Load**
Figure 17. Current Ripple 100% Load

Figure 18. Load Transient 0% - 50%
Figure 21. Load Transient 50% - 100%

Figure 22. LLC Stage Switching Waveform
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-010062.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-010062.

4.3 PCB Layout Recommendations
A careful PCB layout is critical in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting.

4.3.1 Power Stage Specific Guidelines
Follow these key guidelines to route the power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This will help reduce EMI and improve the converter's overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- Keep the power ground and control ground separate for each power supply stage. Tie them together (if they are electrically connected) in one point near the DC input return or output return of the given stage.
- When multiple capacitors are used in parallel for current sharing, the layout should be symmetrical across both capacitor leads. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents, and become hotter (I^2R).
- Tie the heat sinks of all of the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device that they are intended to protect, and route with short traces to reduce inductance.
- Choose the width of PCB traces based on an acceptable temperature rise at the rated current as per IPC2152, as well as acceptable DC and AC impedances. The traces should withstand the fault currents (such as short circuit current) before electronic protection devices, such as fuses or circuit breakers, are activated.
- Determine the distances between various traces of the circuit, according to the requirements of applicable standards. For this design, the UL 60950-1 safety standard is followed to maintain the creepage and clearance from live line, to neutral line, and to safety ground.
- Adapt the thermal management to fit the end equipment.

4.3.2 Gate Driver Specific Guidelines
Follow these key guidelines to route the high-frequency, high-current gate driver:

- Place the driver device as close as possible to the power device to minimize the length of high current traces between the output pins of gate drive and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD.
- Minimize the turn-on and turn-off current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) as much as possible to keep the stray inductance to a minimum.
- Minimize noise coupling with star point grounding from one current loop to another. Connect the driver GND to the other circuit nodes, such as the power switch source or the PWM controller ground, at one
single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

4.3.3 Layout Prints
To download the layer plots, see the design files at TIDA-010062.

4.4 Altium Project
To download the Altium Designer® project files, see the design files at TIDA-010062.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-010062.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-010062.

5 Software Files
To download the software files, see the design files at TIDA-010062.

6 Related Documentation
2. Texas Instruments, Designing an LLC Resonant Half-Bridge Power Converter Seminar
3. Texas Instruments, Resonant LLC Half-Bridge DC/DC Converter Software Design Guide
4. Texas Instruments, Resonant LLC Half-Bridge DC/DC Converter Hardware Design Guide
5. Texas Instruments, LMG341xR070 600-V 70-mΩ GaN with Integrated Driver and Protection Data Sheet
6. Texas Instruments, TMS320F28004x Piccolo™ Microcontrollers Data Manual

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7 About the Author
DESHENG GUO is a System Application Engineer at Texas Instruments, where he is responsible for developing customized power solutions as part of the power delivery, industrial segment. Desheng brings to this role his extensive experience in power electronics, power conversion, EMI/EMC, power and signal integrity, and analog circuits design spanning many high-profile organizations. He got his master degree from Harbin Institute of Technology with Power electronics in 2007, and has been working in DPEC of DELTA for many years, focusing on the high efficiency power supply's research and design.
# Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from A Revision (September 2019) to B Revision

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## Changes from Original (September 2019) to A Revision

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