*Design Guide: TIDA-010232*

# *AFE for Insulation Monitoring in High-Voltage EV Charging and Solar Energy Reference Design*

## Description

This reference design features an Electric Bridge DC Insulation Monitoring (DC-IM) method; which allows for an accurate symmetrical and asymmetrical insulation leakage detection mechanism, as well as an isolation resistance detection mechanism.

This design is based on a new generation of isolated amplifiers and switches which enable an isolated measurement without an additional isolated supply on the *hot side.* Instead the whole design is powered from the *cold side*. The insulation monitoring diagnostic can be added to an existing power conversion or charging protocol microcontroller (MCU).

## Resources

| | |
|---|---|
| TIDA-010232 | Design Folder |
| TPSI2140-Q1 | Product Folder |
| AMC3330 | Product Folder |
| TPS7A24 | Product Folder |
| REF2033 | Product Folder |
| TLV6001 | Product Folder |

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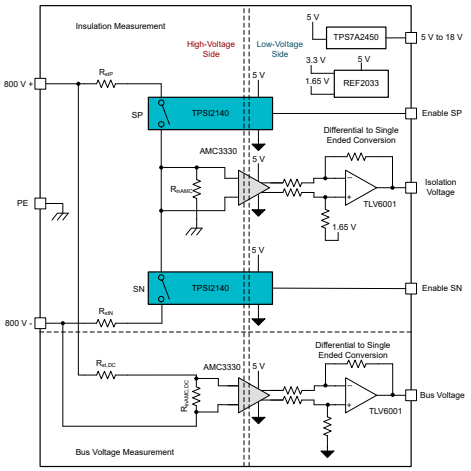
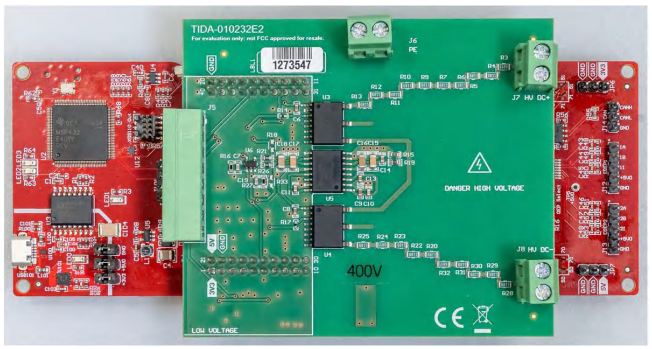
## Features

- Monitors isolation resistance and insulation leakage from DC to Protective Earth (PE)
- Method: switched in resistive divider to determine isolation resistance of DC+ or DC– to PE
- Reinforced isolated analog front end (AFE) with integrated power on *hot side* for MCUs sitting on the *cold side*
- BoosterPack™ Plug-in Module approach implemented for standalone insulation monitoring connected to LAUNCHXL-F280049C LaunchPad™ with isolated CAN transceiver and fast serial interface
- Isolation resistance measurement range:
  - 20 kΩ to 1 MΩ: 5% accuracy for symmetric faults
  - > 1 MΩ: Insulation good indication
  - 20 kΩ to 200 kΩ: 5% accuracy for symmetric and asymmetric faults
- Designed to support IEC 61557-8 and IEC 61851-23

## Applications

- String inverter
- DC-fast charging
- DC wallbox charger



# 1 System Description

The rapid adoption of electric vehicles in the market, along with the democratization of solar energy designs, is increasing the demand on systems for safe energy transmission.

Currently, high-voltage (HV) batteries of around 400 V are used as storage elements in electric cars, and there is a strong trend emerging towards higher voltage batteries, which allow for faster charge times. DC fast chargers supply power to the battery management system in the electric vehicle (EV) bypassing the onboard battery charger. This translates into HV DC lines flowing directly from the electric vehicle supply equipment (EVSE) to the vehicle. In the case of solar string inverters, there are HV DC lines coming from the photovoltaic (PV) string panels of up to 1 kV.

User protection is necessary in these kinds of HV DC distribution systems. All HV parts of the system are isolated to protective earth through high-omic paths. This insulation limits the maximum leakage current. International standards demand that the leakage current must be limited to 10 mA, to avoid personal injury from contact with the system. The insulation monitoring device monitors this insulation resistance and initiates a shutdown in case the insulation resistance is not sufficient.

Designers must consider the isolation requirements that apply to achieving basic or reinforced isolation (these can be determined based on line and peak voltages). Monitoring proper operation of the isolation barrier is mandatory for avoiding accidents.

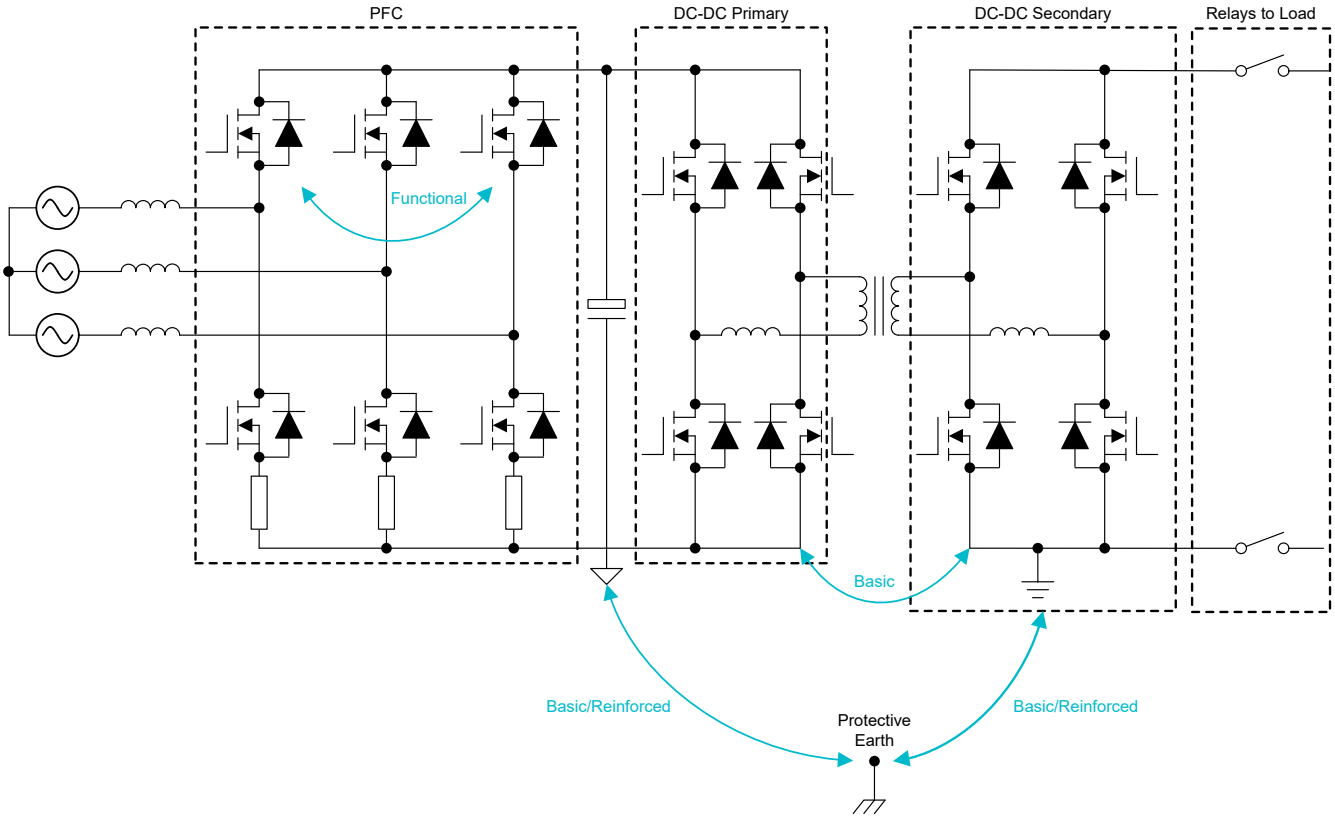



**Figure 1-1. Isolation Barrier in DC Unearthed Distribution Systems.**

Degradation or loss of isolation can occur due to many factors such as deterioration of the wire harnesses, general aging of power-handling components, or peak electrical stress on semiconductors. A single point of failure in regards to isolation does not have much impact on the operation of the system, but is a potential hazard when operators come in contact with the HV operating environment.

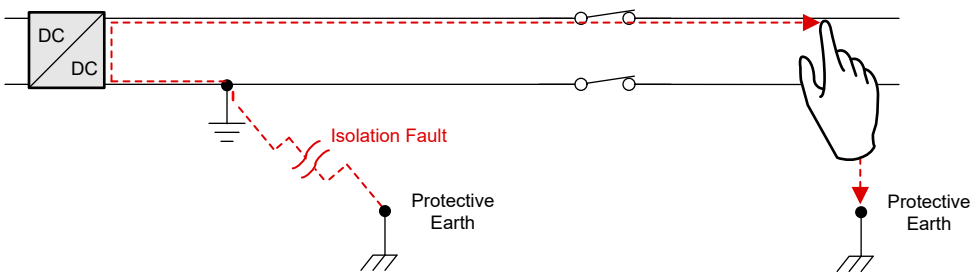



**Figure 1-2. Isolation Barrier Leakage in Unearthed DC Distribution Systems**

Unearthed power distribution systems such as DC fast-charging stations and solar string inverters, must be compliant with safety standards such as the IEC 61557-8: *"Electrical safety in low voltage distribution systems up to 1 000 V a.c. and 1 500 V d.c."*, which is further specified in IEC 61851-23 for DC fast charging stations.

These safety standards demand monitoring of the isolation barrier at regular intervals during energy transfer. In EVSE, charging protocols also establish insulation monitoring tests prior to charge. The idea is to prevent isolation barrier breakdowns that can lead to a fatal short.

As per the previously-mentioned standards, *warning* (500 Ω / V d.c. - 2mA); and *fault* (100 Ω / V d.c. - 10 mA) thresholds are set for the isolation barrier resistances. While the isolation barrier resistances do not fall under those limits, a proper condition is proven and no actions are expected.

If warning states are detected, visual indications through the *Human-Machine Interface* (HMI) trigger and then control actions are executed by the central control unit. If a fault state is detected, energy distribution stops.

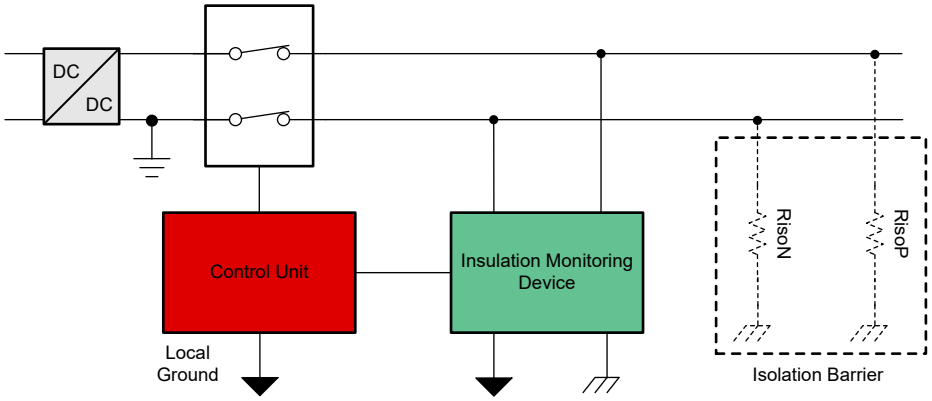



**Figure 1-3. Insulation Monitoring Device in DC Unearthed Distribution Systems**

This design is designed for 400-V systems by default, but can be adjusted to voltages up to 1000 V by modifying the resistor network of the switched-in resistive branch.

## 1.1 Insulation Monitoring

Various techniques coexist in the insulation monitoring market. The two most popular methods are AC current injection and an electric bridge switch.

The AC current injection method is based on generating a square wave signal that is injected into the RC circuit between the HV lines and Protective Earth (PE) through an RC filter or transformer. Impedance is computed based on charge and discharge of the capacitor. The main drawback of the AC current method is the difficulty on achieving a reliable and accurate design, as well as the need for a bulky transformer to isolate the injection circuit from the HV lines. The AC current method has the advantage that there is no influence of the isolation capacitance. See Section 1.2 for more information.

The electric bridge switch method is proposed in safety standards, such as the IEC 61851-23. The electric bridge switch method is where a known resistive branch is switched across the isolation barrier. In normal operation, no current flows through the resistor bridge because there is no path to PE. This indicates that the system is safe without any isolation breakages.

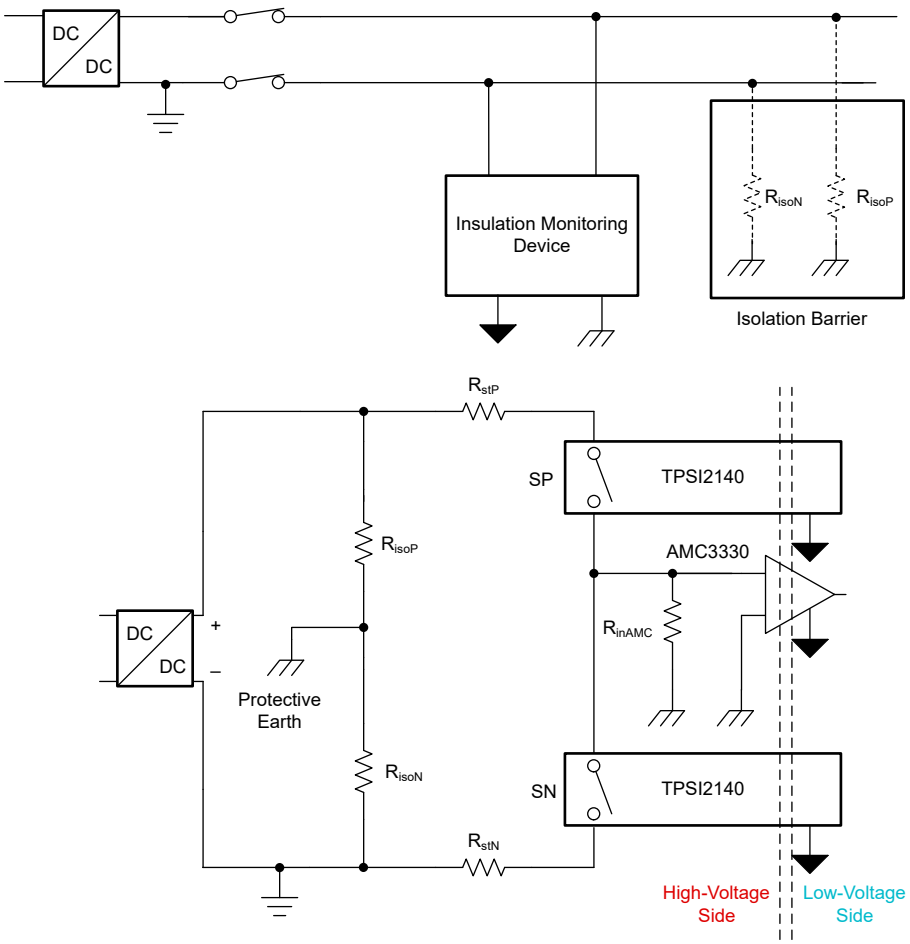



**Figure 1-4. Insulation Monitoring Analog Front End (Simplified)**

The design of electric bridge DC insulation monitoring is straightforward and accurate. No bulky transformers are needed, and only small amounts of power are dissipated across the isolation barrier during normal operation.

Apart from industrial *low-voltage distribution systems*, this is also the most popular design in automotive hybrid electric vehicles (HEV) and EV systems, where isolation is also a critical parameter.

As stated on the safety standards, limit the operating time of this resistive branch to less than ten seconds. This is due to the safety of the system being compromised while the circuit is in operation.

Figure 1-4 is an example of isolation breakdown measurement using this reference design. The negative side switch (SN) and positive side switch (SP) are implemented with the new TPSI2140 seamless relay isolated switches used to temporarily break the isolation barrier with the known resistive divider path.

$R_{stP}$ and $R_{stN}$ are ±0.1% high-resistance divider branches that are switched between DC+ and PE and DC– and PE respectively. $R_{inAMC}$ is the voltage sensing resistor that serves as the scaled-down voltage input to the AMC3330 reinforced isolated amplifier.

During measurement time, the two resistor branches are switched in at different times. Figure 1-5 shows the equivalent circuit when the SP is on while SN is kept off. The current across the isolation barrier, $I_{iso}$, is proportional to the bus voltage, the isolation resistances, and the resistive branch switched in.

Under normal conditions, where the isolation barrier is unbroken and the insulation resistance, $R_{isoN}$, between DC– and PE is in the order of MΩ, there is only a very small current flow over the switched-in resistor divider, leading to a small input signal at the AMC3330.

In case of deterioration of the isolation barrier, $I_{iso}$ increases which leads to a higher input signal at the AMC3330. The same behavior is true, depending on $R_{isoP}$, for the case where SN is closed and SP is opened.

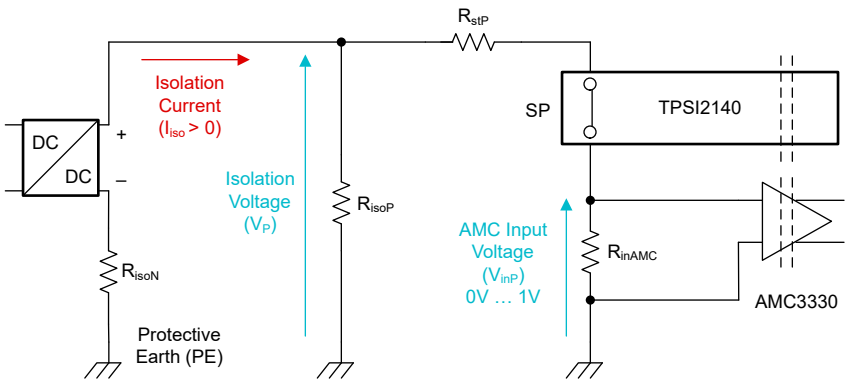



**Figure 1-5. Isolation Voltage on Positive Side Switch – Isolation Current**

To calculate the exact values for $R_{isoN}$ and $R_{isoP}$ the equivalent circuits shown in Figure 1-5 and Figure 1-6 are used.

When SP is closed while SN is opened, the leakage current creates a voltage in the resistive branch – here referenced as the *isolation voltage* $V_P$. According to Kirchhoff's voltage law, Equation 1 can be derived.

$$I_{iso} \times R_{isoN} - V_{DC} + V_P = 0 \tag{1}$$

Solving for $V_P$ Equation 2 is the result.

$$V_p = V_{DC} - I_{iso} \times R_{isoN} \tag{2}$$

The leakage current across the isolation barrier is given by Equation 3:

$$I_{iso} = \frac{V_P}{R_{isoP} \;||\; (R_{stP} + R_{inAMC})} \tag{3}$$

Substituting Equation 2 and Equation 3:

$$V_P \times \left(1 + \frac{R_{isoN}}{R_{isoP} \;||\; (R_{stp} + R_{inAMC})}\right) - V_{DC} = 0 \tag{4}$$

Hence, the value of the *isolation voltage* that is served *scaled down* to the AMC3330 ±1-V range through $R_{inAMC}$ is given by Equation 5.

$$SP \;\; closed \rightarrow V_P = \frac{V_{DC}}{\left(1 + \frac{R_{isoN}}{R_{isoP} \;||\; (R_{stp} + R_{inAMC})}\right)} \tag{5}$$

$V_P$ can be calculated from the measurement of $V_{inP}$ with Equation 6.

$$V_P = V_{inP} \times \frac{R_{stP} + R_{inAMC}}{R_{inAMC}} \tag{6}$$

Similar equations are found for the reverse state where SP is opened and SN is closed.

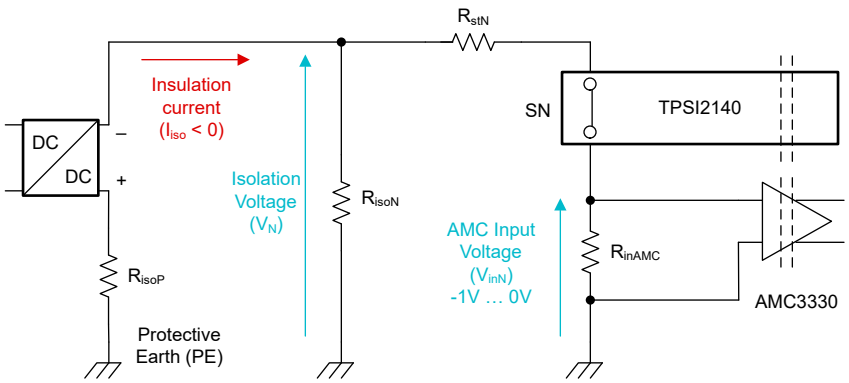



**Figure 1-6. Isolation Voltage on Negative Switch – Isolation Current**

In this case the sign of $V_{DC}$ is changed since for this equivalent circuit the polarity of the DC connection changes, which also leads to a negative isolation current $I_{iso}$.

$$I_{iso} \times R_{isoP} + V_{DC} + V_N = 0; \quad (7)$$

$$V_N = -V_{DC} - I_{iso} \times R_{isoP} \quad (8)$$

$$I_{iso} = \frac{V_N}{R_{isoN} // (R_{stN} + R_{inAMC})} \quad (9)$$

$$V_N \times \left(1 + \frac{R_{isoP}}{R_{isoN} \;||\; (R_{stN} + R_{inAMC})}\right) + V_{DC} = 0 \quad (10)$$

$$SN \;\; \text{closed} \rightarrow V_N = \frac{-V_{DC}}{\left(1 + \frac{R_{isoP}}{R_{isoN} \;||\; (R_{stN} + R_{inAMC})}\right)} \quad (11)$$

$$V_N = V_{inN} \times \frac{R_{stP} + R_{inAMC}}{R_{inAMC}} \quad (12)$$

From Equation 7 through Equation 11, the isolation resistances between the DC lines and PE can be computed as with the assumption $R_{stP} = R_{stN} = R_{st}$:

$$R_{isoP} = \frac{-(R_{inAMC} + R_{st}) \times (V_{DC} + V_N - V_P)}{V_N} \quad (13)$$

$$R_{isoN} = \frac{(R_{inAMC} + R_{st}) \times (V_{DC} + V_N - V_P)}{V_P} \quad (14)$$

The polarity of the isolation voltage observed at $R_{inAMC}$ for the negative case, is the opposite of when the resistive branch is switched in for the positive case. AMC3330 is a good fit here, because of the bipolar input voltage range.

## 1.2 Impact of Parasitic Isolation Capacitance

In an unearthed power distribution system, the isolation barrier protects the user and components sitting on the low-voltage side by preventing high currents flowing to protective earth. The isolation barrier is expected to be of a resistive nature. Nevertheless, some factors such as improper earth connection or humidity can increase the isolation capacitance to earth of the system.

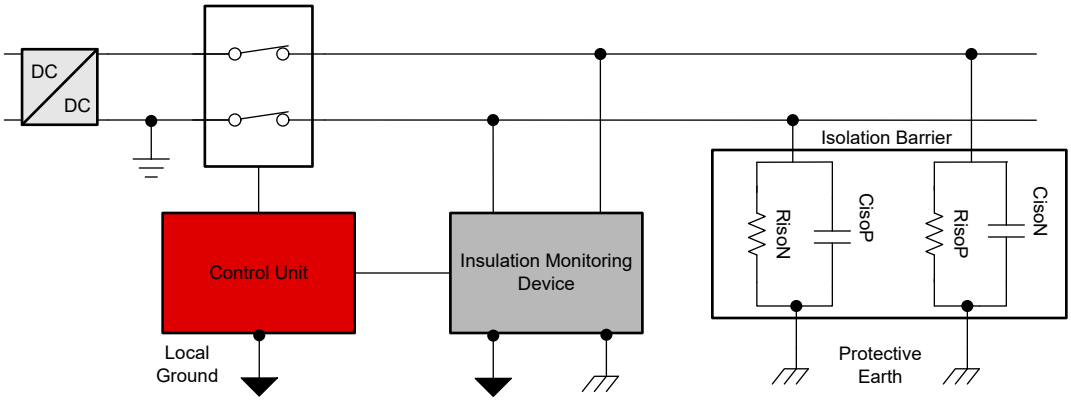



**Figure 1-7. Isolation Barrier Capacitance Effect on Insulation Monitoring Device**

In this system, under proper operation or asymmetrical fault of the isolation barrier, this static capacitance to earth forces a delay in the settling time of the isolation voltage when the resistive branch is switched in. A period of wait time must occur after the resistive branch is switched in and before the measurement of the insulation voltage is done. This reduces overall measurement speed in systems with higher insulation capacitance. The time constant of the resulting RC circuit is shown in Equation 15, assuming $R_{isoN}$ is small and $R_{isoP}$ is high.

$$\tau = (R_{isoP} // R_{stP}) \times C_{isoP} \quad (15)$$

As an example, in case of a insulation capacitance of 10 nF and a $R_{stP}$ of 68.1 kΩ, as observed on the 400-V version of this design, and $R_{isoP}$ of 10 MΩ, a time constant of 676 µs is the result. A delay between the closing of the switch and the start of the measurement of at least 3 τ is recommended to let the voltage settle to 95% of the final value.

By allowing higher currents across the isolation barrier through the switched-in resistive branch, faster settling times can be achieved. The current through the switched-in branch $I_{st}$ can be calculated using Equation 15

$$I_{st} = \frac{V_{Bus}}{(R_{stP} + R_{inAMC})} \quad (16)$$

Hence, consider the tradeoff between faster settling times and power dissipation when designing a resistive divider branch, while keeping the maximum allowed current in mind. Further details on the implementation in this reference design are found in Section 2.3.

## 1.3 IEC 61557-8 Standard for Industrial Low-Voltage Distribution Systems

The purpose of this design is to offer an analog front-end for isolation barrier monitoring in unearthed industrial low-voltage distribution systems, such as DC fast-charging stations or solar string inverters. As per the safety standards, these systems include equipment for testing the isolation barrier compliant with the IEC 615578-8 standard. For more details on the IEC 615578-8 standard, see the IEC Webstore.

The circuit is designed to support IEC 615578-8:

- Monitor the insulation resistance from DC lines to PE at regular intervals
- Ground warning current is defined as 2 mA, which results in an isolation resistance of 500 Ω/V
- Ground fault current is defined as 10 mA, which results in an isolation resistance of 100 Ω/V
- Symmetrical and asymmetrical warning and fault detection
- Isolation resistance monitoring accuracy < 15%
- Measurement time < 10 s
- Thermal stability (–5°C to +45°C)
- Method proposed: switched-in resistive divider branch to determine isolation resistance of DC+, DC– vs PE
- Test function: Report fault connections (to DC line or to PE)

This reference design offers additional advantages such as a reinforced isolated AFE with no external supply on the secondary. This allows the MCU to sit on the *cold side* and foster lower power consumption.

## 1.4 Key System Specifications

**Table 1-1. Key System Specifications**

| PARAMETER | SPECIFICATION | MEASUREMENT(1) |
|---|---|---|
| Isolation voltages accuracy | 1% | 0.37% |
| Isolation voltage settling time at ADC input | 400 µs | 300 µs(2) |
| Isolation resistances | 20 kΩ < RISO < 5 MΩ | |
| Symmetrical fault (40 kΩ) | 5% | 1.54% |
| Asymmetrical fault (40 kΩ) | 5% | 3.63% |
| Symmetrical warning (200 kΩ) | 5% | 1.51% |
| Asymmetrical warning (200 kΩ) | 5% | 3.78% |

(1) 400-V system, uncalibrated gain and offset, 0.1% accurate resistors, room temperature
(2) Test system with negligible insulation capacitance. For systems with higher insulation capacitance see Section 1.2.

**Table 1-2. Key Electrical Specifications**

| PARAMETER | VALUE | COMMENT |
|---|---|---|
| DC input voltage | 5 V ±5% (typical)<br>5 V to 12 V | 5-V input can come from the LAUNCHXL-F280049C break-out power output, current limited by LMR6242, nominal rating 2.1 A.<br>If evaluation without the LAUNCHXL-F280049C takes place, the board can also be powered from a 5- to 12-V voltage source through the front connector. |
| DC input current | 50 mA (typical) | When the switches are on and the bus voltage monitoring is used |
| Power consumption | 0.25 W (typical) | Total board consumption, measured on the 5-V supply |
| I/O interface signaling voltage | 3.3 V | 3.3-V fail-safe I/O. Compatible with the TI LaunchPad Development Kit |
| Temperature range | –40°C to 85°C | Industrial temperature range –40°C to 85°C |

**CAUTION**

*Do not leave the design powered when unattended.*

**WARNING**

**High voltage!** There are *accessible high voltages present on the board*. Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

**WARNING**

**Hot surface! Contact can cause burns. Do not touch!**

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

**WARNING**

TI intends this reference design to be operated in a ***lab environment only and does not consider the reference design to be a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board***. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

# 2 System Overview

## 2.1 Block Diagram

Figure 2-1 shows the TIDA-010232 block diagram

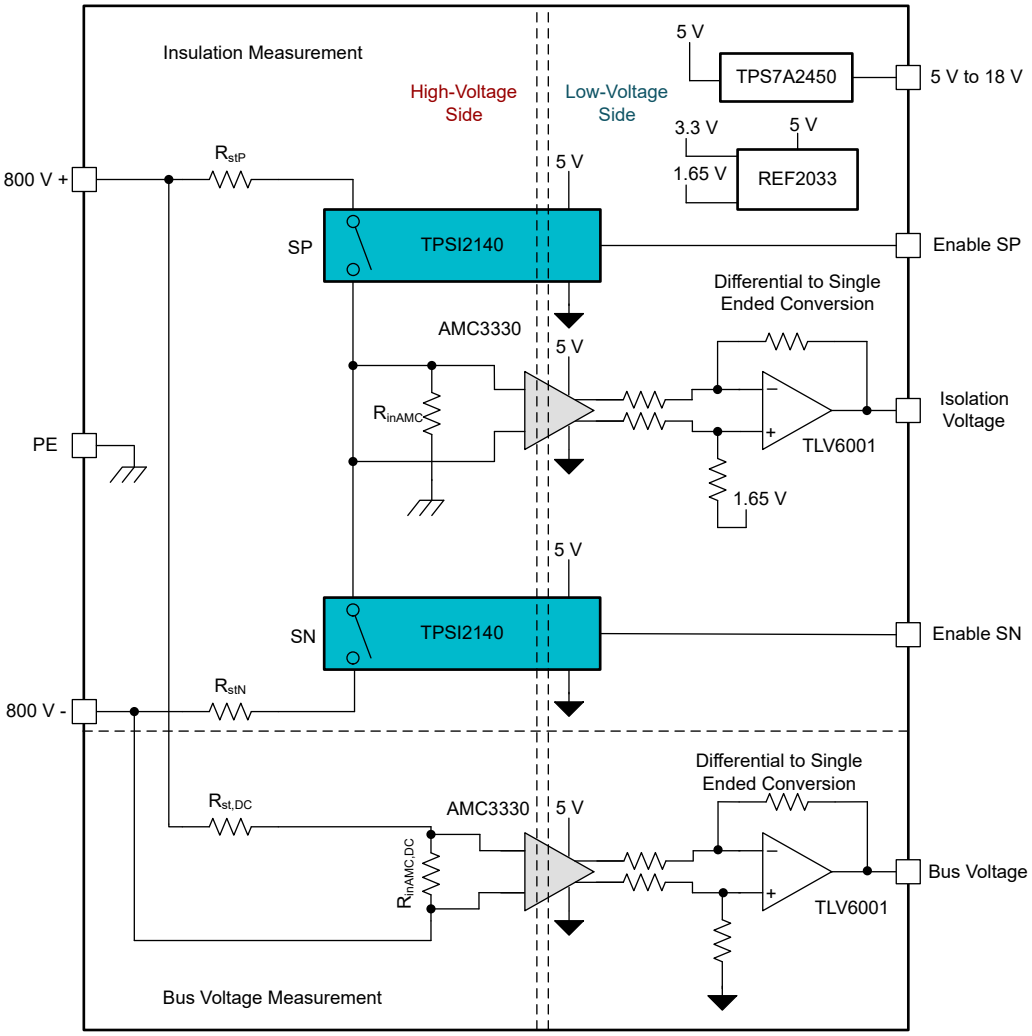



**Figure 2-1. TIDA-010232 Insulation Monitoring Analog-Front-End Block Diagram**

## 2.2 Highlighted Products

### 2.2.1 TPSI2140

The TPSI2140-Q1 is an isolated solid-state relay that utilizes TI's high reliability capacitive isolation technology in combination with internal back to back MOSFETs to form a completely integrated solution requiring no secondary side power supply. The primary side consists of four differential drivers that deliver power and enable logic information to each of the internal MOSFETs on the secondary side.

When the enable pin is brought HI, the oscillator starts causing the drivers to send power and a logic HI across the barrier. When the enable pin is brought LO, the drivers are disabled. On the secondary side, each MOSFET has a full-bridge rectifier to feed a band pass amplifier and demodulator that determines the logic state delivered by the primary side. The slew rate drivers control the gate of the MOSFET according to the logic delivered.

The avalanche robust MOSFETs and thermally conscious package design allow it to survive system-level High Potential (HiPot) Screening and DC fast charger surge currents of up to 2 mA without requiring any external components. The Thermal Avalanche Protection (TAP) feature included in the TPSI2140T-Q1 devices further improve the avalanche current capability by monitoring the junction temperature and enabling the MOSFETs to keep the temperature in a safe operating range.

Key features include:

- AEC-Q100 qualified with –40°C to 125°C ambient operating temperature
- Capacitive isolation barrier up to 3750 $V_{RMS}$, 5300 $V_{DC}$
- 1200-V standoff voltage across secondary S1, S2 switch terminals
- Creepage and clearance ≥ 8 mm (primary-secondary)
- Creepage and clearance ≥ 6 mm (across S1, S2 switch terminals)
- Low power consumption: < 9-mA input current

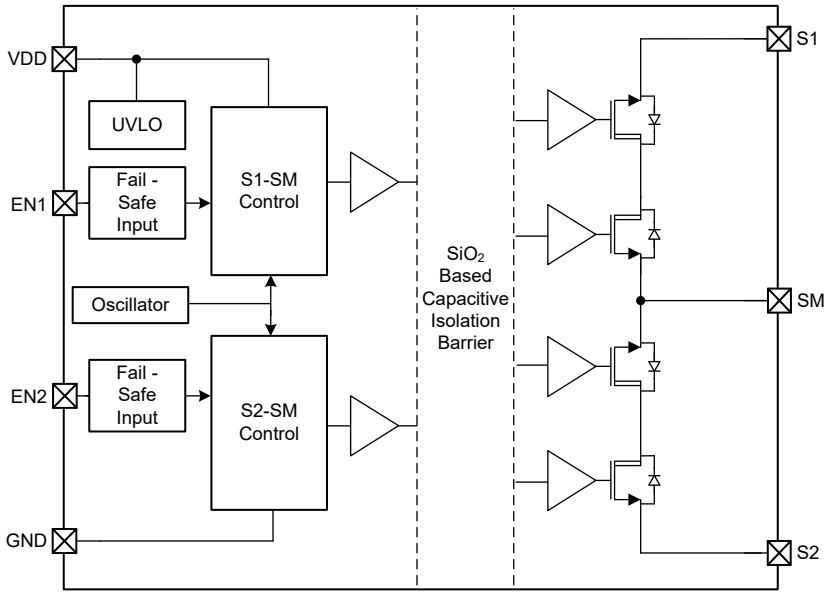



**Figure 2-2. TPSI2140 Functional Block Diagram**

### 2.2.2 AMC3330

The AMC3330 is a fully-differential precision isolated amplifier with high-input impedance, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage supply source from the low voltage side. The input stage of the device drives a 2$^{nd}$-order, delta-sigma (ΔΣ) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a 4$^{th}$-order analog filter on the low-side and presented as a differential analog output.

Figure 2-3 shows the AMC3330 block diagram. The 1.2-GΩ differential input impedance of the analog input stage supports low gain-error signal-sensing in high-voltage applications using high-impedance resistor dividers. The signal path is isolated by a double capacitive silicon-dioxide (SiO 2) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

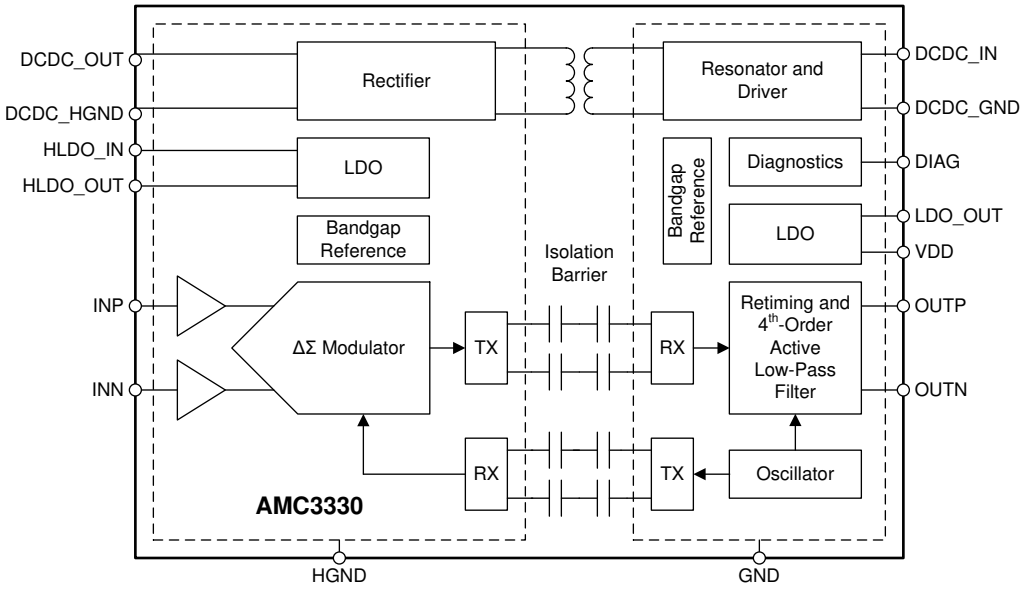



**Figure 2-3. AMC3330 Functional Block Diagram**

### 2.2.3 TPS7A24

The TPS7A24 is an 18-V, low quiescent current, low-dropout (LDO) linear regulator. The low $I_Q$ performance makes the TPS7A24 an excellent choice for battery-powered or line-power applications that are expected to meet increasingly stringent standby-power standards. The fixed-output versions have the advantage of providing better accuracy with fewer external components, whereas the adjustable version has the flexibility for a far wider output voltage range.

The 2% accuracy overtemperature makes this device an excellent choice for meeting a wide range of microcontroller power requirements.

For increased reliability, the TPS7A24 also incorporates overcurrent, overshoot pulldown, and thermal shutdown protection. The operating junction temperature is –40°C to +125°C, which adds margin for applications concerned with higher working ambient temperatures.

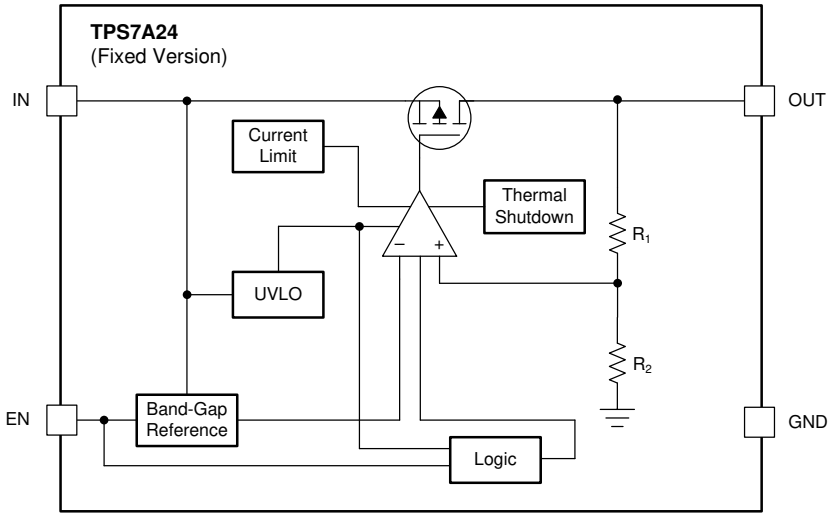



**Figure 2-4. TPS7A24 Functional Block Diagram**

### 2.2.4 REF2033

The REF20XX are a family of dual-output, VREF and VBIAS (VREF / 2) band-gap voltage references. Figure 2-5 provides a block diagram of the basic band-gap topology and the two buffers used to derive the VREF and VBIAS outputs. Transistors Q1 and Q2 are biased such that the current density of Q1 is greater than that of Q2 . The difference of the two base emitter voltages (VBE1 – VBE2) has a positive temperature coefficient and is forced across resistor R5 . The voltage is amplified and added to the base emitter voltage of Q2 , which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate VREF and VBIAS from the band-gap voltage. The resistors R1 , R2 and R3 , R4 are sized such that VBIAS = VREF / 2.

The e-Trim™ integrated circuit, which is a method of package-level trim for the initial accuracy and temperature coefficient of VREF and VBIAS, implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the VREF and VBIAS outputs.

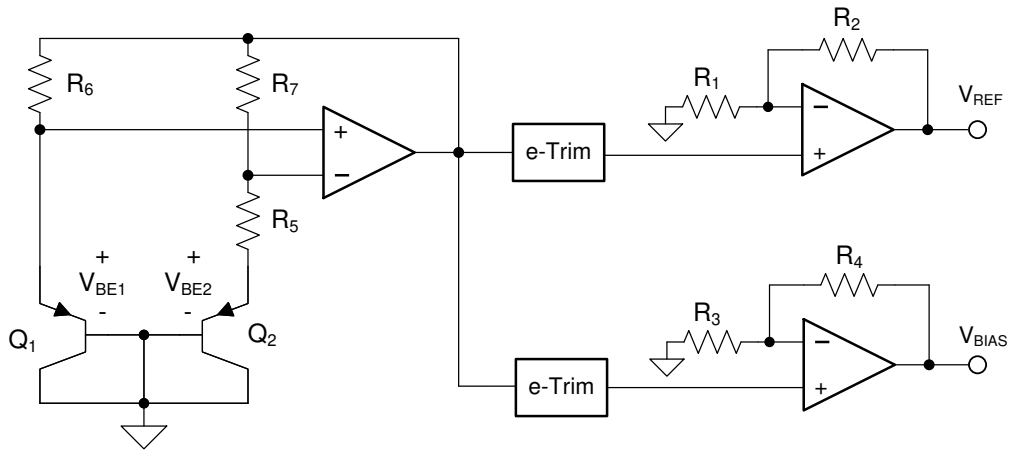



**Figure 2-5. REF2033 Functional Block Diagram**

### 2.2.5 TLV6001

The TLV600x family of operational amplifiers are general-purpose, low-cost devices that are suitable for a wide range of portable applications. Rail-to-rail input and output swings, low quiescent current, and wide dynamic range make the op amps well-suited for driving sampling analog-to-digital converters (ADCs) and other single-supply applications.

## 2.3 Design Considerations

In this chapter different submodules of the reference design are described, explaining component selection considerations and circuit design processes.

### 2.3.1 Resistive Bridge

As explained in Section 1, isolation and a high-voltage bus monitoring circuit is implemented in the schematics and printed-circuit board (PCB). Hardware that measures isolation resistance and leakage current is built with a temporary isolation breaking circuit.

Figure 2-6 shows that $R_{stP}$ consists of R3, R4, R5, R6, R7, R9, R10, R11, R12, and R13, whereas $R_{stN}$ consists of R29, R30, R31, R32, R28, R22, R23, R24, R25, and R20, while $R_{inAMC}$ is implemented in R15. Thin film resistors are chosen because these resistors have less tolerance, high reliability, and a low temperature coefficient of resistance (TCR). Any deviation in resistor values has an impact on the error of interlock leakage current and isolation resistance calculations. Multiple resistors are chosen to reduce the maximum voltage stress and limit the maximum power dissipation per resistor.

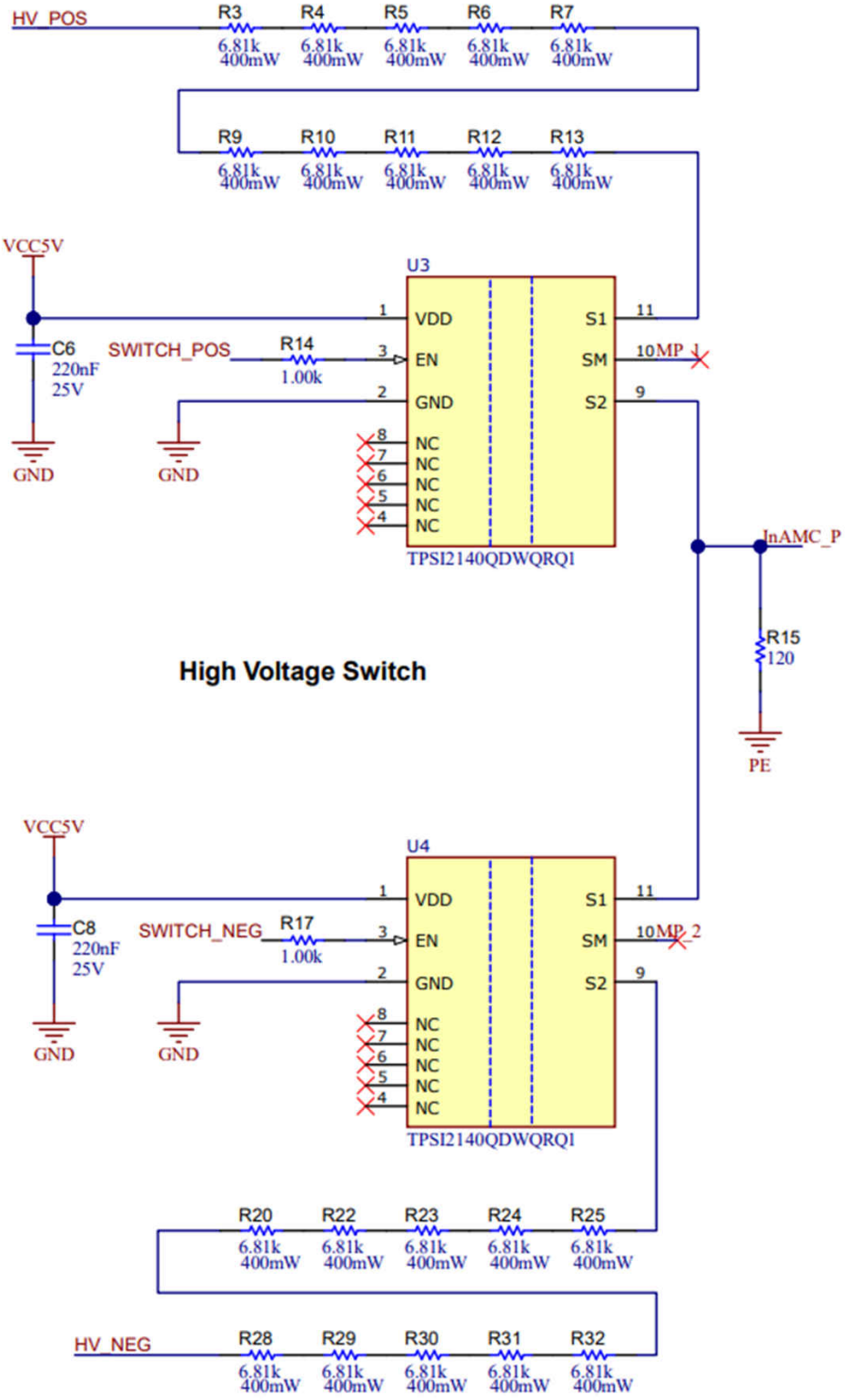



**Figure 2-6. Schematic High-Voltage Resistive Bridge**

DC fast chargers supply power to 400-V or 800-V battery management systems bypassing the onboard battery charger. Conversely, in string inverters, DC lines coming from the PV string panels go up to 1 kV.

The resistive bridge shown in Figure 2-6 is designed for a 400-V application. In the worst-case situation, the insulation voltage across the restive divider formed by $R_{stP}$ and $R_{inAMC}$ is equal to the bus voltage of 400 V.

As Equation 17 shows, this leads to a maximum input voltage of 0.7 V at the AMC3330 for the selected values of $R_{st\,P}$ = 68.1 kΩ and $R_{RinAMC}$ = 120 Ω.

$$V_{inAMC} = V_{BUS} \times \frac{R_{inAMC}}{R_{inAMC} + R_{stP/N}} \quad (17)$$

The current allowed through the resistive bridge and the insulation capacitance determines the delay time in the isolated voltage. Further details are found in Section 1.2.

### 2.3.2 Isolated Analog Signal Chain

As a first part of the signal chain, the AMC3330 amplifies the measured voltage and provides the necessary isolation barrier, to protect the system from the high voltages. The ±2.05-V differential output signal of the AMC3330 is converted to a signal-ended 0-V to 3.3-V signal using the TLV6001 in a difference amplifier configuration, which is described in Section 2.3.2.1.

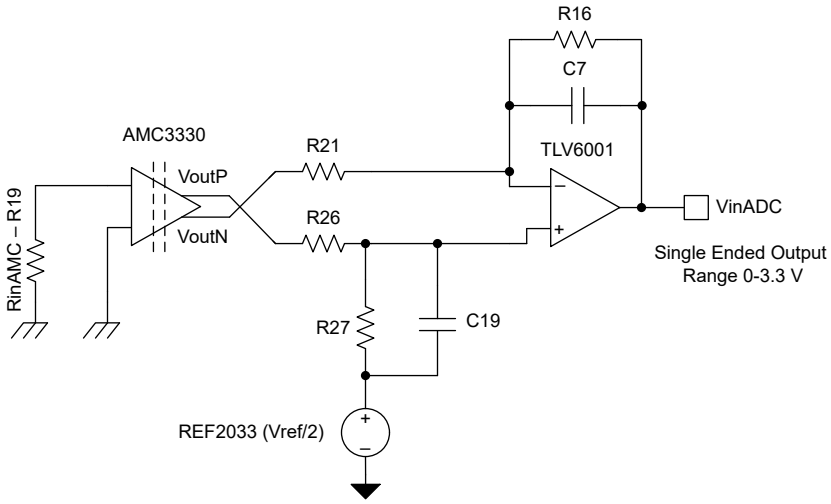



**Figure 2-7. Isolated Analog Signal Chain**

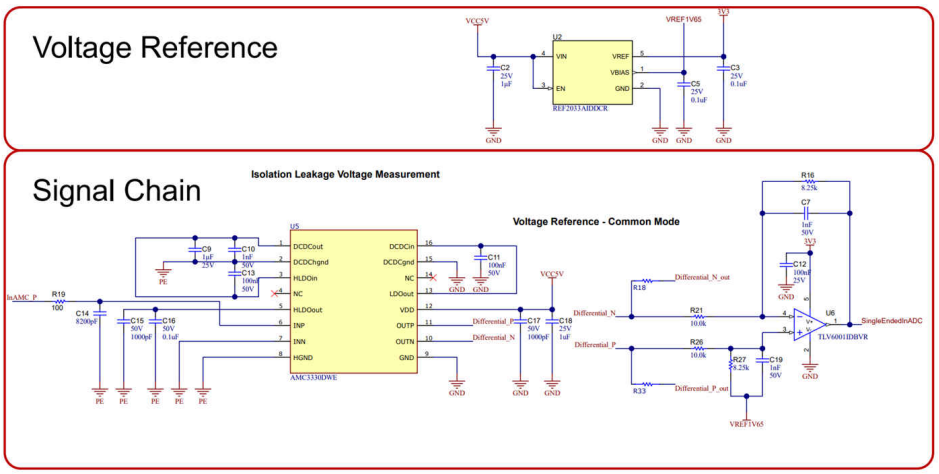



**Figure 2-8. Schematic Isolated Analog Signal Chain + Reference**

The output voltage of the differential to single-ended conversion is fed into a internal ADC of the C2000 microcontroller. The measured voltage at the ADC can be converted back to the insulation voltage using Equation 18:

$$V_{isolation} = \frac{V_{inADC} - V_{ref}}{Gain_{diff2single}} \times \frac{R_{inAMC} + R_{st}}{R_{inAMC}} \times \frac{1}{Gain_{AMC}} \quad (18)$$

where

- $V_{isolation}$ is the actual isolation voltage monitored
- $V_{inADC}$ is the voltage at the input of the ADC
- $V_{ref}$ is the 1.65-V voltage reference coming from REF2033
- $Gain_{diff2single}$ is the differential-to-single ended gain set with the resistor divider, as explained in Section 2.3.2.1
- $Gain_{AMC}$ is the gain of the AMC3330 which is a fixed gain of 2.0
- $R_{st}$ is the switched resistive bridge equivalent resistance($R_{stP}$ = $R_{stN}$ = $R_{st}$)
- And $R_{inAMC}$ is the resistor that serves the scaled down isolation voltage to the input of the AMC3330

### *2.3.2.1 Differential to Single-Ended Conversion*

As stated, the isolation voltage is monitored with an AMC3330 across the isolation barrier. The output of the AMC3330 is a fully-differential analog signal comprised of the OUTP and OUTN pins centered around a common-mode voltage of 1.44 V that can be fed directly to a stand-alone analog-to-digital converter (ADC).

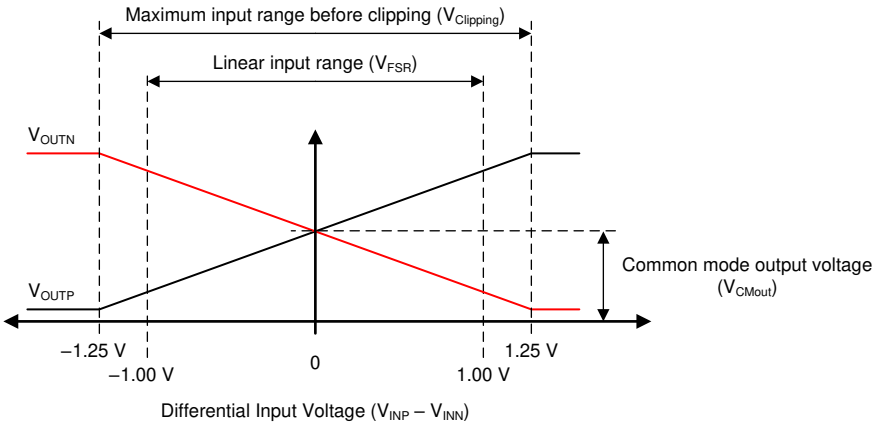



**Figure 2-9. AMC3330 Output Behavior**

The MSP430 and C2000 family of processors have embedded single-ended input ADCs. The addition of a differential to single-ended amplifier output stage, illustrated in Figure 2-10, allows the full output range of the AMC3330 to be converted to the 3.3-V range which is designed for the single-ended embedded ADC. The signal range is amplified, and the common-mode voltage is set to half of the ADC range using 1.65 V provided by REF2033.

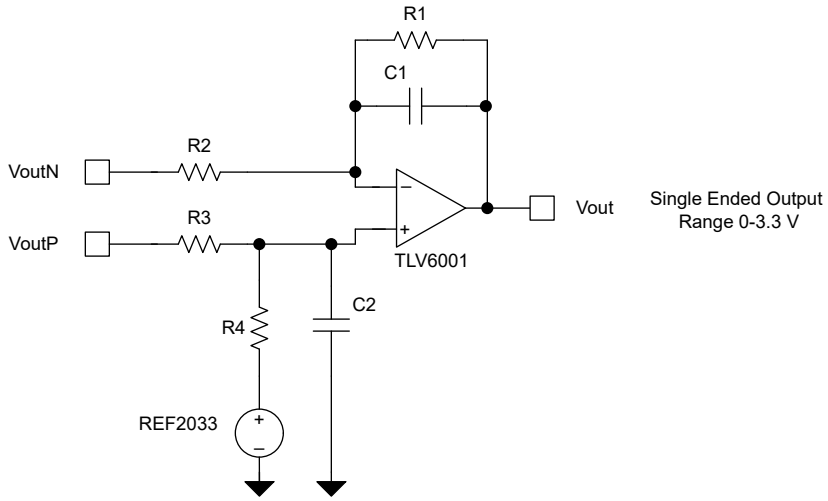



**Figure 2-10. Differential to Single-Ended Conversion – Output AMC3330**

If R1 = R4 and R2 = R3 Equation 19 describes the behavior of the differential-to-single-ended conversion.

$$V_{out} = V_{outP} \times \frac{R4}{R3} - V_{outN} \times \frac{R1}{R2} + V_{ref} \quad (19)$$

The TLV6001 operational amplifier for cost-sensitive systems is used for this purpose. Further details on the TI isolated amplifier family differential output conversion to singled ended are found in the *Interfacing a Differential-Output (Isolated) Amplifier to a Single-Ended Input ADC* application brief.

The AMC3330 has a maximum output voltage swing of ±2 V. This has to be translated to a single-ended signal between 0 V and 3.3 V. Hence, a gain of 0.825 is set with the ratio of R1/R2 and R4/R3. The common-mode voltage of 1.65 V is set with the Vref / 2 output of the REF2033 voltage reference.

#### *2.3.2.2 High-Voltage Measurement*

The high bus-voltage value is required to calculate the isolation leakage current and isolation barrier resistances. The bus voltage monitoring is an optional feature to the insulation monitoring AFE, as in low-voltage distribution systems, the bus voltage is monitored for loop compensation features. If the insulation monitoring feature is not a standalone design, and the analog front end is integrated into the power conversion stage or the central unit of the system, the bus voltage monitoring feature does not have to be duplicated.

In reference designs such as TIDA-01541, TI's isolated amplifiers are used to perform these measurements. The new AMC3330 is specifically designed for HV measurements because the device provides reinforced isolation, high-input impedance, 2-V input range, and integrated DC-to-DC to avoid external supply on the hot side.

As Figure 2-11 shows, the $R_{inAMC,DC}$ (R47) monitoring resistor is placed in series to a high-ohmic potential divider network (R34, R35, R36, R37, R38, R39, R41, R42, R43). Voltage measurements are performed with the floating ground of the AMC3330. The AMC3330 can measure a bidirectional signal of ±1 V. In EVSE and solar string inverters, bus voltages are only in the positive range, so the usable range of the AMC3330 is +1 V. A potential divider network must be chosen in such a way that the voltage drop in shunt resistance must be ≤ 1 V at the maximum bus voltages. The TLV6001 device is used to amplify the signal range and give a single-ended output to an MCU or logic interface, see Section 2.3.2.1 for further details.

Equation 20 is a simple equation that does not consider the influences of bias currents or offset voltages, which can lead to deviations in measurements.

$$HV_{Bus} = \frac{V_{Out,\,DC(TLV6001)} \times \left(R_{st,\,DC} + R_{inAMC,\,DC}\right)}{R_{inAMC,\,DC} \times Gain_{AMC3330} \times Gain_{Dif2Sing,\,DC}} \quad (20)$$

where

- $V_{Out,DC(TLV6001)}$ is the output voltage measured by the ADC or relevant device from the output of the TLV6001 in the bus voltage measurement path
- $R_{ST,DC}$ is the sum of the series resistors from positive to negative bus voltage
- $Gain_{AMC3330}$ is the gain of the AMC3330 internal circuit
- $Gain_{Dif2Sing,DC}$ is the gain set by the external resistors for the TLV6001 circuit

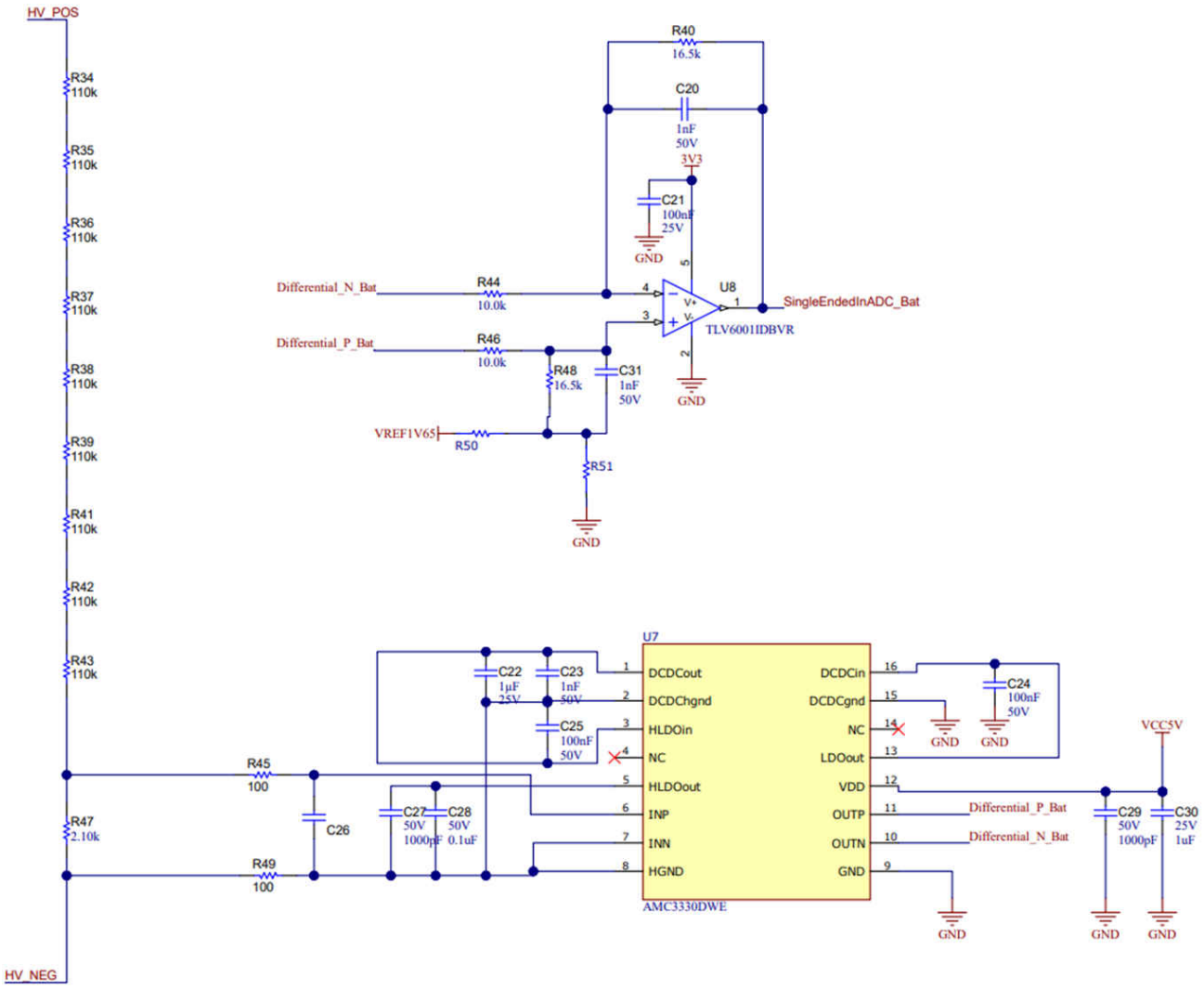



**Figure 2-11. Schematic High-Voltage Bus Monitoring**

To enable the insulation monitoring for AC unearthed systems, the reference design gives the option of bringing the REF2033 Vref / 2 as common-mode voltage to the differential-to-single-ended conversion. Hence, when evaluating in AC line systems, a jumper enables the design to shift up the common-mode voltage and the negative side of the wave is brought at the input of the ADC. The user can evaluate in AC systems by changing the common-mode voltage reference jumper and the resistors gain accordingly.

#### 2.3.2.3 Signal Chain Error Analysis

The conditioning can be done through the calculation tool *Isolated Amplifier Voltage Sensing Excel Calculator*. The tool offers a detailed worst-case error analysis across temperature considering gain error and drift, and offset error and drift, and non-linearity drift. Note that the error analysis is output referenced.

The main sources of error in the signal chain are the resistor tolerances, gain and offset errors off the AMC3330, and gain and offset errors in the differential-to-single-ended conversion circuitry. There is another TIDA-010232 specific worst-case error calculation excel sheet available on the reference design page. This sheet assumes the absolute worst-case for each parameter in the signal chain and finds the combination of these which results in the worst accuracy. As shown in Section 3.5, the actual measured accuracy is in most cases better than the worst-case assumption.

If higher accuracy is desired, precision op amps can be used for the differential-to-single-ended conversion, such as the TLV6001 pin-to-pin compatible OPA320 ($V_{offset}$ 0.15 mV). To improve accuracy even further, the differential-to single-ended conversion can be removed by choosing a dedicated differential input ADC instead of the internal ADC of the C2000 microcontroller.

### 2.3.3 Loss of PE Detection

In many systems, testing the connection of the PE to the insulation monitoring device is mandatory. The reason is that if the PE connection is lost, there is no current flowing through the switched-in measurement branch, resulting in no voltage at the input of the AMC3330. This is interpreted as an infinite insulation resistance, and possible insulation breakdowns can no longer be detected as shown in Figure 2-12.

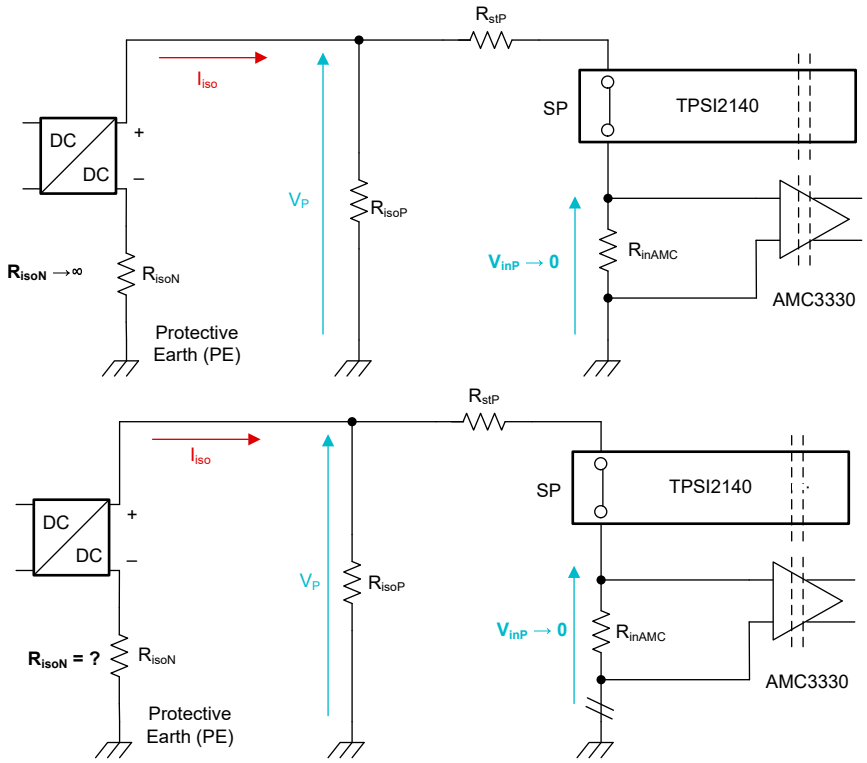



**Figure 2-12. Problem of Lost PE Connection**

To avoid a lost connection, implement a method to detect a loss of PE connection.

Such a method can be implemented by adding two known resistors between DC+ and PE and DC– and PE in the low MΩ range as shown in Figure 2-13.

**Note**

These additional resistors must have a separate connection to PE.

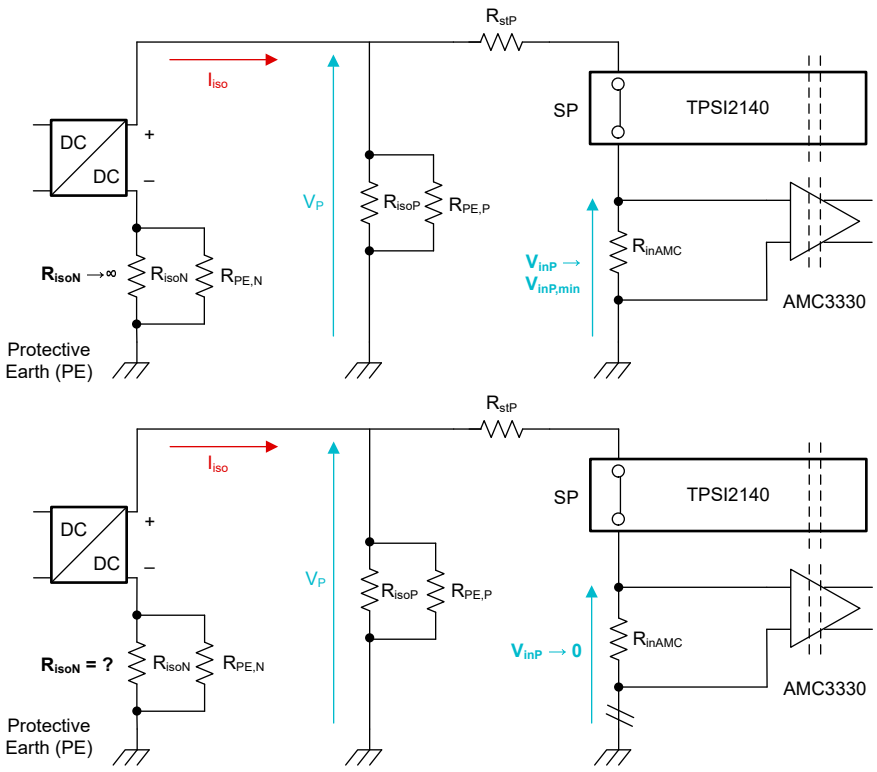



**Figure 2-13. Equivalent Circuit With Added Resistors for Detecting Loss of PE**

These resistors are in parallel to the parasitic insulation resistances, which limits the upper value of the insulation resistance. With a fixed limited insulation resistance, the input voltage at the AMC3330 can only drop below a certain value if the PE connection is valid.

With the additional resistors across DC+ to PE and DC– to PE, the calculations of the remaining insulation resistance must be adjusted accordingly. The original Equation 13 and Equation 14 for $R_{isoN}$ and $R_{isoP}$ are used now to calculate the parallel resistance of $R_{isoP}$ || $R_{PE,P}$ and $R_{isoN}$ || $R_{PE,N}$. The values for $R_{isoN}$ and $R_{isoP}$ can be calculated by using Equation 21 and Equation 21.

$$R_{isoN} = \frac{R_{PE,N} \times \left(R_{isoN} \left|\right| R_{PE,N}\right)}{\left(R_{PE,N} - \left(R_{isoN} \left|\right| R_{PE,N}\right)\right)} \tag{21}$$

$$R_{isoP} = \frac{R_{PE,P} \times \left(R_{isoP} \left|\right| R_{PE,P}\right)}{\left(R_{PE,P} - \left(R_{isoP} \left|\right| R_{PE,P}\right)\right)} \tag{22}$$

If the design cannot feasibly have a high-omic resistor permanently connected between the DC lines and PE, there is the option to add another pair of TPSI2140 isolated switches which can also disconnect the additional resistors for loss of PE detection.

### 2.3.4 Insulation Monitoring on AC Lines

Since this reference design is capable of doing a measurement in less than 2 ms, the design is capable of measuring insulation resistance on 50-Hz and 60-Hz AC signals as well. In this case, begin the measurement close to the maximum of a sinusoidal voltage as shown in Figure 2-14. Continuously measuring the AC line voltage and setting a trigger to start the insulation monitoring measurement at, for example, 95% of the known peak voltage of the AC line leads to an accurate result, since the voltage is close to the maximum. Figure 2-14 shows the AC line voltage in green and in the two measurement periods necessary for the insulation monitoring are indicated by a high level on the yellow waveform.

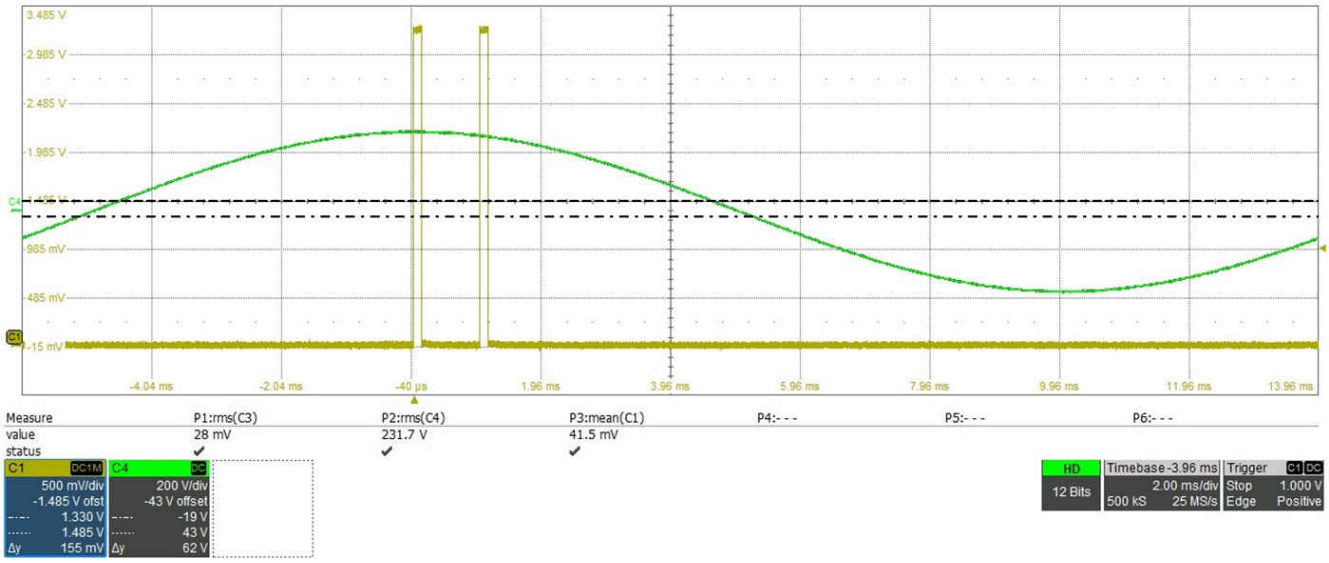



**Figure 2-14. Insulation Monitoring on AC Lines**

To get accurate results, the parasitic capacitance between L1 and PE or N and PE must be below 5 nF.

### 2.3.5 PCB Layout Recommendations

The PCB layout for isolation leakage current measurements must be based on the requirements and components selected for the design.

- The high-voltage section of the system must not have any polygons to HV positive, HV negative, or PE.
- Maintain creepage and clearance distances required for isolation between the HV positive, HV negative, and PE.
- Place thin film resistors in series or a series parallel combination that maintains the isolation and does not allow any low-ohmic paths due to PCB, humidity, or liquids, which are all probable occurrences on the PCB.
- Maintain creepage and clearance distances required for isolation components (AMC3330 and TPSI2140) as explained in the device data sheet.
- To minimize noise, take care when placing analog lines to avoid noise from relays and power switching components.
- Follow the component data sheet to minimize the EMC issues on layout.

Figure 2-15 shows the PCB layout recommendations.

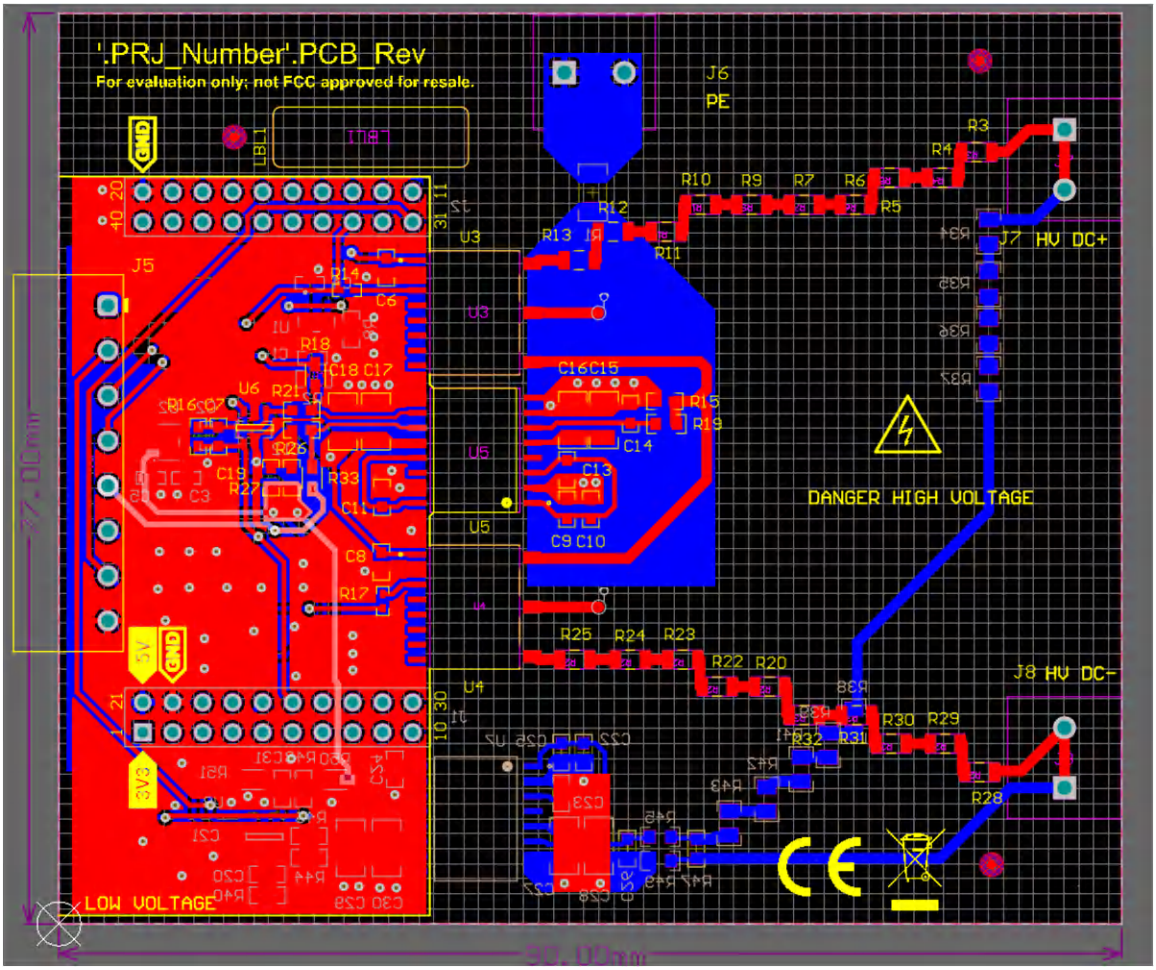



**Figure 2-15. Layout Recommendations - Creepage**

# 3 Hardware, Software, Testing Requirements, and Test Results

## 3.1 Hardware Requirements

### 3.1.1 Connectors

The connector assignment and jumper settings are outlined in Table 3-1.

The 5-V nominal input voltage can be supplied from the **LAUNCHXL-F280049C** through the J7 BoosterPack™ plug-in module, or an alternative 5- to 12-V supply can be fed through the J1 connector to enable the TPS7A2401 to provide the 5-V point of load.

### 3.1.2 Default Jumper Configuration

Prior to working with the TIDA-010232 board, make sure that the correct jumper settings are applied. Table 3-1 shows the default jumper configuration.

**Table 3-1. Jumper Settings**

| HEADER | JUMPER SETTING |
|---|---|
| R18 and R33 | Insert the jumper to enable the differential output of the AMC3330 to be fed to the J1 connector, in case isolation voltage is sampled with a fully-differential input ADC with higher resolution than the 12-bit ADC in the LAUNCHXL-F280049C. |
| R50 | Insert a jumper to enable the REF2033 voltage reference as common-mode voltage in the differential-to-single ended conversion for the high-voltage bus monitoring. Specifically meant for AC bus monitoring where there is a negative sign side signal. Make sure the R51 jumper is not placed simultaneously and the resistors R40, R44, R46, and R48 are sized accordingly to the differential-to-single desired gain. |

### 3.1.3 Prerequisites

The hardware equipment in Table 3-2 is required for the evaluation of the TIDA-010232 reference design.

**Table 3-2. Prerequisites**

| EQUIPMENT | COMMENT |
|---|---|
| High-voltage DC power supply | 400-V output power brick with at least 1-A output current capability |
| High power rating resistors | To simulate the isolation barrier break. Those high-power rating resistors must stand the testing voltages of greater than 400 V |
| TIDA-010232 hardware | With the default jumper settings per Section 3.1.2 |
| LAUNCHXL-F280049C | LaunchPad Development Kit with C2000™ Real-Time Controllers TMS320F280049C device |
| Micro-USB port to connect to LAUNCHXL-F280049C | For interaction between the LaunchPad Development Kit and the computer |

## 3.2 Software Requirements

- Code Composer Studio™ integrated development environment
- Example Code is found on the TIDA-010232 tool folder

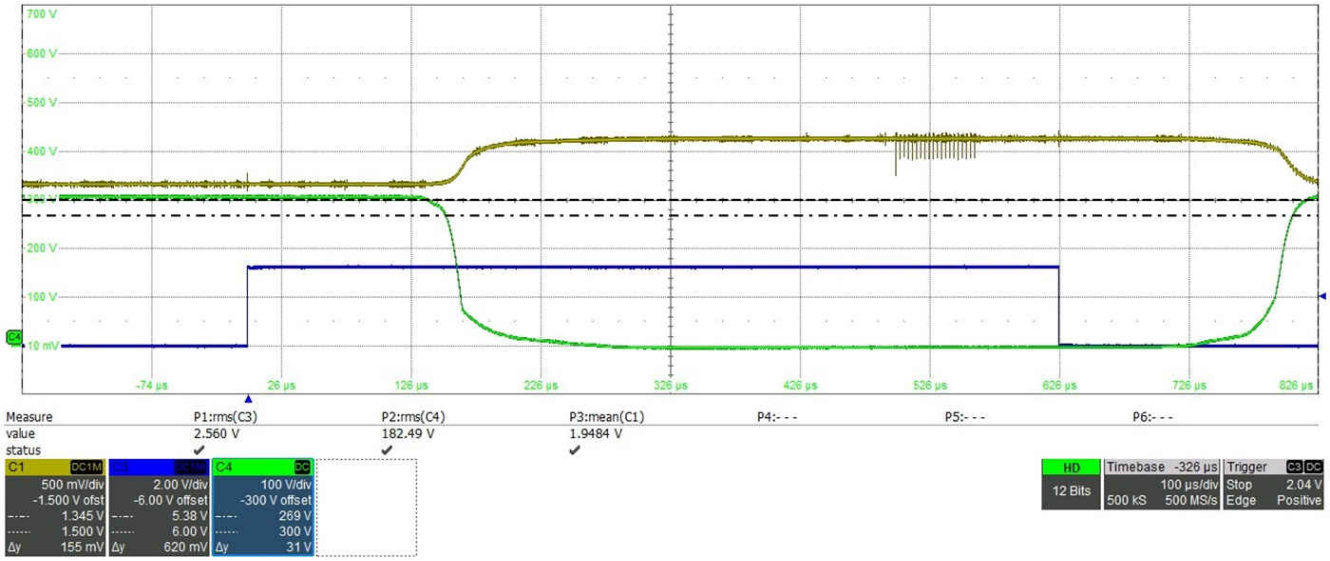
## 3.3 Software

Table 3-3 details the software flow.

**Table 3-3. Software flow and timing**

| STEP | TIME (µs) | COMMENT |
|---|---|---|
| Board initialization | 2929 | One time after power up |
| Close SP + ADC Voltage settling | 500 | Time to close the switch SP and delay of 500 µs for the voltage at the ADC input to settle. Depending on capacitive loading this time needs to be adjusted (see Section 1.2). |
| Measure $V_{iso,P}$ and $V_{DC,P}$ | 126 | Both voltages are measured 20 times interleaved and averaged, to minimize noise |
| Open SP and close SN | 400 | A delay of 400 µs is implemented between the opening SP and closing SN. |
| ADC Voltage settling | 500 | Delay of 500 µs for the voltage at the ADC input to settle. Depending on capacitive loading this time needs to be adjusted (see Section 1.2). |
| Measure $V_{iso,N}$ and $V_{DC,N}$ | 126 | Both voltages are measured 20 times interleaved and averaged, to minimize noise |
| Calculate $R_{iso,P}$ and $R_{iso,N}$ | 13 | Final calculation of $R_{iso,P}$ and $R_{iso,N}$ |

The software initialization takes about 3 ms and must be completed once after power up. Each measurement of the insulation resistances afterward takes 1.7 ms. This fast measurement time is one of the big advantages of using the TPSI2140 compared to a traditional relay for switching in the measurement path. The switching behavior of the TPIS2140 and voltage settling at the ADC input is shown in Figure 3-1.




Blue: Enable Signal, Green: Voltage across TPSI2140, Yellow: Voltage at ADC input

**Figure 3-1. Switching Behavior of TPSI2140 and ADC Input Voltage**

## 3.4 Test Setup

The board is populated differently for 400-V and for 800-V testing:

- 400 V:
  - $R_{stP}$ = $R_{stN}$ = 68.1 kΩ
  - $R_{inAMC}$ = 120 Ω
- 800 V:
  - $R_{stP}$ = $R_{stN}$ = 280 kΩ
  - $R_{inAMC}$ = 250 Ω
- All resistors used for the switched-in resistive branch are 0.1% resistors
- $R_{isoN}$ and $R_{isoP}$ are simulated by HV resistors between DC+ and PE and DC– and PE.
- The measured values of $R_{isoP}$ and $R_{isoN}$ are read out via the *Expression* window of the Code Composer Studio

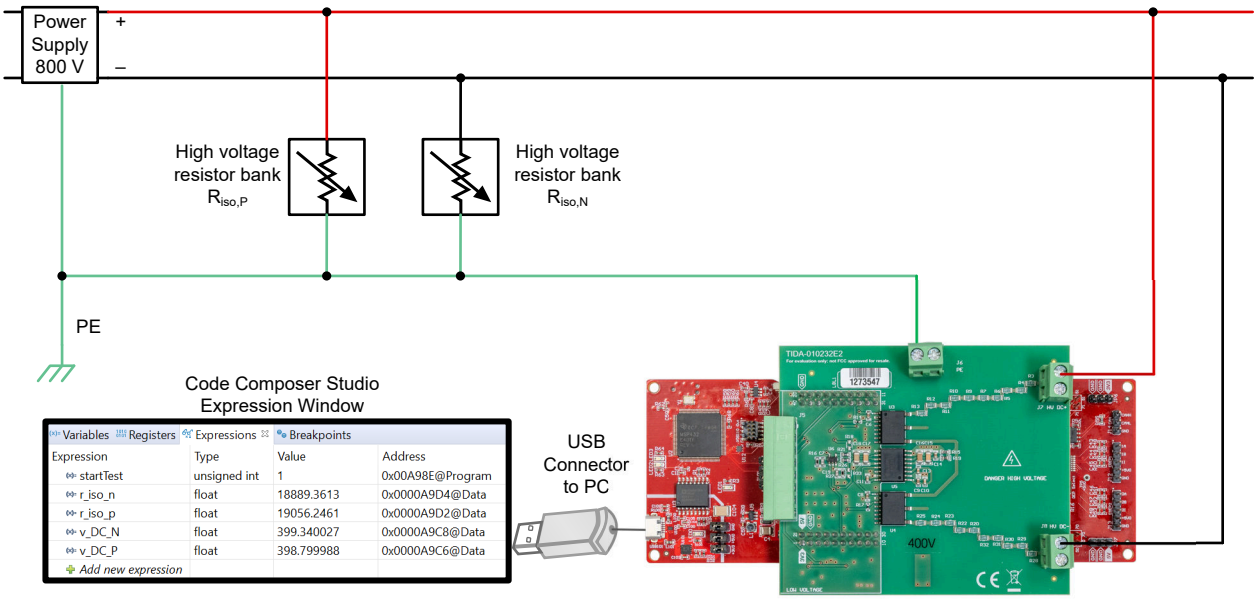



**Figure 3-2. Test Setup**

## 3.5 Test Results

Figure 3-3 and Figure 3-4 show the relative error for the 400-V and 800-V tests. The color scheme in the tables from green over yellow to red shows the small to big relative errors and is used to indicate performance in different areas of the measurement range. The test results show that the measurement accuracy is best in the important range of 20 kΩ to 200 kΩ, where the insulation faults must be detected. With higher insulation resistance values, the accuracy falls off, especially above 1 MΩ. This reduction in accuracy is not a problem since in this range the insulation is far above the fault and warning levels. For this reason, the actual software for this reference design does not return values above 1 MΩ. Every calculation result which indicates a resistance higher than 1 MΩ is set to 1 MΩ. This feature was disabled for the measurements in the following tables.

**TIDA-010232 400V Accuracy**

**Board Configuration: 400 V**

**|RisoN Error|**

| | RisoP Plan | 20 kΩ | 60 kΩ | 100 kΩ | 200 kΩ | 400 kΩ | 600 kΩ | 1000 kΩ | 5000 kΩ |
|---|---|---|---|---|---|---|---|---|---|
| | RisoP Real | 20076 | 60206 | 102006 | 214066 | 423776 | 617766 | 1020176 | 5071176 |
| RisoN Plan | RisoN Real | | | | | | | | |
| 20 kΩ | 20043 | 3.63% | 2.62% | 2.55% | 1.15% | 0.92% | 1.85% | 1.42% | 2.36% |
| 60 kΩ | 60143 | 1.80% | 2.07% | 1.59% | 1.83% | 1.34% | 1.51% | 1.12% | 1.62% |
| 100 kΩ | 102013 | 2.48% | 1.81% | 1.63% | 1.77% | 1.50% | 1.72% | 1.48% | 1.37% |
| 200 kΩ | 214063 | 2.63% | 1.78% | 1.90% | 0.91% | 1.00% | 1.65% | 0.95% | 1.40% |
| 400 kΩ | 422843 | 10.05% | 2.41% | 1.92% | 2.08% | 1.22% | 1.37% | 1.04% | 1.53% |
| 600 kΩ | 616863 | 11.84% | 3.52% | 2.79% | 3.14% | 2.10% | 1.68% | 1.38% | 3.06% |
| 1000 kΩ | 1022243 | 13.96% | 6.56% | 7.82% | 5.52% | 5.14% | 5.40% | 4.13% | 5.61% |
| 5000 kΩ | 5072243 | 41.52% | 28.14% | 20.05% | 19.49% | 18.04% | 11.24% | 22.45% | 16.37% |

**|RisoP Error|**

| | RisoP Plan | 20 kΩ | 60 kΩ | 100 kΩ | 200 kΩ | 400 kΩ | 600 kΩ | 1000 kΩ | 5000 kΩ |
|---|---|---|---|---|---|---|---|---|---|
| | RisoP Real | 20076 | 60206 | 102006 | 214066 | 423776 | 617766 | 1020176 | 5071176 |
| RisoN Plan | RisoN Real | | | | | | | | |
| 20 kΩ | 20043 | 2.03% | 0.84% | 0.16% | 3.78% | 11.13% | 5.71% | 19.34% | 19.58% |
| 60 kΩ | 60143 | 0.16% | 0.33% | 0.39% | 0.01% | 4.30% | 5.17% | 10.43% | 49.35% |
| 100 kΩ | 102013 | 0.10% | 0.13% | 0.65% | 0.98% | 2.19% | 4.85% | 8.50% | 42.63% |
| 200 kΩ | 214063 | 0.24% | 0.21% | 0.44% | 1.51% | 1.65% | 3.20% | 4.10% | 57.29% |
| 400 kΩ | 422843 | 0.75% | 0.32% | 0.40% | 1.33% | 2.85% | 1.62% | 4.39% | 36.44% |
| 600 kΩ | 616863 | 0.80% | 0.31% | 0.59% | 0.78% | 1.81% | 2.96% | 3.89% | 42.54% |
| 1000 kΩ | 1022243 | 0.05% | 0.44% | 0.17% | 1.22% | 1.20% | 2.75% | 4.04% | 36.89% |
| 5000 kΩ | 5072243 | 0.17% | 0.37% | 0.55% | 0.77% | 1.15% | 3.15% | 4.76% | 23.33% |

**Figure 3-3. Accuracy 400-V Test**

| TIDA-010232 800V Accuracy | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Board Configuration: 800 V | | | | | | | | | |
| | | | | | | | | | |
| \|RisoN Error\| | | | | | | | | | |
| | RisoP Plan | 20 kΩ | 60 kΩ | 100 kΩ | 200 kΩ | 400 kΩ | 600 kΩ | 1000 kΩ | 5000 kΩ |
| | RisoP Real | 20076 | 60206 | 102006 | 214066 | 423776 | 617766 | 1020176 | 5071176 |
| RisoN Plan | RisoN Real | | | | | | | | |
| 20 kΩ | 20043 | 5.76% | 1.28% | 0.76% | 0.94% | 1.36% | 2.20% | 1.61% | 1.54% |
| 60 kΩ | 60143 | 6.03% | 1.67% | 1.12% | 0.06% | 0.02% | 0.20% | 0.24% | 0.57% |
| 100 kΩ | 102013 | 0.18% | 3.51% | 1.79% | 0.67% | 0.57% | 0.62% | 0.35% | 0.03% |
| 200 kΩ | 214063 | 1.20% | 3.24% | 2.81% | 1.90% | 1.24% | 1.48% | 0.91% | 0.72% |
| 400 kΩ | 422843 | 1.25% | 0.87% | 0.47% | 1.12% | 1.78% | 1.50% | 1.72% | 1.17% |
| 600 kΩ | 616863 | 5.33% | 0.31% | 0.27% | 0.93% | 1.73% | 1.49% | 1.54% | 1.67% |
| 1000 kΩ | 1022243 | 3.94% | 0.48% | 0.64% | 0.10% | 0.70% | 0.51% | 1.23% | 1.60% |
| 5000 kΩ | 5072243 | 15.60% | 10.67% | 3.79% | 1.07% | 3.01% | 2.67% | 0.45% | 1.46% |
| \|RisoP Error\| | | | | | | | | | |
| | RisoP Plan | 20 kΩ | 60 kΩ | 100 kΩ | 200 kΩ | 400 kΩ | 600 kΩ | 1000 kΩ | 5000 kΩ |
| | RisoP Real | 20076 | 60206 | 102006 | 214066 | 423776 | 617766 | 1020176 | 5071176 |
| RisoN Plan | RisoN Real | | | | | | | | |
| 20 kΩ | 20043 | 5.08% | 0.46% | 0.21% | 2.08% | 6.08% | 6.60% | 12.77% | 48.36% |
| 60 kΩ | 60143 | 4.91% | 0.73% | 0.82% | 0.94% | 0.89% | 2.53% | 3.41% | 29.62% |
| 100 kΩ | 102013 | 0.78% | 2.16% | 1.25% | 1.21% | 0.27% | 0.31% | 1.52% | 16.39% |
| 200 kΩ | 214063 | 0.14% | 0.48% | 1.42% | 1.90% | 0.05% | 1.30% | 0.41% | 6.27% |
| 400 kΩ | 422843 | 1.52% | 0.72% | 0.12% | 0.20% | 0.06% | 0.13% | 0.57% | 6.81% |
| 600 kΩ | 616863 | 0.75% | 0.66% | 0.17% | 0.46% | 0.02% | 0.39% | 0.32% | 0.28% |
| 1000 kΩ | 1022243 | 2.40% | 0.12% | 0.23% | 0.03% | 0.45% | 0.35% | 0.03% | 1.64% |
| 5000 kΩ | 5072243 | 0.09% | 0.56% | 0.03% | 0.48% | 0.17% | 0.21% | 1.29% | 4.69% |

**Figure 3-4. Accuracy 800-V Test**

# 4 Design and Documentation Support

## 4.1 Design Files

### 4.1.1 Schematics

To download the schematics, see the design files at TIDA-010232.

### 4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010232.

## 4.2 Documentation Support

1. Texas Instruments, *TPSI2140-Q1 Isolated Switch With 1.4-kV Integrated FETs* data sheet
2. Texas Instruments, *AMC3330 Precision, ±1-V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter* data sheet
3. Texas Instruments, *TPS7A24 200-mA, 18-V, Ultra-Low $I_Q$, Low-Dropout Voltage Regulator* data sheet
4. Texas Instruments, *REF20xx Low-Drift, Low-Power, Dual-Output, VREF and VREF / 2 Voltage References* data sheet
5. Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet

## 4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 4.4 Trademarks

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# 5 About the Author

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# 6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (January 2023) to Revision C (June 2023) | Page |
|---|---|
| • Updated Equation 19 | 16 |

| Changes from Revision A (December 2022) to Revision B (January 2023) | Page |
|---|---|
| • Updated *1400-V* to *1200-V* | 11 |
| • Updated *Low power consumption: < 5-mA input current* to *Low power consumption: < 9-mA input current* | 11 |

| Changes from Revision * (May 2022) to Revision A (December 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • The second revision of this document is a broad update to the Design Guide. Features were added, for example, *Loss of PE Detection* and *Insulation Monitoring on AC Lines*. More detailed and additional HV measurements are shown in the *Test Results*. Corrected minor issues within different chapters and illustrations were added or improved. Added an additional chapter describing *Software* | 1 |

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