Design Guide:

Automotive, High-Power, High-Performance SiC Traction Inverter Reference Design

Description

TIDM-2014 is a 800-V, 300 kW SiC-based traction inverter system reference design developed by Texas Instruments and Wolfspeed which provides a foundation for design engineers to create high-performance, high-efficiency traction inverter systems and get to market faster. The design features high-performance isolated gate driver with real-time variable gate drive strength, isolated bias supply with integrated transformer along with TI's high real-time performance, MCUs that can control traction motor even at speeds greater than 20,000 RPM while supporting functional safety requirements.

Resources

TIDM-02014	Design Folder
UCC5880-Q1, AM2634-Q1	Product Folder
TMS320F280039C-Q1, UCC14240-Q1	Product Folder
UCC12051-Q1, AMC3330-Q1	Product Folder
TCAN1462-Q1, ISO1042-Q1, ALM2403-Q1	Product Folder

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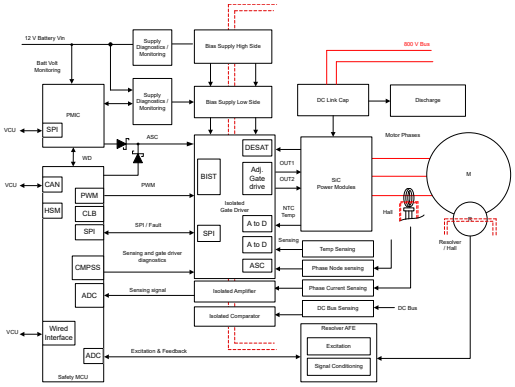
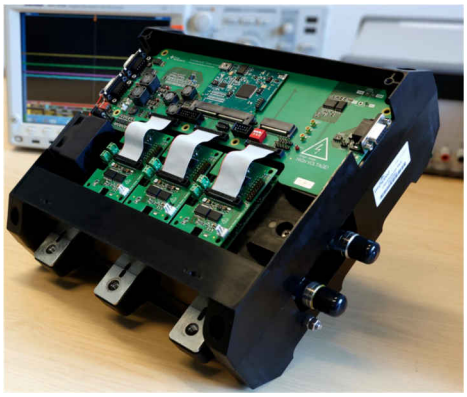
Features

- Real-time variable gate drive strength features enable improvement in system efficiency by minimizing the SiC switching power losses and accurate bias supply minimizes conductive losses .
- Isolated gate drivers and bias supply module reduce PCB area by 30%.
- High performance MCUs enable industry's fastest motor control loop (<2 µs), which helps to minimize torque ripple and provides smooth speed and torque current profiles to the traction motor.
- UCC5880-Q1 and AM2634-Q1 are Functional Safety-Compliant targeted devices.
- Enhance system reliability with reinforced rated capacitive isolation technology and early failure detection.

Applications

- HEV/EV Traction Inverters





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1 System Description

The traction inverter system is a core sub-system of an electric vehicle. The system not only contributes directly to the driver experience in terms of acceleration and speed, but also impacts the useful range of an electric vehicle. The TIDM-02014 reference design is a 800 V, 300 kW SiC based inverter reference design from TI and Wolfspeed that attempts to provide a starting point for designers and engineers to achieve a high-performance, high-efficiency traction inverter system.

This design demonstrates the traction inverter system technology that improves system efficiency by reducing the overshoot in available voltages with a high-performance isolated gate driver. The real-time variable drive strength of the gate driver enables inverter efficiency improvement. The isolated gate driver coupled with TI's isolated bias supply design significantly reduces the PCB size providing more than two times smaller PCB area, less than 4 mm height and eliminating 30+ discrete components improving system power density. In addition, TI's high-control performance MCUs featuring tightly-integrated and remarkable real-time peripherals enable effective traction motor control even at speeds greater than 20,000 RPM. A fast current loop implementation helps minimize motor torque ripple and provides smooth speed-torque profiles. The mechanical and thermal design of the system is provided by Wolfspeed.

WARNING

TI intends this reference design to be operated in a lab environment only and does not consider the reference design to be a finished product for general consumer use.

TI intends this reference design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

High voltage! There are accessible high voltages present on the board. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

CAUTION

Do not leave the design powered when unattended.

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1.1 Key System Specifications

The key system specifications are summarized in Table 1-1.

Table 1-1. Key System Specifications

Parameter	Specifications (units)	Notes
P_{out}	300 kW	Rated output power
V_{DSmax}	1200 V	Maximum Dain-Source Voltage
V_{DC}	800 V	DC bus voltage recommended
I_{DC}	300 A	DC Bus current
f_{swmax}	60 kHz	Based on the gate driver bias power
I_L	360 A	AC output RMS current
L_{PL}	5.3 nH	Parasitic Inductance including DC link capacitors and Bus bar
C_{DC}	300 uF	DC link capacitor
L_{DC}	3.5 nH	DC Bus capacitor ESL
Power Density	32 kW/L	
Dimensions	28 cm x 29 cm x 11.5 cm	
Weight	6.2 kg	
Volume	9.3 L	
Area	812 cm^2	
P	5 bar	Coolant Operating Pressure
ΔP	200 mbar	Pressure Drop

- For information on the isolated gate driver, please refer to UCC5880-Q1 data sheet.
- For information on the Microcontroller, please refer to AM2634-Q1 and TMSF280039C-Q1 data sheet.
- For information on the bias supply, please refer to UCC14240-Q1 data sheet.
- For information on the integrated modules, please reference the CAB450M12XM3 data sheet.
- For higher ambient temperatures, the DC-Link voltage and DC-Link current must be de-rated according to the included DC-Link capacitor ratings. Please refer to the 1100 V / 100 µF CX100µ1100d51KF6 data sheet provided by FTCAP GmbH for more detailed information.
- The included cold plate is a Wieland MicroCool CP3012-XP. To calculate the thermal resistance (°C/W) and pressure drop (bar) versus flow rate (liters/min.), please refer to the CP3012-XP data sheet provided by Wieland MicroCool Inc. for more detailed information.
- The included current sensor board uses the LEM LF 510-S. Please refer to the LF 510-S data sheet provided by LEM USA Inc. for more detailed information.

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2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of this reference design with key TI components highlighted.

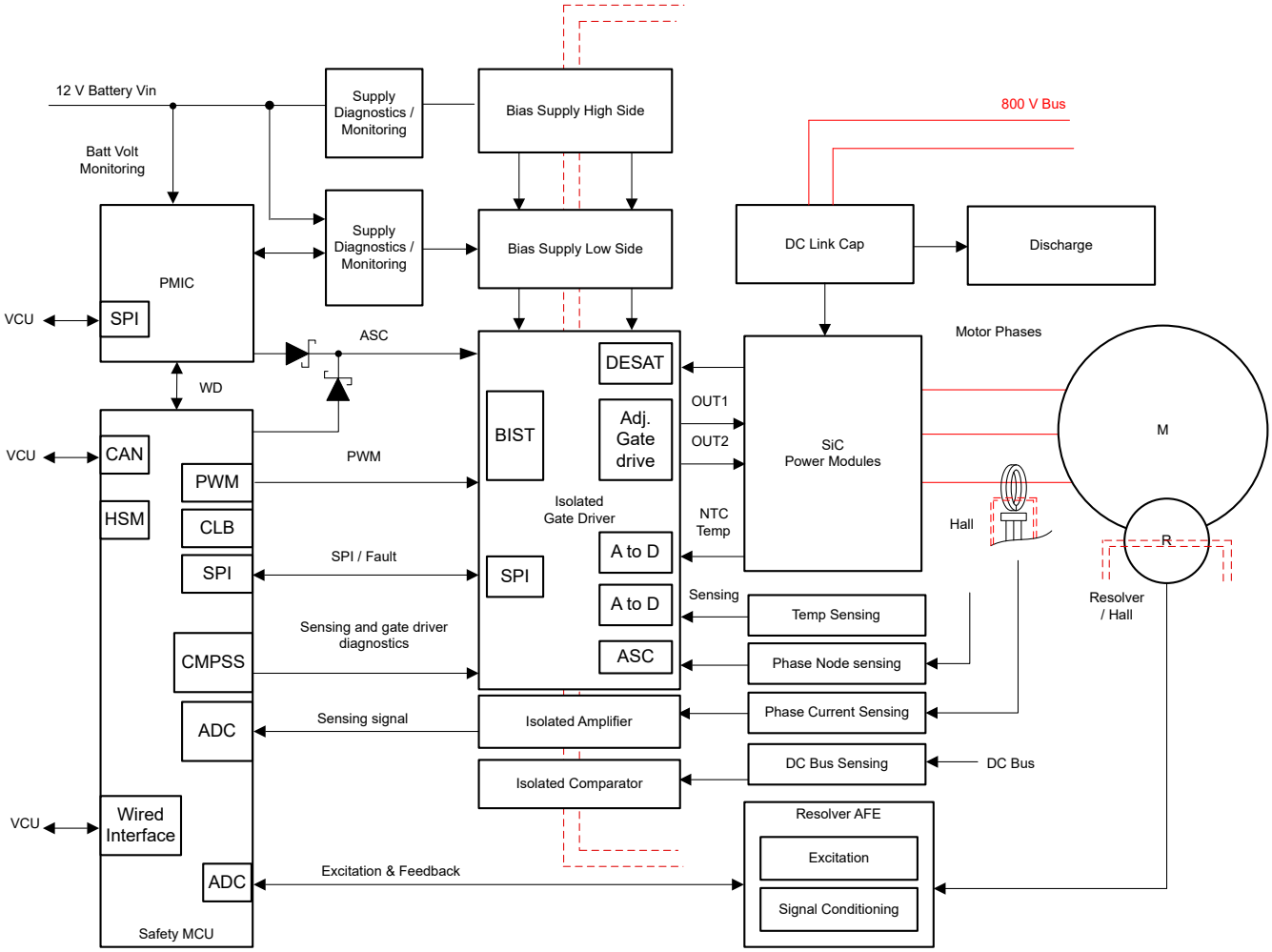

Figure 2-1. TIDM-02014 SiC Inverter System Block Diagram

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2.2 Design Considerations

The primary goal of a traction system is to efficiently drive the traction motor, typically an induction or an interior permanent magnet synchronous motor (IPMSM), with a high control bandwidth. For this, TIDM-02014 features the C2000 real-time control MCU to implementing a field oriented control (FOC) scheme to drive the motor. The design also supports TI's Sitara™ AM263x MCU based control implementation to achieve high real-time performance while supporting functional-safety requirements.

To achieve high-efficiency operation of the SiC inverter, the UCC5880-Q1 functional-safety compliant isolated gate driver design is leveraged. In addition to advanced configuration and protection features, the real-time variable gate driver strength feature of the UCC5880-Q1 enables efficiency optimization. The gate drive bias supply design features the UCC14240-Q1 bias supply device with integrated isolation transformer and post regulation. The tight regulation capability of the UCC14240-Q1 minimizes the device conduction loss during operation. With these designs the gate-drive BOM and PCB footprint can be reduced by up to 30%.

The design philosophy for the power stage aims to maximize performance through high-ampacity, low-inductance design while minimizing the cost and complexity. To achieve this, five key parameters are considered. First, due to the high current density and relatively small size of the SiC modules, a high-performance thermal stackup is implemented to maximize heat transfer. Second, the stray inductance introduced by the busbar structure is minimized through the use of low-inductance, overlapping planar structures. Third, low-inductance and high ripple rating capacitors must are utilized to close the high-frequency switching loop effectively. Fourth, the gate driver high-speed protections and high-noise immunity features are leveraged for effective switching of the SiC moduels and providing maximum survivability under fault conditions. Lastly, the power stage's engineering is aimed to minimize complexity for assembly, manufacturing and the system cost. The inverter measures 279 mm by 291 mm by 115 mm for a total volume of 9.3 L and a power density of up to 32.25 kW/L which is more than 2x comparable Silicon (Si) based inverters.

2.3 Highlighted Products

This reference design features the following Texas Instruments devices.

2.3.1 UCC5880-Q1

The UCC5880-Q1 is a functional safety compliant isolated gate driver targeted for EV/HEV traction inverter applications. The flexibility of SPI programing of adjustable gate drive strength, blanking times, deglitches, thresholds, function enables, and fault handling allow for the UCC5880 to support a wide variety of IGBT or SiC power transistors that are used across all EV/HEV traction inverter applications. UCC5880-Q1 integrates all of the protection features required in most traction inverter applications. Additionally, the 20-A gate drive capability eliminates the need for external booster circuit, reducing overall design size. The integrated Miller clamp circuit holds the gate off during transient events and can be configured to use the internal 4-A pull-down, or drive an external n-channel MOSFET. Advanced, internal capacitor-based isolation technology maximizes CMTI performance, while minimizing the radiated emissions.

2.3.2 AM2634-Q1

The AM263x Sitara™ Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263x MCU family consists of multiple pin-to-pin compatible devices with up to four 400-MHz Arm® Cortex®-R5F cores. The multiple Arm® cores can be optionally programmed to run in lock-step option for different functional safety configurations. The industrial communications subsystem (ICSS) enables integrated industrial Ethernet communications such as PROFINET IRT, TSN, or EtherCAT® (among many others), or for standard Ethernet connectivity or custom I/O interfacing.

The AM263x family is designed for advanced motor control and digital power control applications with advanced analog modules.

2.3.3 TMS320F280039C-Q1

TMS320F280039C-Q1 is a 32-bit DSP from C2000™ real-time microcontroller family, which provides 120 MHz of signal processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Floating-Point Unit (FPU), Trigonometric Math Unit (TMU), and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

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The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has their own dedicated memory resources and the CLA can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

2.3.4 UCC14240-Q1

The UCC142140-Q1 integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter provides greater than 1.5 W of power across a 3000 V_{RMS} basic isolation barrier. TI also has the newer reinforced isolation device, UCC14341-Q1 that takes in a 15 V input and similarly provides an adjustable isolated output up to 25 V. For an optimized BoM, the UCC14341-Q1 can be directly connected to the 15 V resolver rail that is commonly available in a traction inverter.

2.3.5 UCC12051-Q1

UCC12051-Q1 is an automotive qualified DC/DC power module with 5-kV_{RMS} isolation rating designed to provide efficient, isolated power to isolated circuits that require a bias supply with a well-regulated output voltage. The module integrates a transformer and DC/DC controller with a proprietary architecture to provide 500 mW (typical) of isolated power with low EMI. UCC12051-Q1 integrates protection features for increased system robustness. The module also has an enable pin, synchronization capability, and regulated 5-V or 3.3-V output options with headroom.

2.3.6 AMC3330-Q1

The AMC3330-Q1 is a fully-differential precision isolated amplifier with high-input impedance, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage supply source from the low voltage side. The input stage of the device drives a 2^{nd}-order, delta-sigma (ΔΣ) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a 4^{th}-order analog filter on the low-side and presented as a differential analog output.

2.3.7 TCAN1462-Q1

The TCAN1462-Q1 is a high-speed Controller Area Network (CAN) transceivers that meets the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification and the CiA 601-4 Signal Improvement Capability (SIC) specification. The device reduces signal ringing at dominant-to-recessive edge and enables higher throughput in complex network topologies. Signal improvement capability allows the applications to extract real benefit of CAN FD (flexible data rate) by operating at 2 Mbps, or operating at 5 Mbps or higher in large networks with multiple unterminated stubs.

The device also meets the timing specifications mandated by CiA 601-4; thus, has a much tighter bit timing symmetry compared to a regular CAN FD transceivers. This provides larger timing window to sample the correct bit and enables error-free communication in large complex star networks where ringing and bit distortion are inherent.

2.3.8 ISO1042-Q1

The ISO1042-Q1 device is a galvanically-isolated controller area network (CAN) transceiver that meets the specifications of the ISO11898-2 (2016) standard. The ISO1042-Q1 device offers ±70-V DC bus fault protection and ±30-V common-mode voltage range. The device supports up to 5-Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of 5000 V_{RMS} and a working voltage of 1060 V_{RMS}. Electromagnetic compatibility has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. While the ISO1042-Q1 device is available for both basic and reinforced isolation, this reference design uses the device featuring reinforced isolation.

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2.3.9 ALM2403-Q1

The ALM2403-Q1 is a dual-power op amp with features and performance that make this device preferable for resolver-based applications. The high-gain bandwidth and slew rate of the device, along with a continuous high-output current-drive capability, make this device an excellent choice to provide the low distortion and differential high-amplitude excitation required for exciting the resolver primary coil. Current limiting and overtemperature detection enhance overall system robustness, especially when driving analog signals over wires that are susceptible to faults.

2.3.10 LM5158-Q1

The LM5158x-Q1 is a wide input range, non-synchronous boost converter that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies. The device can start up with a minimum of 3.2 V. The device can operate with input supply voltage as low as 1.5 V if the BIAS pin is greater than 3.2 V. The internal VCC regulator also supports BIAS pin operation up to 60 V (65-Vabsolute maximum) for automotive load dump. The switching frequency is dynamically programmable from 100 kHz to 2.2 MHz with an external resistor. Switching at 2.2 MHz minimizes AM band interference and allows for a small design size and fast transient response. The device provides an optional dual random spread spectrum to help reduce the EMI over a wide frequency span.

2.3.11 LM74202-Q1

LM74202-Q1 is a diode with integrated back-to-back FETs and enhanced built-in protection circuitry. LM74202-Q1 provides robust protection for all systems and applications powered from 4.2 V to 40 V. The device integrates reverse battery input, reverse current, overvoltage, undervoltage, overcurrent and short circuit protection. The precision overcurrent limit (±5% at 1 A) helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.1 A and 2.23 A with an external resistor. The device monitors the bus voltage for brown-out and overvoltage protection, asserting the FLTb pin to notify downstream systems.

2.4 System Design Theory

2.4.1 Microcontrollers

The microcontroller, as the primary control unit, is at the heart of the system. To demonstrate the wide range of features and capabilities offered by TI's MCU devices, the TIDM-02014 design supports devices from TI's C2000™ and Sitara™ MCU families. To simplify switching between the two devices, their respective control card evaluation modules with mutual pin compatibility are used. The features of the control cards are described further.

2.4.1.1 Microcontroller – C2000™

The F280039C controlCARD (TMDSCNCD280039C) provides a great way to learn and experiment with F28003x devices. This controlCARD is intended to provide a well-filtered robust design that is capable of working in demanding applications such as traction inverters, on-board chargers, DC-DC converters among others. With an on-board debugger, the F280039C controlCARD provides and easy way to evaluate the powerful real-time capabilities of F28003x MCU devices.

Similar to the AM263x control card, the F280039C control card plugs directly into the Wolfspeed main control board. However,note that several resistors on the control need to be populated or depopulated when switching between the control cards. The details of the resistor changes are provided in Section 3.1.

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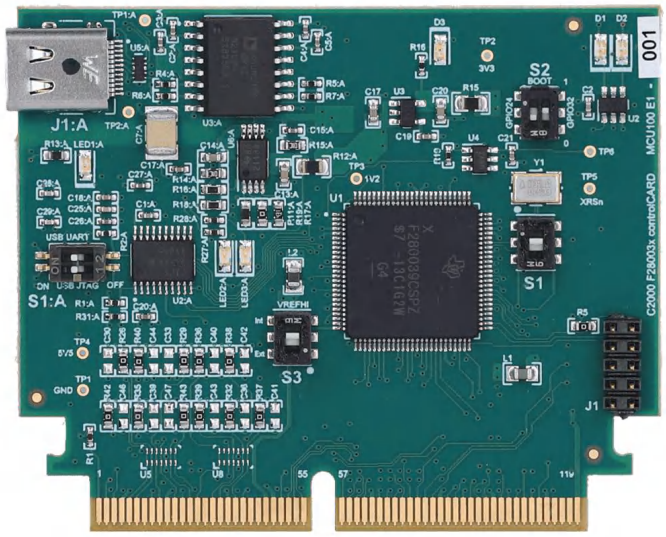

Figure 2-2. F280039C Control Card

2.4.1.2 Microcontroller – Sitara™

The AM263x Control Card Evaluation Module (EVM) is an evaluation and development board for the Texas Instruments Sitara™ AM263x series of microcontrollers (MCUs). This EVM provides an easy way to start developing traction inverter designs on the AM263x MCUs with on-board emulation for programming and debugging as well as buttons and LED for a simple user interface. The control card also enables header pin access to key for rapid prototyping.

The Control card plugs directly into the Wolfspeed main control board and is fully supported with software for customers to quickly develop their traction inverter designs to maximize the performance and integration built into the AM263x MCUs.

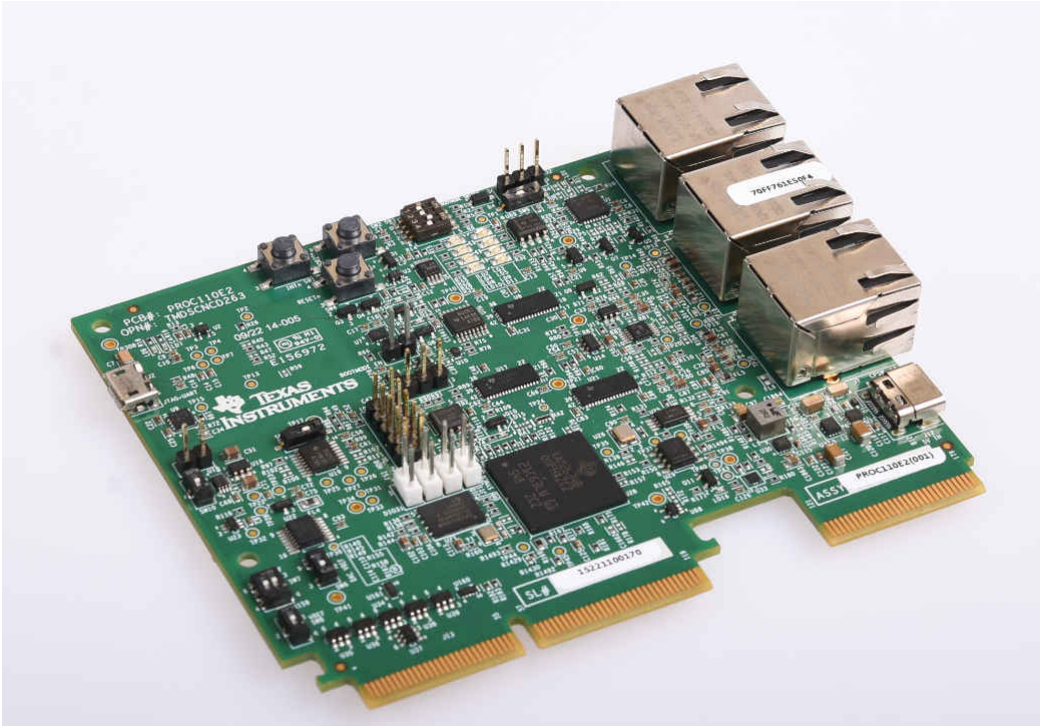

Figure 2-3. AM263x Sitara™ Control Card

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2.4.2 Isolated Bias Supply

As shown in the schematic in Figure 2-4, the UCC14240-Q1 DC/DC converter module operates from a single 24-V (P24V) input and is configured to provide dual, +15 V (VCC2), -4 V (VEE2), 3-kV RMS isolated, bias supply voltage rails to the UCC5880-Q1 isolated gate driver. VCC2 and VEE2 are programmed by resistor dividers R13, R19 and R15, R20 and are tightly regulated to within ±1.3%, providing +15 V and -4 V as recommended by the Wolfspeed XM3, SiC Half-Bridge Module. Startup is initiated when the digital host first provides the enable signal (EN_PS) required to pull the UCC14240-Q1 ENA pin to an active high state, allowing VCC2 and VEE2 to soft-start. The UCC14240-Q1 then provides an active low, LVTTL compatible, power good signal (N_PG), notifying the host that P24V is above the 21-V, UVLO turn-on threshold and VCC2 and VEE2 are above 90% of their set regulation target values (VCC2>13.5 V and VEE2>3.6 V respectively). This connection between the host and UCC14240-Q1 makes sure the UCC5880-Q1, gate driver has sufficient bias voltage present to safely allow inverter switching to begin.

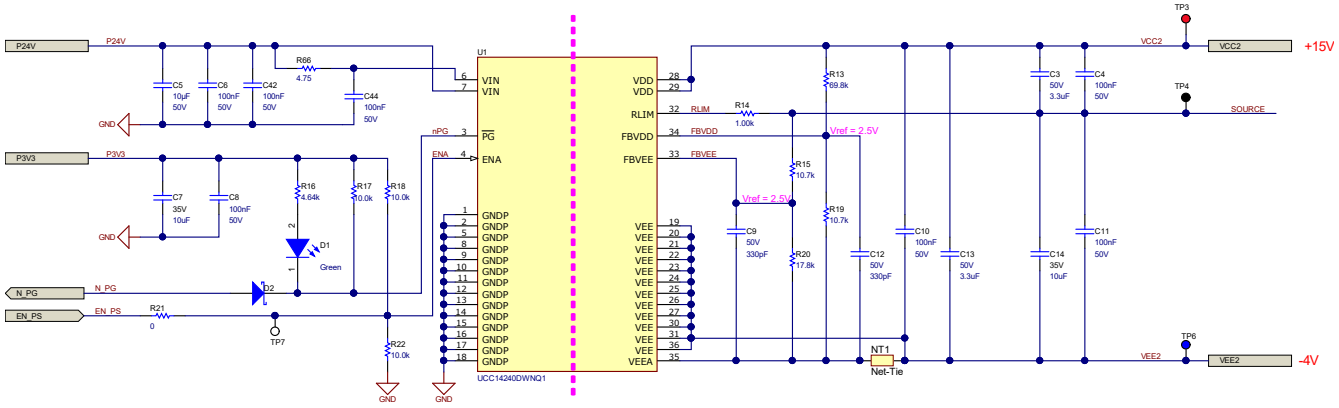

Figure 2-4. UCC14240-Q1 Bias Supply Schematic

2.4.3 Power Tree

2.4.3.1 Introduction

The control board contains complete power supply tree to run all features on the system. The power tree provides power to:

- All on-board peripherals
- Gate-driver boards
- MCU control card (both C2000-based or AM263x-based)
- Internal and external sensors

The external off-line DC adapter is assumed to be used with the board. Adapter must be specified as 12VDC nominal (8-16VDC) 3.3ADC.

Power is connected through barrel jack connector with 2 mm center pin J100 (see part data sheet).

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2.4.3.2 Power Tree Block Diagram

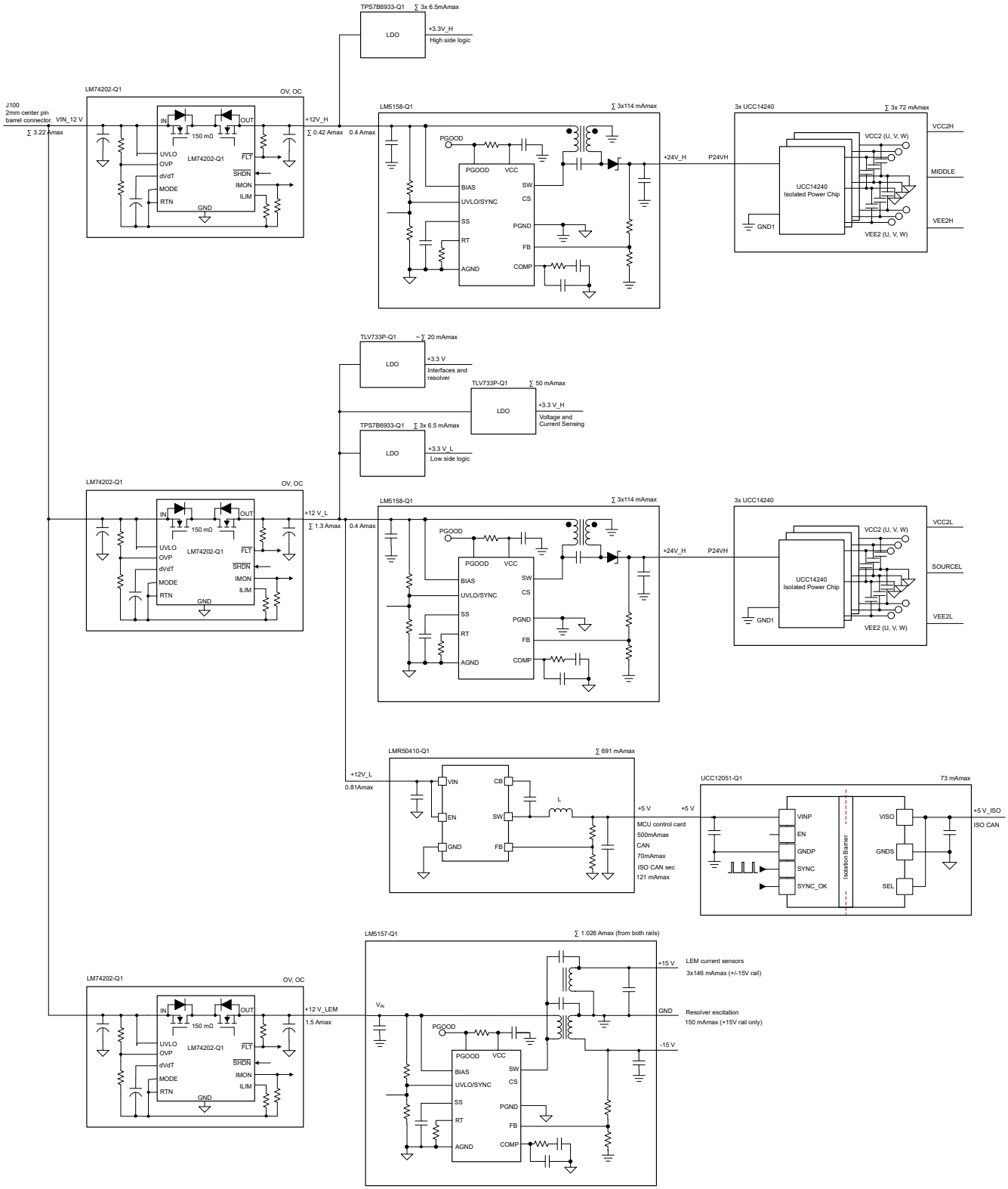

Figure 2-5. Power Tree Block Diagram

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2.4.3.3 12 V Distribution and Control

The 12-volt domain is distributed into three separate rails.

Table 2-1. 12 V Distribution and Control

Rail	Regulator	Load	Maximum current
+12V_H	LM5158-Q1 based SEPIC	High-side 24-volt domain	0.4 A
	TPS7B6933-Q1 LDO	High-side 3.3-volt logic	0.02 A
+12V_L	LM5158-Q1 based SEPIC	Low-side 24-volt domain	0.4 A
	TPS7B6933-Q1 LDO	Low-side 3.3-volt logic	0.02 A
	TLV733P-Q1 LDO	High-voltage sensing and current sensing signal conditioning	0.05 A
	TLV733P-Q1 LDO	Digital interfaces and resolver front-end	0.02 A
	LMR50410-Q1 simple switcher®	5-volt supply domain	0.81 A
+12V_LEM	LM5157-Q1 based SEPIC	LEM current sensor modules	1.5 A
		Resolver excitation	

These rails are separated and protected with LM74202-Q1 ideal diodes.

The primary function of LM74202-1 is to provide overvoltage (OV) and short circuit protection. For debugging or experimental purposes the MCU can control the LM74202-Q1 with a logic signal (Power_EN_LoadSW) when powered from different power source for example through programming USB cable.

2.4.3.4 Gate Drive Supply

Low voltage domain of the isolated gate driver units (GDU) (UCC5880-Q1) is powered by the TPS7B6933-Q1 LDO. The high-voltage (HV) domain of the GDU is powered using UCC14240-Q1 isolated DC/DC modules. These modules were selected for their compactness and ease of use.

The voltage generated by UCC14240-Q1 is set to total 19 V (V_{CC2} = 15 V and V_{EE2} = -4 V). The high-voltage negative pole is a virtual ground for UCC14240-Q1.

The maximum power consumption on the high-voltage side of each UCC14240-Q1 DC/DC module can be estimated as a worst-case switching condition for f_{SWmax} = 30 kHz and C_L = 100 nF:

$$P2 = f_{SWmax}(V_{CC2} - V_{EE2})^2 C_L + \left(V_{CC2} - V_{EE2}\right) I_{CCq2} \quad (1)$$

The secondary quiescent current of UCC5880-Q1 can be found in the data sheet as I_{CC2q} = 15 mA. Resulting secondary power consumption is then calculated as 1.368 W. Assuming 50% efficiency this corresponds to 114 mA of supply current on 24-volt input side of each UCC14240-Q1.

These UCC14240-Q1 DC/DC modules require pre-regulated 24 V. 24-volt pre-regulator is implemented as LM5158-Q1 based SEPIC with coupled inductors. The SEPIC topology supports appropriate input voltage range and the LM5157/8-Q1 converters are designed for in this case because of their versatility and due to random spread spectrum also for the noise properties.

The component values for the power supply design were calculated using the *LM5158 Quick Start Calculator tool for SEPIC*. The main input parameters of the supply are shown in Table 2-2.

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Table 2-2. SEPIC Converter Design Parameters for Gate Drive Power Supply

Parameter	Value			
	Min	Nom	Max	Unit
V_{INPUT}	8	12	16	V
f_{sw}		435		kHz
V_{LOAD}		24		V
I_{LOAD}		0.35		A

Each 24-volt SEPIC powers three UCC14240-Q1 therefore I_{LOAD} = 0.35A is listed (see Figure 2-5).

2.4.3.5 5-Volt Supply Domain

The 5-Volt power supply features LMR50410-Q1 Simple Switcher®. The power supply mainly powers the MCU control card plugged into the HSEC PCB connector.

LMR50410-Q1 has maximum output current of 1 A which gives power budget of 10 W. At efficiency of 90% it draws about 0.92A from the 12-Volt power rail at maximum power. Realistic estimate of the load current in all branches is shown in Figure 2-5.

Out of assumed MCU control cards, the AM2634 control card consumes higher power so the sizing of the power budget is based on the consumption estimate of AM2634 control card.

The AM2634 based control card consumes in average 2.5 W with all unused peripherals disabled. The 5-volt power supply domain then offers sufficient margin to support various use cases and operation profiles.

CAN interface consumes 70 mA and the isolated CAN 122 mA totaling 192 mA from 5-volt rail. The isolated CAN interface is powered using UCC12051-Q1 DC/DC power module. This module provides maximum 500 mW of power at 5 V and 5 kVrms isolation. At 73 mA loading on the isolated side by the ISOCAN1042-Q1 we expect 122 mA on the primary side assuming 60% efficiency.

2.4.3.6 Current and Position Sensing Power

The current and position sensing (resolver) is powered from the +12 V_LEM power rail. The LEM LF 510-S current transducers require symmetrical power supply of positive and negative 15 V.

The current draw for one current measurement channel from +/-15 V power supply is defined as (for details see LEM LF 510-S data sheet):

$$I_{CCLEM}[mA] = 44\ mA + 0.2\ I_{MEAS}[A] \quad (2)$$

Where 44 mA is the quiescent current of the transducer and I_{MEAS} is the measured current. Peak measured current determines the maximum power draw. In our case we assume maximum 509 A of peak measured current (see note in the schematic diagram). This corresponds to 146 mA current consumption.

+15 V rail powers the resolver excitation amplifier. The current consumption naturally depends on the resolver type. Estimated current budget for this function is 150 mA from the +15 V rail.

A dual output SEPIC topology was selected to provide symmetrical 15V supply featuring LM5157-Q1. Similarly, as LM5158-Q1 this wide Vin converter has random spread spectrum for better noise performance. LM5157-Q1 simultaneously drives two independent SEPIC stages connected in series. To be able to use the LM5157/58 calculation spreadsheet for component calculation the total I_{LOAD} must be determined. If we assume to be the V_{LOAD} = 15 V we need to multiply the current transducer consumption by a factor of two. This represents two driven branches (creating the +/-15 V). I_{LOAD} can be calculated as:

$$I_{LOAD} = 150\ mA + 2 \times 3 \times 146\ mA = 1026\ mA \quad (3)$$

Where factor of three represents the three channels connected to the power supply and 150 mA represent the power budget for resolver excitation.

For component calculation in the calculation spreadsheet following parameters have been used:

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Table 2-3. SEPIC Converter Design Parameters for Current and Position Sensing Circuits

Parameter	Value			
	Min	Nom	Max	Unit
V_{INPUT}	8	12	16	V
f_{sw}		435		kHz
V_{LOAD}		15		V
I_{LOAD}		0.35		A

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

This section details the hardware and explains the different sections on the board and how to set them up for the test outlined in this design guide.

3.1.1 Hardware Board Overview

Figure 3-1 shows the assembled inverter system with the functional sections highlighted. Hardware details of the sections are provided further.

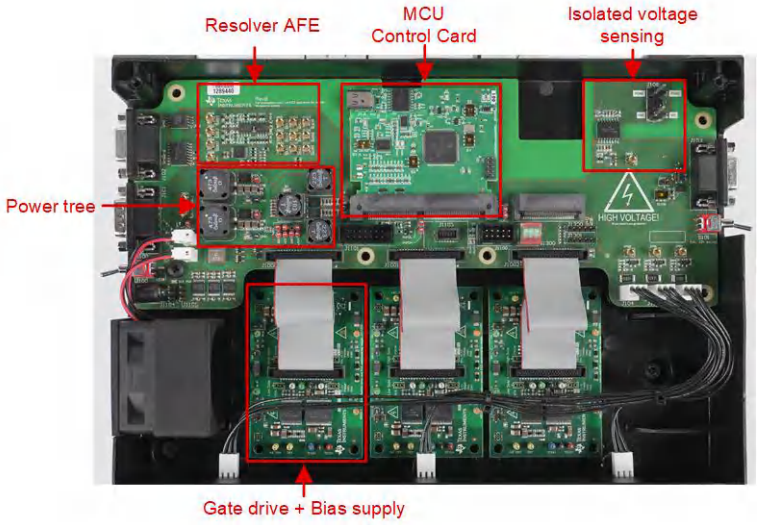

Figure 3-1. Functional Sections of TIDM-02014 Inverter System

3.1.1.1 Control Board

The control board accepts the MCU control cards, provides auxiliary power, provides interfaces for position, voltage and current sensing, communication. The control board also interfaces to the gate drive and bias supply board, providing power and SPI connection between MCU and gate drivers. Since the control board accepts control cards, the same board maybe used to test the TIDM-02014 system with TI's AM263x MCU as well as the TMS320F280039C MCU. It is to be noted, however, that several 0R resistors need to be changed between the two configurations. The list of changes in shown in Table 3-1.

Table 3-1. Resistor Changes for AM263x and F280039C Configurations

MCU Control Card	Populate	Depopulate
F280039C	R1110, R1113, R1116, R1118, R1120, R1121, R1126, R1127	R1109, R1114, R1115, R1125, R1123, R1124, R1122
AM263x	R1109, R1115, R1118, R1122, R1123, R1124, R1125	R1110, R1113, R1114, R1116, R1120, R1121, R1126, R1127

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3.1.1.2 MCU Control Card – Sitara™

The key interfaces and connections to the AM263 Control card are shown in Figure 3-2.

The pinout of the *AM263x Control Card* is available in the *Control Card user guide*.

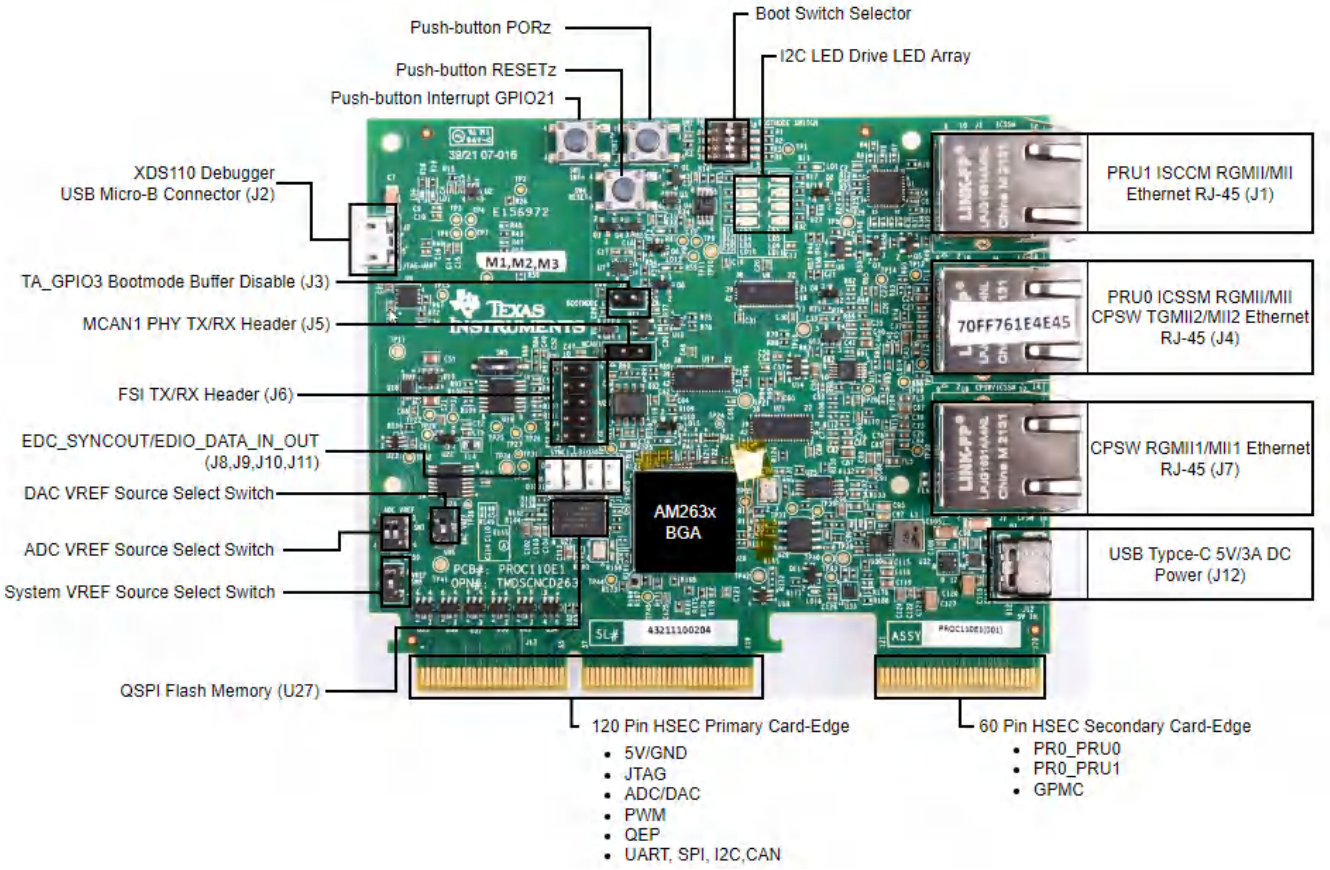

Figure 3-2. AM263x Control Card Hardware Description

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3.1.1.3 MCU Control Card – C2000™

The components and their corresponding functions for F280039C Control card are shown in Figure 3-3.

The *Control Card user guide* provides further details on configuring and debugging the board.

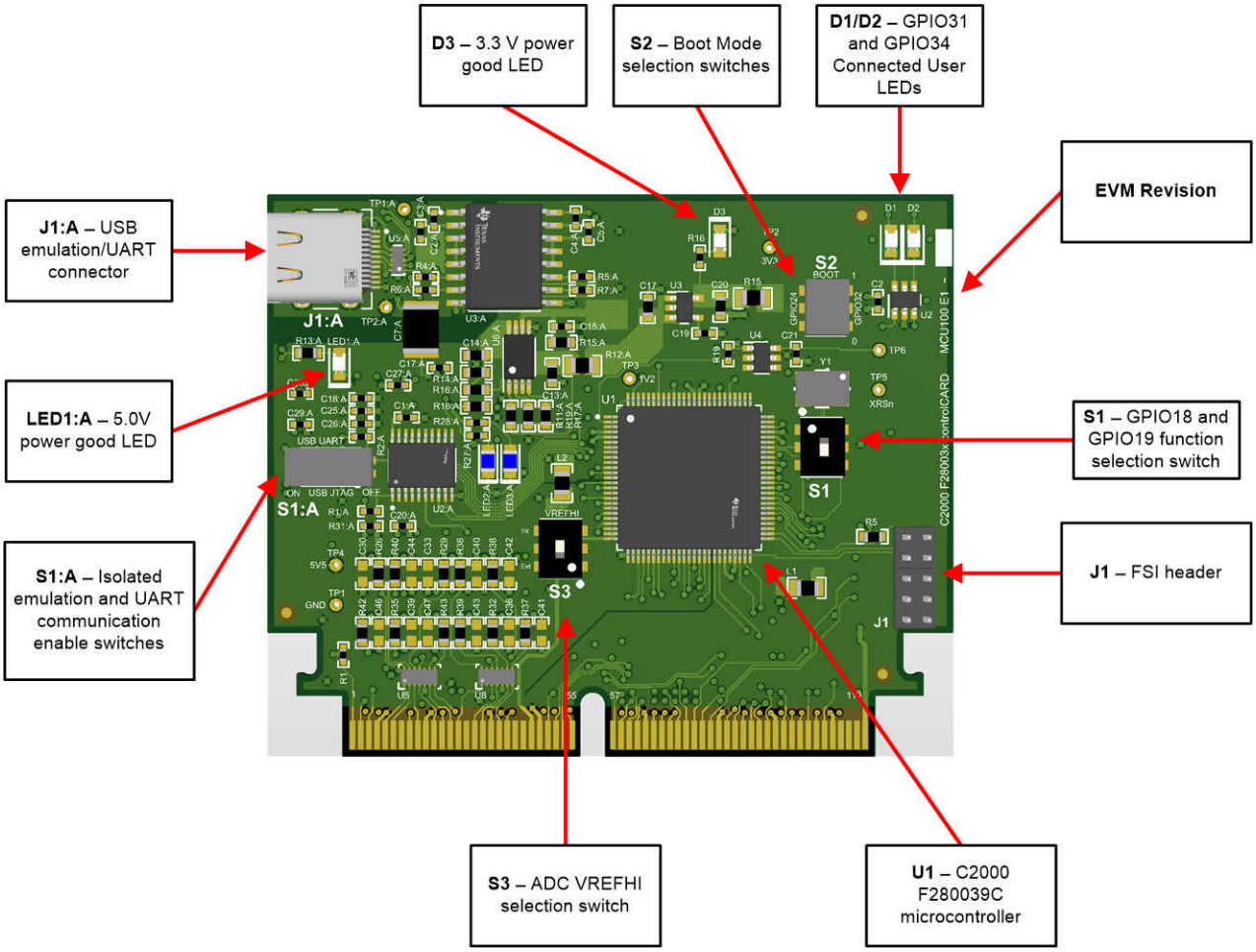

Figure 3-3. F280039C Control Card Hardware Sections

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3.1.1.4 Gate Driver and Bias Supply Board

The components and accessible test points on the gate drive and bias supply board are shown on the Figure 3-4. Pinouts of the J9 connector are described in the Table 3-2.

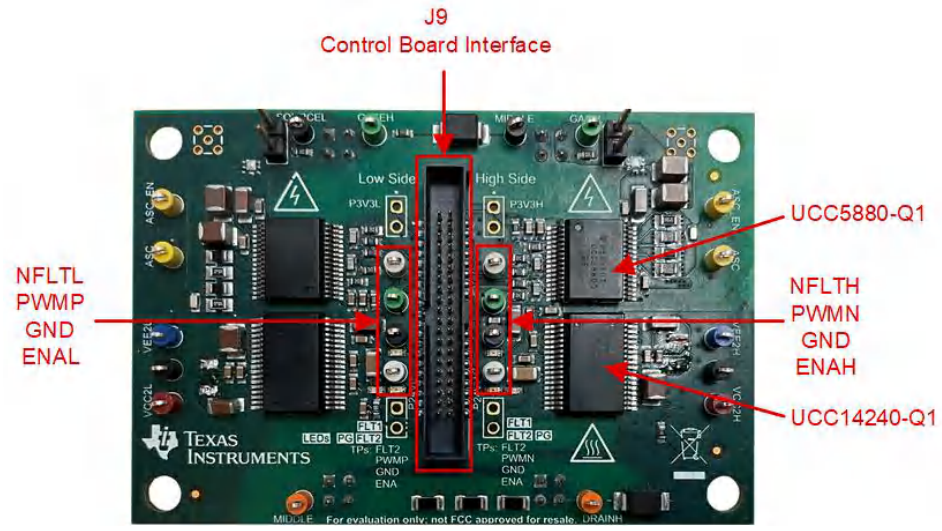

Figure 3-4. Gate Driver and Bias Supply Board

Table 3-2. Connector J9 Pinout

Pin	Signal	Pin	Signal
1	P3V3H_T	2	GND
3	PV3VL_T	4	GND
5	SDIL_T	6	NCSH_T
7	NCSL_T	8	SDOH_T
9	GND	10	CLK
11	GND	12	PWMN
13	GND	14	PWMP
15	GND	16	GND
17	ASCL_T	18	N_FLT2H_T
19	GND	20	N_FLT1H_T
21	GD2L_T	22	GD0H_T
23	GD1L_T	24	GD1H_T
25	GD0L_T	26	GD2H_T
27	GND	28	ASC_EN
29	N_FLT1L_T	30	ASCH_T
31	N_FLT2L_T	32	GND
33	EN_PSL_T	34	N_PGH_T
35	N_PGL_T	36	EN_PSH_T
37	P24VH_T	38	GND
39	P24VL_T	40	GND

3.1.1.5 DC Bus Voltage Sense

A voltage sense connection for the DC bus voltage is provided by a board-to-board connector between the discharge PCB and the connector on the bottom side of the controller. This allows the controller application to monitor the DC bus voltage. The full bus voltage is present at connector J8 on the controller and is stepped down through a voltage divider and filtered before reaching the ADC input. A 0-1200 V DC bus voltage signal is scaled to a 0-3 V ADC voltage.

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3.1.1.6 SiC Power Module

3.1.1.6.1 XM3 SiC Power Module

Wolfspeed's XM3 module is designed to simplify SiC power modules by creating an all new package that is both high-performance and easy to use. Wolfspeed has developed a high-performance next generation module that is easy to use and has been optimized in a manner that is intended to achieve the maximum performance out of all sizes of commercially available 650–1700 V Wolfspeed C3M™ SiC MOSFETs. It offers the capability to carry high currents (300 to >600 A) in a small footprint (53 x 80 mm) with a terminal arrangement that allows for straight-forward bussing and interconnection. A low-inductance, evenly matched layout results in high quality switching events, minimizing oscillations both internal and external to the module. The module has a stray inductance of only 6.7 nH. When coupled with the low-inductance bussing and capacitors in this reference design, a total loop inductance of 12 nH is obtained, which is lower than the internal stray inductance of many standard power module packages. The XM3 platform offers 40% of the volume and 45% of the footprint of a package that is typically used in the industry as shown in Figure 3-5 and therefore offers a more compact power module for high power density systems. Table 3-3 lists which variant of the XM3 module is included with each three-phase inverter reference design.

Figure 3-5. Size Comparison Between XM3 (Left), 62 mm (Center), and EconoDUAL™(Right)

Table 3-3. XM3 Power Module Part Number Reference

Reference Design	Module Part Number
CRD300DA12E-XM3	C4B450M12XM3
CRD250DA12E-XM3	C4B425M12XM3
CRD200DA12E-XM3	C4B400M12XM3

3.1.1.6.2 Module Power Terminals

The current loops in the XM3 power module have been designed such that they are wide, low profile, and evenly distributed between the devices so that they each have equivalent impedances across a switch position. The power terminals are vertically offset as shown in Figure 3-6 such that the bus bars between the DC link capacitors and the module can be laminated all the way up to the module without requiring bends, coining, standoffs, or complex isolation. A representative 3-phase inverter bussing is illustrated in Figure 3-7. Ultimately this achieves a low-inductance throughout the entire power loop from the DC link capacitors to the SiC devices. A XM3 module without devices was connected to a Keysight E4990A Impedance Analyzer to extract the parasitic inductance of the package. The power loop inductance from V+ to V- is 6.7 nH measured at 10 MHz.

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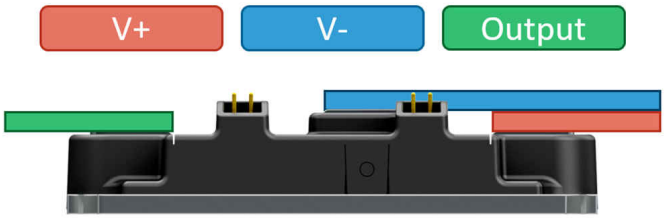

Figure 3-6. Side View of XM3 Module Showing Non-planar Power Leads

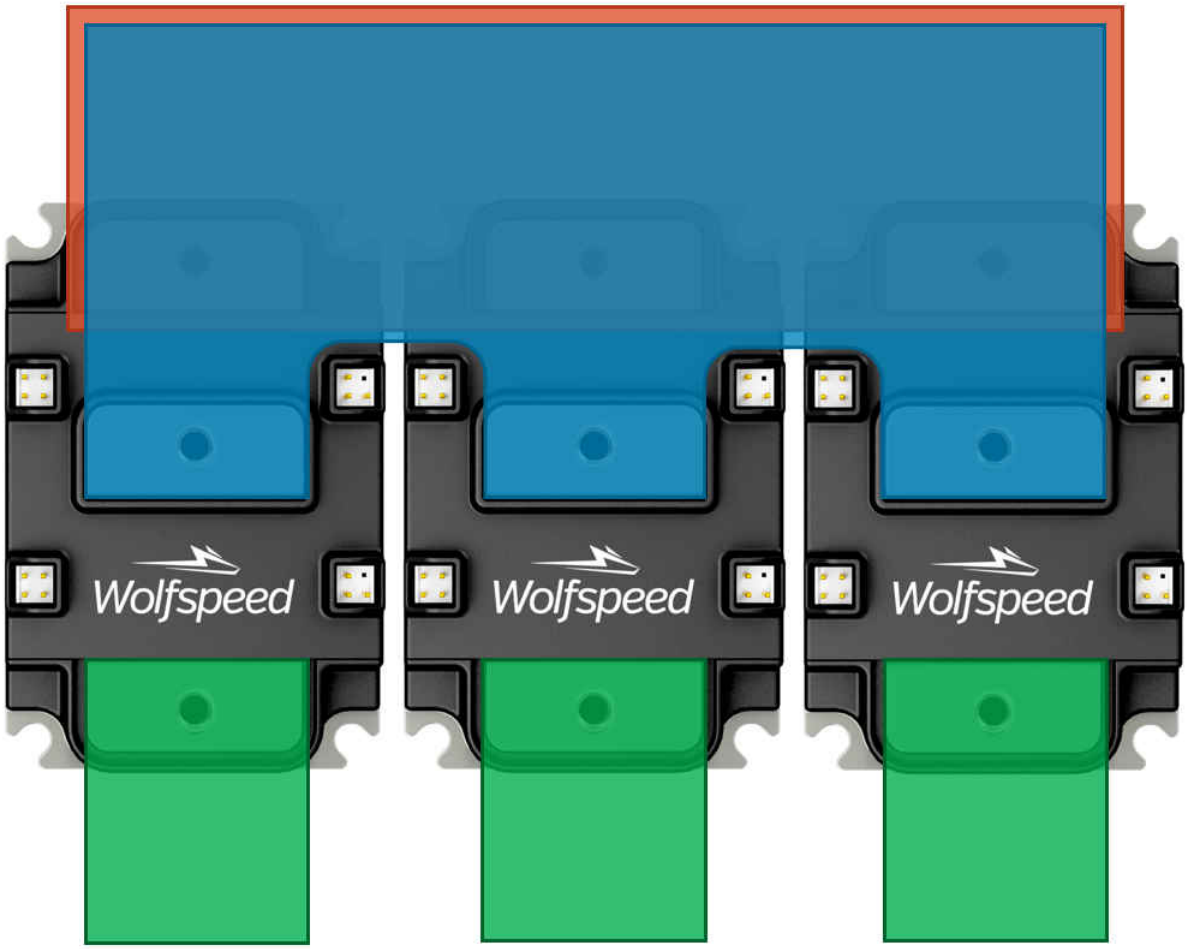

Figure 3-7. Illustration Showing 3-Phase Bussing Layout

3.1.1.6.3 Module Signal Terminals

The signal pins on the XM3 module consist of four sets of male header pins grouped by function located on the left and right edge of the module as shown in Figure 3-8. Along the left side are the gate pins for both the high side and low side switch positions and their associated source-kelvin pins. In the upper right position is the Desat/Overcurrent pins which are internally connected to the V+ power terminal to provide a connection point for high side gate driver protection circuitry to measure VDS. In the lower right position are the pins for the internal negative temperature coefficient (NTC) temperature sensor. The NTC is located on an electrically isolated substrate pad in close proximity to the lower switch power devices and can need additional galvanic isolation according to application requirements. With UCC5880-Q1 gate driver the NTC measurement signal is isolated up to 5.7 kV. The signal connectors on the right side both have one pin not populated so that the gate driver can be keyed to prevent improper installation.

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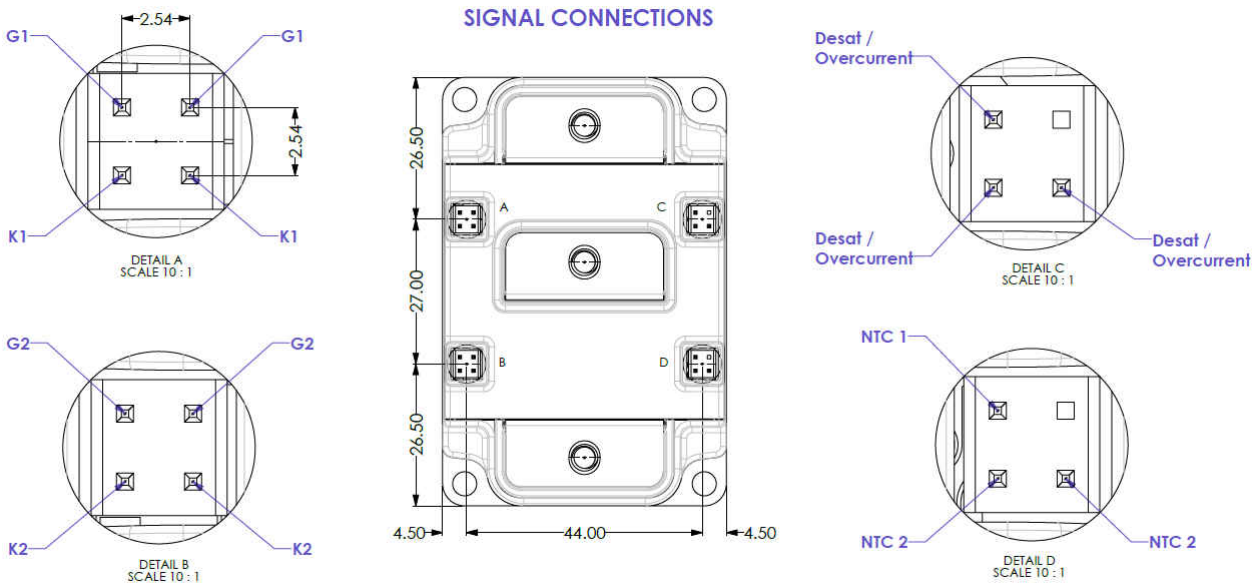

Figure 3-8. XM3 Module Signal Terminal Pinout

3.1.1.6.4 Integrated NTC Temperature Sensor

The NTC temperature sensor built into the power module is sensed and fed back to the controller via an isolated digital signal. This signal is a 50% duty cycle square wave with varying frequency. The temperature sensor is positioned as close as possible to the power devices while remaining electrically isolated from them and therefore provides an approximate baseplate temperature. The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs and must not be used as an accurate junction temperature measurement. There are two ways to measure the NTC feedback signal for the three XM3 modules with the controller. The first method is using the enhanced capture (eCAP) peripheral to digitally measure the frequency of the signal coming directly from the differential receivers. The relationship of the NTC signal frequency to the NTC temperature is given in Figure 3-9 and Table 3-4. For the second method, the frequency signal is filtered and converted into an analog signal which can be measured by ADC on the controller. The analog voltage measures 0.38 V when the frequency is 4.6 kHz and 2.5 V when the frequency is 30.1 kHz.

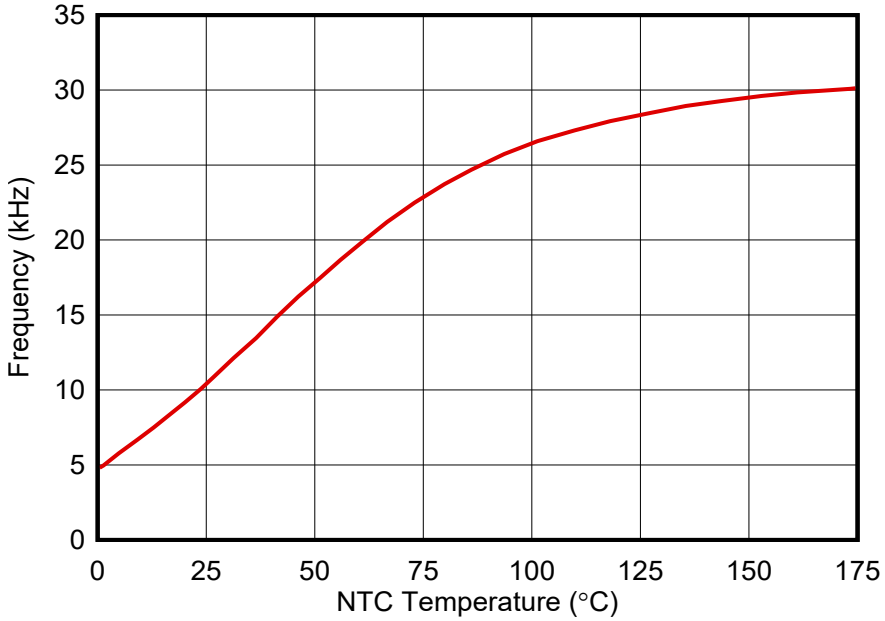

Figure 3-9. NTC Temperature vs Signal Frequency

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Table 3-4. NTC Temperature, Resistance, and Frequency Correlation

NTC Temperature (°C)	NTC Resistance (Ω)	Frequency Output (kHz)
0	13491	4.6
25	4700	10.3
50	1928	17.1
75	898	22.8
100	464	26.4
125	260	28.3
150	156	29.5
175	99	30.1

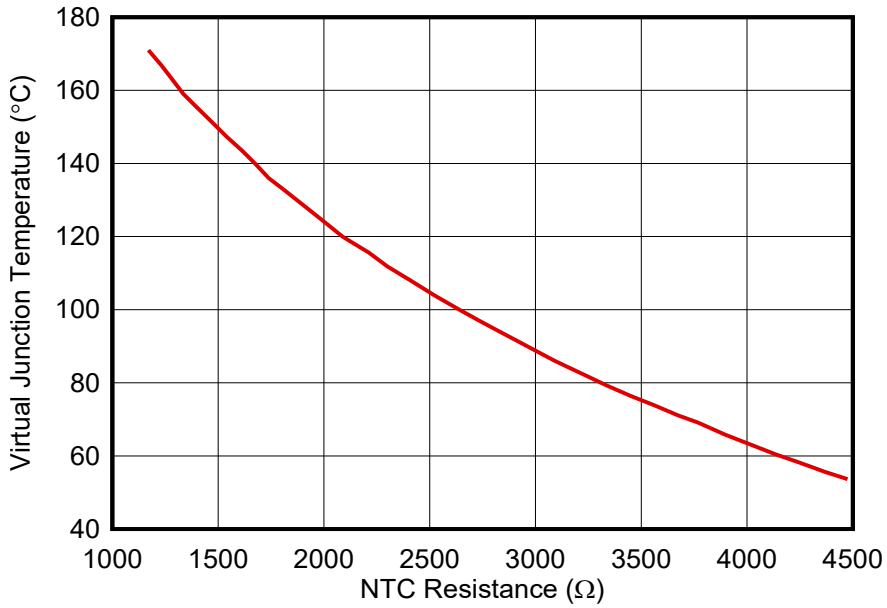

Figure 3-10. CAB450M12XM3 Virtual-junction Temperature (T_{VJ}) vs NTC Resistance with 25°C Coolant.

The mapping between the NTC resistance (R_{NTC} in Ohms) of the CAB450M12XM3 module and the virtual junction temperature (T_{VJ}) is shown in Figure 3-10. It is the calculated using the following equation:

$$T_{VJ} = -87.12 \times \ln(R_{NTC}) + 786.14 \quad (4)$$

One additional temperature sensor is installed on the controller PCB to provide a measurement of the ambient temperature inside the reference design case. This temperature sensor consists of a 10 kΩ NTC surface mount thermistor and a 10 kΩ fixed resistor forming a voltage divider. As the temperature increases so will the voltage at the midpoint of the voltage divider. This voltage is low-pass filtered to remove any high-frequency noise from the slowly changing temperature. The conversion between this voltage signal, V_T, and the temperature of the thermistor (in Kelvin) can be done with the following:

$$T = \left(\frac{\ln(3.3/V_T - 1)}{3900} + \frac{1}{298.15}\right)^{-1} \quad (5)$$

3.1.1.7 Laminated Busing and DC Bus Capacitors

The vertical offset of the module's power terminals allows the busbar design to remain simple and cost-effective while maintaining a low power loop inductance. A low-inductance busbar is utilized to interconnect the DC-link capacitors (located under the busbar) to the power modules. Again, the offset power module terminals enable the busbar assembly to have no bends or standoffs, which reduces cost and maximizes overlap. The capacitors are affixed as close as possible to minimize the total loop area. As can be seen in Figure 3-11, the busbars consist of one flat plate connecting V+ terminals of the modules and capacitors followed by an insulator and then a second flat plate connecting to the raised V- terminals of the modules and the capacitors with coining or spacer

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for the capacitor terminal. The structure is simple enough that it can be made with minimal fabrication which reduces the cost and lead-time.

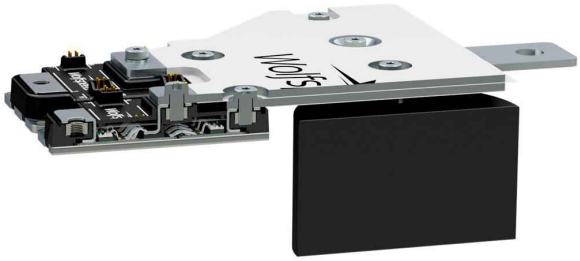

Figure 3-11. Cross-Section View of Laminated Busbar Structure Showing Power Loop

Optimized orientation for the capacitors was determined by measuring the inductance of three prototypes of the bussing geometry fabricated as two-layer PCBs. Between each prototype the capacitor terminals were rotated vertically, horizontally, and diagonally at 45 degrees. The horizontal orientation offered the lowest relative inductance with capacitors installed and is the orientation used for the laminated bussing.

The film capacitors serve two purposes: to close the high-frequency power loop and to provide local energy storage. To fulfill these roles the bus capacitors must be both low-inductance and have a high ripple current rating. The reference design features three Fischer & Tausche® CX100µ1100d51KF6 capacitors each rated to 100 A ripple current and 100 µF. A 1100 V voltage rating is sufficient for operating on a 900 V maximum DC bus with allowance for peak overshoots from aggressive switching rates. Each capacitor has an equivalent series inductance (ESL) of 10.5 nH. Having three of these capacitors reduces the total ESL for the capacitor bank to 3.5 nH which with a total measured inductance for the DC bussing and capacitors of 5.3 nH means the bussing by itself contributes 1.8 nH. The 5.3 nH inductance of the DC bus plus 6.7 nH power loop inductance for the XM3 module results in a combined power loop inductance of 12 nH which is lower than the stray inductance of many standard footprint modules alone.

3.1.1.7.1 Discharge PCB

Due to the large amount of energy storage possible in the DC bus capacitors, discharge resistors are required to bring the DC bus to a safe voltage in a reasonable amount of time. The Discharge PCB mounts to the V+ and V- terminals of one of the DC bus capacitors and has high-power surface mount resistors in addition to a board-to-board connector for the DC bus voltage sense measurement on the Controller. The resistors are sized to discharge the bus from a nominal voltage of 800 V to less than 50 V in under a minute. This requires the resistor network to dissipate a maximum of 9.4 W across 9 resistors and it has a working voltage rating of 1500 V.

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3.2 Test Setup

3.2.1 Software Setup

If not installed, download and install Code Composer Studio (CCS) which is needed to build and run the project. CCS version 12.2.0 or newer is recommended for this project. CCS User's Guide provides more details about CCS installation and use.

The software for TIDM-02014 is provided as part of C2000Ware MotorControl SDK. Note that C2000Ware MotorControl SDK installation is separate from CCS installation. Once the SDK is installed, use the following guidelines to import and run the project in CCS.

3.2.1.1 Code Composer Studio Project

To import the software project for TIDM-02014 into CCS, click **Project** → **Import CCS Projects**, and browse to `<SDK install location>\designs\tidm_02014\<device>\ccs` and click **Select Folder**. Select the project named *tidm_02014_<device>* and click **Finish**. The project is now be visible in the **Project Explorer** pane in CCS. The user's guide provides further details on *Importing Projects into CCS*.

The folder *src_foc* includes the typical FOC modules, including park and clarke transforms, PID functions, and estimators. These modules are independent of the specific device and board and are used across several other designs in the SDK.

The folder *src_control* includes motor drive control files that call motor control core algorithm functions within the interrupt service routines and background tasks. The folder *src_sys* includes some files reserved for other system features such as drivers for CAN communication. The user can their own code for system control, communication, and so forth. These modules are specific to this reference design project but are independent of the device and board.

Board-specific, motor-specific and device-specific files are in the folder *src_board*. These files consist of device-specific drivers to run the design. If you want to migrate the project to your own board or other devices, you only need to make changes to the files *hal.c*, *hal.syscfg* (or *hal_dclinkss.syscfg* if used), *hal.h*, and *user_mtr1.h* based on the pin assignments and features of your device or board.

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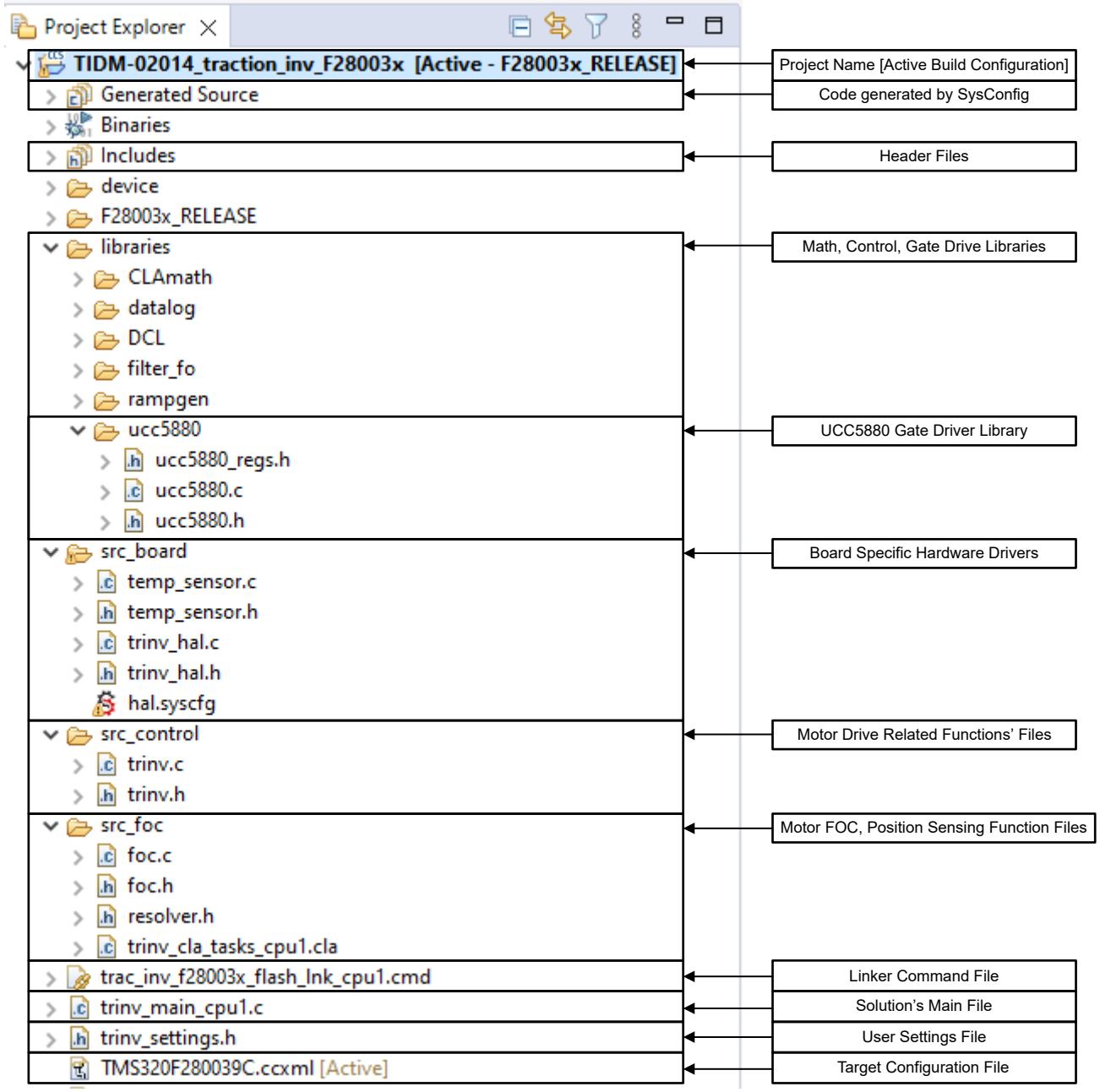

Figure 3-12. Project Explorer View of the Reference Project

The default build configuration for the *tidm_02014* project is named *F28003x_RELEASE* and uses *hal.syscfg* file to configure the ePWM, CMPSS, and ADC peripherals and the GPIOs. The project's predefined symbols and include the single-shunt current reconstruction library files and function calls as part of the build.

The default build configuration can be modified by right-clicking the project and going to **Build Configurations → Manage**. Users can add or modify build configurations for different test cases.

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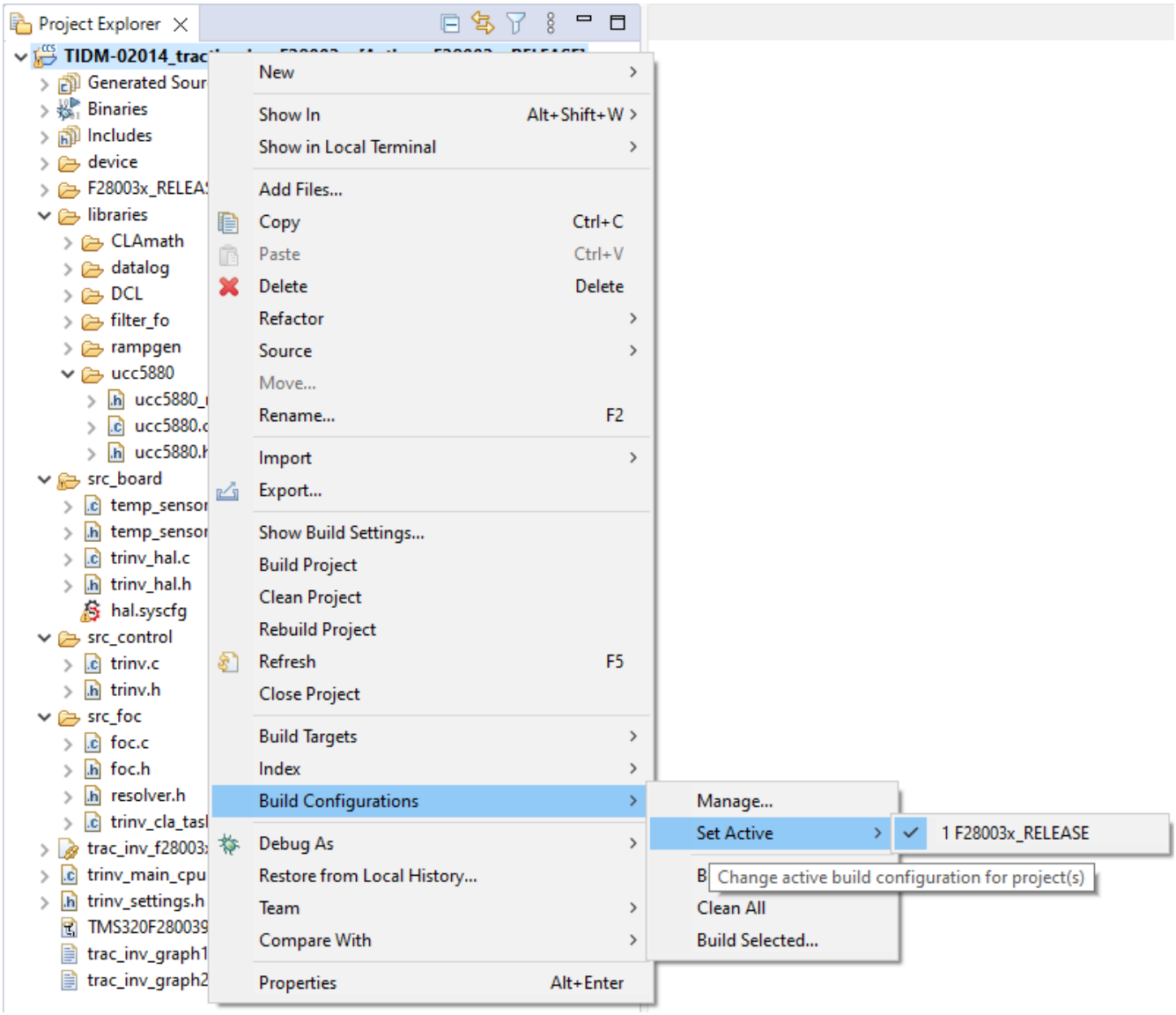

Figure 3-13. Selecting Active Build Configuration

Different operational modes of the system can be enabled or disabled using predefined symbols in the project properties. The options are as follows:

- **CLOSED_CURRENT_LOOP** to enable closed-loop

  control of the d and q axis motor currents.
- **CLOSED_SPEED_LOOP** to enable

  closed-loop speed control.

Adding these symbols to the predefined symbols list enables the respective functionality. To view and edit the predefined symbols, right-click on your project and select **Properties**. Then go to the **Predefined Symbols** section of the **C2000 Compiler** options as shown in Figure 3-14. By default the above symbols are defined in the pre-defined symbols list and the corresponding features are enabled.

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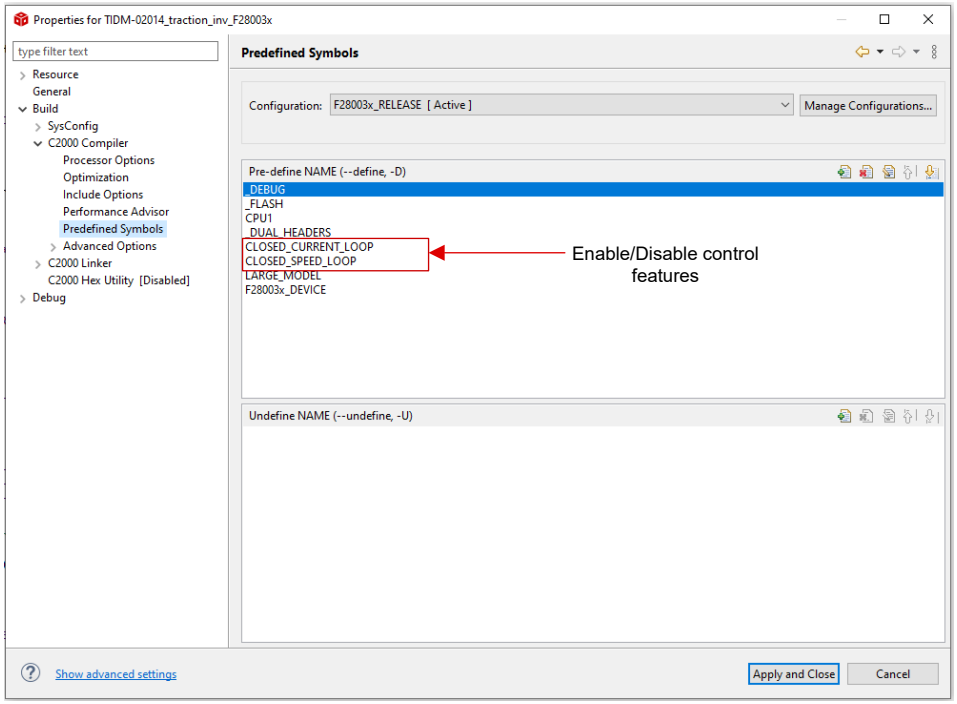

Figure 3-14. Selecting Predefined Symbols in the Project Properties

3.2.1.2 Software Structure

The general structure of the project is shown in Figure 3-15. The device peripheral configuration is based on C2000Ware Driverlib and is partially generated using SysConfig, making the code portable across hardware and devices. To port the reference design software to a different board or device, the user only needs to change the *trinv_hal.c*, *trinv_hal.syscfg*, and *trinv_hal.h* files and the parameters in *trinv_settings.h*.

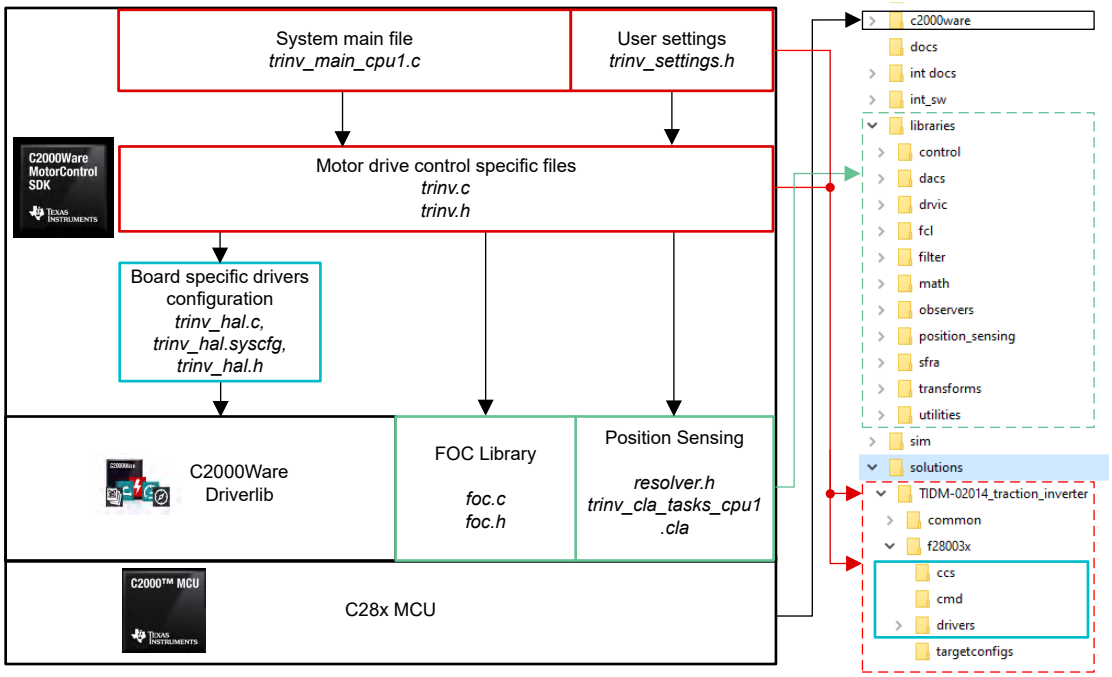

Figure 3-15. Project Structure Overview

Figure 3-16 shows the project software flow diagram of the firmware that includes one ISR for real time motor control, a main loop that allows the user to update motor control parameters through debug window. The ISR is triggered by ADC End of Conversion (EOC). The functions that run in the main ISR are defined in *trinv.h* header

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file. In addition, in this design, accurate motor position is sensed through a resolver interface. The function that reads the ADC values for the resolvers signals and performs corresponding position, speed calculations runs in the control law accelerator (CLA) which is an independent processing core. The function is defined in *trinv_cla_tasks_cpu1.cla* file.

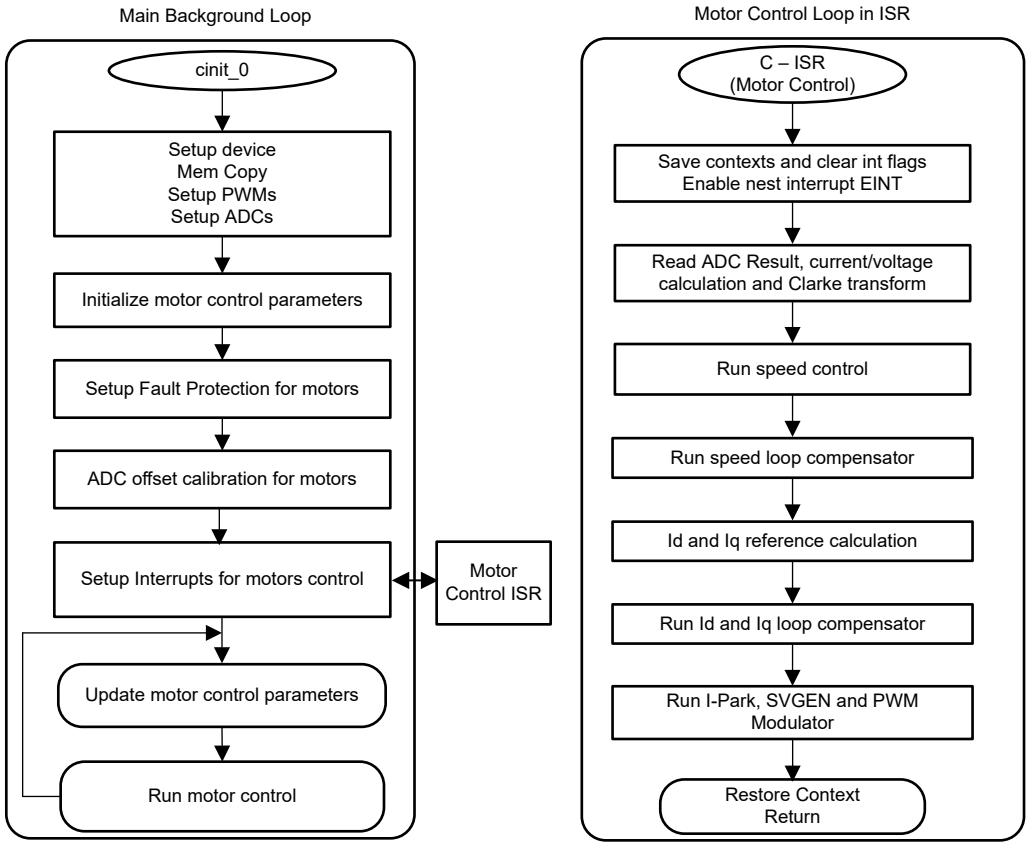

Figure 3-16. Flowcharts of Background Software and Motor Control ISR

3.3 Test Procedure

The motor control software can be configured for different test modes to enable incremental software testing. For example, if neither of the **CLOSED_CURRENT_LOOP** or **CLOSED_SPEED_LOOP** symbols are defined, the V_d and V_q reference values are directly set to default test values. This mode can be used for testing the PWM setup and open-loop inverter operation. Similarly, only defining **CLOSED_CURRENT_LOOP** and not **CLOSED_SPEED_LOOP**allows setting up the i_d, i_q references directly. In this case, the motor speed can be set by setting the ramp generator frequency.

The user motor type and the corresponding parameters can be found in the *trinv_setting.h* file. The default setting can be changed by changing the value of the *USER_MOTOR* macro. If the user intends to use an outside the list of predefined motors, the user can copy the template used.

3.3.1 Project Setup

Import the project into CCS and select the appropriate build configuration. Right-click on the project in the **Project Explorer** and select **Rebuild Project**. Confirm that the **Console** pane shows that the project built without any errors.

On successful completion of the build, with the *tidm_02014* project selected, go to **Run** → **Debug** or click the **Debug** button on the tool bar. By default the project will launch a debug session using the *TMS320F280039C.ccxml* file in the project. *TMS320F280039C.ccxml* is configured to use the Texas Instruments XDS110 USB Debug Probe on board the TMDSCNCD280039C controlCARD.

After clicking **Debug**, CCS will automatically connect to the target, load the output file into the device, and change to the **CCS Debug** perspective. The program should be halted at the start of main().

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If the **Expressions** pane is not already open, click **View** → **Expressions** in the CCS menu bar. You can either add variables manually or you can import a recommended list of variables associated with this build level by right-clicking within the **Expressions** window, selecting **Import...**, and finding the file `<SDK install location>\solutions\tidm_02014\common\debug\tidm_02014.txt`. Click **OK** and the window will be populated with variable.

Click the **Continuous Refresh** button in the Expressions window tool bar to tell CCS to update the data continuously at a rate defined in the CCS debug preferences.

3.3.2 Running the Application

Run the code by going to **Run** → **Resume** or clicking the **Resume** button in the tool bar. The project can now run and the variables display in the Expressions window. Check the following to confirm the application and hardware set up are working:

- The green power LEDs on the gate-drive boards must be on. If the gate-drivers are initialized without faults, none of the red, nFault LEDs are on. Gate drive initialization status can be checked through the *tripFlagDMC.fault.UCC5880_status* variable.
- Similarly other variables in the *tripFlagDMC* struct show the status of other faults. If no fault flags are set, to run the test motor, the *runMotor* can be set to RUN_MOTOR. Your variables need to appear similar to what is shown in Figure 3-17.
- If no faults are detected, the *motor1.isrCount* must increment continuously.
- Check the calibration offsets of the motor inverter board. The offset values of the motor phase current sensing values must be equal to approximately half of the scale current of ADC.
- The PWM output for motor drive can also be probed with an oscilloscope.

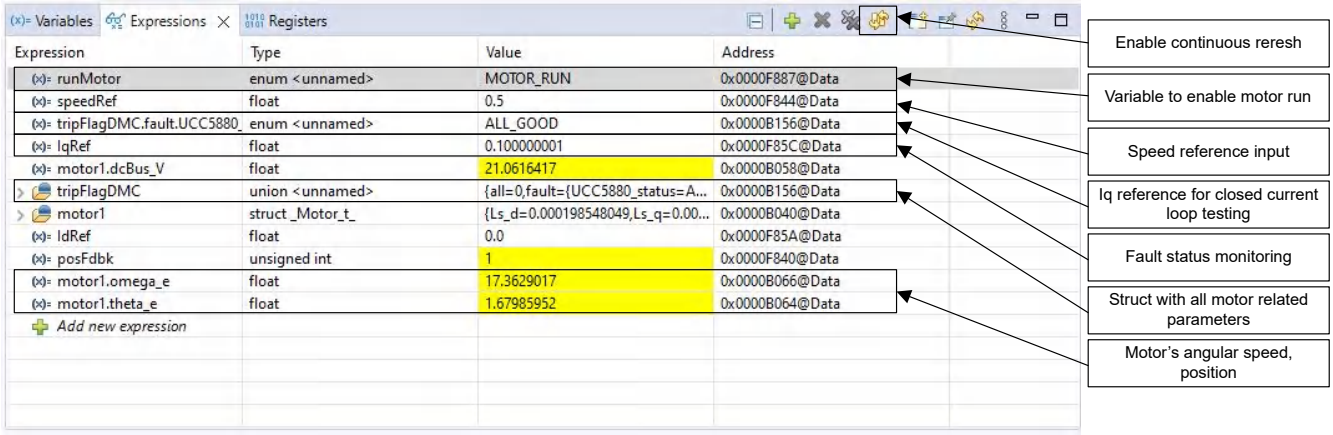

Figure 3-17. Runtime Control and Debug through Expressions View

You can halt the CPU by first clicking the **Suspend** button on the toolbar or by selecting **Target** → **Suspend**. To run the application from the start again, reset the controller by clicking on the **CPU Reset** tool bar button or clicking **Run** → **Reset** → **CPU Reset** and then clicking on the **Restart** button or **Run** → **Restart**. You can close the CCS debug session by clicking the **Terminate** button or by clicking **Run** → **Terminate**. This will halt the program and disconnect CCS from the controller.

Note that it is not necessary to terminate the debug session each time you change the code. Instead you can go to **Run** → **Load** → **Load Program...** (or **Reload Program...** if it is the same file). CCS will also automatically prompts to ask if you want to reload your executable if it detects you have rebuilt it.

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3.4 Test Results

In this section, results of tests performed on the system components are presented. The results for the gate drive and bias supply are presented followed by full inverter system.

3.4.1 Isolated Bias Supply

The startup behavior of UCC14240-Q1 is validated as shown in Figure 3-18.

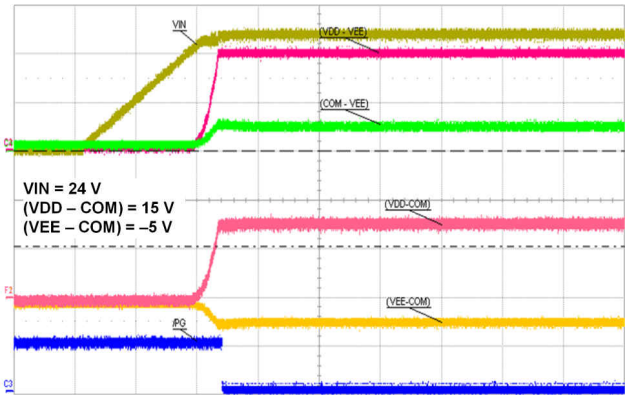

Figure 3-18. UCC14240-Q1 Power-up Sequence

The load regulation test is performed to verify the stability of UCC14240-Q1. The electronic load is connected between VEE and VCC, with the load steps from 0 to 80 mA. Measured output voltage is presented in Table 3-5.

Table 3-5. UCC14240-Q1 Load Regulation

Load(mA)	V_{out}(V)	Power(W)
10	18.853	0.188
20	18.848	0.377
30	18.84	0.565
40	18.834	0.753
50	18.83	0.941
60	18.828	1.13
69	18.825	1.3
80	18.819	1.505

The nominal voltage value is 19 V and the equation for the load regulation is:

$$\text{Load regulation} = \left(\frac{V_{max} - V_{min}}{V_{nom}}\right) \times 100 = 0.18\% \quad (6)$$

3.4.2 Isolated Gate Driver

Double pulse test under 800 V is carried out to evaluate the switching behavior for the different adjustable gate drive strengths. The following results show the difference between weak drive (5 A) and strong drive (15 A). The waveforms of the gate-source voltage, drain-source voltage and drain currents are shown in the following figures. The turn off energy is measured at the end of the first pulse, while the turn on energy is measured at the beginning of the second pulse. The measurement results are presented in Figure 3-19.

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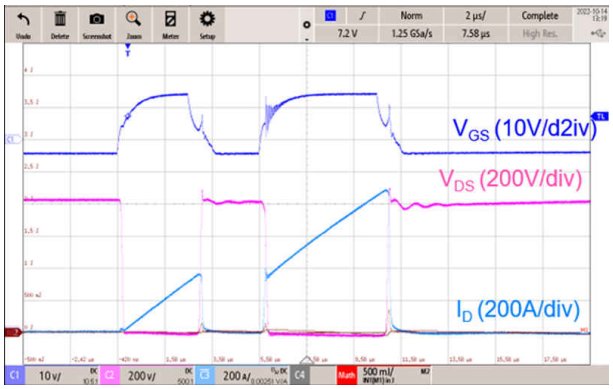

Figure 3-19. Double Pulse Test with Weak Drive Strength

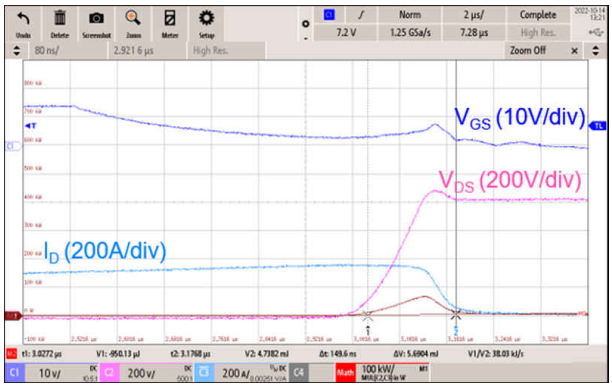

Figure 3-20. Turn-off Waveforms with Weak Drive Strength

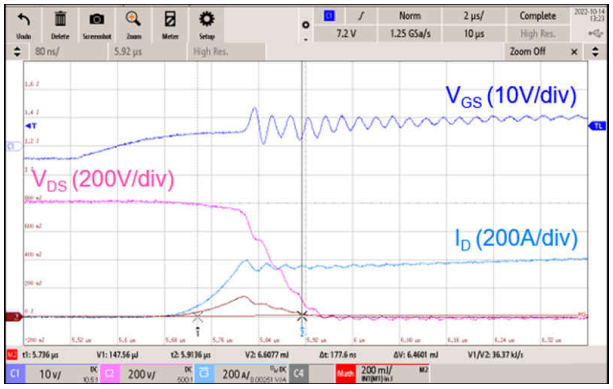

Figure 3-21. Turn-on Waveforms with Weak Drive Strength

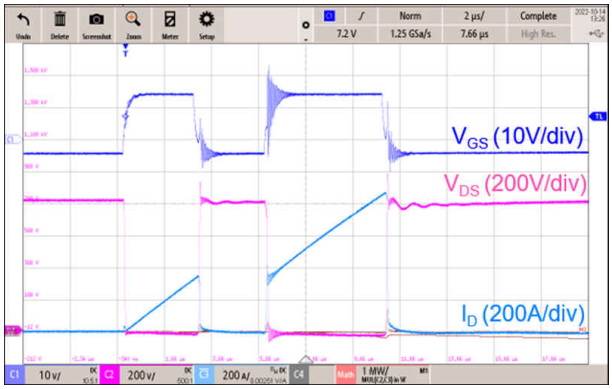

Figure 3-22. Double Pulse Test with Strong Drive Strength

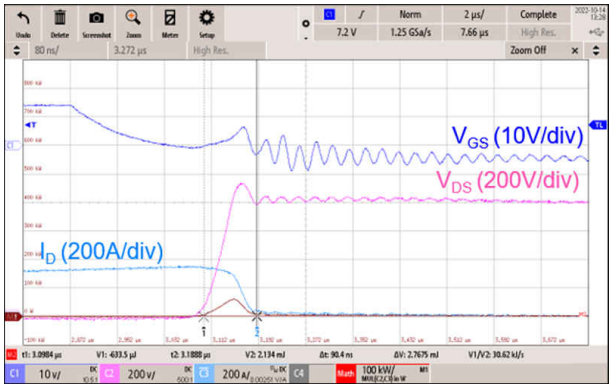

Figure 3-23. Turn-off Waveforms with Strong Drive Strength

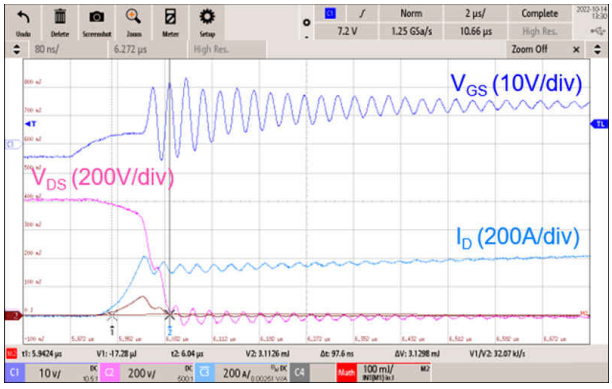

Figure 3-24. Turn-on Waveforms with Strong Drive Strength

Table 3-6. Switching Energy Measurements

	Weak drive (5 A)	Strong drive (15 A)
Turn-off energy	5.65 mJ	2.77 mJ
Turn-on energy	6.46 mJ	3.13 mJ

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3.4.3 Inverter System

The traction inverter system was tested at the rated voltage and power levels with an inductive load. The UCC5880-Q1 gate driver's drive strength was varied to study its impact on the system's efficiency. The scope plots for the SiC MOSFET's drain-source voltages (V_{ds}) and phase currents are shown in the following figures. The test waveforms with weak and strong gate drive stregths are shown in Figure 3-25 and Figure 3-27 respectively. The test conditions and obtained power results are shown in Table 3-7. In an inductive load test, the load power recirculates. Therefore, external DC supply only supplies the system losses, which is quantified as P_{loss}. It is seen that with a higher drive strength, the system losses also reduce. This is primarily due to the reduction in switching losses. However, as seen in Figure 3-27, higher drive strength also increases the drain-source voltage overshoot on the SiC MOSFETs. The variable drive strength feature of the UCC5880-Q1 gate driver allows the real-time optimization of system losses.

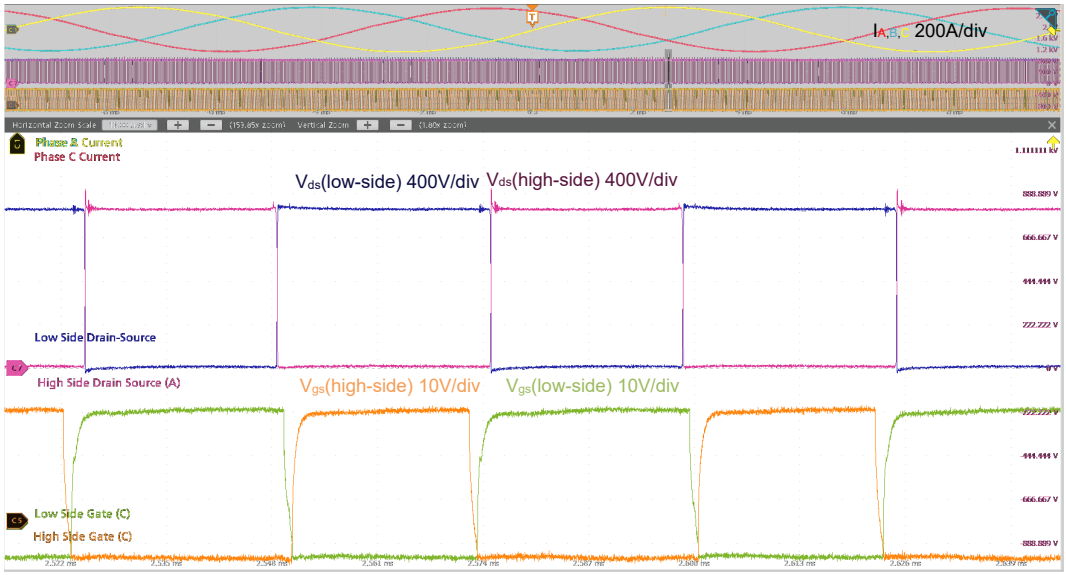

Figure 3-25. Voltage and Phase Current Waveforms with Weak Gate Drive Strength (I_{RMS} = 285 A)

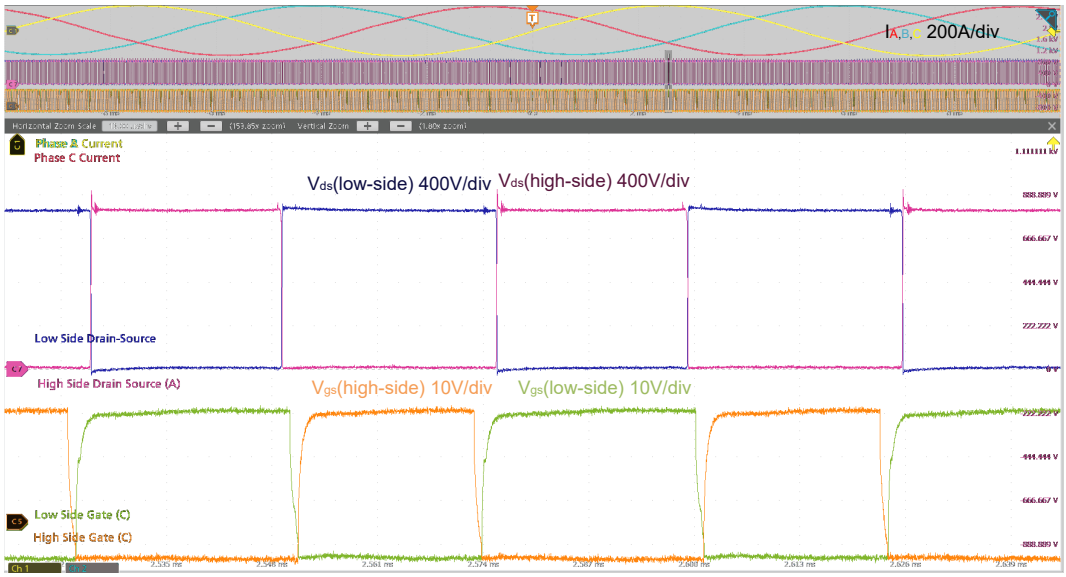

Figure 3-26. Voltage and Phase Current Waveforms with Weak Gate Drive Strength (I_{RMS} = 320 A)

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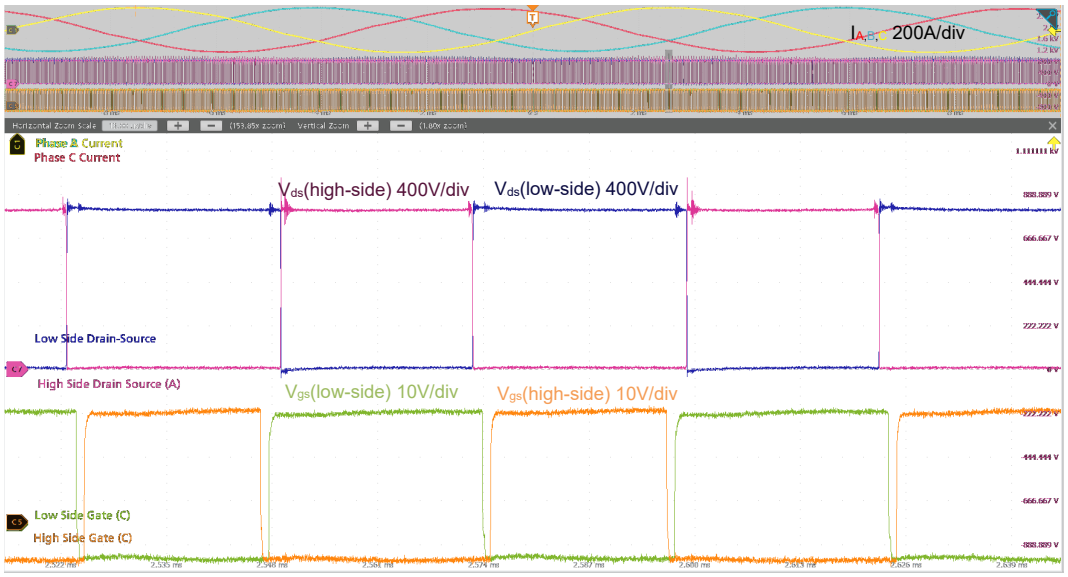

Figure 3-27. Voltage and Phase Current Waveforms with Strong Gate Drive Strength (I_{RMS} = 285 A)

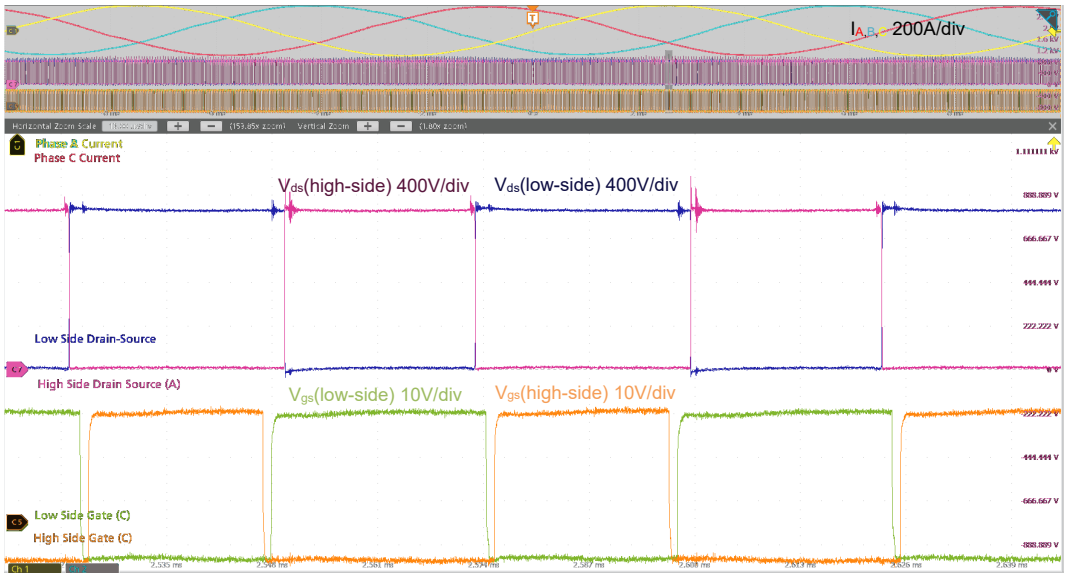

Figure 3-28. Voltage and Phase Current Waveforms with Strong Gate Drive Strength (I_{RMS} = 320 A)

Table 3-7. Test Conditions and Results

Gate-drive Strength	DC Bus Voltage	RMS Current	P_{loss}
Weak	800 V	285 A	4.2111 kW
Weak	800 V	320 A	5.1627 kW
Strong	800 V	285 A	2.273 kW
Strong	800 V	320 A	2.747 kW

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4 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center for further information.

Save all warnings and instructions for future reference.

> **WARNING**
>
> Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Re-validate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

   > **WARNING**
   >
   > While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

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5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDM-2014.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDM-2014.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at TIDM-2014

5.1.4 Altium Project

To download the Altium project files for each board, see the design files at TIDM-2014

5.1.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDM-2014

5.1.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at TIDM-2014

5.2 Tools and Software

Tools

TMDSCNCD280039C	The TMS320F280039C evaluation module controlCARD is a low-cost evaluation and development board for the series of F28003x devices. TMS320F280039C is used as a daughter card for this design connected to the reference board through a standard 180-pin controlCARD HSEC interface.
TMDSCNCD263	TMDSCNCD263 is an HSEC180 controlCARD based evaluation and development tool for the AM263x series Sitara™ high-performance microcontrollers. This board is designed for initial evaluation and prototyping as it provides a standardized and easy-to-use platform to develop your next application.

Software

C2000WARE-MOTORCONTROL-SDK	The MotorControl SDK is a set of software, tools, and documentation designed to C2000 real-time controller based motor control system development time.
MCU-PLUS-SDK-AM263X	The AM263x microcontroller (MCU) plus software development kit (SDK) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations.

5.3 Documentation Support

1. Mouser, *Easy 1B/2B Automotive Power Modules Power Module for Hybrid- and Electric Vehicles*, product brief.
2. Texas Instruments, *Dual Isolated Outputs Fly-Buck Power Module Reference Design for Single IGBT Driver Bias*, design folder.
3. Wurth Electronics, *Specification Sheet: 750315445*.
4. Texas Instruments, *Passing CISPR25 Radiated Emissions Using the TPS54160-Q1*, application note.
5. Texas Instruments, *TPS54xx0-Q1 and TPS57xx0-Q1 Design Calculation Tool*.
6. Wurth Electronics, *Specification Sheet: 760390014*.

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5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Terminology

AFE – Analog Front End

NTC – Negative Temperature Coefficient Thermistors

LDO – Low-dropout regulator

UVLO – Under Voltage Lock Out

TVS – Transient Voltage Suppression

CMTI – Common Mode Transient Immunity

DESAT – Desaturation

IGBT – Insulated Gate Bipolar Transistor

MOSFET – Metal-oxide-semiconductor field-effect transistor

PWM – Pulse Width Modulation

SiC - Silicon Carbide

MCU – Microcontroller Unit

BJT – Bipolar Junction Transistor

PCB – Printed Circuit Board

RPM – Revolutions Per Minute

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