Technical White Paper

Optimizing Chopper Amplifier Accuracy

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ABSTRACT

Zero-drift amplifiers have very low input offset voltage (V_{os}), low offset drift, and no flicker noise. The two main types of zero-drift amplifiers are chopper and auto-zero amplifiers. This paper focuses on chopper amplifiers because these amplifiers are by far the most common type of zero-drift amplifier and most of the chopper concepts apply to auto-zero devices as well. Chopper amplifiers achieve the low V_{os} and V_{os} drift through the use of an internal calibration circuit that uses metal-oxide semiconductor field-effect transistor (MOSFET) switches to commutate the inputs. However, this calibration technique generates current transients within the amplifiers input bias current. These transients flow through the amplifiers feedback network and source impedance generating additional offset voltage, offset drift, and transient noise tones. The magnitude of this error increases when large feedback resistances or source impedances are used. Furthermore, this error is dependent on the details of the chopper amplifier design, so that some products are more susceptible to V_{os} shift than others. This white paper provides details on how the magnitude of offset, drift, and noise can be impacted by source and feedback impedance for different chopper amplifier products. The document covers a method for selecting the best chopper amplifier for your application, and clarifies when a chopper amplifier is not an appropriate choice.

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1 Benefit of Zero-Drift Amplifiers

Zero-drift amplifiers use an internal calibration method to minimize the amplifiers input offset voltage (V_{os}). Since this calibration happens continuously, the change in offset over temperature is also minimized. Zero-drift amplifiers additionally improve some other parameters that relate to how offset changes versus system or environmental factors. For example, power supply rejection ratio (PSRR) is a measurement of how the amplifiers offset is impacted by changing in power supply voltage, so this specification is generally better for zero-drift amplifiers than traditional topologies. Power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and open loop gain (A_{OL}) are all measurements of how the V_{os} is impacted by changing different amplifier operating conditions, so those specifications are generally much better for zero-drift amplifiers than for traditional topologies. Similarly, electromagnetic rejection ratio (EMIRR) is a measurement of how offset changes versus applied electromagnetic interference, so this is also generally improved in choppers.

For traditional amplifiers the noise increases at low frequency (called 1/f or flicker noise). Flicker noise can be thought of as a variation of input offset voltage versus time. Thus, chopper amplifiers eliminate 1/f noise. Figure 1-1 and Figure 1-2 compare a traditional amplifier noise spectral density to a zero-drift amplifier.

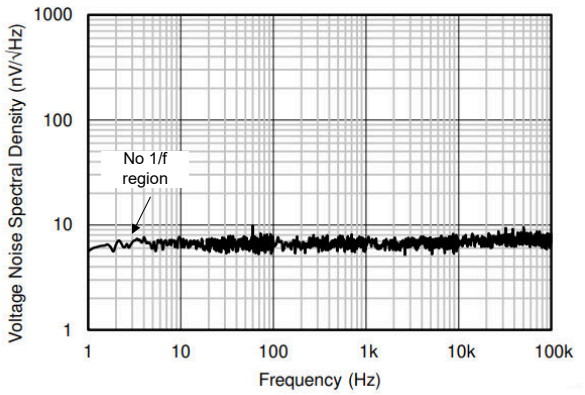

Figure 1-1. OPA388 Noise Zero-Drift Example

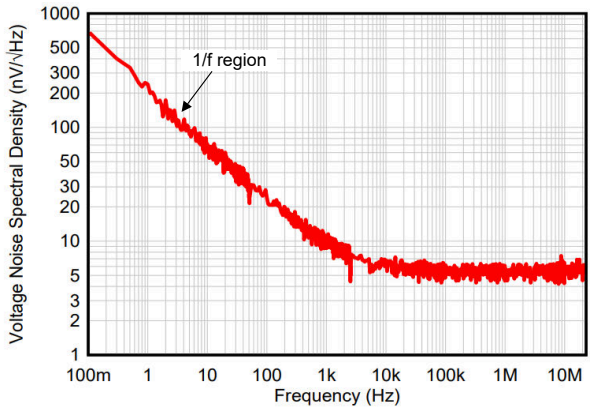

Figure 1-2. OPA328 Noise Traditional CMOS Example

The low offset voltage of chopper amplifiers makes them an excellent choice for applications requiring high DC precision. However, as with most innovations, there are some tradeoffs that limit the effectiveness in certain applications. The goal of this document is to show the limitations of zero-drift amplifiers so that you can make an informed decision whether a zero-drift amplifier is the right choice for your specific application.

Table 1-1 compares the DC specifications like V_{os} and V_{os} drift of zero-drift amplifiers to traditional amplifiers with the best-in-class DC performance. The offset voltage of the zero-drift device is on average two to five times better than a traditional precision amplifier. The traditional devices used in this comparison are the best-in-class for DC precision and use package or laser trim to achieve the precision specification. Many other traditional amplifiers can have offsets much greater than the examples in Table 1-1 (hundreds of microvolts). The V_{os} drift of the zero-drift amplifiers is often tens or even hundreds of times better than traditional counterparts. The excellent stability of offset over temperature is the is the greatest advantage of zero drift amplifiers.

Table 1-1 also compares the 0.1Hz to 10Hz noise. Broadband noise is inversely correlated to the quiescent current. Therefore, when comparing noise between two different amplifier topologies, comparing devices with similar quiescent current is the best practice. With this in mind the comparison shows a significant low frequency noise advantage for zero-drift devices.

Table 1-1. Comparison of Zero-Drift Specifications to Comparable Traditional Amplifiers

Amplifier	Feature	Tech.	Max V_{os} (µV)	Max V_{os} Drift (µV/°C)	I_Q TYP (mA)	0.1Hz to 10Hz Noise (μV_{PP})	TYP PSRR (µV/V)	TYP CMRR (dB)	TYP Aol (dB)	EMIRR at 100MHz (dB)
OPA392	e-Trim™	CMOS	10	0.6	1.22	2.0	0.5	120	132	29
OPA277	Laser trim	Bipolar	20	0.15	0.79	0.22	0.3	140	140	38
OPA206	e-Trim™	Bipolar	25	0.5	0.22	0.2	0.05	140	132	45
OPA928	e-Trim™	CMOS	25	0.8	0.275	1.4	0.3	140	134	27
OPA191	e-Trim™	CMOS	25	0.8	0.14	1.4	1.0	140	120	27
OPA210	Laser trim	Bipolar	35	0.5	2.20	0.09	0.05	168	132	35
OPA189	Zero-drift	CMOS	3	0.02	1.30	0.1	0.005	168	170	63
OPA182	Zero-drift	CMOS	4	0.012	0.85	0.119	0.005	168	170	55
OPA388	Zero-drift	CMOS	5	0.05	1.70	0.14	0.1	138	148	41
OPA333	Zero-drift	CMOS	10	0.05	0.017	0.3	1.0	130	130	65
OPA187	Zero-drift	CMOS	10	0.015	0.10	0.4	0.01	145	160	49
OPA186	Zero-drift	CMOS	10	0.04	0.09	0.075	0.02	134	148	51
OPA188	Zero-drift	CMOS	25	0.085	0.425	0.25	0.075	146	136	48

2 Internal Operation of Choppers

From a very high level, a traditional op-amp internal topology has at least two stages: transconductance, and transimpedance. The transconductance stage amplifies the differential input signal and converts the signal to a current ($V_{in} \times g_m = i_{out}$). The output current of the transconductance stage drives the transimpedance stage which converts the transconductance current to a voltage. The feedback element in the transimpedance stage is the Miller capacitance (C_c), and the transconductance output current charges this capacitor to convert the current to a voltage. The chopper amplifier has the same two stages as the traditional amplifier, but the input and output of the transconductance stage is connected through a switch matrix that reverses the polarity of the input and output connections during each chopping calibration cycle (see Figure 2-1). The rest of this section documents how this switching of the chopper allows for normal amplifier amplification while minimizing offset.

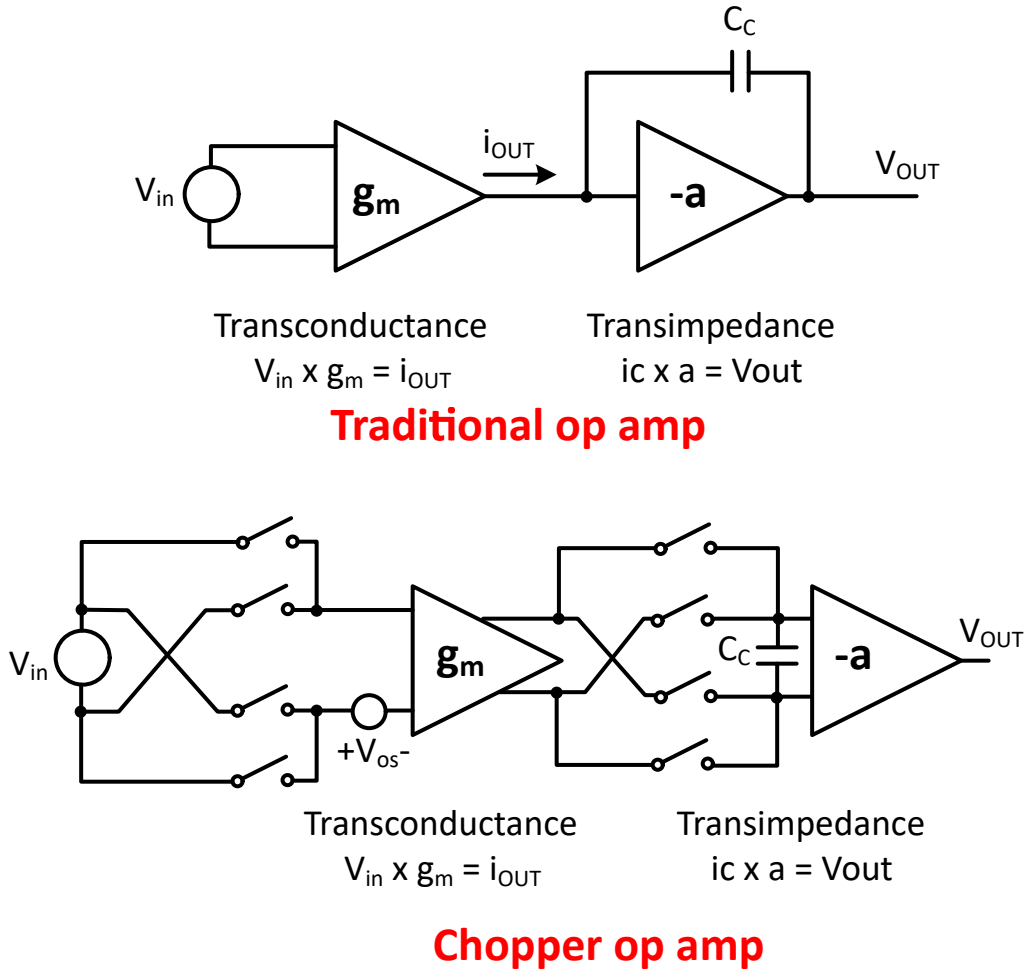

Figure 2-1. Basic Topology of Zero-Drift and Traditional Amplifiers

Figure 2-2 illustrates the relationship between the input and output for each half of the chopping calibration cycle. In the first half of the calibration cycle, the input signal is inverted at the input of the transconductance amplifier. The output of this stage is simultaneously inverted before the output is applied to the transimpedance stage Miller capacitance. During the second half of the calibration cycle neither the input or output are inverted. Thus, in each half of the calibration cycle, the signal driving the transimpedance stage Miller capacitance is the same, and the amplifier is effectively the identical to the traditional op amp from a signal phase perspective.

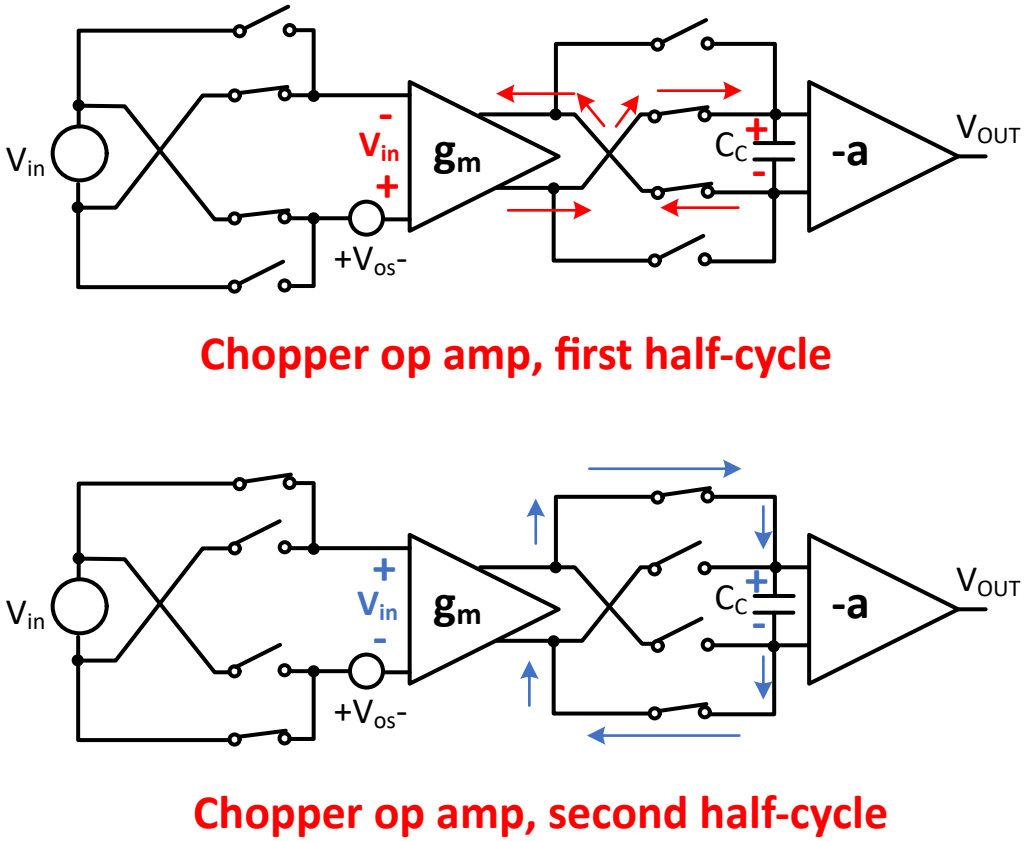

Figure 2-2. Chopper Amplifier Input Signal Path During Each Calibration Cycle

Figure 2-3 illustrates the relationship between the input offset voltage and output for each half of the chopping calibration cycle. Notice that the polarity of the input offset on the input of the transconductance (g_m) stage is the same for both cycles. The resulting V_{os} signal at the output of the transconductance stage is flipped each half-cycle so that the Miller capacitor is charged oppositely each half-cycle. The transconductance stage converts the constant input offset voltage to a constant current. When a constant current is applied to a capacitor, the voltage on the capacitor changes linearly. Thus, the transconductance stage output current generated by the input offset voltage causes the voltage on the Miller capacitor (C_c) to ramp linearly. The ramp signal changes direction each half-cycle, so that the offset voltage is translated into a triangle wave across the Miller capacitor (see Figure 2-4). The triangular waveform multiplied by a gain factor becomes the output offset of the amplifier. Since the average is close to zero, the average input offset voltage is approximately zero. Thus, in the case of an actual amplifier with inherent input voltage offset of ±1mV and offset drift of ±1µV/C, the addition of chopping scheme lowers both of them by the factor of 100, down to about ±10µV and ±10nV/C, respectively. Thus, the calibration achieved the goal of minimizing the average offset voltage; however, the triangle waveform is an undesirable signal at the amplifier output. For this reason, the triangular waveform is minimized through the use of a synchronous notch filter.

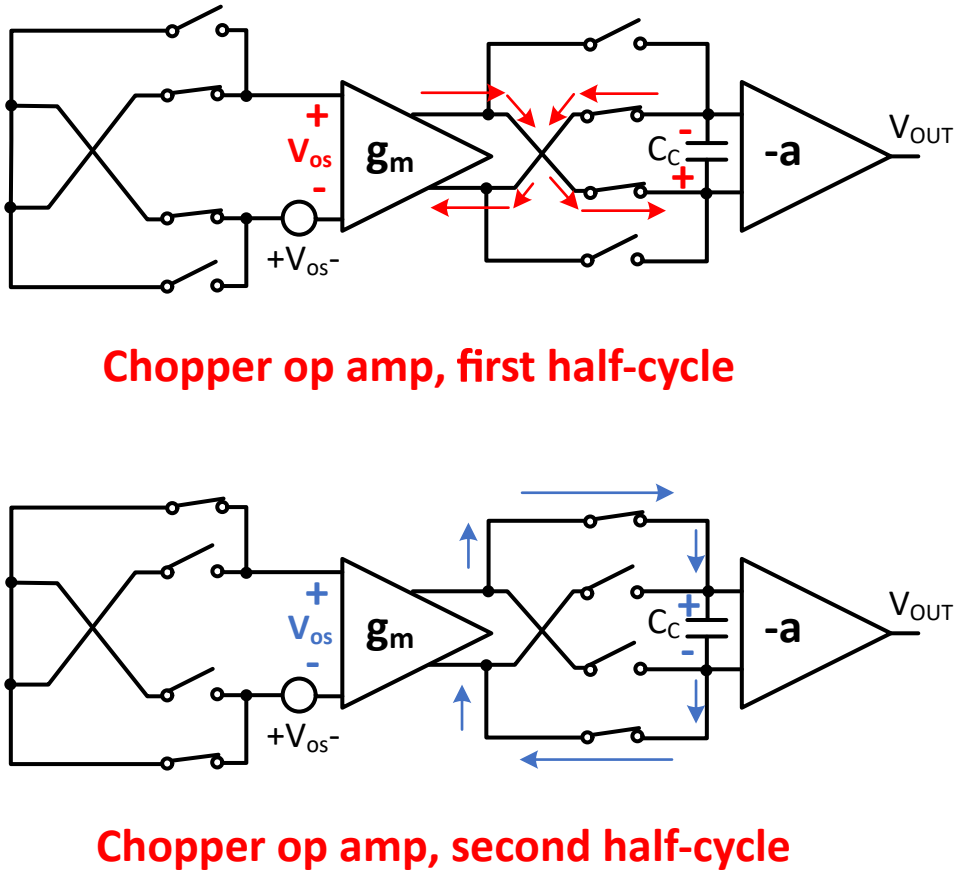

Figure 2-3. Chopper Amplifier Input Offset Voltage Path During Each Calibration Cycle

The Fourier theorem states that any periodic waveform can be expressed as a series of sinusoidal waveforms called a Fourier series. The different sinusoids in the series are called harmonics and appear at multiples of the fundamental frequency. Figure 2-4 shows the Fourier series for a triangular waveform. Triangle waveforms only have harmonics at odd multiples of the fundamental frequency. In this example the chopper calibration frequency is 100kHz so the triangle fundamental frequency is also 100kHz. Figure 2-4 also shows the synchronous notch filter frequency response. This filter is implemented with a switched capacitor circuit that synchronously integrates the chopped offset signal. Since the filter is synchronized to the chopping frequency, the filter has deep attenuation notches at all the harmonics of the triangle wave. Typical attenuation of the triangular offset ripple is on the order of 500 ×.

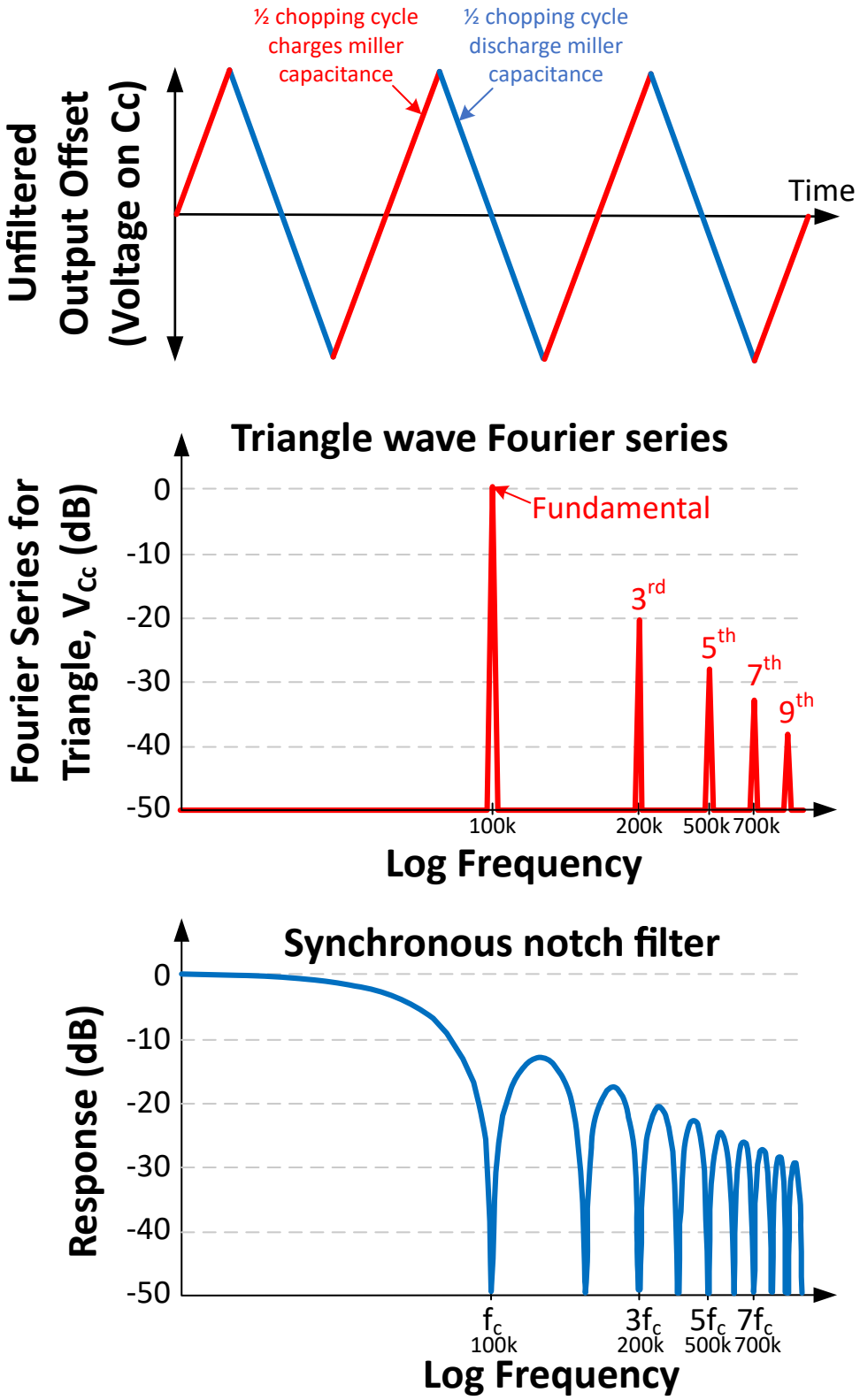

Figure 2-4. Offset Ripple and Synchronous Notch Filter

Figure 2-5 shows a more comprehensive chopper block diagram that includes the synchronous notch filter and a high-frequency path. The DC precision is determined by the transconductance input stage. At low frequencies, the high-frequency path has a much lower gain than the DC precision path, so the precision path controls the output. At higher frequencies, the gain of the high-frequency path dominates allowing for proper rolloff and phase margin.

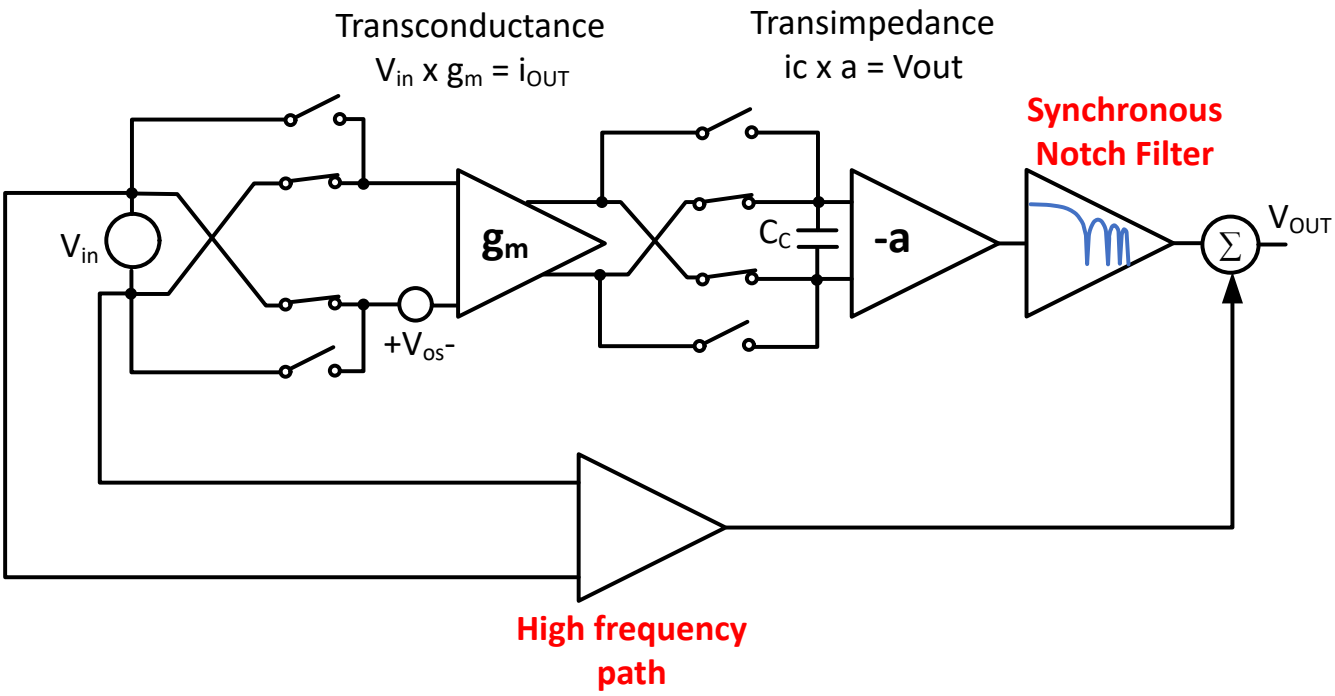

Figure 2-5. Detailed Chopper Block Diagram

3 Chopping Input Current Transients

The input switches on chopper amplifiers are MOSFET transistors. Depending on the op-amp design either an N-channel metal-oxide semiconductor (NMOS) or a complementary metal-oxide semiconductor (CMOS) transistor switch is used. This section provides a short theoretical background of NMOS transistor operation, before covering the concept of charge injection and clock feedthrough. Charge injection and clock feedthrough are the phenomena that generate the transient current pulse at the switch input.

To turn on an NMOS switch, the gate-to-source is driven to a voltage greater than the threshold voltage. Driving the gate-to-source positively places the transistor into the linear region where the drain-to-source on-resistance is very low. To turn off the NMOS switch, the gate-to-source voltage is driven to zero to cut off the transistor so that the transistor effectively acts as an open. From a semiconductor physics perspective, driving the gate-to-source to a voltage less than the threshold voltage allows a depletion layer to form in the channel which means that the drain-to-source impedance is very high and only small leakage currents will flow (see Figure 3-1). Increasing the gate-to-source voltage above the threshold draws electrons from the drain and source into the channel creating a conductive inversion layer (see Figure 3-2).

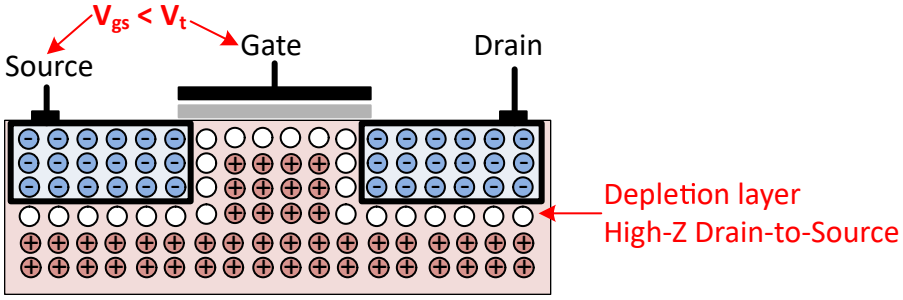

Figure 3-1. Charge Distribution on NMOS Transistor Cutoff Operation

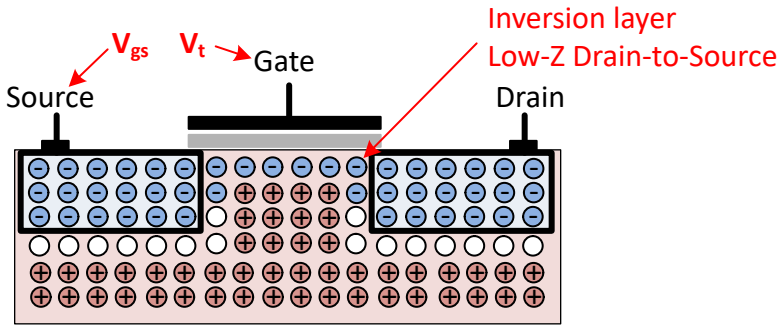

Figure 3-2. Charge Distribution on NMOS Transistor Linear Operation

Unfortunately, when the NMOS transistor is turned on and off, there are transient events called clock feedthrough and charge injection that generate a brief pulse of current at the input of the switch (transistor source). When the transistor turns on, the charge flows from the source and drains into the channel creating the inversion layer. When the transistor turns off, the charge in the inversion layer must return to the source and drain (see Figure 3-3). This transfer of charge, when the transistor turns on or off, is called charge injection. Clock feedthrough is the coupling of the clock signal through the parasitic gate-to-source capacitance. Both mechanisms generate a very brief but high amplitude current transient on the input of the NMOS switch.

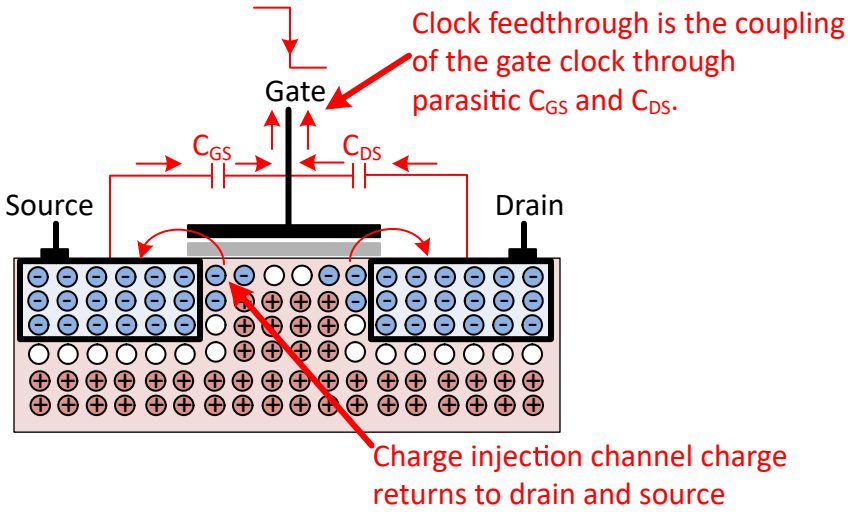

Figure 3-3. Charge Injection and Clock Feedthrough

Figure 3-4 shows the switched input of a chopper amplifier with NMOS transistor switches. Notice that the clocking signal for Q1 and Q2 is inverted on Q3 and Q4. Thus, when Q1 and Q2 are turned on, Q3 and Q4 are off and vise versa. Each time the clocking signal transitions, charge injection and clock feedthrough introduces a transient current at the inputs.

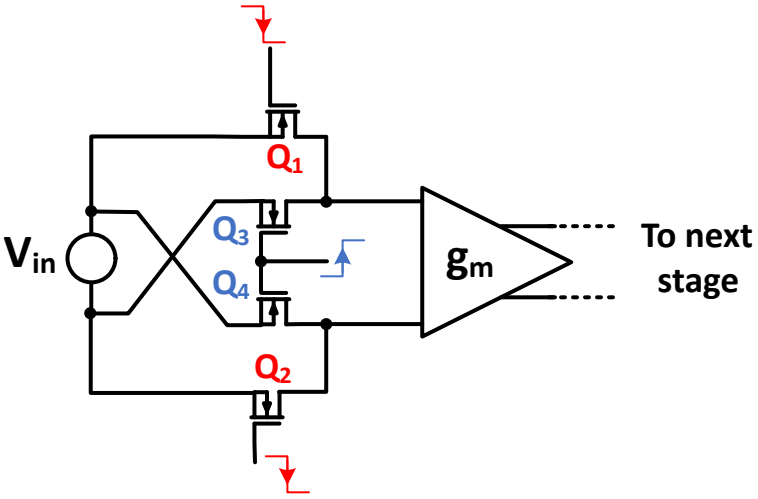

Figure 3-4. NMOS Switch Connection on Chopper Input Stage

Figure 3-5 shows the measured transient current on OPA188. The bias current is defined as the average current flowing into the inputs of the amplifier. In this example the bias current is typically 160pA and is very small relative to the transients. The measured transients are 2µA in this example which is 12,500 times the magnitude of the bias current. The two large transients correspond to transitioning of the calibration circuit input switches. The smaller transient between the large transients occurs when the synchronous notch filter is switched. The notch filter is designed to switch half-way through the calibration cycle. The period of the calibration cycle for this example is 1.54µs (f_{chop} = 650kHz). The measured noise density of this device shows noise tones at the chopping frequency and the harmonics. The notch filter switching time is between the main chopping transition points. Thus, there is also a noise tone in the middle between the clocks due to the small transient from the notch filter (see Figure 3-6). Since these transients are currents, the impact of the transients can be minimized by reducing the source and feedback impedance.

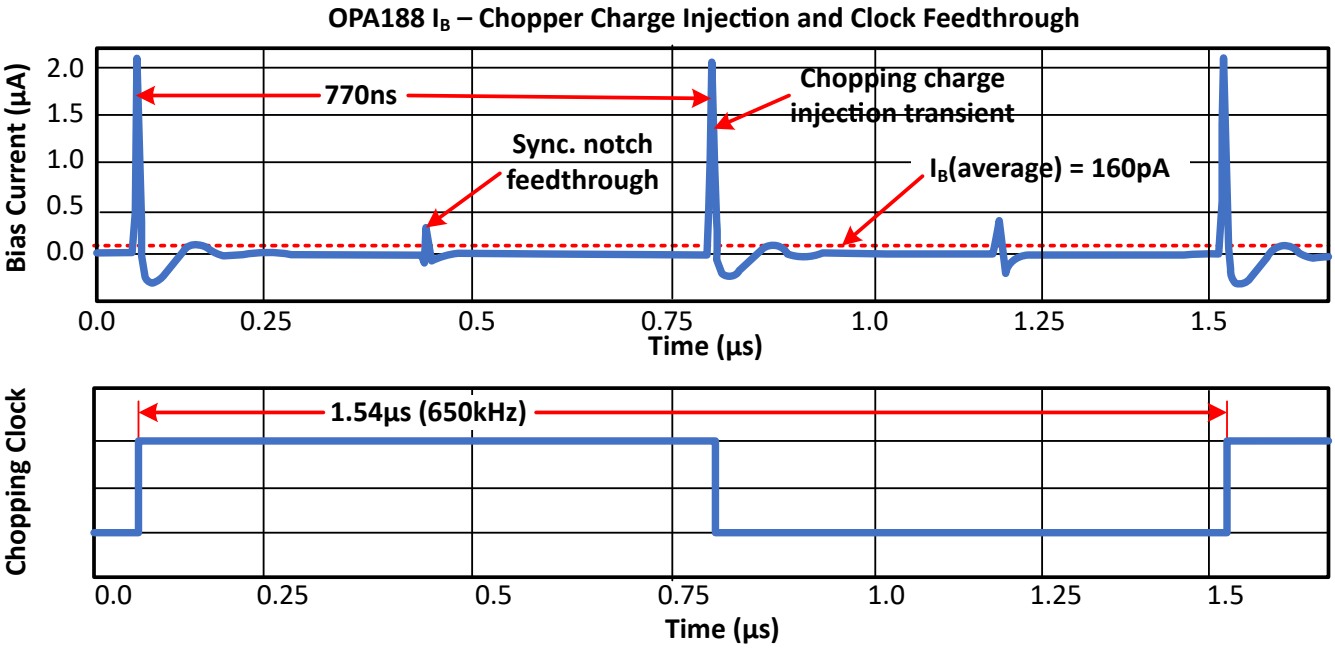

Figure 3-5. Chopper Input Current Transients for OPA188

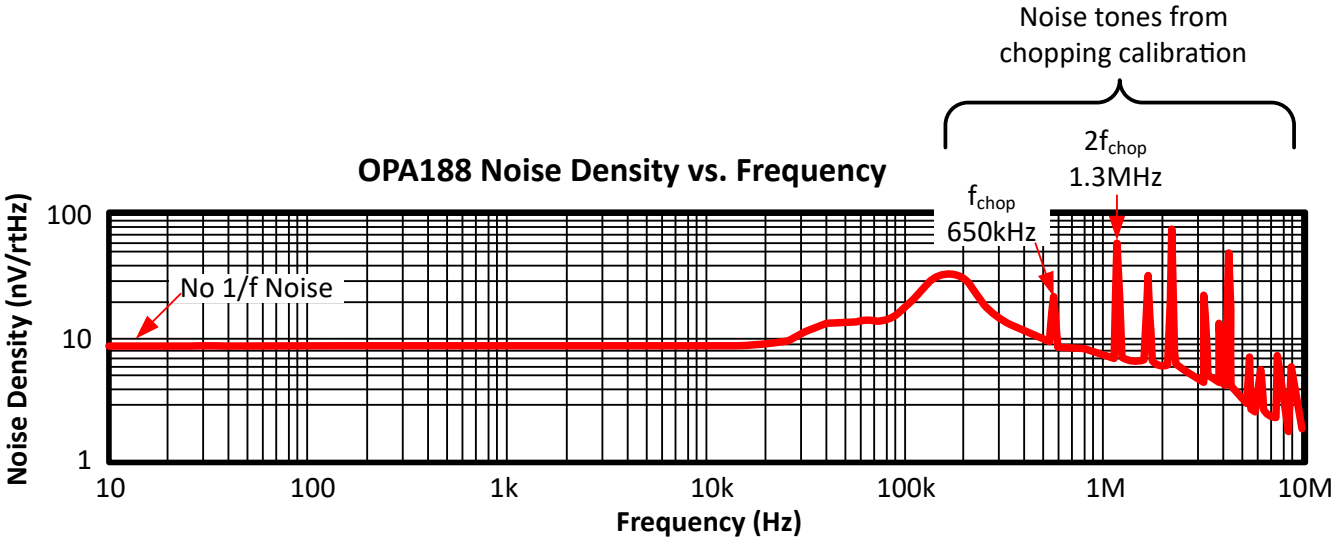

Figure 3-6. Chopper Noise and Calibration Feedthrough for OPA188 (Buffer Configuration)

4 Bias Current Translation Into Offset

The remainder of this document focuses on the translation of bias current and bias current transients into offset voltage in chopper amplifiers. This section reviews the general theory on how bias currents translate into offset voltages. This theory applies to both chopper and traditional amplifiers, and is pertinent background information for the discussions in the following sections.

Figure 4-1 shows the op amp model for bias current. Using the principle of superposition, you can determine the offset shift for each of the bias current sources separately, then combine the result. In superposition, only one source is considered at a time and the unused current sources are replaced with opens while the unused voltage sources are replaced with shorts. Figure 4-2 shows the superposition diagram for calculation of the output offset due to I_{BN}. Considering the amplifier to be ideal, there is a virtual short between the inverting and non-inverting input terminals. Since the non-inverting input is grounded, the inverting input is virtually grounded and the voltage across R_g is 0V. Thus, there is no current through R_g so all the bias current flows through R_f. The output offset is $-I_{BN}R_f$ (see Equation 1). This offset can be referred to the input by dividing by the op amp closed loop gain. Simplifying this equation yields Equation 2. Thus, the offset referred to the input from I_{BN} is the bias current multiplied by the parallel combination of R_f and R_g.

$$V_{IBN\_RTO} = -I_{BN}R_f \tag{1}$$

$$V_{IBN} = -I_{BN}R_f / \left(\frac{R_f}{R_g} + 1\right) = -I_{BN}\frac{R_f R_g}{R_g + R_f} = -I_{BN}\left(R_f \left|\right| R_g\right) \tag{2}$$

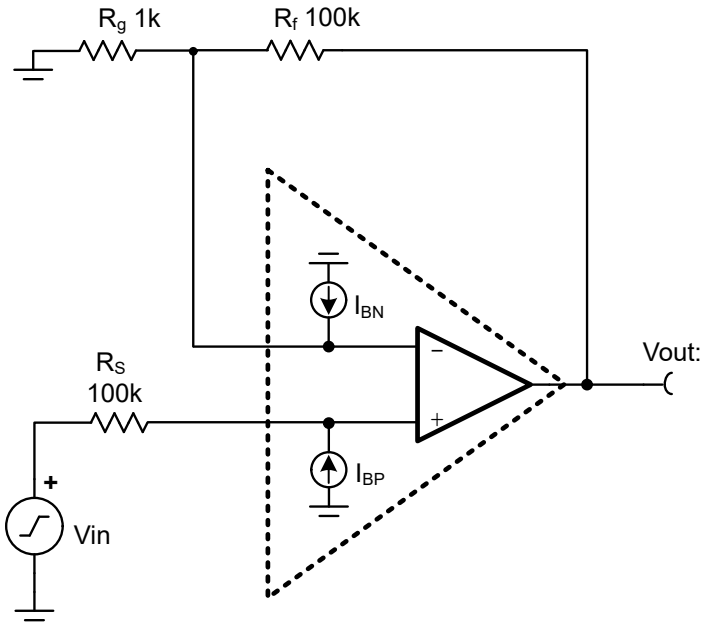

Figure 4-1. Op Amp Model for Bias Current

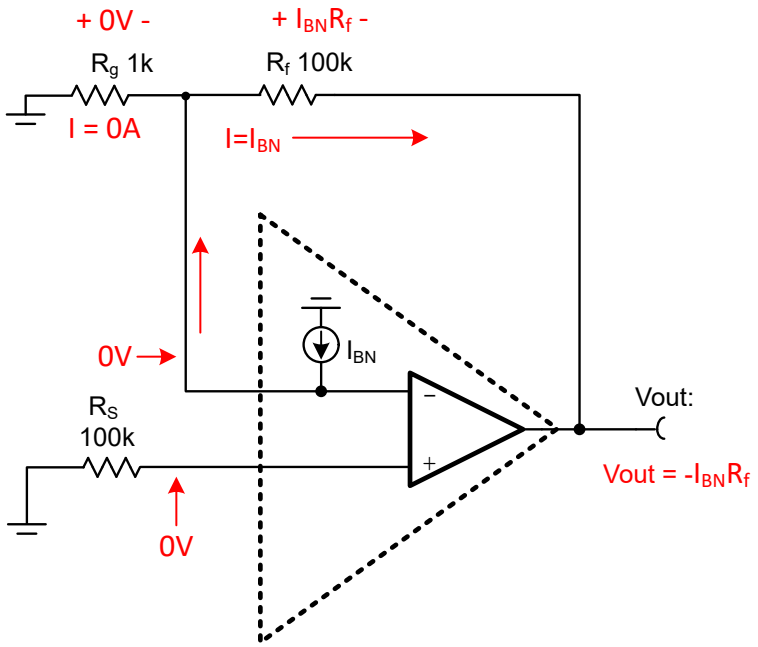

Figure 4-2. Offset due to I_{BN} for Superposition Calculation

Figure 4-3 shows the superposition diagram for calculation of the output offset due to I_{BP}. In this case the offset calculation is simply the bias current multiplied by the source impedance, $V_{IBP} = I_B R_S$. Note that when the bias current from both the inverting and non-inverting input flow in the same direction, the polarity of the offset generated by inverting and non-inverting inputs oppose each other. In cases where $I_{BN} = I_{BP}$ and both currents flow in the same direction, the feedback network impedance and source impedance can be balanced to cancel the bias current effects, $R_s = (R_f \parallel R_g)$. However, in general CMOS bias currents and chopper transients are not equal, so balancing the impedances may not improve the bias current related offset voltage error much and can actually make the error worse. Section 6 covers this topic in more detail.

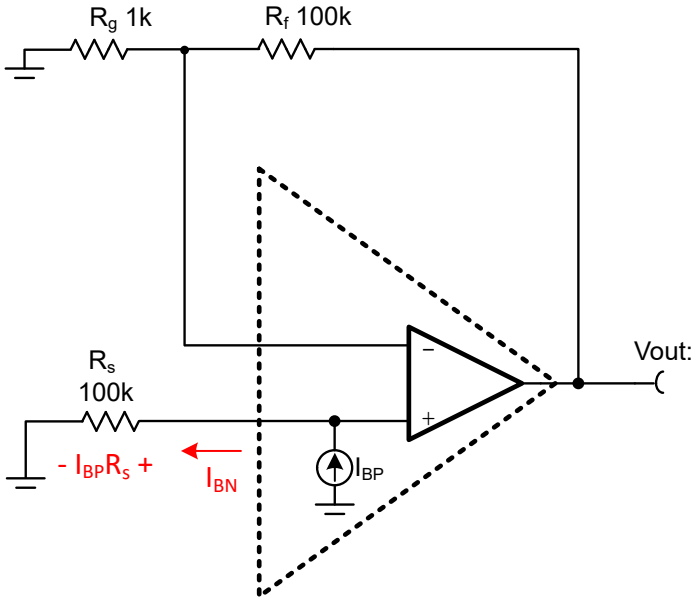

Figure 4-3. Offset due to I_{BP} for Superposition Calculation

5 Chopping Current Transient Impact on Offset Voltage

Figure 3-5 illustrates the amplifier transient input current due to the charge injection and clock feedthrough of the chopper input metal–oxide–semiconductor (MOS) switches. When these input transient currents flow through the feedback network and source impedance connected to the amplifier, the transients convert into voltage. The transients are very fast compared to the bandwidth of the op amp, so the transients do not fully settle. The average of the AC voltage signal from the chopping transients has a non-zero value. This average value acts as an additional input offset voltage that adds to the offset of the amplifier. Depending on the magnitude of the source and feedback impedance, the offset due to the chopping transients can be either negligible or can be significant compared to the offset of the amplifier. The specific resistance value where the transients begin to be significant depends on the bandwidth of the amplifier, chopping frequency, and transient I_B glitch magnitude.

Figure 5-1 shows a simple TINA-TI model for OPA188 that includes the transient current pulses (I_{G1} and I_{G2}), bandwidth, and input capacitance. The current transient on the non-inverting input flows through the source impedance, and the transient on the inverting input flows through the impedance network. If these two transients are identical, and the feedback impedance matches the source impedance, then the transient input currents create offset voltages from the feedback and source impedance that cancel each other.

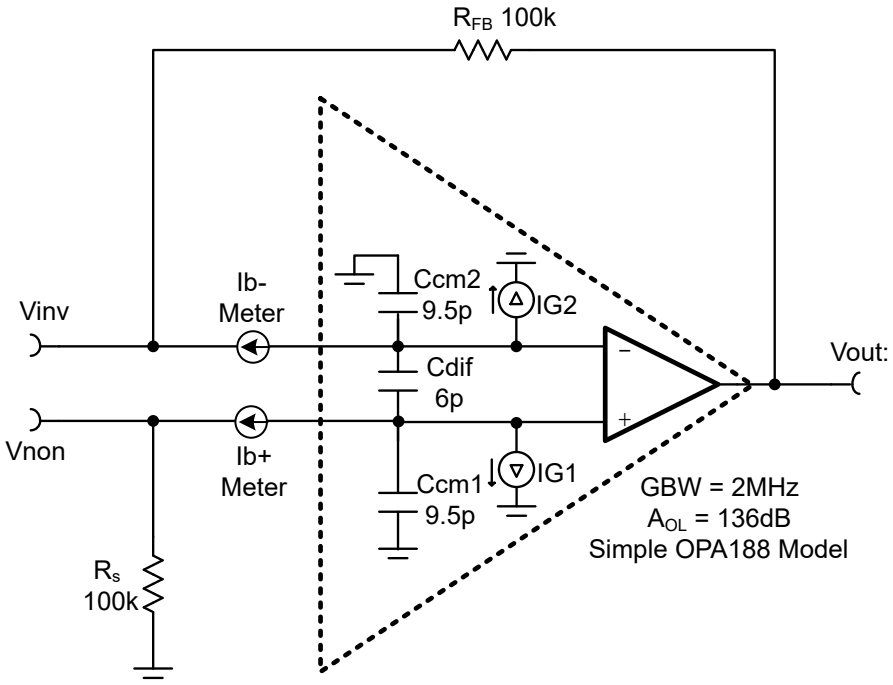

Figure 5-1. TINA-TI model for Chopper Transients on OPA188

Figure 5-2 shows the response for the circuit shown in Figure 5-1. Since there is a slight mismatch in the current transients, the transients do not fully cancel and the output shows an offset error signal that varies with time. The DC average of the output offset signal is 25.8µV. Figure 5-3 shows the response for the same circuit with the feedback resistor shorted. Since R_{FB} is shorted, there is no canceling effect between the inverting and non-inverting signal. Thus, the average output offset increases to 204µV. Figure 5-4 shows the response for the same circuit with the source resistor shorted. Again, there is no canceling effect between R_{FB} and R_s since R_s is shorted (average offset is –187µV).

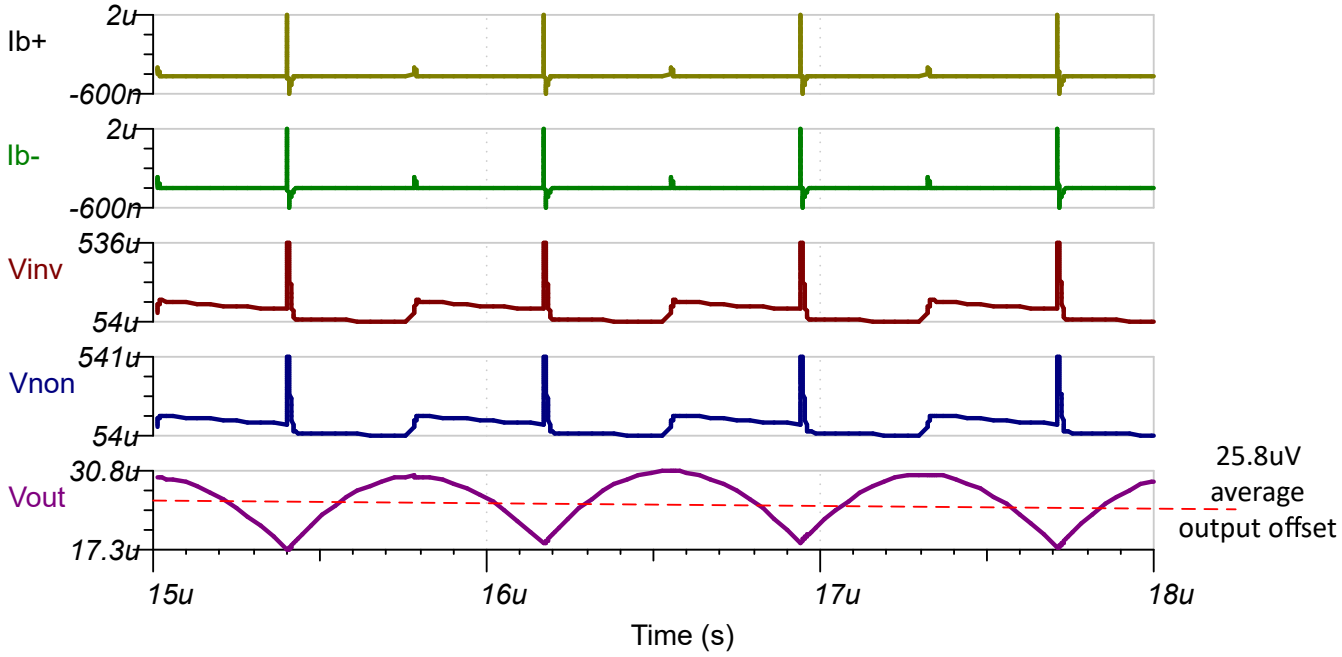

Figure 5-2. Simulated Output Offset for OPA188 Model (R_{FB} = R_s = 100kΩ)

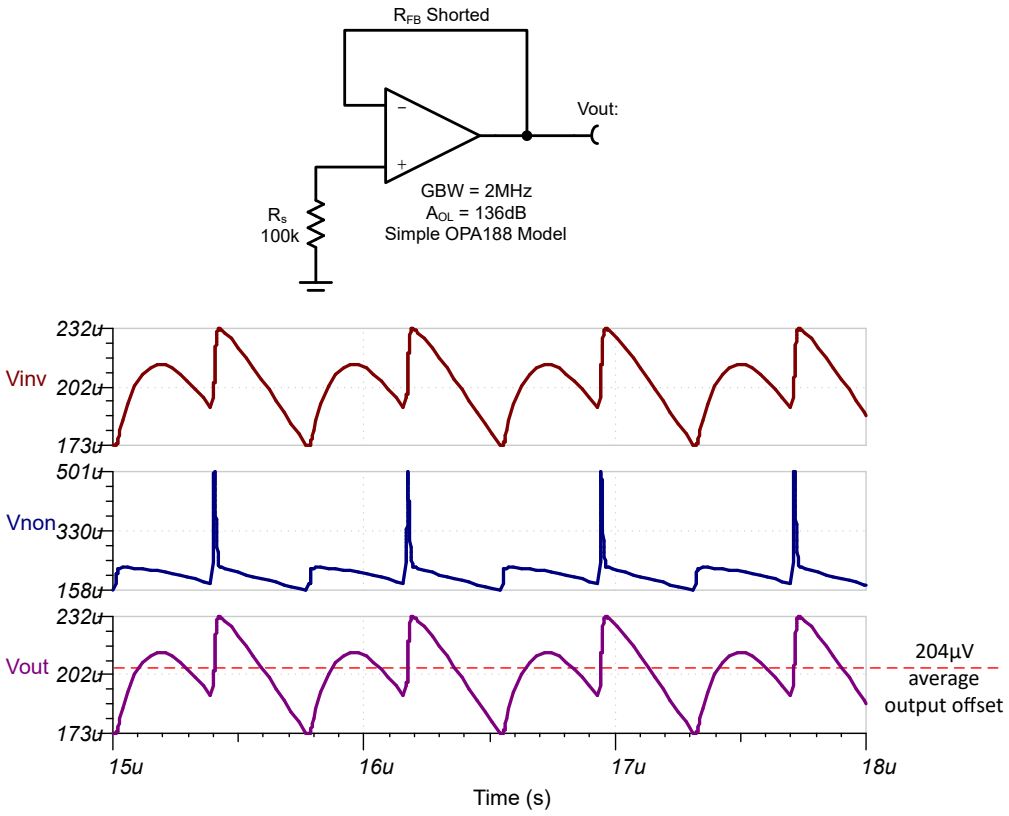

Figure 5-3. Simulated Output Offset for OPA188 Model (R_{FB} = 0Ω, R_s = 100kΩ)

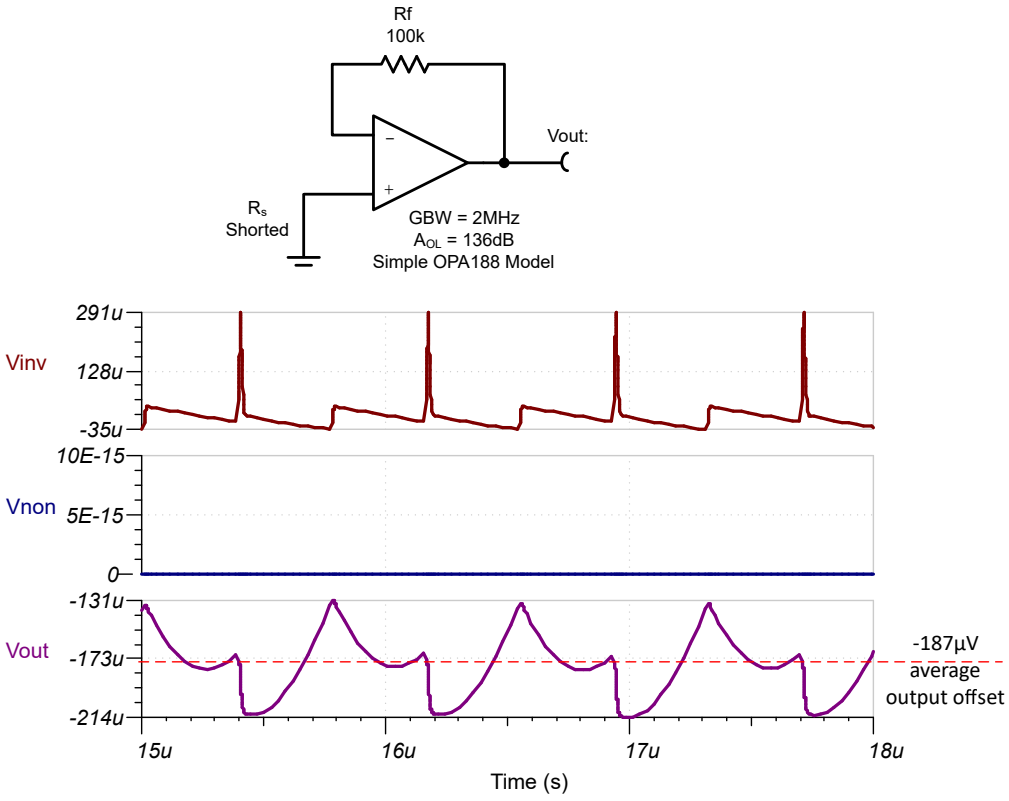

Figure 5-4. Simulated Output Offset for OPA188 Model (R_{FB} = 100kΩ, R_s = 0Ω)

It is undesirable for the bias current transients of a chopper amplifier to produce offsets that are larger than the V_{os} of the device. The offset voltage generated by these current transients is dependent on the magnitude of the source impedance and the impedance of the feedback network. Figure 5-5 shows a graph of OPA388 offset voltage versus source impedance. The flat region on the left-hand side of the graph is where the inherent offset of the amplifier is dominant. The region where the curve increases with source impedance is where the current transients dominate the offset. In general, do not use the chopper amplifier with the larger source impedances where the transients dominate. The transition point where the source impedance is considered large is different for each chopper amplifier. Table 5-1 provides a list of chopper amplifiers and the associated maximum impedance to avoid the increase in offset voltage.

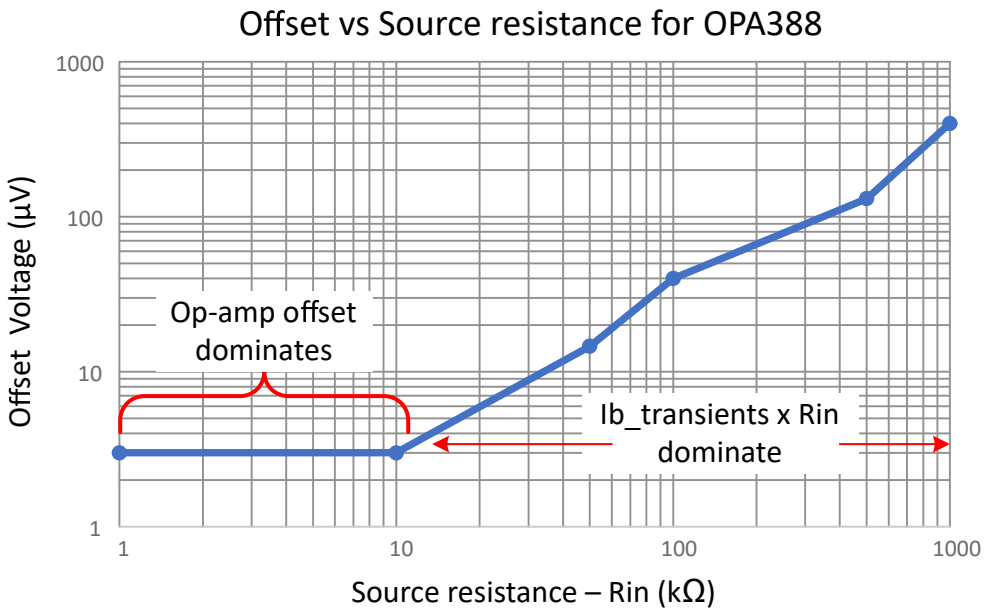

Figure 5-5. Offset vs Source Resistance for OPA388

Table 5-1. Maximum Recommended R_s and Feedback Resistance (R_f || R_g)

Op Amp Model	Maximum Recommended R_s and R_f||R_g (kΩ)
OPA189	1
OPA388	10
OPA333	1000
OPA187	500
OPA188	10
OPA186	500
OPA182	10
OPA387	10

6 Input Bias Current versus Bias Transients

Up to this point, this article focused on bias current transients due to charge injection and clock feedthrough in the input MOSFET switches. Beyond this effect, there is a DC bias current on all CMOS amplifiers due to the leakage of ESD diodes. This ESD leakage varies somewhat for different op-amp models, but typically the leakage is in the low picoamps range at room temperature. The bias current specified for chopper amplifiers is the average of the transient current from chopper-switch charge injection combined with the ESD diode leakage. Compared to the magnitude of the current transients these bias currents are generally negligible at room temperature, but can become significant at higher temperatures. For example, for OPA186 the typical bias current increases from ±5pA at 25°C, to ±900pA at 125°C (see Figure 6-1). This increase in bias current is mainly due to the change in ESD diode leakage because the MOSFET switch charge injection remains relatively constant over temperature.

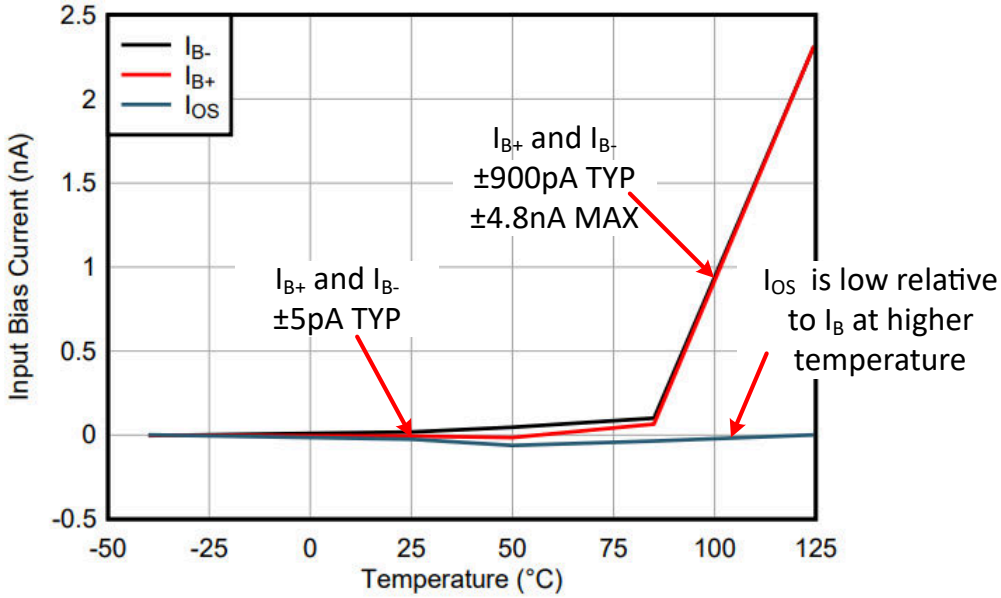

Figure 6-1. Bias Current vs Temperature for OPA186

Therefore, in addition to using Table 5-1 to select a source impedance that does not generate significant offset due to the bias transients, it is important to make sure that increasing bias current over temperature does not translate into significant input offset voltage. Equation 3 can be used to calculate I_B over temperature given the maximum value at 125°C from the data sheet table. This equation is based on the principle that the ESD diode leakage increases roughly double for every 10°C increase in temperature. Equation 4 uses the bias current at temperature and the offset voltage to determine the maximum resistance to be used due to bias current. Example 1 applies the equations to the OPA186 at 100°C. Based on this example, the OPA186 can be used up to 100°C with 11.7kΩ source impedance or feedback impedance with minimal impact on offset. Note that Table 5-1 recommends using resistances less than 500kΩ. This recommendation is correct for room temperature, but at 100°C lower impedances are required because bias current increases at high temperature. Thus, for higher temperature applications, it is necessary to look at both Table 5-1 and also the data sheet bias current specification over temperature to determine the maximum source and feedback impedances.

$$I_{B(T)} = \frac{I_{B(125℃)}}{2^{\left(\frac{125℃ - T}{10}\right)}} \quad (3)$$

where

$I_{B(T)}$ – I_B and any temperature greater than 25°C

$I_{B(125C)}$ – maximum I_B specified at 125°C

T – Temperature in degrees °C

$$R_{MAX} = \frac{V_{osMax}}{I_{B(T)}} \quad (4)$$

where

R_{MAX} – the maximum recommended resistance that avoids translation of bias current into offset

$I_{B(T)}$ – I_B calculation from Equation 3

V_{osMax} – Maximum input offset specified in op amp data sheet

Example 1: OPA186 at 100°C

$$I_{B(T)} = \frac{I_{B(125℃)}}{2^{\left(\frac{125℃ - T}{10}\right)}} = \frac{4.8nA}{2^{\left(\frac{125℃ - 100℃}{10}\right)}} = 0.849nA \quad (5)$$

$$R_{MAX} = \frac{V_{osMax}}{I_{B(T)}} = \frac{10\mu V}{0.849nA} = 11.7k\Omega \quad (6)$$

Bias current cancellation is a method where the input impedance and feedback network impedance are balanced to make the inverting and noninverting bias current offset equal so that they cancel. However, this method only works when the bias currents are approximately equal. The bias current offset (I_{BOS}) specification is a measurement of how close the bias current are to each other ($I_{BOS} = I_{BP} – I_{BN}$). For bias current cancellation to be effective the bias current offset must be much less than bias current ($I_{BOS} << I_B$). Bias current cancellation can help to minimize the effect of bias current transients if the transient amplitude and wave shape is well balanced between the inverting and non-inverting inputs. Unfortunately, there is generally some imbalance in the bias current transient amplitude. Furthermore, parasitic capacitances and filter capacitances influence the bias current transients. To avoid translation of bias current transients into offset voltage, keeping the source and feedback resistance below the minimum specified in Table 5-1 is recommended, rather than relying upon bias current cancellation to minimize offset. Considering DC bias currents, balancing source and feedback impedance can be helpful at higher temperatures as bias current offset (I_{BOS}) is often significantly lower than bias current at high temperatures.

7 Amplifier Intrinsic Noise

The selection of the best chopper amplifier as well as the associated feedback network has a significant impact on the overall amplifier noise. This theory applies to both chopper and traditional amplifiers, and is pertinent background information for the discussions in the following sections. For full coverage of intrinsic noise see Amplifier Precision Labs.

Intrinsic noise refers to the noise generated by circuit components themselves. Amplifiers generate an intrinsic voltage and current noise that is specified in the data sheet. Using simulation or calculation it is possible to make accurate predictions on total RMS intrinsic noise for an amplifier. However, the resistors used in the feedback network and source impedance also generate an intrinsic noise. This noise can be calculated using the thermal noise equation.

$$e_n = \sqrt{4kTR} \tag{7}$$

where

e_n – the noise density generated by the resistor (nV/ $\sqrt{\text{Hz}}$)

k - Boltzmann's constant 1.38 × 10^{-23} J/K

R – Resistance in ohms

T – Absolute temperature in degrees Kelvin (K): $T_K = T_C + 273.15$

Two uncorrelated noise sources are added using the square-root sum of the squares as shown in Equation 8. When adding two noise sources, one noise source is considered to be insignificant compared to another when the larger noise source is at least three times the magnitude of the smaller source. For example, adding a 3nV/ $\sqrt{\text{Hz}}$ noise source with 1nV/ $\sqrt{\text{Hz}}$ gives a total noise of about 3.2nV/ $\sqrt{\text{Hz}}$, so the 1nV/ $\sqrt{\text{Hz}}$ source is insignificant ($\sqrt{\left(3.0nV/\sqrt{Hz}\right)^2 + \left(1.0nV/\sqrt{Hz}\right)^2} = 3.2nV/\sqrt{Hz}$).

$$e_{nTotal} = \sqrt{(e_{n1})^2 + (e_{n2})^2} \tag{8}$$

where

e_{nTotal} – the total noise from combining e_{n1} and e_{n2}

e_{n1}, e_{n2} – two random uncorrelated noise sources

The noise model for an amplifier circuit is shown in Figure 7-1. The amplifier has a voltage noise source and current noise sources. These are specified in the amplifier data sheet. The current noise source is normally very low in CMOS amplifiers (i_{bn} < 100fA/ $\sqrt{\text{Hz}}$) and can be neglected in most applications. Do not confuse the current noise source with current transients generated by the chopping calibration. Those transients do generate noise which is discussed in section Section 8. Aside from the amplifier noise sources each resistor has an associated noise source defined by Equation 7.

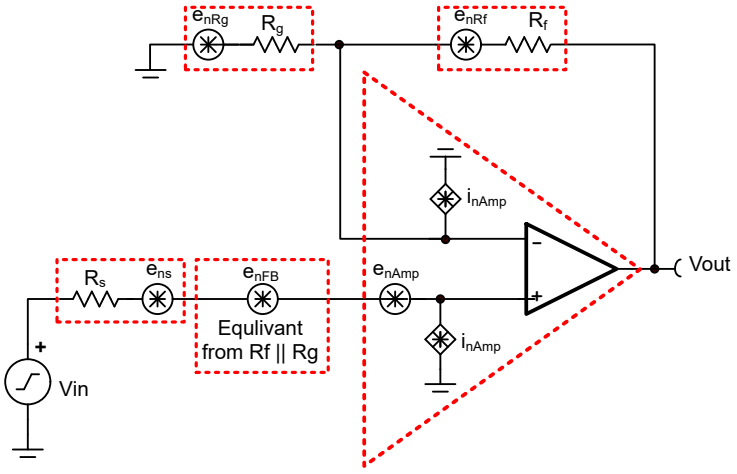

Figure 7-1. Amplifier Noise Model

For the equivalent circuit, notice that the amplifier voltage noise source is located at the non-inverting input. Any noise from the source impedance is also at the non-inverting input and adds as the square-root sum of the squares (Equation 8). Additionally, the noise from the feedback network can be reflected to the non-inverting input as the parallel combination of R_f and R_g.

From a noise perspective, a circuit is generally considered to be optimized when the total noise is approximately equal to the amplifier noise. The idea is that you do not want to choose an amplifier for the excellent noise characteristics and use large noisy resistors that dominate the total noise. Therefore, to optimize the overall noise, the resistor noise is set to one-third of the amplifier noise (see Equation 9). Table 7-1 summarizes the maximum noise optimized equivalent feedback resistances for common chopper amplifiers.

$$R_{eq} = \frac{\left(e_{nAmp}/3\right)^2}{4kT} \tag{9}$$

Table 7-1. Choosing the Best Zero-Drift Amplifier for the Application

Device	Noise (nV/ $\sqrt{\text{Hz}}$)	GBW (MHz)	Noise Optimized $R_f \| \| R_g$ (kΩ)	Noise for Optimized $R_f \| \| R_g$ (nV/ $\sqrt{\text{Hz}}$)
OPA189	5.2	14	0.183	5.5
OPA388	7	10	0.331	7.4
OPA333	55	0.35	20.4	58.0
OPA187	20	0.55	1.51	21.1
OPA188	8.8	2	0.523	9.3
OPA186	40	0.75	10.8	42.2
OPA182	5.7	5	0.219	6.0
OPA387	8.5	5.7	0.488	9.0

The main trade-off involved in choosing a feedback network that can achieve the optimal thermal noise is the amplifier output current required to drive the feedback network. For example, the OPA388 has a voltage noise density of 7nV/ $\sqrt{\text{Hz}}$. The optimal noise feedback network for this case is 331Ω. Remember that this equivalent impedance is the parallel combination of R_f and R_g. When using this optimal feedback impedance, the load seen by the amplifier depends on the amplifier gain. Figure 7-2 shows the examples for a gain of 2V/V and a gain of 11V/V. Clearly, increasing the gain allows for a larger value of R_f and decrease of the overall amplifier loading.

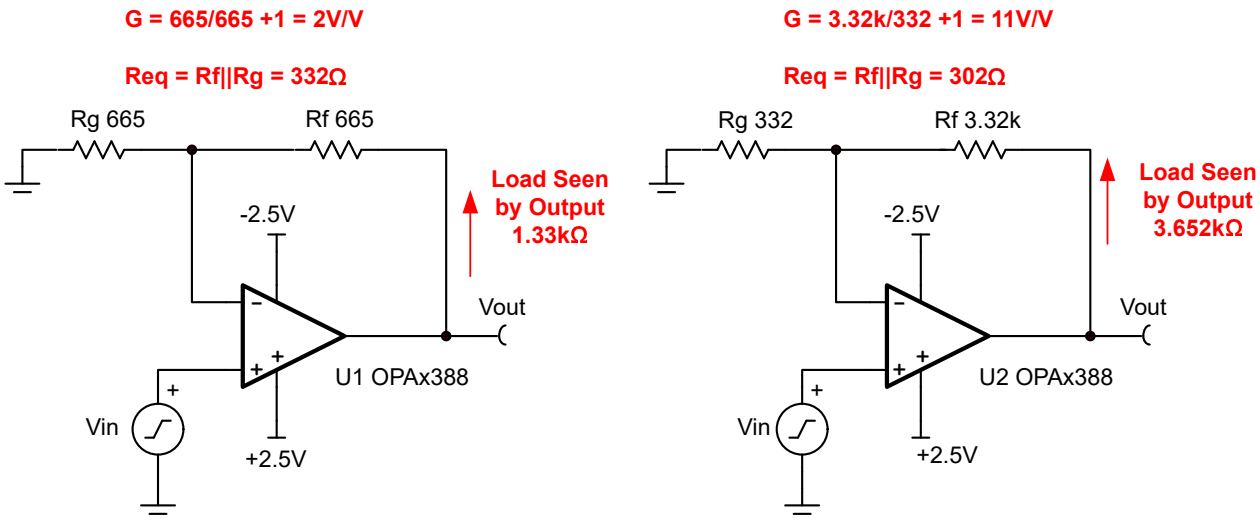

Figure 7-2. Noise Equivalent Resistance and Load vs Gain

The source impedance is frequently determined by the system requirements. For example, the source can be a sensor with a particular source impedance and the system designer does not have the flexibility to adjust the value. In this case, to minimize the overall system noise the source impedance is supposed to dominate the total noise and thus the amplifier noise is, in the best circumstance, one-third of the source impedance noise. However, in some cases it is not practical to find an amplifier with noise low enough for the source impedance noise to dominate. Figure 7-3 illustrates source resistance noise and recommended amplifier noise versus resistance.

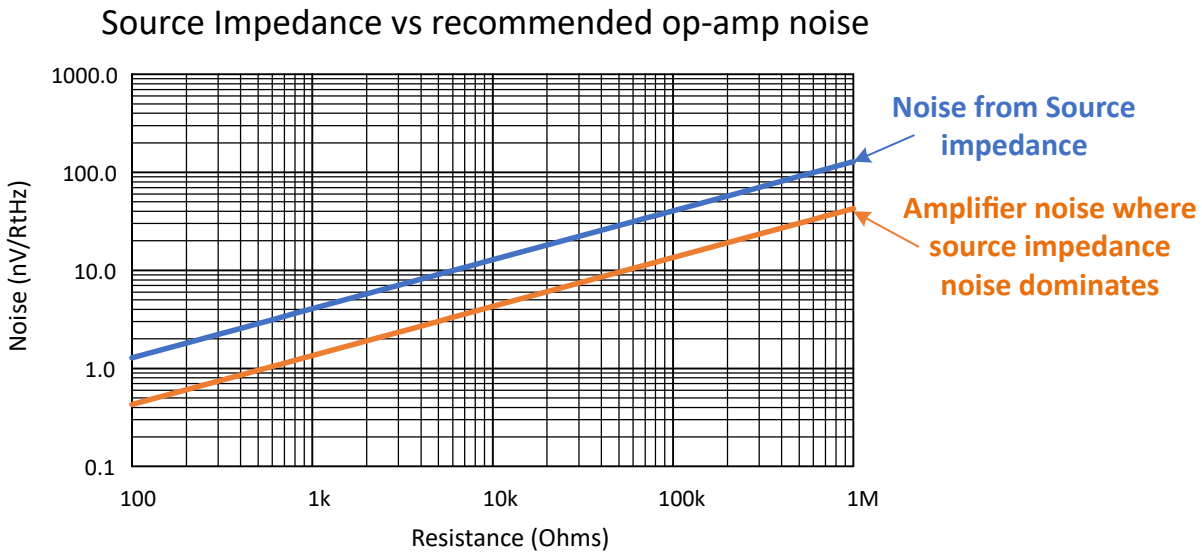

Figure 7-3. Choosing an Op Amp Where Source Impedance Noise Dominates

8 Chopper Transient Noise

This section covers noise generated by the chopper input switching. Chopper switching noise is at the chopping calibration frequencies and multiples of this frequency. This noise results from the translation of transient current pulses into voltage through the source impedance and feedback network impedance. Thus, larger impedances increase the amplitude of this noise. The chopping noise shows up in the frequency domain as tones at specific frequencies, and in the time domain as regular transients (see Figure 8-1, and Figure 8-2 respectively).

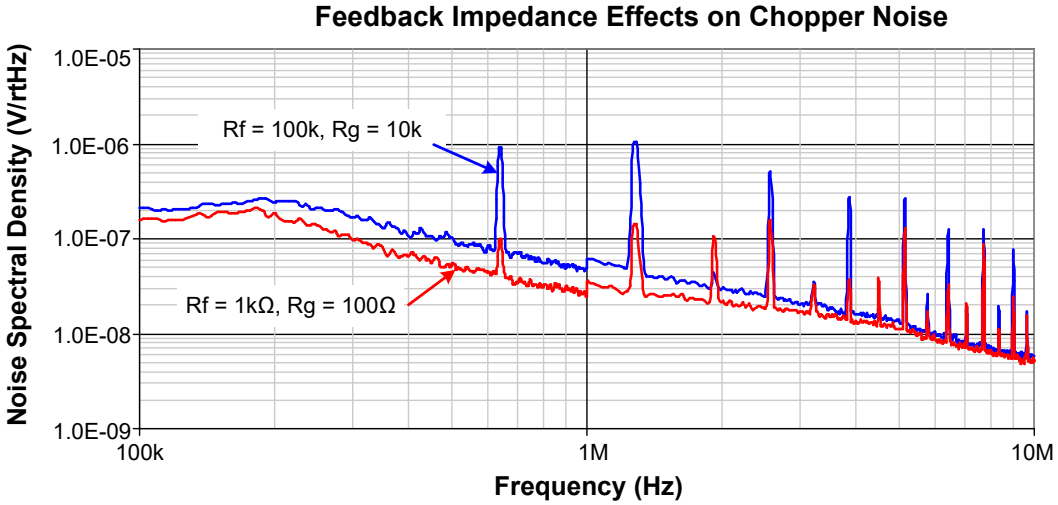

Figure 8-1. Frequency Domain Noise vs Feedback Impedance for OPA188

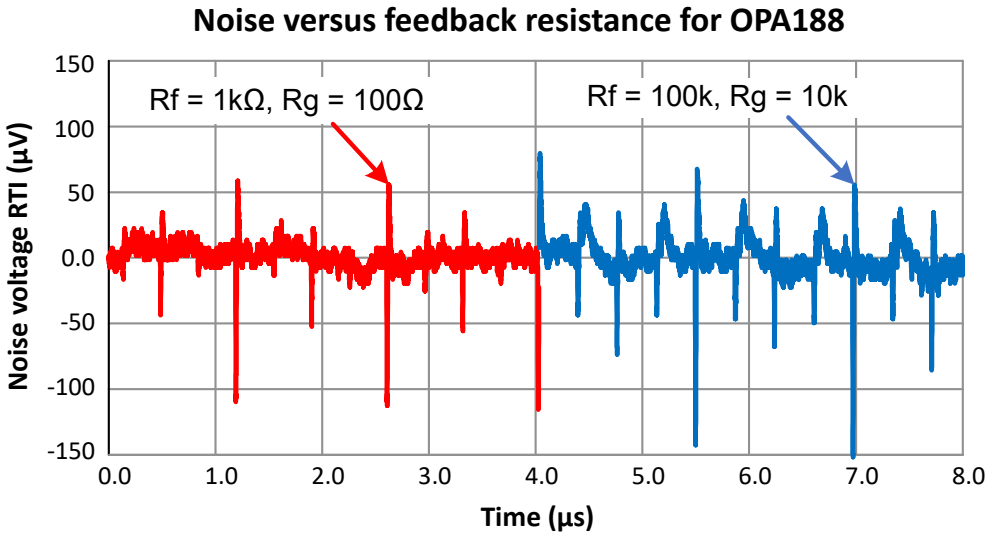

Figure 8-2. Noise vs Feedback Resistance for OPA188

The amplitude of the transient signals at the amplifiers output is relatively independent from closed loop gain. This is because the transient noise signal at the output is the bias current transient multiplied by the feedback resistor (V_O(chop noise) = I_{B_TRANS} x R_f). Conversely, the broadband noise at the output increases with gain, so the transient noise decreases relative to the broadband noise floor. Figure 8-3 shows the output noise density for OPA188 in different gain configurations. Notice how the broadband noise increases with gain but the transient noise tones are relatively constant for each gain case.

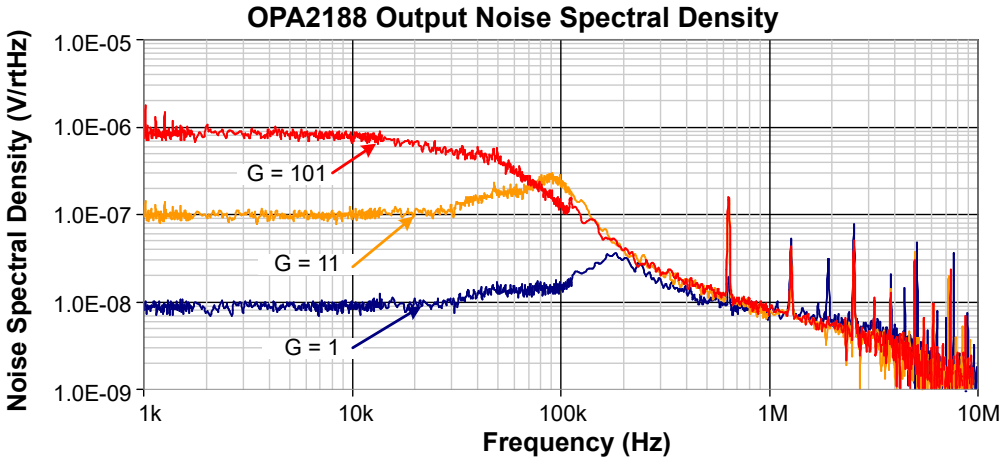

Figure 8-3. Frequency Domain Noise vs Gain for OPA188

Noise and other error sources are normally referred to the input (RTI). Since the noise transients at the amplifier output are relatively independent of gain, the amplifier intrinsic noise referred to the input decreases by the gain factor (V_{nRTI} = V_{nRTO}/G). Figure 8-4 shows the measured noise for gain of 101V/V and 11V/V RTI. The important point is that relative to other error sources, the chopping noise error becomes less significant at higher gains.

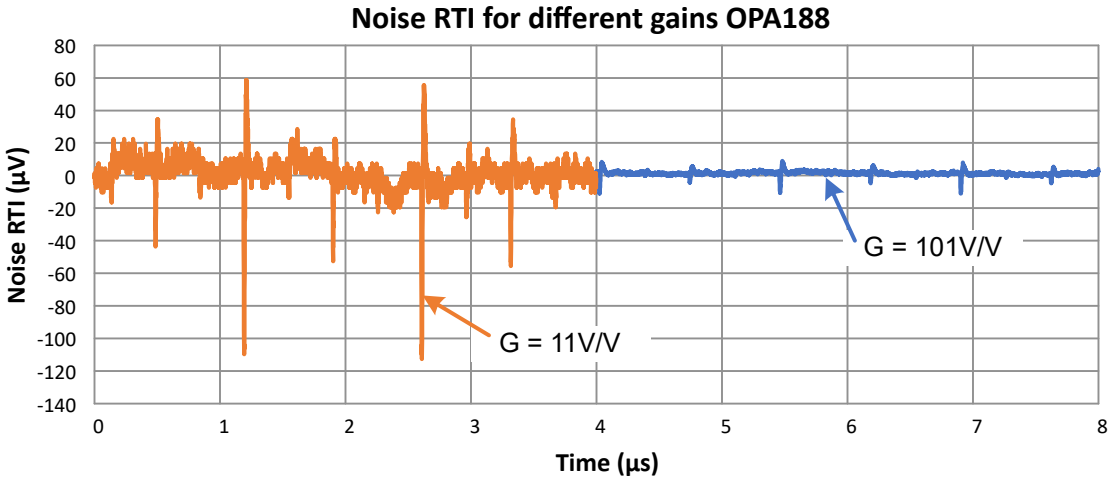

Figure 8-4. Noise Referred to the Input vs Gain

The chopping transients can be minimized by using a simple RC filter on the amplifier output (see Figure 8-5). Although noise tones start at 650kHz for OPA188, much of the transient content is in the higher frequency harmonics. Thus, it is not necessary to use a very low frequency filter to minimize the transient noise signal. Figure 8-6 shows the noise without an external filter and with filters at 3.2MHz and 7.2MHz for the OPA188 in a gain of 101V/V. The 3.2MHz filter reduces the transient to be practically negligible compared to the broadband noise. Set the filter cutoff to less than 650kHz to minimize all of the transient harmonic content. In this example, the OPA188 closed loop bandwidth is 19.8kHz (BW = GBW/G = 2MHz/101 = 19.8kHz). Thus, adding an external RC filter with a cutoff less than the 650kHz chopping frequency does not impact the AC performance of the amplifier.

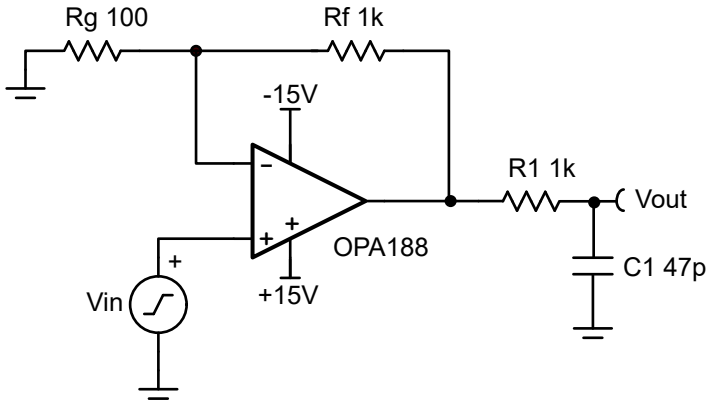

Figure 8-5. Simple Output Filter to Minimize Chopper Noise

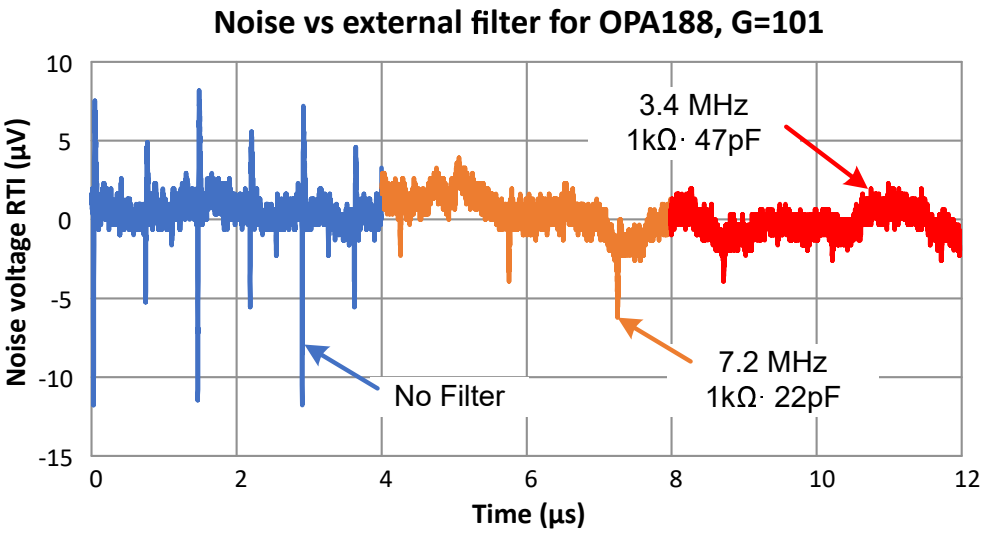

Figure 8-6. Noise vs External Filter for OPA188

9 Procedure for Selecting a Zero-Drift Amplifier

Use the following steps to select a zero-drift amplifier:

1. Does your application benefit from an amplifier with low input offset voltage, very low offset drift, or low flicker noise? If these parameters are not important in your application,look at traditional amplifiers as opposed to zero-drift amplifiers. Review columns B through E of Table 9-1 to find zero drift amplifiers that meet your requirements.
2. Compare your source impedance to column F in Table 9-1. Only use amplifiers less than or equal to this maximum source impedance (see Section 5 for details).
3. To optimize noise, the feedback network and source impedance needs to be less than column G in Table 9-1 (see Section 7 for details).
4. Check to make sure that the DC bias current does not translate into significant offset. This is most important in higher temperature applications, because the DC bias current increases over temperature. See Section 6.
5. Some applications can benefit from balancing the source impedance with the feedback impedance. This is generally useful for higher temperature applications as I_{BOS} at higher temperature can be significantly less than I_B. Nevertheless, this approach typically does not help for the chopping bias current transients, because these transients are generally not well balanced. For I_B cancellation, the feedback network parallel impedance is set equal to the source impedance ($R_s = R_f \parallel R_g$). See Section 6.
6. Consider the chopper noise. If your circuit is in gain, the closed-loop bandwidth generally is significantly less than the chopping frequency. Thus, the broadband noise will be gained up relative to the chopping transients. Adding an external filter can also be used to minimize the chopping noise. Chopping noise is of the greatest concern when the amplifier is in unity gain, with no external filter. Also, large source or feedback impedances increase the amplitude of the chopping noise (see Section 7 for details).
7. Finally, assuming all other criteria are acceptable, check all other amplifier specifications. For example, is bandwidth, slew rate, and output drive meeting your application specific requirements.

Table 9-1. Zero-Drift Selection Table

A	B	C	D	E	F	G
Device	Offset (µV)	Drift (µV/°C)	GBW (MHz)	N (nV/√Hz)	MAX Recommended R_{IN} and $R_f \parallel R_g$ (kΩ)	Noise Optimized $R_f \parallel R_g$ (kΩ)
OPA189	3	0.02	14	5.2	1	0.183
OPA388	5	0.05	10	7	10	0.331
OPA333	10	0.05	0.35	55	1000	20.4
OPA187	10	0.015	0.55	15	500	15.2
OPA188	25	0.085	2	8.8	10	0.523
OPA186	10	0.04	0.75	40	500	10.8
OPA182	4	0.012	5	5.7	10	0.219
OPA387	2	0.012	5.7	8.5	10	0.488

10 Summary

Zero-drift amplifiers have many benefits when compared to traditional precision amplifiers. Most notably, the offset and offset drift of zero-drift amplifiers are usually substantially better than similar traditional amplifiers. However, there are some error sources related to the internal switching of the chopper calibration circuit. In many cases the chopper errors are not significant. Section 9 lists a procedure that provides guidance in the selection of the zero-drift amplifier and the associated discrete components to minimize these errors.

11 References

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