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# Ultra-low-power pioneers: TI slashes total MCU power by 50 percent with new “Wolverine” MCU platform

## Introduction

Texas Instruments (TI) invented the microcontroller (MCU) in the 1970s\* and has leveraged this technology into numerous platforms, including the ultra-low-power MSP430™ MCU portfolio. The MSP430 MCU has been the industry’s ultra-low-power leader for more than a decade and each new generation of the architecture has been focused on setting new records for power consumption and efficiency.

The MSP430 architecture already provides intelligent peripherals that wake only when needed, flexible clocking that allows modules within the MCU to operate at different frequencies and advanced power management technology, just to name a few of its innovations. Not content to rest on its industry leadership, TI has continued to make substantial investments in developing cutting edge ultra-low-power technology.

With the “Wolverine” MCU platform, code named for its aggressive power-saving technology, TI has created the next generation of the MSP430 architecture (see Figure 1). This new platform achieves new levels of ultra-low-power by cutting the power and energy consumption of MCUs by more than half.

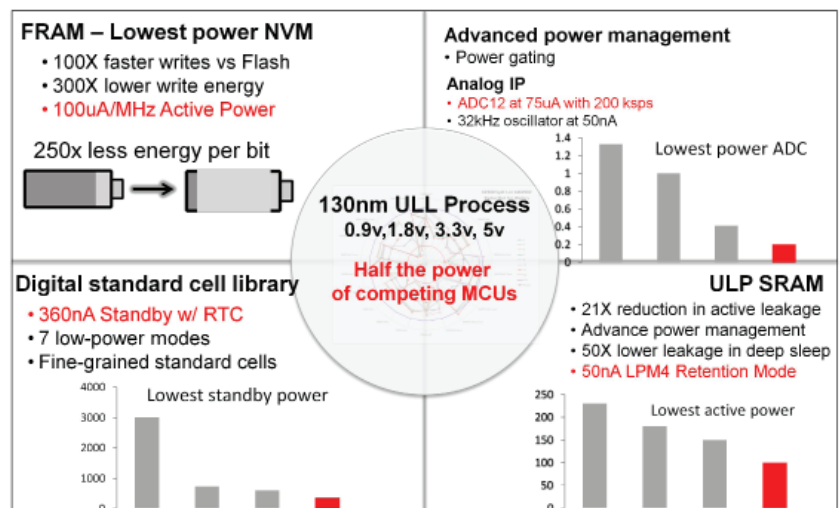


Figure 1. With the “Wolverine” MCU platform, codenamed for its aggressive power-saving technology, TI has created the next generation of the MSP430 architecture achieving new levels of ultra-low power by cutting the power and energy consumption of MCUs by more than half.

- Active power as low as 100 µA/MHz
- <400 nA standby with RTC and brown-out protection
- 250× less energy per bit with FRAM
- < 7 µs to wake to active from standby

TI achieves the “Wolverine” platform’s impressive power gains through its new 130-nm ultra-low-leakage (ULL) process technology, integrated low-power non-volatile memory and enhanced MSP430 DNA with advanced power management and precision low-power analog.

## 130-nm ultra-low-leakage (ULL) process technology

Given that ultra-low-power devices spend 99.9 percent of the time in standby mode, leakage current has become a key factor in determining power efficiency in smaller process geometries. The challenge for low-power design arises from the exponential increase in transistor leakage

\*According to Smithsonian Institution

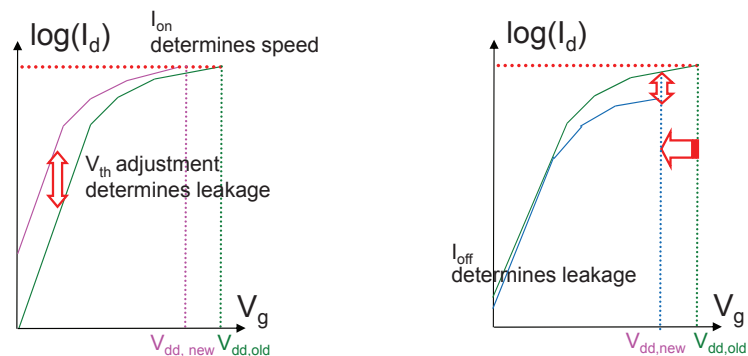
from ever-shrinking gate lengths and gate oxides. Leakage current is based on the distance electrons have to travel between nodes and as this distance continues to shrink, the easier it is for electrons to leak across. High-performance microprocessors (MPUs) for PCs that are based on a 25 or 45 nm, for example, must use special materials to manage leakage. For MCUs, leakage current becomes a significant consideration beginning with 180-nm CMOS process nodes.

TI is intimately familiar with leakage current at smaller process nodes through its GHz smartphone processors and digital signal processors (DSPs) designed at 65 nm, 45 nm and 28 nm, and its engineers took everything learned about leakage current at these smaller geometries and applied them to “Wolverine’s” 130-nm process.

Historically, MCU designers have targeted higher performance and greater density as the main focus of their innovation. Since 1965, Moore’s Law has driven transistor and chip performance. While this pace has slowed over the past decade, process technology has seen 2× improvement in performance every 18 months for more than 30 years.

For the 130-nm “Wolverine” platform, TI has reclaimed the gains of Moore’s Law in the dimension of power instead of performance through circuits designed for power efficiency optimized for lower leakage current and other characteristics inherent in silicon. Rather than improve performance by 2× as is the traditional approach, TI has instead achieved a 2× improvement in power consumption while maintaining the high performance of today’s MSP430 MCU architecture.

The result is at least 10× lower minimum leakage in individual transistors and an overall 15 percent reduction in active power compared to other 130-nm CMOS processes (Figure 2).



**Figure 2.** Using a low leakage approach instead of high performance, power losses can be kept low while capitalizing upon the active power benefits from technology scaling. The result is 10× lower leakage current and an overall 15 percent reduction in active power.

### Ultra-low-power foundation

To achieve the maximum benefit from the new 130-nm process technology, TI has completely redesigned its entire library of design tool kits to focus on power efficiency rather than high performance. These tool kits – including standard cell libraries, capacitors, analog components and I/O – are based on basic-level transistor configurations that form the underlying building blocks used to design today’s complex MCUs.

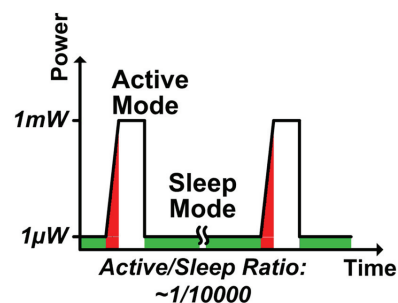
The new tool kits for 130-nm have a rich analog component list to enable peripherals like high-precision analog-to-digital converters (ADCs) and internal power management to dramatically lower power. For example, “Wolverine’s” module portfolio includes a high-precision 12-bit ADC that can sample 200,000 times per second while consuming only 75  $\mu$ A. Similarly, the real-time clock (RTC) module with calendar and alarm capabilities can run at only 100 nA. The 130-nm ultra-low-leakage process combined with rich mixed-signal integration makes for the lowest overall system power consumption in the industry.

### Advanced power management

Power efficiency does not apply solely to the power consumption of the CPU. Active current is also dependent upon how efficiently the system implements clocking, precision analog peripherals and communications interfaces. The use of advanced power management technology is essential to minimizing power consumption under various operating loads.

The “Wolverine” architecture offers an enhanced version of the MSP430 MCU power management module. In addition to supporting seven operating modes, the “Wolverine” power management module is capable of advanced power gating and uses a highly responsive adaptive regulator. Internally, the MCU is divided into multiple power domains to enable the system to dynamically manage each part of the device according to the specific demands of the application.

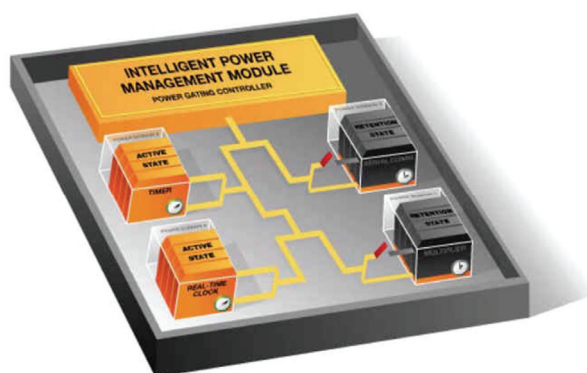
Total system power consumption is minimized when the amount of time a system spends in standby mode is maximized. However, there is a power cost each time the system switches between standby and active mode. Specifically, it takes time for the voltage supplied to circuitry to reach the expected level as well as to re-initialize the subsystem or peripheral to become operational again. During this time, the circuitry draws an increasing amount of power without performing any useful work (see Figure 3). These wake up losses result in decreased performance, reduced responsiveness and lower power efficiency, especially in systems that frequently switch between active and standby.



*Figure 3. When a system wakes, it draws power without performing any useful work. These wake losses result in decreased performance, reduced responsiveness and lower power efficiency, especially in systems that frequently switch between active and standby mode.*

“Wolverine” takes a different approach to reducing wake-up losses. Traditionally, the entire module or peripheral is shut down when it is not in use. “Wolverine” improves power efficiency by keeping more of the module or peripheral active in a “retention” mode using a power gating controller. In this mode, modules that are active and requesting a clock are kept fully powered. Modules that are idle and not in use, however, are powered at retention levels. This means that only the logic specific to retaining the state of the module is powered.

Power gating can result in significant power savings without sacrificing performance. Consider a timer in use in standby mode. While the timer actively requests a clock, the power-gating controller detects the request and maintains the timer in a fully functional state. However, once the timer function is complete, it is powered down to retention levels while maintaining the configuration state to minimize power consumption. When the timer is needed again, it’s available quickly, minimizing wake losses. Power gating is transparent to developers, enabling them to take advantage of industry-leading power efficiency without having to manually manage each module or peripheral (see Figure 4).

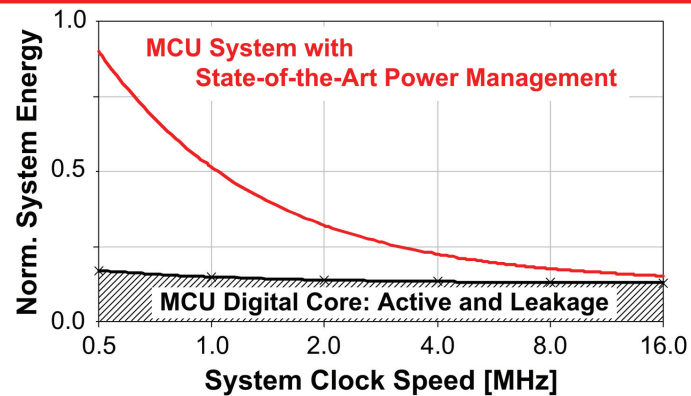


**Figure 4.** This is a simple visualization of the advanced power-gating capability in action. Portions of the device not in use are kept at “retention state,” allowing them to wake up much faster than in other architectures.

Another important capability required of an ultra-low-power MCU is the ability to respond quickly to changing application loads. Substantial power savings can be gained through technology that reduces the power to the main CPU when its full performance is not required. However, rather than require developers to manually adjust this power, the intelligent power management module in the “Wolverine” platform automatically adapts to changes in application load such as when a high frequency module is powered on (see Figure 5 on the following page).

## Operating speed is scaled depending on:

- Application requirements
- Maximum power available



## Low regulator overhead at low digital activity

Figure 5. “Wolverine’s” intelligent power management module automatically adapts to changes in application load for transparent scaling.

Specifically, the adaptive low dropout regulator (LDO) that powers the digital core of the MCU responds to changing power requirements by increasing its load as needed (see Figure 6). In effect, “Wolverine” automatically detects the current needs of the application and provides the clock and power as required.

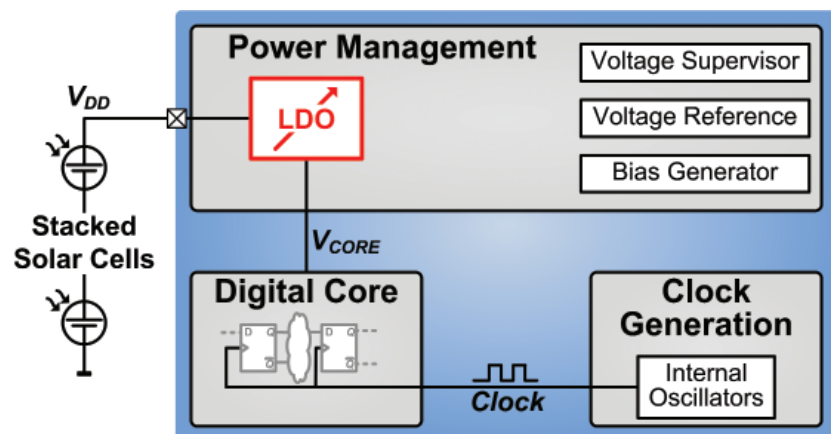


Figure 6. “Wolverine” automatically detects the current needs of the application, then dynamically adjusts the adaptive LDO to match the power and clocking needs of the application to maximize power efficiency.

With a high level of granularity, the LDO can match a wide range of diverse application loads. This approach also eliminates the need for external components such as buffer capacitors, used when switching from low- to high-load currents. As with power gating, this power-saving technology automates power management in a manner that is seamless and transparent to developers.

### **Ferroelectric random access memory (FRAM)**

MCU program code and key system parameters are typically stored in non-volatile memory, most commonly Flash or EEPROM. The slow write time of Flash, combined with its high power and low endurance, prevents its use for data storage. As a consequence, MCUs typically have at least two types of memory: Flash for code storage and SRAM for data.

To overcome the limitations of Flash, TI integrated a revolutionary non-volatile memory bit – Ferroelectric Random Access Memory (FRAM) – into the “Wolverine” architecture. TI has been investing in FRAM technology for 15 years and has produced standalone FRAM devices in partnership with Ramtron since 2007, in addition to its MSP430FR57xx devices with embedded FRAM available today.

FRAM is like DRAM except that data is stored in a crystal state, not by charge. As a consequence, it has read/write access and fast cycle times similar to DRAM.

It is also a random access memory where each bit can be read or written individually. In addition, FRAM features a simple, single-step write process. This means no separate erase is required before a write as is the case with Flash.

FRAM is highly efficient compared to Flash memory (see Table 1). To write to Flash requires 10–15 V and a charge pump, which adds a few milliseconds of charge time. Writing to Flash is also a multi-stage operation during which interrupts must be disabled. This factor complicates block writes to Flash since the system must break up such writes into smaller blocks between which interrupts can be enabled so that no critical signals or events are missed.

**Table 1. Comparison of non-volatile memory technologies**

	FRAM	SRAM	EEPROM	Flash
<b>Non-volatile</b> Retains data without power	Yes	No	Yes	Yes
<b>Write speeds</b> (13 KB)	10 ms	<10 ms	2 secs <sup>1</sup>	1 sec
<b>Average active power</b> ( $\mu$ A/MHz)	100	<60	50 mA+ <sup>1,2</sup>	260
<b>Write endurance</b>	100 trillion+	Unlimited	100,000	10,000
<b>Dynamic</b> Bit-wise programmable	Yes	Yes	No	No
<b>Unified memory</b> Flexible code and data partitioning	Yes	No	No	No

<sup>1</sup> – Standalone EEPROM Write

<sup>2</sup> – Total power consumption

Data for FRAM, SRAM and Flash are representative of embedded memory performance within device

In contrast, FRAM requires only 1.5 V to write. Combined with write times 100× faster than Flash, FRAM active write energy is up to 250× lower. System reliability is also maintained without added programming complexity since interrupts can be active during FRAM operations.

The efficiency of FRAM compared to Flash can be illustrated by looking at how non-volatile memory is used in automotive infotainment applications. When the vehicle is turned off, a variety of system data needs to be collected and stored so it can be reinstated when the vehicle is turned back on. Among the data the system saves includes driver and passenger temperature settings, radio presets, GPS location and radio volume.

Because the vehicle doesn't know when its power is going to be turned off, a capacitor must be used and is charged while the vehicle is on. This capacitor powers the Flash and MCU during the time that the data is written. The more data that needs to be saved, the larger the capacitor required. In addition, the relatively slow write speed of the Flash impacts how much data can be saved.

FRAM, with its fast write speed and power efficiency, can access 900× more data than Flash using a comparable capacitor. This enables developers to create less complex systems using smaller – and less expensive – capacitors. This tremendous difference in write capabilities enables a whole new range of low-power applications, including those requiring real-time data logging and/or using energy harvesting technology. The ability to write faster also means the system can spend more time in sleep mode.

The use of FRAM, however, also impacts how systems are designed. Flash has limited endurance, on the order of 100K writes, before its reliability begins to degrade. As a consequence, system parameters are often only saved to Flash when the system is powered down. The effectively unlimited endurance of FRAM – on the order of  $10^{15}$  write cycles – enables developers to rethink how they store system parameters. Specifically, rather than store parameters in SRAM and save them to Flash upon power down, all data can be already stored in non-volatile FRAM, even when it frequently changes. This yields even further cost savings since parameters do not need to be actively saved and a capacitor is no longer required.

System wake-up is also improved. In the automotive application described above, settings do not need to be restored to the data memory upon power up since they are already available in the common FRAM memory space. This also increases the efficiency of highly power-constrained applications like those using energy harvesting. Since no power is required to store and restore data between sleep sessions, applications can operate with smaller energy-harvesting circuitry, thus reducing system complexity and cost. This is just one example of how FRAM enables developers to rethink their system architecture in ways that will increase operating life, reduce system cost and make more reliable products.

Another key capability of FRAM is its ability to stand as both program and data memory. In Flash-based systems, the ability to optimize a system based on code and data size is limited to how much Flash and SRAM an MCU has integrated on it.

FRAM, with its fast write access and effectively limitless endurance, enables it to serve as both program and data memory. The MSP430FR58xx series, the initial “Wolverine”-based devices, will offer 64 KBytes of memory and offer developers full flexibility in how they allocate this memory between code and data. This



also gives designers the ability to use smaller MCUs with different memory ratios than what has previously been available. In addition, TI has integrated a memory protection unit (MPU) to prevent data operations from accidentally overwriting system code as well as lockable code segments for additional memory protection.

“Wolverine”-based devices will also have a block of SRAM. This memory is available for applications that truly require the unlimited endurance of SRAM for certain operations. The SRAM block is also made available to help simplify porting of existing MSP430 MCU designs.

### ***Effective processing efficiency***

For ultra-low-power applications, cutting power consumption in half is actually much more desirable than doubling processor speed. By increasing how quickly the system can go to sleep and wake, developers can fit more processing into the same time and power profile, providing an effective increase in processing speed. This also gives developers more control over managing power in their designs. Rather than have to use a smartphone-class MCU for an embedded application, developers can leverage power-efficient “Wolverine”-based devices and scale to the exact level of performance they need.

“Wolverine” devices will be consistent with existing MSP430 MCU tools and software, enabling developers to leverage the extensive MSP430 MCU ecosystem. Built-in hardware in the silicon and tool chain will enable developers to track energy usage in real-time for accurate power profiling that eliminates guesswork when estimating system power consumption and effective operating life. TI will also provide optimization tools designed to analyze code to assure power efficiency.

For the past decade, TI has made ultra-low power its mission. With the breakthroughs in performance and transparent power management technology made available through “Wolverine,” developers can spend less time optimizing for power and more time building the core functionality of their applications.

The “Wolverine” platform truly changes the ultra-low-power landscape by slashing the power MCUs consume in half. This power efficiency, combined with advances in low-power harvesting technology, brings the industry another step closer to a battery-free world.

### ***For more information***

Additional information can be found at [www.ti.com/wolverine](http://www.ti.com/wolverine).

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